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Numerical Simulation of Impedance Discontinuities Resulting from Degradation of Interconnections on Printed Circuit Boards

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Abstract

A 3-D model was developed for numerically simulating the effect of solder joint cracking on impedance. Some initial reflectometry results are reported of a microstrip transmission line as a crack propagates through a solder joint. Observations are made on the information obtained when using low-pass vs. band-pass modes for reconstructing reflectometry data from frequency domain results. A qualitative comparison is made with experimental results on samples with a design which is similar to the model. On the basis of these observations, approaches for improving the model and future applications are discussed.

Introduction

Electronic circuits rely on interconnects for the transmission of signals between devices. Because they are so prevalent, and because they often also support mechanical loads, the reliability of interconnects is frequently the limiting factor in the lifetime of an electronic product.

In the case of printed circuit boards, solder joints are the most commonly used type of contact between a device and the interconnection network. The failure of a solder joint typically involves the nucleation of a crack at a surface or interface and the propagation of that crack across the solder joint until it causes a loss of electrical continuity. In circuits operating at RF or microwave frequencies, even a partial crack will alter the impedance and could adversely affect its performance. Proper design of these electronic circuits requires an understanding of how they will perform throughout their useful lifetime, part of which may be affected by solder joint degradation which is not sufficient to cause loss of continuity but could affect signal integrity.

Experimental studies of this phenomenon, previously reported in [1, 2, 3, 4], have shown that the impedance changes resulting from cracks as small as 30 μm in length are detectable using time domain reflectometry (TDR). Sensitive measurements such as these are valuable in demonstrating the validity of concerns over the effects of intermediate stages of degradation of the interconnections on signal integrity, but they are difficult and time consuming to carry out. Thus experimental studies cannot easily be used to investigate the effect of a wide range of experimental and material parameters. For this purpose, numerical simulation provides a convenient means to predict the effects of degradation. The availability of experimental data on well-characterized samples provides a basis for validating the qualitative and quantitative results of the simulations.

The objectives of this paper are to introduce the approach which was developed for simulating the impedance discontinuity resulting from degradation of a solder interconnection, and to report initial results obtained using this model. We provide a brief summary of the experimental studies which were the basis for this modeling effort. We then describe the model and discuss issues associated with the creation of a suitable mesh for the modeling of solder joint cracks. We report the results in the time domain for the purposes of comparison with experimental data, and discuss the conversion from frequency domain into the time domain. This effort provides the groundwork for future numerical simulation of a variety of circuit designs and possible scenarios.

Measurements on Cracked Solder Joints

Experimental studies of solder joint degradation were performed using a simple circuit that allowed continuous monitoring of RF signals during stress testing. The test specimen, shown in Figure 1, consisted of a surface mount low-pass filter soldered to a grounded co-planar waveguide (GCPW) which had a 50 Ohm controlled impedance. SMA connectors provided the interface to the RF cables that connected the specimen to the test equipment. The solder joints connecting the filter to the signal trace were mechanically stressed by applying a cyclic shear load directly to one side of the filter, thus causing fatigue cracks to form in the solder. The load was generated using an MTS Tytron 250 mechanical test system with servo control, transferred to the filter through a ceramic probe to avoid electrical interference with the test circuit. The system was programmed to apply a 40 N offset load, to maintain constant contact between the probe and filter, superimposed upon a sinusoidally varying load of 10 N amplitude and 4 second period (0.25 Hz).

During stress testing the specimen was electrically monitored using time domain reflectometry to detect changes in the response which were indicative of solder joint cracking. The TDR measurements were carried out using an Agilent E8364A vector network analyzer (VNA), which was configured with an option that allowed the instrument to convert its frequency domain measurements into the time domain using either a low-pass or band-pass conversion mode. The advantage of displaying measurements in the time domain was the ability to localize the source of changes to the impedance, eliminating the influence of other far-away components of the circuit (e.g., bias-tees, connectors, etc.). By monitoring the reflections originating in the specific location of the solder joints, the sensitivity to changes in the solder joints was elevated.

The band-pass mode was used in the experiments, which

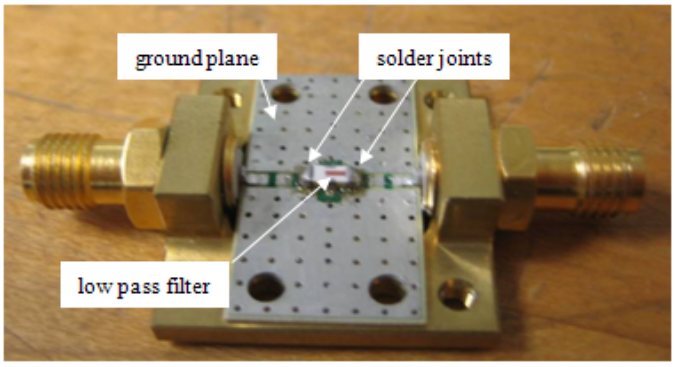

Figure 1: Photo of test board indicating surface mount filter with solder attachments to signal trace, and ground plane.

used signals in the frequency range from 0.5 GHz to 6.0 GHz to construct the TDR response of the circuit. The upper frequency was within the pass band of the surface mount filter, which had a cutoff frequency of 6.7 GHz. This minimized the influence of the filter on the TDR response and ensured good sensitivity to changes in the solder joints. The band-pass mode with a lower frequency of 0.5 GHz was selected in order to allow the TDR response to be clearly distinguished from DC resistance measurements, which were made simultaneously during the stress tests by means of bias-tees which were located in the test circuit (shown in Figure 2). Since one of the original objectives of the experiments was to demonstrate that RF signals were more sensitive to initial stages of interconnection degradation than the DC resistance, the lower cutoff frequency of 0.5 GHz ensured that there was no DC or low frequency contribution to the RF response.

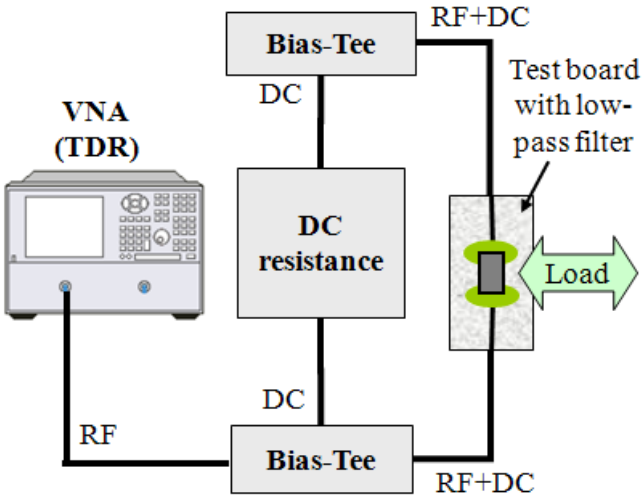

Figure 2: Schematic of test circuit.

Time domain data were collected every 30 seconds throughout a stress test. Sample plots of the TDR reflection coefficient collected before and after solder joint cracking are shown in Figure 3. For graph readability, the reflection coefficient, which assumes bounded values, is plotted instead of impedance. However, the reflection coefficient Γ carries the same information as impedance Z and they can be related to each other by

$$Z = 50\frac{1+\Gamma}{1-\Gamma}. \tag{1}$$

The plots show a small reflection associated with the intact solder joints and low-pass filter. The reflection coefficient associated with the filter and its solder joints rose considerably when the solder joints cracked as a result of repeated cyclic loading. The frequency range used for the TDR measurements did not provide sufficient resolution to distinguish the individual solder joints, but the signal from the component and its interconnections provided clear indications of the impedance discontinuity represented by a crack in one of the solder joints. Failure analysis of partially and fully cracked solder joints [1, 2, 3, 4] has confirmed that the elevated TDR reflection coefficients observed during stress testing were due solely to cracking.

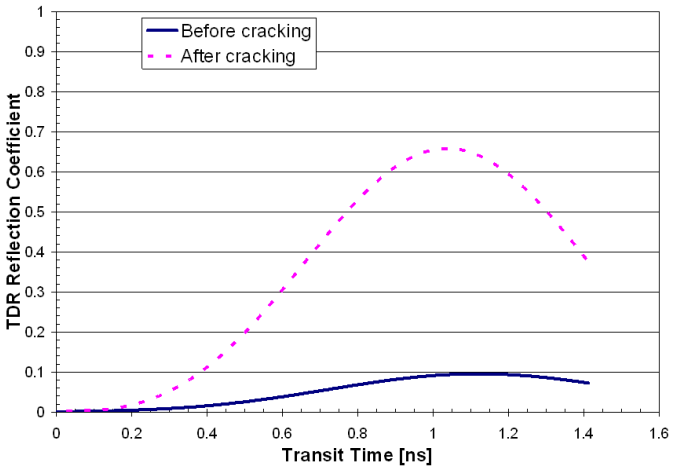

Figure 3: Sample plots of TDR reflection coefficient before and after solder joint cracking.

Numerical Simulation of Cracked Solder Joints

In order to address the problem in a more flexible way and to support the interpretation of experimental results, a numerical model of the cracked solder joint was created. This allowed us to arbitrarily change relevant parameters and to perform a parametric analysis. On the other hand, the choice of simulation type (in time or frequency domain) and assumptions on the implemented model must be assessed as a preliminary step, with the aim of being as consistent as possible with the actual test sample and its measurements.

Since data were collected using a VNA, a frequency-domain simulator was chosen, namely Ansoft HFSS [5]. Therefore, the simulation results were native in the frequency domain just as the measurements were, and they were then converted to the time domain using a post-processing scheme similar to that implemented by the instrument.

The main limitation of numerical simulations concerns the mesh dimension. Of course, it is expected that the finer the

mesh is, the more accurate the solution will be. However, the drawback of a huge mesh is that it may exceed the capabilities of available computer resources. Because of this, in the device model of Figure 4, a 50 Ohm microstrip transmission line was chosen in place of the GCPW, since it has fewer details (e.g., no vias) thus reducing the mesh complexity. Moreover, for the same reason, the filter, that behaves basically as a matched transmission line in the considered bandwidth, was replaced by another 50 Ohm microstrip, though with a different substrate height in order to introduce a vertical discontinuity between the traces. The electrical continuity between the two traces was assured by a solder joint, that in our model was represented using a rectangular metallic block. The crack was introduced as a vacuum box partially obstructing the adhesion of one of the two solder joints to the lower microstrip. To summarize, the simulated structure was composed of three microstrip sections, all having a trace width of 1 mm and a thickness of 20 μm. The first and the last sections had a substrate with $\varepsilon_r = 3.66$ and $h = 0.47$ mm, while the intermediate microstrip had $\varepsilon_r = 8$ and $h = 0.87$ mm and a length of 3 mm. The total length and width of the device were 12 mm and 24 mm, respectively. The solder joints were metallic boxes with size $1 \times 0.4 \times 0.25$ mm^3.

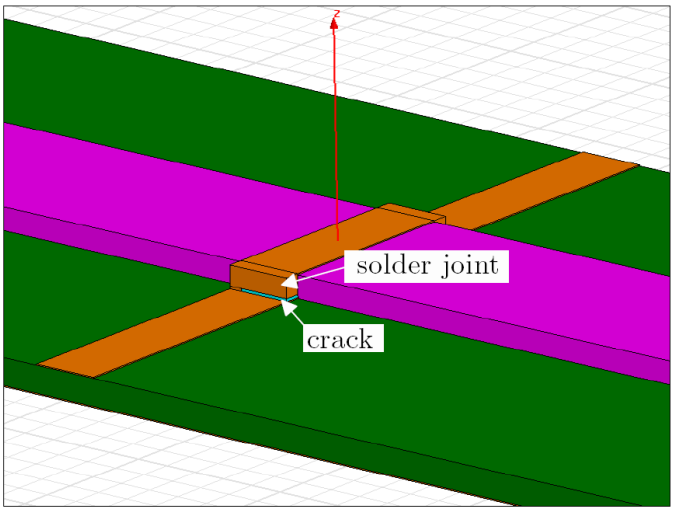

Figure 4: Simulation model, consisting of three microstrip sections connected by means of two metallic blocks representing the solder joints.

Typical crack heights that occur in practice are of the order of 5-10 μm [6], thus requiring very small mesh edges in that region. In order to perform the simulation using available computer resources, we used in our simulation a crack height that was approximately one order of magnitude larger than the real value. Figure 5 shows the TDR reflection coefficient for a parametric simulation of a 100-μm-high crack (i.e., about 10 times the height of realistic cracks) for different width values. The original S-parameters were computed from 0 to 6 GHz and the two panels refer to band-pass and low-pass conversion modes. This refers to the type of processing adopted to convert original frequency-domain data into a synthetic TDR waveshape: low-pass provides the inverse Fourier Transform (FT) of all frequency samples of the simulation, while the band-pass conversion uses only the samples in a narrow bandwidth and generates the absolute value of the inverse FT (more details can be found in [7]). The measured data are processed using band-pass mode in the range 0.5 – 6 GHz and therefore they should be compared with the top panel. A qualitative agreement in the shape of the responses as well as in the trend of reflection increment as the crack grows can be observed. Yet, one of the main limitations concerning the use of band-pass mode is the reduction of resolution and the loss of information about the nature of the discontinuity. Figure 5 shows that the trend is more evident in curves obtained through low-pass mode and the inductive nature (positive peak followed by a negative peak) of the discontinuity can be appreciated, thus providing more complete information.

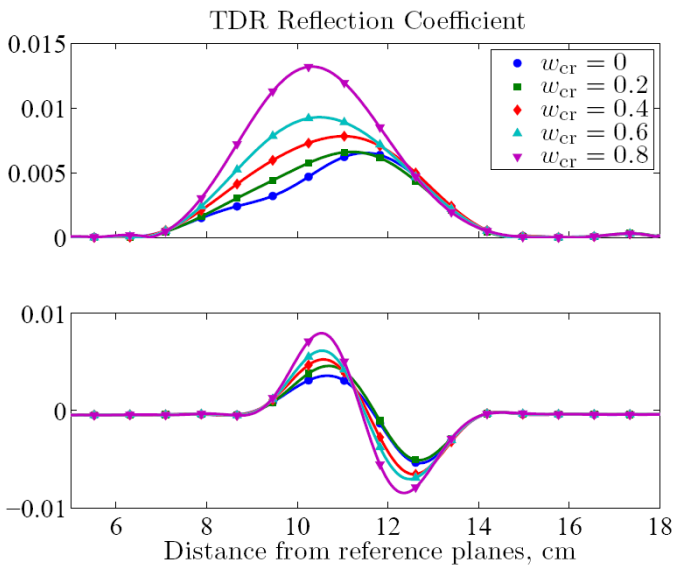

Figure 5: TDR reflection coefficient for different crack widths, ranging from 0 to 1 mm (crack height: 100 μm). Two different frequency-time conversion modes are adopted: band-pass (top panel) and low-pass (bottom panel).

Conclusion

This paper addresses the simulation of the impedance changes caused by solder joint degradation. Time-domain results were presented because they match prior experimental studies and provide qualitative insight into the nature of the discontinuity arising from a cracked solder joint. Experimentally, time domain measurements also have the advantage of localizing the impedance discontinuity, allowing one to eliminate from consideration other possible sources of impedance discontinuities.

The numerical simulation based on a frequency-domain electromagnetic solver reproduced the basic characteristics of the actual measurement setup and was used to gather more information about how parameters as well as the processing affect the final results. In particular, the simulations confirmed the trend of the reflection growth as the crack propagates inward across the solder joint.

Numerical results provide helpful insights about how the

measurement conditions affect the quality of information. First of all, it is appropriate to restate that the device dimensions are smaller than the shortest measurement wavelength (i.e., 5 cm at 6 GHz in vacuum), thus making the exact resolution of discontinuities and the quantitative detection of impedance changes impossible. Nonetheless, the qualitative variation of curves with the crack dimensions suggests that a signature of the device can be still tracked and monitored over time as a means of continually assessing the health of the interconnections.

In addition, the use of low-pass conversion mode improves the system resolution and clarifies the nature of the crack discontinuity (i.e., whether it behaves inductively or capacitively).

The results reported here provide motivation for further refinement of the numerical model, as well as additional experimentation. The correspondence between the model and the experimental system would be improved by reducing the crack height to more realistic dimensions, which will require additional computational resources. The test specimen would be better represented by the incorporation of a model for the low-pass filter that more accurately reproduces its electrical characteristics. Concerning the experimental measurement system, since there is no longer a need to distinguish the DC response from the TDR response, a low-pass conversion mode would provide improved sensitivity to degradation as well as information regarding the nature of the impedance discontinuity. Results of further experimentation using this mode can be used to obtain a more quantitative validation of the numerical model.

A robust and validated model of the impedance changes caused by solder joint cracking has numerous and significant potential applications. Such a model can be used to predict how degradation throughout the lifetime of a circuit can affect signal integrity, providing information to design engineers regarding the amount of additional performance margin needed to compensate for this effect. The ability to easily modify the configuration and material properties of the model makes it possible to investigate how variabilities in manufacturing processes and material quality can affect the performance, and thus the reliability, of high speed circuits. The model also has value for predicting the effect of board design and material properties on the ability to detect solder joint degradation using TDR or signal integrity measurements, providing guidance for experimental design of test circuits to further investigate these phenomena.

This model can also be used to translate experimentally obtained TDR results into a real-time measurement of solder joint crack dimensions. This capability can help to solve some long-standing problems in electronics reliability, such as how crack propagation kinetics are affected by different or arbitrary loading conditions. For example, the effect of temperature cycling combined with mechanical vibration is typically not a linear combination of the two loads, making it very difficult to predict the expected life of a solder joint under these conditions. The numerical model, combined with in situ measurement of impedance, provides a powerful tool for direct, non-destructive measurement of crack dimensions under complex or arbitrary loading conditions.

Acknowledgments

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