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An Application of Volterra Series to IC Buffer Models

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Abstract

This paper presents a Volterra-based method of behavioral modeling for the I/O buffers of digital ICs. While this technique brings a slight improvement in accuracy over previous ones, its main strength is a greater degree of generality. With a modeling approach less dependent on the nature of the devices and more easily extendable to include the effects of multiple inputs one may hope better meet the challenges of advancing technology. The proposed models can be obtained from device port transient responses only and can be easily implemented in any simulation environment, including SPICE-based circuit description software. Two illustrative examples conclude the paper.

Introduction

The modeling of digital Integrated Circuits (IC) input and output buffers is of paramount importance for the assessment of Signal Integrity (SI) and ElectroMagnetic Compatibility (EMC) in high-end digital systems. The most effective modeling solution for this problem is based on the development of behavioral models (or macromodels) that seek to mimic system behavior rather than its internal physics.

The current paper benefits from previous research on two-piece non linear models of integrated circuit buffers but uses a different identification technique with respect to previously published solutions [2,3]. It is organized around two main sections: a first one that briefly explains the principles of the proposed algorithm after reminding the best known state of the art methods and a second one that illustrates the technique with a couple of examples.

Overview of IC buffer modeling

The main challenge when seeking to model IC buffers is to choose an appropriate description accounting for the non-linear relations that bind the device ports. The state-of-the-art contributions available in literature provide diverse solutions [1-4].

In [4] the output current of a driver is modeled via a purely black-box approach based on a suitable class of neural-networks. The strength of this technique is that it does not use any prior information on the internal structure of the device, it is aimed at providing the most general solution to the problem and the results published by the authors demonstrate the feasibility of the proposed technique for the generation of accurate models of some devices. However the complexity of the model representation might increase for devices with a rich dynamical behavior, like drivers with pre/de-emphasis features, thus impacting on the efficiency of the obtained models. Furthermore, the modeling procedure is basically expressed in terms of finding the solution to a nonlinear optimization problem where the parameters involved in the

estimation need application-specific tuning. What is more important, the approach turns out to be hardly extendable to additional inputs like the power supply voltage or multiple output terminals. As an alternative, a two-piece model has been more commonly adopted by the other methodologies available in the literature [1,2,3].

In these approaches, the model representation describing the output port of a buffer like the one shown in Fig. 1 writes:

$$i(t) = w_H(t)i_H(v(t), d/dt) + w_L(t)i_L(v(t), d/dt) \quad (1)$$

where, i and v are the output electrical variables (see Fig. 1), i_H and i_L are submodels describing the nonlinear dynamic behavior of the port in the fixed high and low logic states, respectively, and w_H and w_L are weighting signals describing state transitions.

This assumption is justified by the inclusion in the model equations of the inherent logical switching operation of this class of devices. This solution has been demonstrated to provide excellent results in terms of both model accuracy and model efficiency. It is worth noticing that modifications of the structure of (1) are available in the literature to account for the effects of the fluctuations of the power supply or the description of different device types (e.g., differential drivers) [2,5].

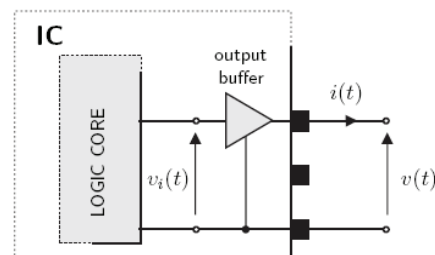


Figure 1. Typical IC buffer with the relevant electrical variables.

Many nonlinear identification tools devised by researchers working in different fields are unable to correctly capture the behavior of a commuting system. The 2-piece split previously described cleverly circumvents this difficulty. At this point it becomes very interesting, rather than continue with a device-oriented approach as done in previous papers, to examine the nature of the two resulting subsystems. The next paragraphs will show the latter are in fact weakly non-linear and fall in what is known as the Volterra class of non-linear systems. This discovery is a valuable tool that provides the 2-piece approach with a higher degree of generality and improves its adaptability to varied types of buffers. Another advantage is confidentiality; the model will mimic system behavior without revealing any technological information.

Two-state Volterra-based models

Volterra series are a well known input-output representation of non-linear systems and have found in the last half-century a variety of applications in different fields of science [6-9]. They have proved to be a valuable and reliable tool in nonlinear system identification and allow a straightforward generalization to multivariable systems. The general discrete time expression of a Volterra series is given in

$$i(k) = \sum_{m=1}^{\infty} \sum_{k_j=0}^{\infty} \dots \sum_{k_m=0}^{\infty} h_m(k_1, k_2, \dots, k_m) \prod_{l=1}^m v(k - k_l) \quad (2)$$

with i being the output variable, v the input and h_m being referred to as the m -th order kernel. One may intuitively see Volterra series as a generalization of a linear system's impulse response function and it is quite obvious that for $m = 1$ expression (2) is reduced to the basic relation binding the input, the output and the impulse response.

At this stage the problem has been practically reduced to the identification of the Volterra kernels. Solving it directly is usually cumbersome but it was shown by Boyd and Chua [9] that any Volterra series can be rewritten as an expansion of Laguerre functions. This further simplifies the problem and allows a straightforward approach to system identification. Due to paper-length constraints the mathematical derivation of the identification process are not reproduced here, the readers should refer to [6,7,8] for additional details on the Volterra-Laguerre structure and on the model parameter extraction procedure. Briefly speaking, the parameters can be computed via a standard least squares method from the transient voltage and current responses of the system.

The method presented in this paper separately identifies sub-systems i_H and i_L as Volterra-Laguerre models. Subsequently the subsystems are properly weighed according to the procedure already described in [2] yielding a complete two-state model.

Simulation results

In this Section, the proposed methodology is applied to the modeling of two commercial devices, a single-ended and differential one, thus confirming the strengths and the generality of the proposed approach in generating multiport models of different device types. The HSPICE transistor-level descriptions of the examples, that are available from the official website of the vendor, have been used for generating the device responses required by the modeling process as well as the curves validating the model's accuracy.

Single-ended drivers. The first example considered in this study is the output port of a 8-bit bus transceiver with four independent buffers produced by Texas Instruments (model name SN74ALVCH16973, power supply voltage VDD=1.8 V). A model is estimated via the procedure outlined in the previous Section.

A first measure of the accuracy of the proposed models in approximating the behavior of the example test case and to highlight its validity range in the space of the input signals, Fig. 2 shows in the $i-v$ plane the reference and the predicted static characteristics of the output port current of the buffer in fixed high logic state. The bunch of curves in the Figures have

been obtained for different values of the power supply voltage v_{dd} within the range [70%,130%] VDD. From the two Figures, it is clear that the proposed models can be effectively used to predict the device behavior for very large variations of the power supply voltage. Also, the accuracy of the prediction is very good even in a region far from the area explored by the $\{v(t), i(t)\}$ samples of the signals used in the model estimation phase. It is ought to remark that the static characteristic of a Volterra-Laguerre model with a small number of kernels is always well-behaved and, if needed, it can be easily conditioned via the sum of a static term that compensate the non monotonic behavior of the curve. As an example, any quadratic ($m = 2$) Volterra-Laguerre model always has a parabolic behavior like the one shown in Fig. 2.

It is worth noticing that these results have been obtained by using a single quadratic Volterra-Laguerre series for each submodel, with 8 coefficients only, that does not need any specific customization of the model structure as suggested by the alternative state-of-the-art solutions proposed in the literature [1-4].

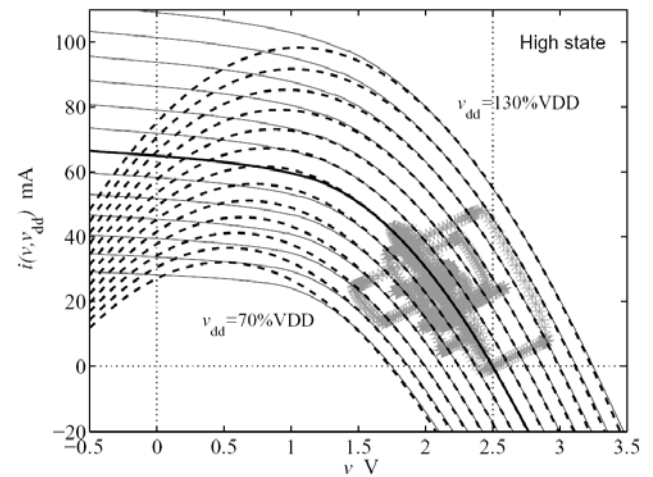


Figure 2. Static characteristic of the current $i_1(v, v_{dd})$ for the first example driver forced in the high output state. The different curves correspond to values of the power supply voltage v_{dd} varying within the range [70%,130%] VDD. Solid lines: reference curves (the thick line corresponds to the characteristic at $v_{dd}=VDD$); dashed lines: Volterra-Laguerre model; gray stars: region explored by the $\{v(t), i(t)\}$ samples corresponding to the responses used in the estimation phase.

As a more realistic validation, Figure 3 collects the results of a simulation test that consists of the example device producing a "010" bit pattern on an open-ended ideal transmission line (characteristic impedance $Z_0 = 50\Omega$, time delay $T_D = 2$ ns). The supply pin of the device is connected to a simplified lumped equivalent of the power distribution network consisting of the series connection of a VDD battery and a 10nH inductance. Figure 3 compares the reference response of the example driver to the responses predicted by the state-of-the-art M π log model [2] and by the proposed two-states Volterra-Laguerre model. From the curves in the Figure, it is clear that both the models allow to accurately reproduce the reference curves, and a small improvement in the description of the power supply fluctuations can be

appreciated in the response of the proposed model in the bottom panel of Fig. 3.

Differential drivers. The second example test case is the output port of the Fairchild FIN1019 LVDS High Speed Differential Transceiver (power supply voltage $V_{DD}=3.3$ V, nominal value of the common mode voltage operation $V_C=1.2$ V).

As done for the single-ended case, the same systematic assessment has been carried and similar results have been found. However, for the sake of conciseness the results of the realistic validation shown in Fig. 4 are reported only. In this validation, the device is connected to the same lossless transmission line of the previous test that is terminated by the shunt connection of a 100Ω differential resistor and of a 2 pF capacitor. The power supply pin of the example device is instead connected to a lumped equivalent of the supply network that consists of the series connection of a V_{DD} battery and a 15 nH inductance, thus highlighting the accuracy of both the functional signals like the port voltages at the output terminals of the driver and the variations of the supply voltage and current responses.

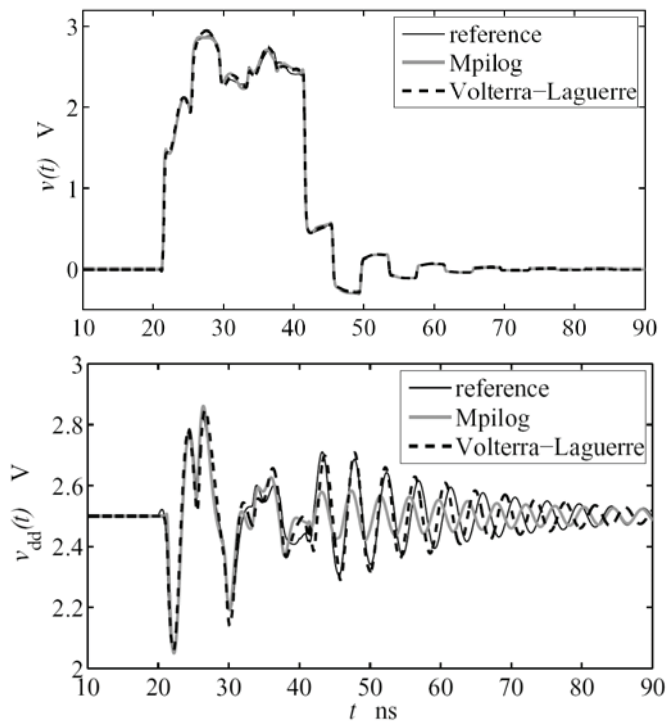


Figure 3. Output port $v(t)$ and supply port $v_{dd}(t)$ voltage waveforms for the first example driver producing a “010” bit pattern on a transmission line load (see text for details). Solid black line: reference; solid gray line: response of the state-of-the-art $M\pi$ log model [2]; dashed line: Volterra-Laguerre model.

The assessment carried out in this Section shows that the proposed two-states Volterra-Laguerre models can be effectively used to accurately predict the responses of different classes of device types. The models turn out to have well-behaved characteristics in the region of the input

variables outside the area explored by the signals used for the estimation of model parameters. The models are stable by construction, allows for the inclusion of different input signals (e.g., three for the latter differential case) and, for the examples of this study, they are small in size, *i.e.*, a low-order Volterra-Laguerre expansion defined by a small number of coefficients can be effectively used to reproduce the behavior of real devices. Finally, the proposed models are as fast as alternative state-of-the-art models like the $M\pi$ log models [2], leading to simulation speed-ups on the order of $10x \div 100x$ w.r.t. the reference transistor-level description of devices.

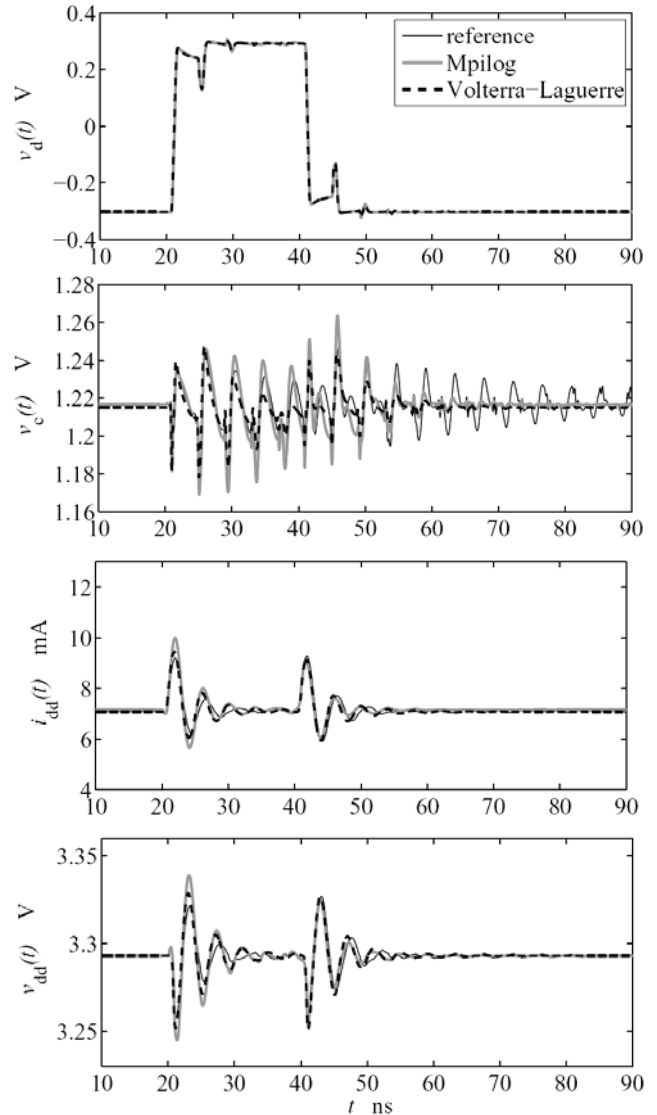


Figure 4. Differential $v_d(t)$ and common mode $v_c(t)$ voltages (top panels) and power supply voltage $v_{dd}(t)$ and current $i_{dd}(t)$ waveforms (bottom panels) computed for the second example driver producing the bit pattern “010” on a coupled interconnect structure. The interconnect is terminated by the shunt connection of a 100Ω resistor and a 2 pF capacitor and the device is supplied by a simplified lumped equivalent of the supply distribution system (see text for details). Solid black line: reference; solid gray line: response of the state-of-the-art $M\pi$ log model [2]; dashed line: Volterra-Laguerre model.

Conclusions

This paper presents a two-state Volterra approach to the modeling of IC buffers. System identification is achieved using a Laguerre expansion of the individual Volterra kernels. While the approach falls in the class of two-piece solutions its strength resides in a greater degree of generality allowing for greater adaptability. The same method is used to identify different types of IC buffers without the need for specific tuning. The performance of the technique is judged both in terms of static and dynamic analysis. It is worth noting that, as illustrated in the previous section, the method manages to estimate the static characteristics of the device, in a significant range, blindly - with no explicit knowledge. In terms of CPU time, the models obtained are practically as fast as the state-of-the-art models available in the literature, and lead to comparable accuracy (a slight improvement may be visible in some cases) with the advantage of being analytically stable.

References

- [1] I/O Buffer Information Specification (IBIS) Ver. 5.0, on the web at <http://www.eigroup.org/ibis/ibis.htm>, Aug. 2008.
- [2] I. S. Stievano, I. A. Maio, F. G. Canavero, "M π log Macromodeling via Parametric Identification of Logic Gates," IEEE Transactions on Advanced Packaging, Vol. 27, No. 1, pp. 15–23, Feb. 2004.
- [3] B. Mutnury, M. Swaminathan, J. P. Libous, "Macromodeling of nonlinear digital I/O drivers," IEEE Transactions on Advanced Packaging, Vol. 29, No. 1, pp. 102–113, Feb. 2006.
- [4] Yi Cao, Runtao Ding, Qi-Jun Zhang, "State-Space Dynamic Neural Network Technique for High-Speed IC Applications: Modeling and Stability Analysis," IEEE Transactions on Microwave Theory and Techniques, Vol. 54, No. 6, pp. 2398–2409, June 2006.
- [5] I. S. Stievano, I. A. Maio, F. G. Canavero, C. Siviero, "Reliable Eye-Diagram Analysis of Data Links via Device Macromodels," IEEE Transactions on Advanced Packaging, Vol. 29, No. 1, pp. 31–38, Feb. 2006.
- [6] R. J.G.B. Campello, G. Favier, "Optimal Expansions of Discrete-Time Volterra Models Using Laguerre Functions," Automatica, Vol. 40, No. 5, pp. 815–822, May 2004.
- [7] T. Dobrowiecki, J. Schoukens, "Measuring a linear approximation to weakly nonlinear MIMO systems," Automatica, Vol. 43, No. 10, pp. 1737–1751, Oct. 2007.
- [8] A. Y. Kibangou, G. Favier, M. M. Hassani, "Laguerre-Volterra Filters Optimization Based on Laguerre Spectra," Journal on Applied Signal Processing, Vol. 2005, No. 17, pp. 2874–2887, 2005.
- [9] S. Boyd, L. O. Chua, "Fading memory and the problem of approximating nonlinear operators with Volterra series," IEEE Transactions on Circuits and Systems, Vol. 32, No. 11, pp. 1150–1161, 1985.