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17 April 2024

Behavioral modeling of IC memories from measured data

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Abstract—This paper addresses the generation of behavioral models of digital ICs for signal and power integrity simulations. The proposed models are obtained by external measurements carried out at the device ports only and by the combined application of specialized state-of-the-art modeling techniques. The present approach exploits a behavioral formulation, leading to models reproducing all the behavior of the IC ports as the I/O buffers and the core power delivery network. The modeling procedure is demonstrated for a commercial NOR Flash Memory in 90 nm technology housed by a specifically-designed test fixture.

Index Terms—Digital integrated circuits, I/O ports, power delivery network, circuit modeling, macromodeling, power integrity.

I. INTRODUCTION

Nowadays, the modeling of the external behavior of high-speed digital integrated circuits (ICs) is of paramount importance for the simulation of many advanced electronic applications. In particular, the availability of computational models of ICs that account for the behavior of both the power delivery network and the I/O ports of devices is highly desirable. The models are used in a system level simulation to predict the integrity of the signals flowing through the system interconnects and the switching noise generated by the current absorption of the circuits, that can interfere on the stable functioning of the entire system. A typical example of devices that demand for the availability of reliable models is represented by the class of digital memories, that are widely used in modern electronic equipments and that are often provided by external suppliers along with low-order or partial models only.

Within this framework, the modeling from external measurements appears to be a very promising strategy to handle the IC complexity and to provide the designers with a useful tool for model generation. The modeling of the power delivery network of ICs is addressed in [1], [2], [3] and the modeling of I/O ports in [4], [5], [6], [7], [8]. In these contributions most of the efforts are made to define and improve the model

structures and to provide general modeling guidelines for the computation of model parameters from both numerical simulations and real measurements. However, the inherent limitations in the estimation of model parameters from measured data are scarcely addressed by the current literature.

The aim of this paper is to provide a unified modeling framework for the combined application of state-of-the-art techniques to the generation of behavioral models of digital ICs from real measured data. The step-by-step modeling procedure and the setup required to collect the responses for parameter estimation is thoroughly described.

All the results presented in this study are based on the measurements carried out on a 512Mb NOR Flash memory in 90 nm technology produced by Numonyx, which is representative of a wide class of memory chips. The test board that has been developed to carry out the measurements used in the modeling process is also described. The board, that allows the accurate modeling of both the IC core power delivery network and the I/O ports at the same time, can be easily adapted to test different ICs.
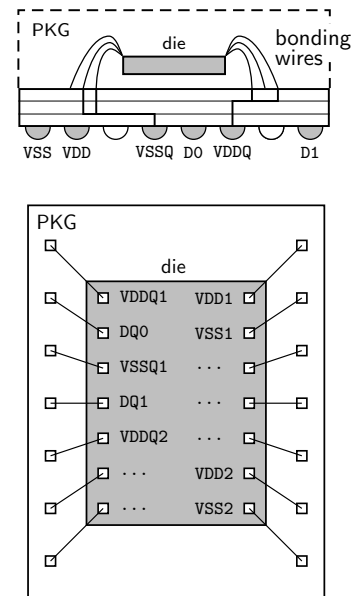

Fig. 1. Typical structure of a digital IC encapsulated in package (top panel: side view; bottom panel; top view).

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II. IC MACROMODELS

This section focuses on the available resources for the modeling of the external behavior of the I/O ports and the core power delivery network of a digital memory circuit like the IC shown in Fig. 1. The structure of the models and the data required for the estimation of the model parameters are shortly outlined in this section.

In the schematic of Fig. 1, that represents the typical structure of a packaged memory IC, the core power delivery network is the structure defined by the VDD and VSS balls that carry the energy to the memory matrix, the digital circuitry and possible additional analog blocks within the die via the VDDn and VSSn pads. On the other hand, the high-speed I/O buffers are defined by the Dn balls connecting the DQn pads of the die. In this class of devices, the buffers are supplied by a dedicated power structure, *i.e.,* the so-called power rail, that consists of two on-chip traces connecting pairs of VDDQn and VSSQn. Also, a limited number of buffers (in general from one to four) is supplied by two adjacent VDDQn and VSSQn pads.

From the above structure, it is clear that a behavioral model of the memory IC is represented by (i) a dynamical model for the core power network that reproduces the port constitutive relation of the two terminal circuit elements defined by the VDD and VSS balls, (ii) a set of dynamical models for the I/O buffers that include the effect of their dedicated power supply structure and that describe the port constitutive relations of the three terminal circuit elements defined by the Dn, VDDQ and VSSQ balls and (iii) the possible coupling between the buffer and the core power delivery networks. However, for the class of devices at hand, the latter coupling contribution turns out to be extremely low and is neglected as verified by a set of on-chip measurements carried out on the same memory chip considered in this study (see Fig. 2).
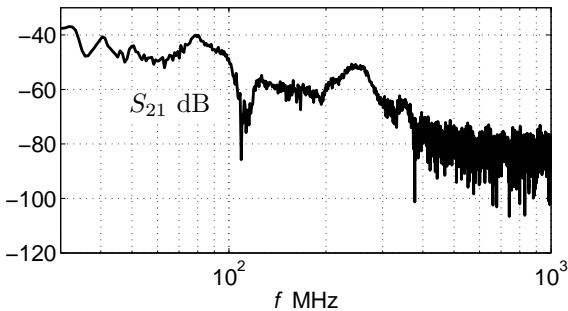

Fig. 2. On-chip measurement of the S_{21} scattering parameter accounting for the coupling between the buffer and the core power delivery networks of the example test chip considered in the study.

A. Core power delivery network

According to [1], [2], [3], the models for the core power supply of ICs are defined by simplified - physically inspired - circuit equivalents that attempt to describe the different blocks involved in the power delivery network of the digital IC. A common assumption in these approaches is the description of the core power delivery network of the IC by means of a Norton equivalent where the short-circuit current generator $A(s)$ accounts for the internal switching activity of the device and the equivalent impedance $Z_e(s)$ accounts for the passive interconnect structure and body diodes (see Fig. 3a). It is ought to remark that this assumption holds when the physical dimension of the silicon die and the frequency bandwidth of interest are compatible with lumped modeling. When these conditions are met, this simplification is the best solution to estimate the model parameters from external measurements.

The estimation of model parameters amounts to computing the short-circuit current source via the transient measurement of the current drawn by the IC core during normal operation and the short-circuit admittance via frequency-domain measurements (e.g., via the scattering parameter responses of the VDD-VSS structure). It goes without saying that the frequency-domain measurements do not directly provide a computational model that can be directly used in a simulation environment like SPICE. Experience, supported also by the evidence that the die is electrically small, teaches us that the interpretation of $Z_e(s)$ and its conversion into an equivalent circuit is rather straightforward. For the class of devices at hand, the behavior of the equivalent impedance can be effectively approximated by $Z_e(s) = 1/sC + r + sL$, being $1/sC$ the main contribution of the core power network at die level and $r + sL$ the effects of the IC package.
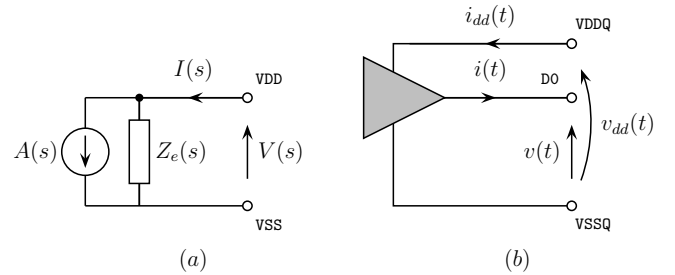

Fig. 3. Model structures: (a) Norton equivalent for the VDD-VSS core power delivery network; (b) nonlinear dynamical model for the I/O buffers (*e.g.,* the D0 ball of Fig. 1).

B. I/O buffers

Different approaches are used to obtain behavioral models of the I/O ports of a digital IC. The most common approach is based on simplified equivalent circuits derived from the internal structure of the modeled devices. This approach leads to the I/O Buffer Information Specification [4], [5], which is widely supported by electronic design automation tools and dominates modeling applications. However, the growing complexity of recent devices and their enhanced features like pre-emphasis and specific control circuit, demand for refinements of the basic equivalent circuits. In order to facilitate the modeling of these features, alternate methodologies based on the estimation of suitable parametric relations have been proposed [6], [8], [9]. These methodologies are aimed at reproducing the electrical behavior of device ports (see Fig. 3b), without any use of physical insights and of equivalent circuit representations. The advantage of these approaches relies in

the flexibility of the mathematical description of models with respect to the circuit representation and on the computation of model parameters from the responses recorded at the device ports only. Furthermore, the parametric approaches offer simple and well-established procedures for the estimation of model parameters from real measured data.

For the case of output buffers, the common assumption in the current state-of-the-art solutions is the description of the port electrical behavior of the circuit via the following two-piece relation:

$$i(t) = w_H(t)i_H(v(t), v_{dd}(t), \frac{d}{dt}v(t), \frac{d}{dt}v_{dd}(t), \frac{d^2}{dt^2} \ldots) + \\ w_L(t)i_L(v(t), v_{dd}(t), \frac{d}{dt}v(t), \frac{d}{dt}v_{dd}(t), \frac{d^2}{dt^2} \ldots) \tag{1}$$

where v, v_{dd} and i are the buffer output and power supply port voltage and current variables, with associated reference directions, w_H and w_L are switching signals accounting for the device state transitions and i_H and i_L are nonlinear dynamical relations accounting for the device behavior in the fixed high and low logic states, respectively. A similar relation holds for the power supply current and a simplified model structure, that can be considered as a subclass of eq. (1), can be adopted for the alternate case of input ports. The readers should refer to [6] for additional details.

The estimation of model (1) amounts to computing the parameters of submodels i_H and i_L and the weighting signals w_H and w_L from suitable port transient responses. In this study, the state-of-the-art modeling procedure suggested in [7] has been considered and further improved. The proposed models are obtained from the device responses recorded during the normal activity of the IC mounted on a real board, thus avoiding specific modeling setup and test fixtures.

III. MODEL ESTIMATION

This section summarizes the procedure for the estimation of the models shown in Fig. 3 and highlights possible difficulties in the computation of model parameters from real measured data.

A. Core power delivery network.

The generation of the Norton equivalent of the core power delivery network requires the estimation of the equivalent impedance and of the short-circuit current source of Fig. 3a.

The computation of the current source is the most critical step of the modeling process and special care must be taken in collecting, interpreting and processing the measured data. From a theoretical point of view, the determination of the A term would require the measurement of the current flowing through an ideal short-circuit terminating the VDD and VSS balls on the left panel of Fig. 1. However, in practice, the balls cannot be shorted and the circuit operation of the die must be assessed with the device mounted on a board. Figure 4 shows the equivalent circuit, in the Laplace domain, of the setup for the external current measurements I_{ss}. The external power supply provided by a voltage regulator and a possible shunt capacitance is simply represented by an ideal battery

connected to the VDD ball. The VSS ball is connected to a SMA connector via an on-board trace, that is represented by a lumped equivalent in the Fig. 4.
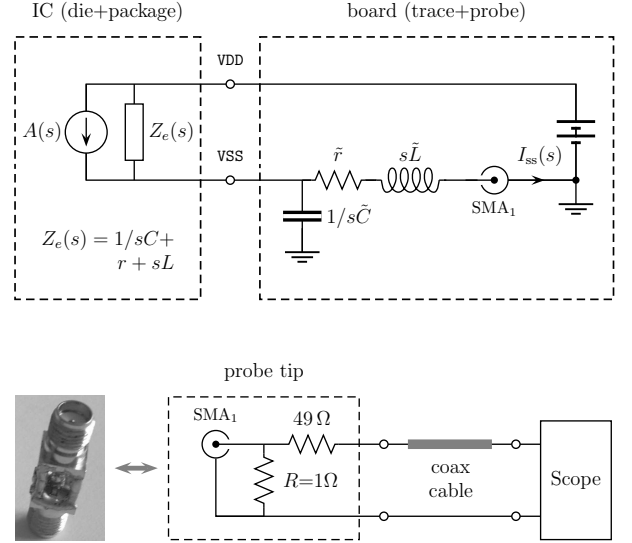

Fig. 4. Simplified equivalent of the setup used for the measurement of the switching current of a digital IC and the equivalent impedance of the core power delivery network (top panel). Specifically designed 1-Ω current probe and its schematic (bottom panel).

In the scheme of Fig. 4, the transient current $i_{ss}(t)$ is obtained via an indirect measurement of the voltage drop across a $R = 1\,\Omega$ resistor mounted on the connector SMA$_1$. This method, following the standard for the measurement of the conducted emission of ICs in the range from dc to 1GHz [11], has been selected among a limited number of possible alternative techniques, since it is simple to implement and has proved to demonstrate accurate results in practical applications [12].

The reconstruction of the source term $a(t)$ from the transient current measurement $i_{ss}(t)$ is obtained in the Laplace-domain by means of the backward application of the current division rule (see Fig. 4):

$$A(s) \approx I_{ss}(s)\frac{Z_e(s) + R + \tilde{r} + s\tilde{L}}{Z_e(s)} \tag{2}$$

The previous equation accounts for the contribution of the current generator $A(s)$ to the external current only. For the sake of simplicity, the ideal supply voltage battery, that provides a contribution for $s = 0$ (*i.e.,* for DC), is replaced by a short-circuit current. Also, the contribution of the capacitance $\tilde{C}$ in the scheme is neglected. As this capacitance is much smaller than that of Z_e (*i.e.,* , C) and, moreover, $\tilde{C}$ is masked by C and cannot be easily (if even possible) separated, it was decided to simplify the model by not considering the $\tilde{C}$ capacitance. For the class of devices at hand, the above simplifications do not impact on the accuracy of results and provide a clear view of the phenomena and a better understanding of the behavior of the external measured current. It is ought to remark that equation (2) is well-conditioned and turns out to be robust to measurement noise, since the transfer function arising from

the example devices of this study does not increase at high-frequency, thus does not amplify the measurement noise.

The information needed to process the measured current via (2) is the equivalent circuit of the board trace and the Norton equivalent impedance $Z_e(s)$. The lumped equivalent of the board trace can be estimated from the measurement carried out on a test structure or on a board implementing the setup of Fig. 4 without the IC mounted on it. In the latter case, the measurement of the scattering parameter response of the structure seen from the connector SMA$_1$ can be processed to fit the measured data to the response of the lumped equivalent. Similarly, the equivalent impedance, $Z_e(s)$, can be obtained by using the same setup of Fig. 4 from the S11 measurement of the scattering parameter response of the structure seen from the connector SMA$_1$ with the IC mounted on the board. As an alternative, the measurement of the on-chip scattering parameters of the core power delivery network of a memory chip has been proposed in [3], where partial results are available for the same test vehicle considered in this study. Once the port impedance at die-level is known, the actual impedance at the IC port is obtained by taking into account the package effects via electromagnetic modeling.

B. I/O buffers.

For conciseness, this section concentrates on the step-by-step modeling procedure for the generation of IC output port behavioral models. As outlined in Sec. II-B, a behavioral model of an input port can be considered as a special case only (see [6] for additional details).

In order to devise a robust modeling procedure from real measurements carried out on a test board, the general two-piece model structure defined by (1) is particularized as follows.

$$\begin{cases} i(t) &= w_H(t)[i_{sH}(v_{dd}-v) + i_{dH}(v_{dd}-v, \frac{d}{dt}\ldots)] + \\ & \quad w_L(t)[i_{sL}(v) + i_{dL}(v, d/dt)] \\ i_{dd}(t) &= w_H(t)i_{sH}(v_{dd}-v) + i_{dH}(v_{dd}-v, \frac{d}{dt}\ldots) \end{cases}$$
$$(3)$$

In the above equation, the output port current is a weighted combination of two submodels accounting for the buffer behavior in the fixed high and low logic states (*i.e.*, $i_{H,L}$ of (1)) that are split into the sum of a static $i_{sH,L}$ and of a dynamic $i_{dH,L}$ contributions to facilitate model estimation and to make the modeling procedure more robust. Also, the specific choice of the variables in (3) as well as the model structure for the description of the power supply current have been adopted to facilitate the parameter estimation from measurements by incorporating in the model equations the typical operation of CMOS output buffers. Specifically, the main contribution of the power supply current i_{dd} of a CMOS buffer is the one drawn during the driver operation in the high output state and therefore provided by the corresponding contibution of the output port current model in the high state.

Once the model structure (3) is assumed, the model parameters can be obtained via the following procedure that is based on the ideal setup shown in Fig. 5.
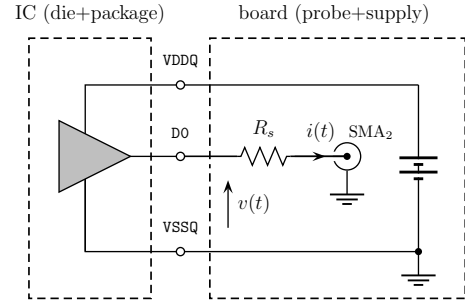

Fig. 5. Simplified equivalent of the setup used for the measurement of the port transient voltage and current of the I/O buffer of a digital IC. Current is indirectly measured through the voltage drop on the series R_s (e.g., R_s=47 Ω).

1) *Estimation of the buffer static characteristics.* In principle, the estimation of the device static characteristics $i_{sH,L}$ can be done by collecting a number of voltage-current pairs $\{v, i\}$ that are observed while an ideal voltage source is applied to the output port of the buffer and the source produces a DC sweep. However, to simplify the modeling setup and to avoid dedicated test fixtures for the extraction of the static curves only, a different solution has been proposed: the buffer under modeling is driven to produce a periodic "01" bit pattern on a transmission line load that is plugged into the SMA$_2$ connector of Fig. 5. A transmission line load forces the port voltage and current waveforms to produce a stepped response like the one shown in Fig. 6. Hence, the static values of the buffer characteristics are extracted from the flat parts of the responses [10], as shown in Fig. 6. It is worth noticing that the number of static points used to approximate the static characteristics of the buffer is defined by the number of steps that are in general $3 \div 5$ for typical buffer circuits loading $50\,\Omega$ distributed interconnects. Also, no specific care must be paid in designing the distributed load. A simple $50\,\Omega$ coaxial cable or the shunt connection of two cables are sufficient to generate a set of responses with some steps like the one of Fig. 6. The only design parameter is the line length, that decides the timing of reflections and the duration of the flat responses, and that must be chosen on the basis of the device transition times. Roughly speaking, a device with $300\,\mathrm{ps}$ rise time would require a $1.5 \div 3\,\mathrm{m}$ long transmission line.

2) *Estimation of the dynamical submodels.* The parametric models used for i_{dH} and i_{dL} in (3) are discrete-time parametric representations based on composite local linear state-space (LLSS) models [13], whose parameters can be estimated by standard algorithms as in [14]. The device responses used to feed the estimation algorithm are the slices of the voltage and current responses of Fig. 6 recorded while the buffer is in the high (low) logic state (see the portion of the signals highlighted with the labels (b) and (d)).

3) *Computation of weighting coefficients.* The weighting signals w_H and w_L are computed after the estimation of
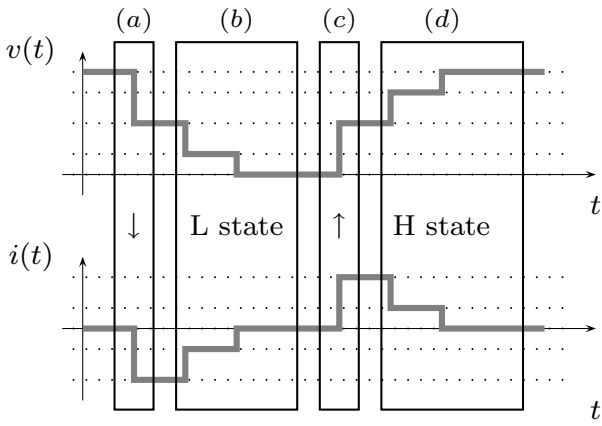
Fig. 6. Typical voltage and current transient response of the output port of a digital buffer obtained as suggested in step 1) of the modeling procedure. The horizontal dotted lines correspond to the static i, v pairs that can be extracted from the flat parts of the responses. Also, the different slices of the signals highlighted in the Figure are used to compute the parameters of (3) (see text for details).

the submodels $i_{sH,L}$ and $i_{dH,L}$ from the portion of the port responses of Fig. 6 occurring during state switching, as discussed in [6], [7] (see the slices labeled with (a) and (c) in the Figure). In our problem, this amounts to solving the single linear equation (3) of the output current where v and i are the advocated voltage and current responses recorded during a single transition event and w_L is assumed to be $w_L = (1 - w_H)$. In principle, such an assumption can be removed and two sets of port responses can be used to compute two independent w_H and w_L signals. However, the latter simplification benefits the quality of the complete model since it reduces possible ill-conditioning or inaccuracies of the solution of the linear problem arising from noisy measured data or from the approximated responses of the static and the dynamic submodels in (3).

4) *Model implementation.* Finally, the last step of the modeling process amounts to translating the model equations in a simulation environment. This can be done by representing the equation (3) in terms of an equivalent circuit and then implementing such circuit as a SPICE-like subcircuit. The circuit interpretation of model equations is a standard procedure that is based on the use of controlled-current sources for the static contributions, and on resistors, capacitors, and controlled source elements for the dynamic parts [6]. As an alternative, model (3) can be directly plugged into a mixed-signal simulation environment by describing model equations via metalanguages like Verilog-AMS or VHDL-AMS. In this paper, the obtained models have been implemented in SPICE.

It is worth noting that the ideal setup of Fig. 5 assumes that the series resistor R_s will be mounted as close as possible to the IC in order to neglect the possible effects of the board trace connecting the D0 ball to the SMD component. However, if needed, the effects of a possible board trace that is sufficiently long to perturb the measured signals can be de-embedded by

post-processing the voltage $v(t)$ and current $i(t)$ responses and thus by re-aligning the reference plane to the output terminals of the IC.

IV. MEASUREMENTS RESULTS

This section collects the results of the real measurements and data processing carried out on the example memory chip mentioned at the end of Sec. I. The results are based on a test board that has been suitably designed for the estimation of the model parameters. Additional details on the identification of the Norton equivalent of the IC core power network and on the buffer models are included as well.

A. Test board

Figure 7 shows the board designed for model estimation. It implements the basic features required by the ideal setups of Fig. 4 and Fig. 5. The board is composed of a general-purpose control circuitry for the operation of the device under test, and of a measurement board holding the IC under test and the measurement fixture. The measurement board is connected to the control board via a pair of 40-pin QTE connectors, and can be replaced to test different ICs. The memory controller, implemented in a FPGA, has been designed to allow the memory to operate at 66MHz and perform repeatedly the basic cycles (*Program, Erase, Read*).
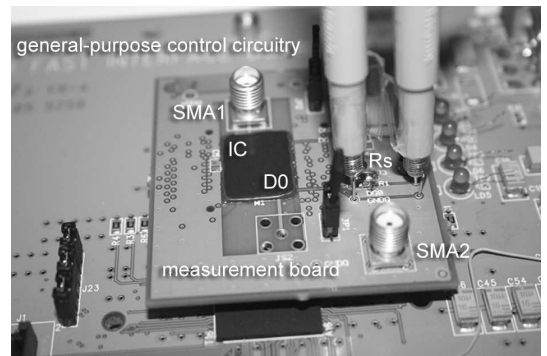

Fig. 7. Measurement board for the modeling of the core power delivery network and the buffers of the example test case. The key elements of the setup of Fig. 4 and Fig. 5 are clearly highlighted in the picture.

The indirect measurement of the transient currents via the voltage drop on series resistors was carried out with a LeCroy WavePro 7300A scope (3GHz bandwidth, 10GS/s). To reduce the effects of the measurement noise, the memory buffers have been forced to produce a periodic bit pattern and the averaging feature of the scope has been set (16 waveforms were considered for the average). The frequency-domain scattering measurements for the computation of the Norton equivalent impedance of the core delivery network has been carried out via a Agilent Vector Network Analyzer (VNA) E5071B (300 kHz to 8.5 GHz).

B. Core power delivery network

As outlined in the previous section, the connector SMA_1 of Fig. 7 has been used to measure both the frequency-domain

network function and the switching current of the IC core power network.

As an example, Fig. 8 shows the impedance seen by the connector that has been recorded with and without the IC mounted on the board. This Figure also compares the measurements with the responses of the lumped simplified equivalent circuits of Fig. 4 that has been estimated via simple fitting. The measured transfer functions in Fig. 8 shows some spurious resonances in a frequency region above 200 MHz that does not need to be modeled by a lumped equivalent accounting for the behavior of the IC. These effects are determined by the test fixture and by the package, and do not belong to the supply structure of the silicon device, that is generally dominated by a smooth capacitive behavior, as observed in a set of systematic on-wafer measurements carried out on the same test case [3].
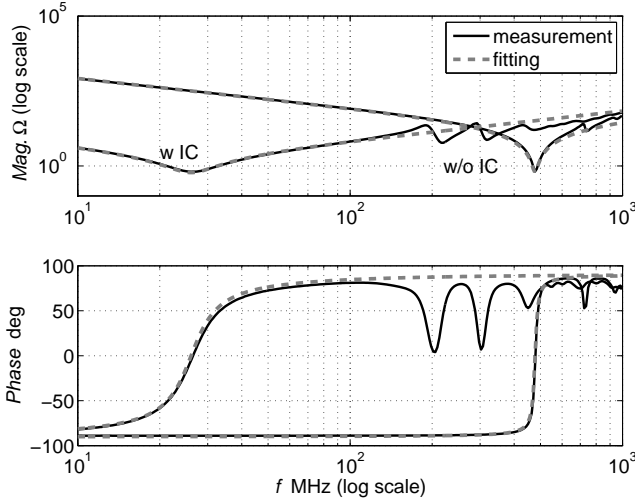
Fig. 8. Impedance seen from the connector SMA$_1$ of Fig. 4 with and without the IC mounted on the board. Solid lines: real measurement carried out on the test board of Fig. 7; dashed lines: prediction obtained via the simplified lumped equivalents of Fig. 4. The values of the circuit elements were estimated via simple fitting ($\tilde{r} = 0.6\,\Omega$, $\tilde{L} = 5.8\,\text{nH}$, $\tilde{C} = 19.15\,\text{pF}$, $Z_e(j\omega) = 1/sC + r + sL$, $r = 0.1\,\Omega$, $L = 5\,\text{nH}$, $C = 3.45\,\text{nF}$)

Figure 9 shows a slice of the measured transient current $i_{ss}(t)$ observed during the erase operation phase and its frequency-domain spectrum. As outlined in Sec. II-A, the response $i_{ss}(t)$ of Fig. 9 is used to compute the Norton current source $a(t)$ via equation (2). Figure 10, in which the measured response and the estimation of the short-circuit current are shown, confirms the feasibility and the robustness of the proposed approach. It is worth noticing that the processing leading to the curve of Fig. 10 is robust to measurement noise. This can be appreciated by the magnitude of the transfer function defining (2) that is shown in Fig. 11.

C. I/O buffers

The model of the output buffers is based on i_H and i_L submodels (see eq. (1)) defined as sum of a static and a dynamic part. The static part is extracted from the measured responses of Fig. 12, that are obtained by driving the buffer to produce a periodic '01' sequence on a transmission line load. It is worth to remark that the design of the transmission
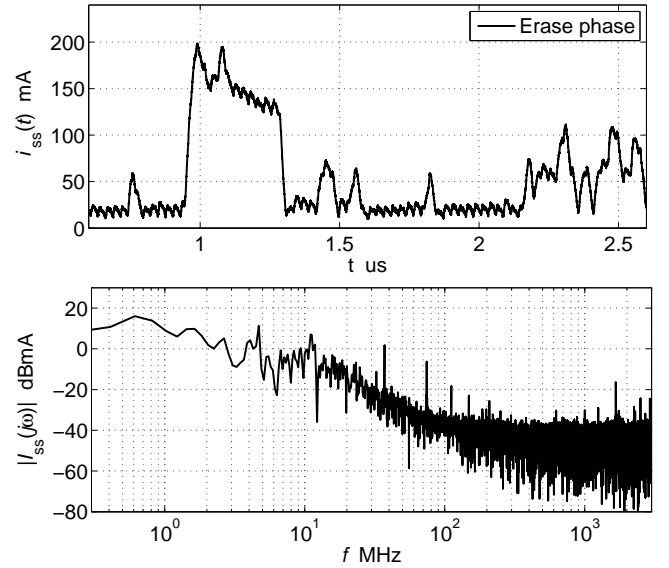
Fig. 9. Portion of the measured transient current $i_{ss}(t)$ carried out on the example commercial memory chip (top panel) and its related amplitude spectrum (bottom panel).
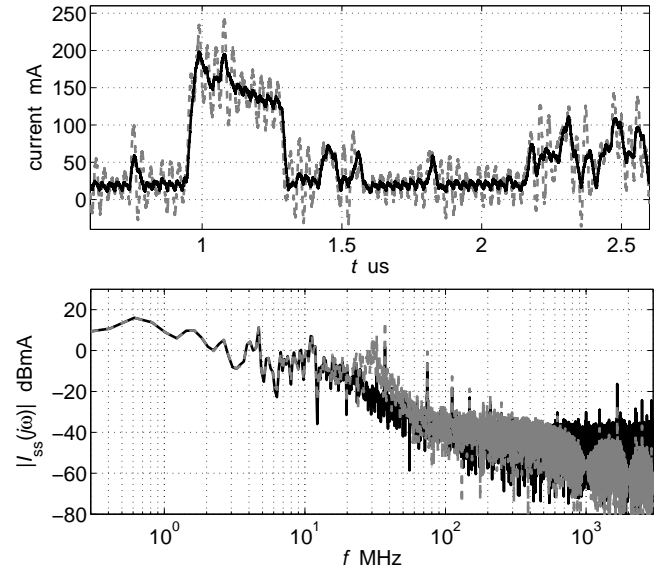
Fig. 10. Top panel: measured transient current $i_{ss}(t)$ of Fig. 9 (solid black curve) and short-circuit current $a(t)$ of the Norton equivalent computed via equation (2) (dashed gray curve). Bottom panel: corresponding amplitude spectrum of the measured and computed currents.

line load to be connect to the SMA connector of Fig. 4 is not critical. An open ended line with characteristic impedance and line length that allows to observe a limited number reflections and steady state operation during the flat parts is adequate for model estimation. In this specific example, the shunt connection of two 2.3 m long RG58 coaxial cables is used. The $\{i, v\}$ pairs corresponding to the flat parts of the waveforms of Fig. 12 are shown in Fig. 13, which proves the excellent accuracy of the static behavior extracted by this approach. The remaining model parameters, including the dynamic parts of submodels and the weighting signals are
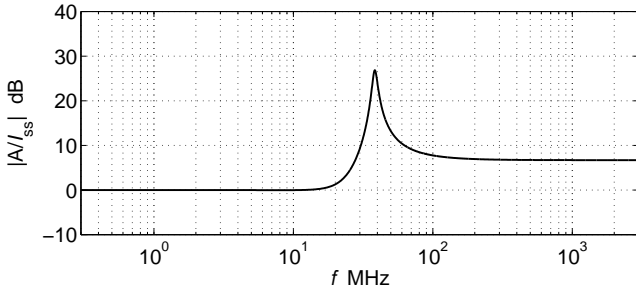
Fig. 11. Magnitude of the transfer function defined in (2) and the values obtained from the fitting of Fig. 8.

estimated as suggested in [7] from the edges of the waveforms of Fig. 12. As an example Fig. 14 shows the signal $w_H(t)$ for the up ($\uparrow$) and the down ($\downarrow$) state transition events computed by linear inversion of model equation superimposed to a possible simple analytical approximation of the signal. It is worth noting that, to possibly reduce the effects of measurement errors, the analytical approximation of the weighting signal by means of smooth functions contribute to the improvement of the model accuracy. Also, due to the typical smooth sigmoidal shape of the weighting signals, the approximation carried out by means of a tanh function and two gaussian functions has been proven to be enough to provide accurate results.
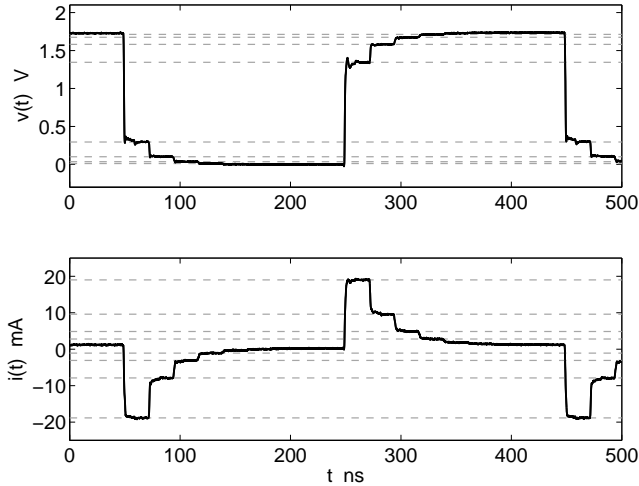
Fig. 12. Responses obtained by driving the buffer DQ0 in Fig. 5 to produce a periodic '010' bit pattern on suitable transmission line load. The dashed lines highlight the steps of the voltage and current responses allowing for the extraction of the static parts of submodels i_H and i_L.

As already done for the power supply case, Fig. 15 shows the amplitude spectrum of current $i(t)$.

The waveforms corresponding to the validation of the complete buffer model built in this way are shown in Fig. 16. This Figure compares the measured and predicted responses of the modeled buffer for two loads different from those involved in the parameter estimation process. The first test corresponds to the buffer connected to a resistive load, *i.e.,* the series connection of the SMD R_S resistor of Fig. 5 and a $50\,\Omega$ termination plugged into the connector SMA$_2$. In the second test, the load consists of a $4\,m$ long RG58 coaxial
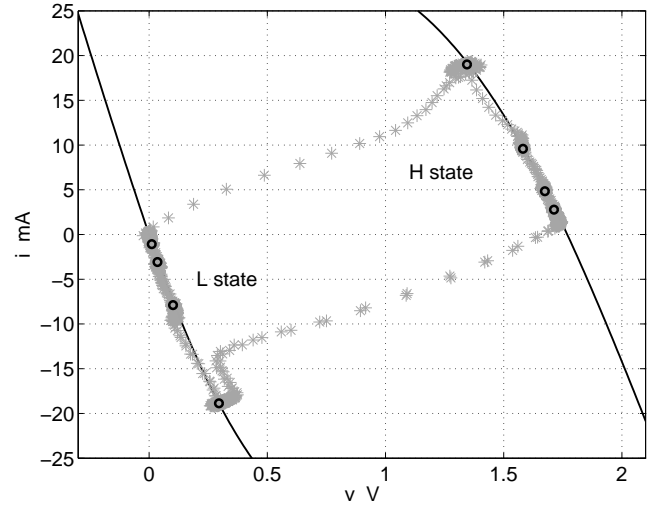
Fig. 13. Static characteristics of the DQ0 buffer. Solid lines: transistor-level response; gray stars: region explored by the $v(t),i(t)$ samples of the transient responses of Fig. 12; Circles: static points extracted from the curves of Fig. 12.
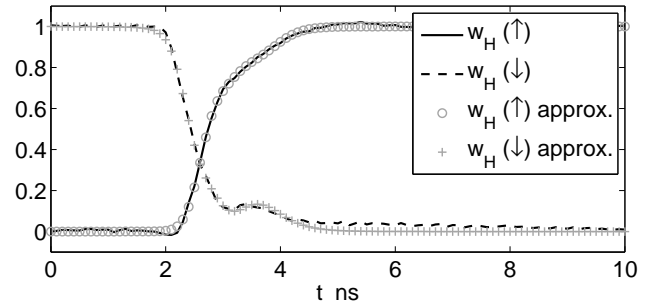
Fig. 14. Weighting coefficient $w_H(t)$ estimated during the up ($\uparrow$) and the down ($\downarrow$) transition events.

cable terminated by a $82\,pF$ capacitor. Both the response of the estimated model and the reference response of the high-order transistor-level model of the buffer provided by the foundry are shown in the Figure.

The very good agreement among the curves of Fig. 16, for different loading conditions, confirms the strengths of the proposed methodology in generating accurate models from measured transient responses. Such models can be easily obtained by the proposed measurement setup and can effectively replace the hardly available and less efficient transistor-level models of ICs.

Fig. 15. Amplitude spectrum of current $i(t)$ of Fig. 12.