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On the Integration of Behavioral Component Descriptions in the Full-Wave Transmission-Line Modeling Method

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Abstract- The simulation of complex digital systems incorporating ICs, lumped components, and field phenomena is a necessary activity for many applications. Predicting the practical behavior of systems based upon just schematical circuit diagrams (which indicate topology) fails to include the consequences of field effects (which require geometrical information), which given the ever increasing frequencies of modern digital systems, are of paramount importance. On the other hand, comprehensive simulation of IC packages using full-wave models is prohibitively computationally expensive and time consuming to complete. Embedding behavioral level descriptions of complex electronic components within a full-wave field solver circumvents these problems, and forms the subject of this paper. The Transmission-Line Modeling (TLM) method is used as the full-wave solver, and two behavioral models, “macro” and “IBIS”, are embedded into the TLM to model the sources and loads presented by complex ICs. The two methods of representing the IC behavior are then illustrated and compared with a canonical test structure.

1. INTRODUCTION

Behavioral models seek to reproduce the input/output port nonlinear behavior of digital integrated circuits (ICs). For example, IBIS (Input/Output Buffer Information Specification) standard [1][2] describes a component by using a collection of voltage and current lookup tables. Macromodels on the other hand, rely on a local linear state-space parametric representation of the currents as a function of the voltages [3]. Both descriptions hide the IC internal structure and enable the insertion of active components as sub-structures within circuit simulators or full-wave solvers. The last option greatly increases the EM simulator capacity where the ideal diode is the only fully inserted nonlinear device. Also, a wider selection of systems can be efficiently modeled. This is both commercially and technologically essential for accurate prediction of electromagnetic compatibility and signal integrity of high-speed electronic applications.

The Transmission-Line Modeling (TLM) [4] method offers a suitable environment for incorporating active non-linear models. The method exploits the analogy between field propagation in space and voltage/current propagation in a transmission-line network. It has the advantage of calculating field components at the same time and at the same location, with guaranteed stability due to the underlying electrical circuit formulation [4]. Coupling IC behavioural models can be realised in two ways: either through an external link to a circuit simulator such as SPICE [5], or by direct embedding [6]. The first approach gives access to a wide range of models via the SPICE libraries. Unfortunately, the calculation speed is hindered due to the repeated need to invoke SPICE for every time-step of the EM solver. The second option removes the slow speed problem. It forms the subject of this paper which builds upon the previous macromodel research [7] to include an IBIS description of a component. Since the IBIS standard is widely used in industry, it offers a wide device selection that can be inserted without the need to use the

SPICE libraries. The paper is organized as follows. Section 2 reviews the IBIS component description while section 3 develops the new IBIS-TLM interface. Finally, section 4 provides a comparison of the TLM-IBIS and TLM-macromodel hybridization before concluding with a discussion on the topics raised and further research suggestions.

2. REVIEW OF IBIS

The IBIS file of a component contains a collection of lookup tables of voltages (V) and currents (I), along with temperature ranges, package parameters (resistance, inductance, and capacitance), die capacitance, voltage ranges and pin configurations. The tables define the I-V relationship of the pullup/pulldown transistors' and clamping diodes of the generic buffer shown in Figure 1. This representation enables the consideration of the input and output ports of a complex device while removing the need to model the internal device structure.

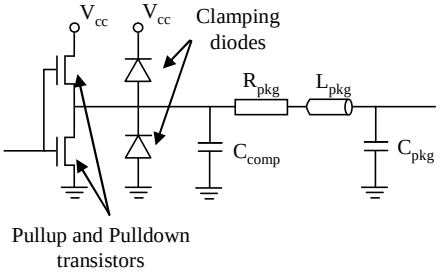

Figure 1 – IBIS buffer representation. I-V tables are stored for each of the components (pulldown and pullup transistors and the clamping diodes).

Depending on the input or output port, the I-V tables differ. For a receiver, only one or both of the clamping diodes are actually necessary. For a driver, the clamping diodes along with the transistors are considered. The inclusion of all or just some of the clamps/transistors is device dependant. Reference [2] contains the methodology behind the IBIS I-V tables and their usage. It also details on how the current is determined as a function of the incident voltage. We will assume in the following that the IBIS current is calculated as in [2] and focus solely upon the interface of IBIS with TLM.

3. TLM - IBIS INTERFACE

TLM is based upon the analogy between the propagation of electromagnetic fields and voltage impulses traveling on transmission-lines. In its simplest form the TLM method discretizes a homogenous space into cubes of side Δl, termed nodes. Voltage impulses scatter at each node according to network theory and subsequently propagate to the neighboring nodes. At any one time-step there are two quantities present upon each transmission-line connecting to each node, the reflected voltage V^r and the incident voltage V^i. Repetition of this scatter-propagate procedure provides an explicit and stable time stepping algorithm that mimics electromagnetic field behavior [4]. For our purposes, this description of TLM is adequate.

Figure 2a shows the new IBIS-TLM interface. It consists of a 1D TLM line, called 'circuit TLM', linking the 3D TLM mesh to the IBIS model. The circuit TLM contains the IBIS package components through the R_{pkg} resistance and Z_{pkg} impedance, calculated from the inductance and capacitance package values. It also includes the IBIS die capacitance C_comp through the TLM link-node impedance Z_{C_comp}. The circuit TLM is connected to the TLM mesh at the boundary of a single cell. The cell is defined by the free space impedance Z_0, which entails a change in impedance at the connection. This is solved using the standard TLM

formulation [4]. On the other side, the circuit TLM is interfaced to the IBIS component description. At that level the situation is complicated by the non-linear nature of the IBIS termination. Figure 2b presents the Thevenin circuit at the interface. For the case of a driver, V_{Drv} is the IBIS source voltage, *i* is the current provided by the IBIS load, while V^r is the reflected voltage from the TLM node interfacing with the IBIS boundary. The subscript *k* denotes the TLM time-step.

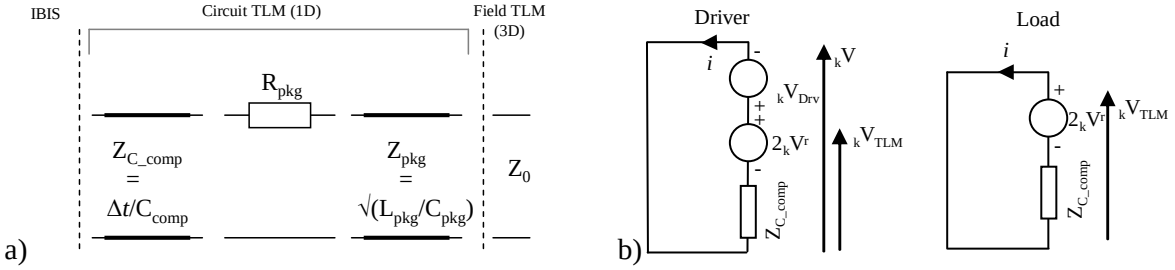

Figure 2 – IBIS-TLM interface: a) Circuit TLM. Δ*t* is the temporal sampling of the TLM model. b) Thevenin circuits for the IBIS driver and load interfaces.

For the driver, the non-linear equation at the interface between IBIS and TLM at time-step *k* is

$$2_k V^r - iZ_{C\_comp} - {}_k V_{Drv} - {}_k V = 0 . \qquad (1)$$

The conventional Newton-Raphson method is used to solve for the unknown quantities (*i* and V) using the IBIS lookup tables to define *i* given V [2]. Knowing V, the reflection of the IBIS termination at the TLM port can be calculated as

$${}_k V^i = {}_k V - {}_k V^r + {}_k V_{Drv} . \qquad (2)$$

where the IBIS term (V_{Drv}) is now injected onto the TLM node. In this manner the IBIS termination is completely defined from the TLM perspective. Equations 1-2 are repeated for each time-step of the TLM simulation. In a similar fashion, the load interface is given by

$$2_k V^r - iZ_{C\_comp} - {}_k V_{TLM} = 0 , \qquad (3)$$

where it is seen the IBIS voltage and TLM voltage are the same. The incident TLM voltage is ${}_k V^i = {}_k V_{TLM} - {}_k V^r$, since the IBIS source term is no longer present. Equations 1-3 allow the embedding of an IBIS description of a component as a boundary condition to a TLM node. The Newton-Raphson procedure typically converges within 5-10 iterations, so is of limited computational impact in comparison to the TLM simulation.

4. MACROMODEL AND IBIS COMPARISON

In this section we provide full-wave simulation results obtained with a simple microstrip test structure and the embedding of the macromodel and IBIS behavioral models. The macromodel-TLM hybridisation [7] is based on the Z-transform TLM formulation [8]. This TLM form enables a device insertion at the node center through a current source or the component of the conductance device-oriented. The macromodels are generated from the Mπlog (Macromodeling via Parametric Identification of LOgic Gates) software [3] using the HSPICE model supplied by the IC manufacturer. The models are established with a sampling time T_s different from the TLM time step Δ*t*, they are thus resampled to Δ*t*.

Figure 3 describes the test structure. It consists of a SN74AHC1GU04 single inverter IC [9] that drives a 50Ω microstrip line loaded by a second SN74AHC1GU04 IC. The strip is 0.8mm wide, 100mm long, zero-thickness and perfectly conducting. The substrate is 0.4mm thick with a relative permittivity ε_r = 4.24 and assumed lossless. For IBIS-TLM, the dielectric permittivity of the substrate is included through the use of stubs [4]. The configuration is surrounded by matched boundary conditions in the lateral and top faces and a perfect electric conductor at the substrate base.

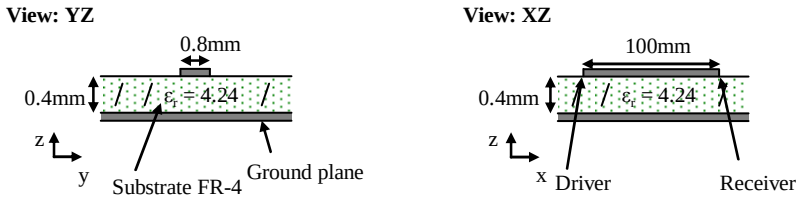

Figure 3 – Test structure. 50Ω microstrip track on FR4 substrate of height 0.4mm and track width 0.8mm. The driver inverter feeds the line at *x*, and the load inverter is placed at *x* + 100mm.

The behavioural models are embedded in a single TLM cell: at the cell boundary for the IBIS-TLM and through a current source at the cell centre for the macromodel-TLM. The driver and receiver are located at the x = 0 (10.4) and x = 100 (110.4) mm nodes for the IBIS (macromodel) simulation. The macromodels are created under the power supply: V_{CC} = 4.4V; V_{ref} = 0V. It has to be noticed that the macromodel has no internal link between receiver and driver for a single IC, so it is not possible to measure both at the same IC.

Figure 4 presents the results for both full-wave simulations with V_{CC} = 4.4V, the spatial sampling Δl = 0.4mm, the temporal step Δt = 0.67ps, and for a 10MHz signal.

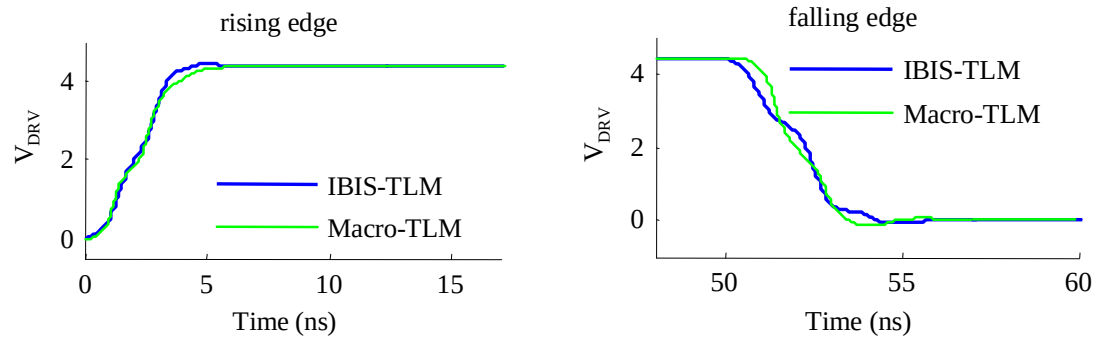

Figure 4 – Rising and falling edges of the voltages for macro and IBIS models embedded into the TLM full-wave model of Figure 3. Δ*l* = 0.4mm, Δ*t* = 0.67ps.

The results indicate a close match between the two modelling methods for the rising edges at the driver and receiver, with a slight overshoot for the IBIS-TLM. The falling edges do not match as closely, but the same behaviour is observed. The differences can be explained by 1) the package parameters and die capacitance (only for IBIS model) that differ and 2) the process to generate the models. For example, to check the macromodel behaviour (before running the EM simulation), HSPICE simulations have been carried out. One with the transistor description of the IC; the other one with the driver and receiver macromodels. The results suggest a model limitation as the ripple presence on the falling edge of the driver does not appear with the transistor description model. In fact, the macromodels are generated under long transmission-line hypothesis while we are dealing here with a short transmission-line (propagation delay about 0.67ns).

5. CONCLUSION

The paper reported on the use of behavioral models within the full-wave field solver TLM. The formulation of the new IBIS component description when embedded into a TLM node was given. It was seen the behavioral component descriptions can be placed at a node centre or boundary, and that the choice between the two does not affect the results. IBIS component descriptions are widely available from IC manufacturers, and so, by successfully embedding an IBIS model into TLM, the paper has demonstrated the wide scope for using behavioral models inside field models. The inclusion of a complete IC port using only a single TLM node, minimizes the runtime of the numerical simulation, while allowing the modeling of complex components and devices. Future work will look at experimental validation of the results and the embedding of more complex structures, attempting to form a link between the input and output ports on a single IC using the IBIS model.

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