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# A New Built-In Current Sensor Scheme to Detect Dynamic Faults in Nano-Scale SRAMs

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***Abstract*—Technology scaling has made possible the integration of millions of transistors into a small area allowing the increase of memory's density. In this scenario, new defects generated during the manufacturing process have become important and challenging concerns for Nano-Scale Static Random Memories' (SRAMs') testing. Thus, functional fault models, traditionally applied in SRAMs' testing, have become insufficient to correctly reproduce the effects caused by these defects. In more detail, new memory technologies have introduced new defects that cause dynamic faults, a previously unknown type of fault. In parallel, the rapidly increasing need to store more information results in the fact that the memory elements occupy great part of the System-on-Chip (SoC) silicon area. Therefore, memories have become the main responsible for the overall SoC yield. In this context, we propose a new Built-In Current Sensor (BICS) scheme to detect dynamic faults associated to resistive-open defects in SRAMs. Experimental results obtained throughout electrical simulation demonstrate the BICS's fault detection capability. Finally, we lay out the benefits and limitations of the BICS's adoption and point out the direction of future works.**

***Keywords: SRAM; Resistive-Open Defects; Dynamic Faults, BICS, Power Consumption.***

## I. INTRODUCTION

Advances in Very Deep Sub-Micron (VDSM) technology have made possible the integration of millions of transistors into a small area, allowing the increase of circuits' density. In parallel the rapidly increasing need to store more information results in the fact that the Static Random Access Memories (SRAMs) occupy great part of the System-on-Chip (SoC) silicon area. This is confirmed by the SIA Roadmap which forecasted memory density to approach 94% of the SoC area in about 10 years [1]. Consequently, memory has become the main contributor to the overall SoC area. In this scenario, technology scaling has led to the development of new fault models which differ from the traditional functional ones usually adopted by SRAM testing, such as stuck-at, transition and coupling faults [2]. In more detail, functional fault models have become insufficient to model the effects produced by some specific defects that can be generated during the manufacturing process and consequently guaranteeing a good test efficiency [5].

Nowadays, resistive-open defects have become one of the most significant problems in VDSM technologies due to the presence of many interconnection layers and an ever growing number of connections between each layer [5]. The importance of resistive-open defects is analyzed and pointed out as the most common cause of test escapes in deep-submicron technology in [4]. In general terms, a resistive-open defect is defined as a defect resistor between two circuit nodes that should be connected [3]. Moreover, this type of defect generally causes timing dependent faults, which means that a two-pattern sequence is usually necessary to sensitize theses faults [14]. According to [15], faults requiring more than one sequentially operation in order to be sensitized are called dynamic faults. Moreover, based on Poison Distribution, resistive-open defects of small size are more probable than larger size defects [16]. Further, the distribution of weak resistive-open defects found in back-end defect monitors is directly correlated to the number of dynamic faults [16]. However, it is important to highlight that currently most used tests are designed for static faults, which are faults sensitized by performing at the most one operation [15], and therefore may not be able to detect dynamic faults. Industrial experiments done at STMicroelectroncis and at Intel show the inability of standard March algorithms to detect dynamic faults and have been reported in [16]. Indeed, dynamic faults require specific test sequences and in contrast with stuck-open faults, resistive-open detection should be performed at-speed. Thus, to provide the detection of dynamic faults in SRAMs is a significant challenge, since it depends on speed testing, and it also demands a large number of operations on each memory cell, generally greater than 24 consecutive reads per memory cell, which is hard to achieve at lower budgets [16].

To finalize, it is important to point out that transistor miniaturization introduces a new challenge related to static power consumption in VDSM circuit design. In more detail, SRAM leakage power has become a more significant component of total chip power, as a large portion of the total chip transistors comes from on-die

SRAM [17]. Indeed, the SRAM cell is particularly sensitive to process variation, as the minimum size of transistors is typically used in the SRAM cell in order to achieve its high density. Detection of such defects is critical for application, where an SRAM memory cell can be respectively accessed at-speed, near to its cycle time, for a very large number of clock cycles. These lengthy read scenarios are not feasible during manufacturing tests. Thus, a defective 6T memory cell which escapes a March test proposed in [16] can still fail in field, after a number of consecutive reads due to weak resistive-opens at its nodes. In this context, the development of new at-speed test solutions able to provide detection of dynamic faults while guaranteeing the minimal leakage power consumption has become essential.

Thus, the goal of this paper is to investigate the possibility to adopt Built-In Current Sensors (BICSs) to detect dynamic faults associated to resistive-open defects in nano-scale SRAMs. The main idea behind our approach is to develop a new BICS scheme, able to monitor the current that flows through the SRAM cell and that provides detection of the targeted faults. The evaluation of the proposed approach has been accomplished considering the BICS's fault detection capability and the leakage power consumption impact of the new BICS scheme on the SRAM's total power. In more detail, we have modeled the dynamic faults according to [14] and identified different values for the resistors able to generate the targeted faulty behavior. The effectiveness of the BICS proposed in this paper has been evaluated through electrical simulations based on 65nm technology library. Finally, we analyzed the impact of the leakage power consumption of the proposed approach.

This paper has been organized as follows: In Section II, we detail the fault model adopted and point out some important aspects related to the BICS presented in [9][10]. Section III presents the new leakage power-aware BICS. In Section IV, we summarize the experimental results. In detail, we present the electrical simulations associated to the fault modeling, the fault detection capability of the BICS as well as the leakage power consumption and area overhead introduced by the proposed technique. Finally, in Section V we draw the conclusions.

## II. BACKGROUND

The technique proposed in this paper aims to detect dynamic faults associated to resistive-open defects produced during the nano-scale SRAMs' manufacturing process. In this section we describe the fault model adopted as well as the structure of BICS presented in [9][10]

### A. Fault Model Adopted

The standard six-transistor CMOS SRAM cell is composed of four transistors that form two cross-coupled CMOS inverters and two NMOS transistors that provide read and write access to the cell. In this paper, we address to detect dynamic faults associated to resistive-open defects. In [14], dynamic faults associated to resistive-open defects have been classified as follows: A cell is said to have an *dynamic Read Destructive Fault* (dRDF), if a write operation immediately followed by a read operation performed on the cell changes the logic state of this cell and returns an incorrect value on the output. Fig. 1 shows the scheme of a standard six-transistor SRAM cell, where it is possible to see the resistor (*Df*) used to model the dRDF.

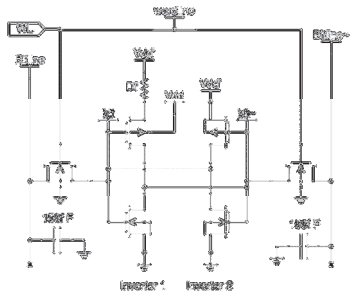

Figure 1. Six-transistor SRAM cell with *Df* associated to dRDF

According to [14] a resistive-open defect in the pull-up of one of the core-cell inverters, as *Df* in Fig. 1, is a classic hard-to-detect fault. More details about the behavior of dynamic faults are available in [14].

It is important to highlight that according to the resistance value, the fault behavior can be different and consequently the fault is detected by different operation sequences. According to [14] the number of read operations necessary to detect a dRDF is inversely proportional to the resistance value of the injected *Df*. Thus, the resistive defect range and the number of read operations required for detection in a specific technology are dependent on the following parameters [16]:

- *Cell Ratio:* the defect depends on the ratio of the access transistor's resistance and pull-down nMOS.
- *Access transistor (Word Line) on-time to off-time ratio for read operation*: Within each read cycle the accumulated charge must be discharged before the next operation.

### B. Built-In Current Sensors for SRAMs

In the past, BICSs have been proposed for Built-In Current (BIC) testing of static CMOS circuits [11][12]. In general terms, BIC testing involves the monitoring of power bus currents in a VLSI circuit in order to detect malfunction-causing defects. Thus, BICSs have been proposed to detect physical defects by monitoring abnormal quiescent currents identifying and facilitating the rejection of defective parts. Later, the use of BICSs has been proposed to provide on-line concurrent detection of radiation-induced leakage currents in circuits [8]. In more details, each BICS monitors the power-bus static current of these circuits to detect excessive current consumption. This excessive current consumption is compared to a predefined reference value in order to

detect radiation-induced multiple parametric failures and system power supply breakdowns. Moreover, BICSs have been presented as a very interesting solution to provide transient fault detection for SRAMs in radiation-exposed environments [9][10]. Recently, BICSs have been proposed to improve the reliability of H-tree RAM memories [13].

The technique presented in [9][10] is based on the idea to monitor the SRAM power-bus by using BICS circuits in order to detect abnormal current dissipation resulted from Single-Event Upsets (SEUs). Thus, the current checking is performed on the SRAM columns and it is combined with a single-parity bit per RAM word to perform error correction. Fig. 2 shows the current sensor's schematic composed of a sensing cell followed by an asynchronous latch. In detail, BICSs are placed on the memory's vertical power lines in order to indicate the bit position on which a failure has occurred. Thus, when a SEU occurs in the corresponding memory column, an internal latch is set. A parity check makes the localization of the affected word possible and thus allows error correction.

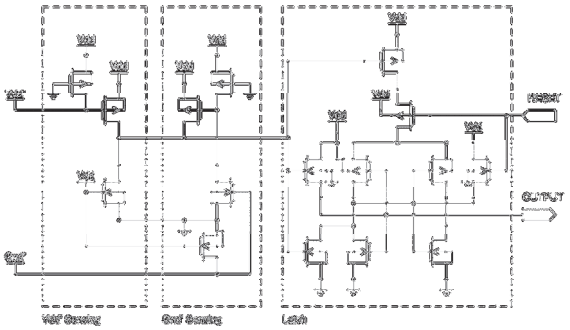


Figure 2. Built-In Current Sensor (BICS)

## III. THE PROPOSED BUILT-IN CURRENT SENSOR

The main idea behind BICSs is to measure the steady state power supply current, assuming that in steady state, when all switching transients are settled down, a fault-free CMOS circuit dissipates almost no static current. Thus, considering defects like resistive-open defects a conduction path from power supply (*Vdd*) to ground (*Gnd*) may induce a significant increase of the steady-state current. Therefore, monitoring current makes possible the detection of faults associated to this type of defects. It is important to point out that the BICS presented in [9][10] worked perfectly for older technologies above 100nm. However, due to the fact that the steady-state current of transistors for technologies below 90nm is not negligible anymore and consequently there is no sufficient difference between dynamic and static currents, the effectiveness of the BICS to detect these faults has been drastically affected. In detail, the previous proposal of the BICS is not appropriated to a nano-scale technology anymore due to the following aspects:

- The BICS is not pre-excited and consequently a great variation at the *Vdd'* node would be necessary in order to flip the inverters' state. Indeed, the previously presented BICS measures the current at both the *Vdd* and the *Gnd* node.
- It has no activation/deactivation control (bypass) and consequently monitors the signals during all instances of time.

Thus, a new BICS has been developed taking into account two of the new challenges posed by the nano-scale technology: (1) the emergence of new manufacturing defects leading to new types of faults, such as dynamic faults and (2) the increase of leakage power as a contributor to the circuits' total power consumption. When the access transistors of the cell are deactivated, the Word Line (WL) signal activates the BICS that captures the current's magnitude. If an abnormal current flows through the cell, the BICS indicates the faulty behavior. The proposed BICS is composed of four stages; the first one is the Voltage Reference Generator, which can be shared between many BICS, and three more stages in series. The components of the BICS are described below:

- Voltage Reference Generator (VRG): it is an inverter in closed loop, whose output is connected to its input, so that the voltage at that node, or the balancing point between the pull-up pMOS device and the pull-down nMOS, will be exactly the inverter's threshold voltage. Simulations have shown that the perfect relation between nMOS and pMOS devices is given by a ratio width:size of 21:40 (typical corner). In this configuration both active devices will conduct the same amount of current. Therefore the voltage in the VRG's transistors is of exactly one half of the nominal *Vdd*, or theoretically of 0.55V. The VGR generates 542.5mV, the pMOS device has 0.30um of width while the nMOS has 0.21um, making the pMOS stronger then the nMOS and consequently the voltage output will be lower then 0.55V. Further, a high threshold voltage has been used in order to obtain a lower static power dissipation. Due to the fact that the VRG is operating in the linear zone, instead of the saturation or cut zone, as digital circuits do, the static power dissipation never becomes zero.
- Sensing Inverter (SI): It is implemented to sense *Vdd'* drops that occur when the bypass feature is turned off and consequently current drains from the *Vdd'* to the *Gnd*. The SI is composed of a pull-up transistor connecting *Vdd* and *Vdd'*, that can be bypassed, and an inverter in between *Vdd'* and *Gnd*. The pull-up transistor is a pMOS device working as a resistor. In case of a high current flow a detectable *Vdd'* drop occurs and since the pMOS source of the inverter is connected to the *Vdd'* node, the voltage of the source and gate of the pMOS decreases. As consequence the weaker current flowing through the pMOS device leads the inverter's output to *Gnd*. As mentioned the

pull-up transistor has a bypass, composed of a pMOS device that connects the *Vdd'* to *Vdd*, redirecting the current's flow around the pull-up transistor avoiding that any *Vdd'* drop occurs while the bypass signal is activated and consequently no fault will be detected by the SI. To conclude, the proposed SI has been calibrated to produce an output of 470mV in idle state when the input is of 542mV. The inverter devices are *High-*$V_{Th}$, which results in a low leakage current. Further, the pull-up transistor is *High-*$V_{Th}$, so high impedance can be obtained avoiding the over-sizing of the transistor. For the same reason the bypass transistor is *Low-*$V_{Th}$ and consequently it can drain much more current when its default size is adopted. However, it is important to note that the current drained will still increase when the width is changed to 1.20um.

- Amplifying Inverter (AI): It is a conventional inverter connected to the global *Vdd* and the *Gnd*. The AI detects output voltage drops of the previous stage (SI) generating a high voltage output. The AI's output has been calibrated to be of 287mV while its input is of 470mV. The controlled output voltage aims at not triggering the Latch erroneously. The AI's threshold voltage is of 450mV and consequently when the input node receives a lower voltage the output value is adjusted in direction of the *Vdd*. In order to guarantee a threshold voltage of 0.45V, the inverter has been designed using one *High-*$V_{Th}$ pMOS and one *Low-*$V_{Th}$ nMOS transistor, because under this configuration the nMOs is stronger than the pMOS and consequently a lower voltage is able to invert the output.
- Latch (L): L is composed of two NOR logic gates, each one composed of only *High-*$V_{Th}$ devices in order to avoid unnecessary power dissipation. The first three stages of the BICS have been calibrated to assure that sensitized as well as non sensitized dynamic faults trigger the L's output to be of 1.1V until reset.

Fig. 3 depicts the schematic of the BICS proposed in this paper.

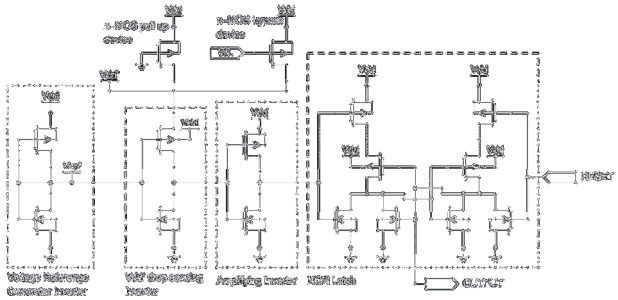

Figure 3. Schematic of the new BICS

Finally, the BICS aims at observing the current variations. It is pre-excited and therefore a small voltage drop at the *Vdd'* node triggers the L and a flag indicates a faulty behavior. The BICS has been calibrated to trigger when detecting a *Vdd'* drop of 4mV. In order to calibrate this value, the pull-up pMOS's length and width have to be accurately defined in order to assure 4mV between drain and source of this transistor at the desired triggering current. Due to the fact that the BICS is pre-excited, it operates in the linear zone of the transistor and consequently always dissipates static power. Thus, to minimize this side effect 14 of the 16 MOS devices are *High-*$V_{Th}$.

## IV. EXPERIMENTS

In this section, we present the results obtained during electrical simulations performed with Synopsys HSPICE. To do so, we modeled dRDFs associated to resistive-open defects following the scheme presented in Fig. 1. The main goal of the experiments performed was to evaluate the effectiveness of the BICS proposed in this paper to detect dynamic faults associated to resistive-open defects in SRAMs. In order to reduce the simulation time, the experiments have been performed on a simplified memory circuit that is composed of the following structures: (1) one six-transistor SRAM cell, (2) sense amplifier and (3) read and write buffers. Fig. 4 depicts the memory circuit adopted during the electrical simulations. It is important to note that the SRAM cell has been connected to *Vdd'*, which is the *Vdd* monitored by the new BICS, instead of being connected to *Vdd*. The memory is accessed each 5ns, the pre-charge and discharge periods are of 2ns, the data assimilation period is of 0.5ns and finally the idle period is of 0.5ns. Moreover, the Word Line (WL) on-time for write operations is of 0.5ns and 2ns for read operations.

The simplified memory circuit and new BICS have been mapped onto a commercial 65nm CMOS technology provided by STMicroelectronics. Indeed, the electrical simulations have been performed adopting the typical process corner, supply voltage of 1.1V and 27ºC as temperature.

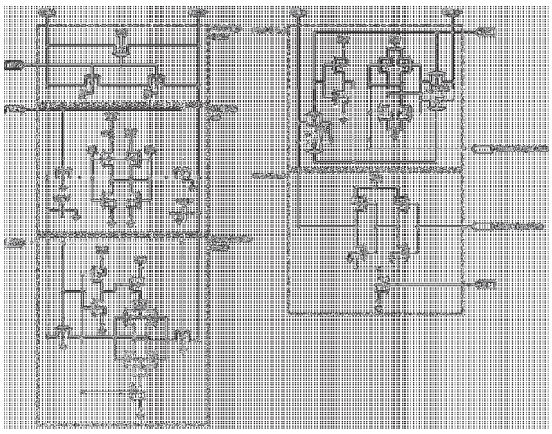

Figure 4. Schematic of the adopted circuit

### A. *Fault Modeling*

A resistive-open defect between the cell's inverters and *Vdd* and *Gnd* can sensitize dRDFs when at-speed read operations are performed consecutively. In other words, to model this type of fault, a resistor has to be placed according to the scheme presented in Fig. 1.

In order to better understand the faulty behavior induced by *Df*, it is assumed that the defective cell stores the value '0'. The Bit node voltage, which is initially of 0V, is driven up due to the voltage divisor's effect created by the access nMOS transistor and the nMOS of the Inversor 2. Due to the fact that the Inversor 1 is defective, it pulls down the Bit'. When the access transistors are deactivated, the cell tends to return to the value stored before the read operation, where the voltage of the Bit is of 0V and on the Bit' is of 1.1V. In a defectless cell, this effect happens very rapidly. However, inappropriate impedance inside the cell causes longer stabilization time and therefore keeps the Inversor 2 longer in linear state. As a consequence, a higher current can be observed at the *Vdd* node until the cell reaches stabilization. In fact, the BICS detects the dRDF by identifying the above described abnormal current. When considering the write operation performed on a faulty SRAM cell, Bit' is not reaching the voltage of 1.1V as fast as Bit is reaching 0V. Further, the cell presents an increased and delayed current starting from the point of time Word Line is switched off.

In this scenario, we performed electrical simulations in order to identify the resistor's value necessary to model the SRAM's behavior under the influence of dRDFs. The results have been classified as follows:

- Fault Free Behavior: resistor's value of 0Ω.
- Non Sensitized Fault Behavior: resistor's value from 1Ω to 3961.761KΩ.
- Sensitized Fault Behavior: resistor's value higher then 3961.762KΩ.

Fig. 5 depicts the current's value [uA] that flows through the SRAM cell associated to the previously defined behaviors during 25ns of simulation. In Fig. 5, we can compare the current's value of a fault free SRAM cell with respect to the current observed in the defective SRAM cells. In more detail, it is possible to see that the abnormal currents are much higher than the current that flows in a fault free cell. To finalize, it is important to note that the BICS monitors this current difference in order to indicate faulty behavior.

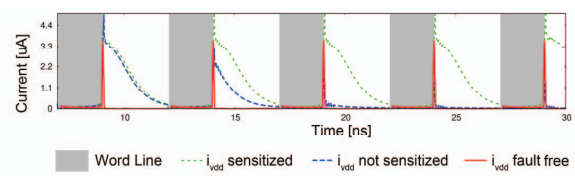


Figure 5. Current's value associated to the SRAM's behavior

For details about the classification above, see the results' discussion in the next sub-section.

### B. *BICS Fault Detection Capability*

The BICS fault detection capability with respect to dynamic faults has been investigated considering four different resistors' values. The next figures depict the waveforms resulted from the simulations associated to dRDF using *Df*. It is important to point out that the operations' sequence performed during the simulations was: $1w0r0^n$, where *n* represents a sequence of n successive r0 operations.

The next figures depict the results performed in order to evaluate the BICS's fault detection capability. At the beginning of each simulations, the cell stores '1' and after the w0 the cell changes to the value '0', part. (a). The next operations performed are r0 and we can observe that the output of the cell has the value '0', part (b). In part (c) we can see that the BICS does not detect any abnormal current as awaited, since there is no defect injected in the cell. Fig. 6 depicts the results obtained injecting a *Df* of 3950KΩ. Although the dRDF has not been sensitized, the BICS is able to detect the abnormal current flowing through the cell and consequently the BICS's output is set to '1' indicating the presence of a defect in the cell.

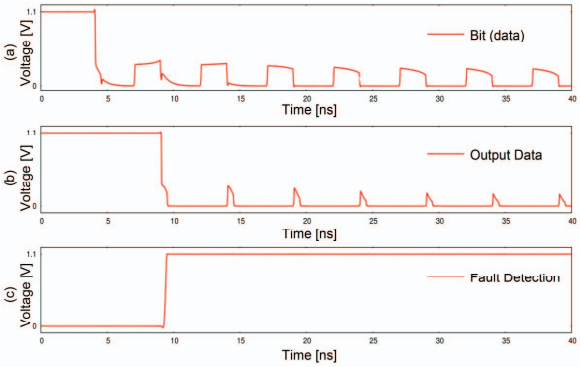


Figure 6. Non Sensitized Fault Behavior (Df = 3950KΩ)

Moreover, the abnormal current is a direct consequence of the resistor's presence in the cell, but consecutive read operations do not guarantee the flip of the value stored in the cell Thus, the cell will have a Non Sensitized Fault Behavior.

The next two figures depict the results related to the Sensitized Fault Behavior. Basically, if the cell does not reach the stable state after a read or write operation and before the next read operation, it is successively self-charged after each read operation until the flip of the stored value. Fig. 8 has been obtained injecting a resistor of 3961.762KΩ. Observing Fig. 7 it is possible to see that the injected defect can be detected by the BICS before the fault being sensitized. In more detail, the value stored in the SRAM cell flips during the sixth read operation. Regarding Fig. 8, the waveform depicts the results obtained from the injection of a defect with the value of 3962KΩ. In this specific case, the fault has been sensitized during the third read operation.

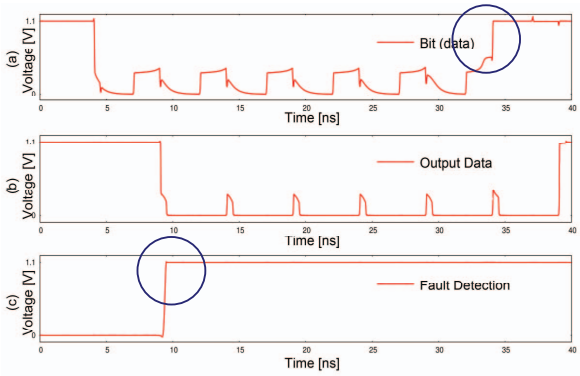


Figure 7. Sensitized Fault Behavior (Df = 3961.762KΩ)

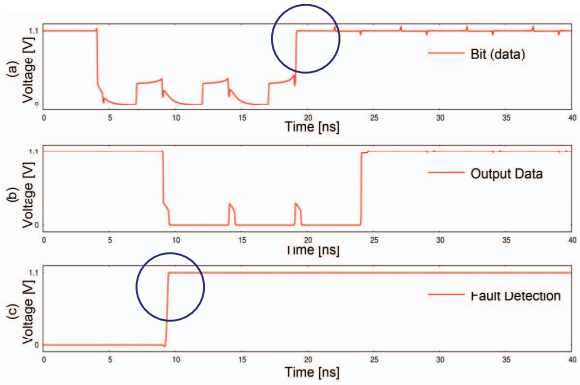


Figure 8. Sensitized Fault Behavior (Df = 3962KΩ)

Thus, it is important to highlight that the faulty behavior is influenced by the following factors: the impedance of the manufacture resistive-open defect, the impedance ratio between the access nMOS and the non faulty inverter's nMOS device and the access transistor on-time and off-time. To finalize, we performed a preliminary estimation of the leakage power consumption overhead introduced by the new BICS. This overhead has been proven to be strongly dependent on the array's geometry adopted by the SRAM and is still problematically high. Therefore its optimization is our main goal of future works.

## V. Final Considerations

This paper presented a new leakage power-aware BICS able to detect dynamic faults associated to resistive-open defects in nano-scale SRAMs. In order to evaluate the effectiveness of the proposed approach, we modeled the dRDFs using one resistor (*Df*) injected into the SRAM cell. Indeed, we identified the current variation observed considering different values for the resistors used to model dRDFs. Therefore, we developed and designed a new BICS taking into account the concerns related to the nano-scale technology. The performed electrical simulations demonstrated the effectiveness of the new BICS, since it assures the detection of dynamic faults associated to resistive-open defects that can be generated during the manufacturing process of nano-scale SRAMs. As future works, we intend to optimize the leakage power consumption of the new BICS scheme and to estimate the area overhead related to its insertion into the SRAM.

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