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***Abstract*—This paper provides a methodology that leverages state-of-the-art techniques for efficient fault simulation of structural faults together with transaction level modeling. This way it is possible to accurately evaluate the impact of the faults on the entire hardware/software system.**

I. Introduction

Structural faults model the consequences of physical defects at the gate and logic level. To validate the reliability of a system, fault injection is often adopted. For structural faults, fault injection must be done on a gate-level model at which simulation is usually not feasible due to its size and availability. Instead, multilevel simulation techniques are used. These techniques use a model at low abstraction level such as gate level for the fault injection and a model at higher abstraction level for the evaluation of the consequences [1].

This paper presents an integrated fault simulation environment for structural faults injection into a multi-level simulation at gate- and transaction level. It is based on a structural fault model with an efficient concurrent fault simulator at gate level. Error propagation is done at transaction level with a rollback mechanism that is simple to use with existing transaction level simulator kernels, yet allowing concurrent error propagation. The approach is adaptive and selects the gate-level model just if a component is subject to fault injection. It also combines the precision of gate-level simulation with the high simulation speed of transaction level.

II. Multi-Level System Model

A TLM of the system is augmented by precise gate-level models of components which are subject to fault simulation and analysis. Fault simulation of a gate-level model determines which faults cause errors at the outputs. For this subset of visible faults, functional error propagation is performed at transaction level. The propagated error is then evaluated at system level to check whether the fault eventually results in a system failure, i.e., an error observable in the application.

The system and target application are modeled at transaction level. To investigate hardware blocks and cores, gate-level fault simulator instances are created using gate-level models. Transactions directed to these cores are handled by gate-level wrappers which translate transactions into the appropriate pin- and cycle-accurate communication protocol of the core and vice versa. The data is then handed to the fault simulator. The wrapper provides the environment and infrastructure to the gate-level component and processes the fault detection information and fault propagation requests of the sequential fault simulator.

To achieve high accuracy, the wrapper properly manages unknown and conflicting values. That cannot easily be represented in a regular TLM flow. Several alternatives are available depending on either pessimistic or optimistic bound on targeted system reliability.

III. Implementation and Evaluation

The system has been implemented based on the sequential gate level fault simulator Hope [2], OSCI SystemC 2.2 and TLM-2.0 libraries. The evaluation concentrates on the fault classification accuracy as well as the run-time for two different applications executed on an AMBA based SoC with a LEON3 processor, hardware accelerator cores for Triple-DES (Data Encryption Standard) encryption and a two-dimensional discrete cosine transformation core. As target hardware/software applications, the Tripe-DES encryption of data blocks, and the JPEG encoding of images, are considered. To benefit from the parallel execution of simulator instances, the experiments were run on a multiprocessor system with 8 Intel Xeon CPUs running at 2.67 GHz and with 48 GB of RAM.

To integrate the Hope fault simulator into the SystemC simulation environment, C++ wrappers have been implemented for the cores. Separate instances of the Hope fault simulator are dynamically created for the considered gate level models. Experimental results gathered on several case studies showed a match of 99.8

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