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Electrostatic Discharge Analysis of Multi Layer Ceramic Capacitors

Cyrous Rostamzadeh [#1], Hamidreza Dadgostar [*2], Flavio Canavero [$3]

[#] *Robert Bosch LLC, Plymouth. MI, USA*
[1] `Cyrous.Rostamzadeh@us.bosch.com`
[*] *University of Stuttgart, Germany*
[2] `hdadgostar@stud.uni-stuttgart.de`
[$] *Politecnico di Torino, Italy*
[3] `flavio.canavero@polito.it`

Abstract—**A rigorous analysis of Electrostatic Discharge susceptibility of Multi Layer Ceramic (MLC) capacitors is carried out. The impact of ESD stress applied at the connector pins of an electronic control module, protected by utilizing 0603 package MLC capacitors is evaluated. Effectiveness of MLC capacitors for protection of integrated circuits cannot be underestimated, nor should it be assumed as an effective ESD robust solution. Meanwhile, any degradation, or physical damage to MLC capacitors should not be ignored. This analysis concentrates on the permanent physical degradation to the ESD capacitors employed for the protection of active components for an automotive control module. However, this does not limit its scope to specialized automotive applications. In general, the same principles are applicable to all electronic products employing MLC capacitors as per ESD protection and filter mechanism.**

I. INTRODUCTION

Electrostatic Discharge (ESD) is one of the most important reliability problems in the electronic circuit industry. Typically in integrated circuits (ICs) industry, one-third to one-half of all field failures (customer returns) are due to ESD. As ESD damage has become more prevalent in newer technologies due to the higher susceptibility of smaller circuit components, there has been a corresponding increase in efforts to understand ESD failures through modeling and analysis. Manufacturers of integrated circuits provide ESD test information. However, the ESD data on IC level standards, Human Body Model (HBM), Charged Device Model (CDM), Machine Model (MM) and latch up to the system level testing is often confusing.

Design of robust ESD circuits remains challenging because ESD failure mechanisms become more acute as critical circuit dimensions continue to shrink. Circuit board designers are further constrained by the ability to design highly congested printed circuit boards (PCB) and meet ESD requirements. HBM provides much insight into device behavior during an ESD event [1,2] .

An ESD event is the transfer of energy between two bodies at different electrostatic potentials, either through contact or via an ionized ambient discharge (a spark). This transfer has been modeled in various standard circuit models for testing the compliance of device targets. The models typically use a capacitor charged to a given voltage, and then some form of current-limiting resistor (or ambient air condition) to transfer the energy pulse to the target.

In order to meet the module level ESD tests, various methods and techniques on printed circuit boards have been implemented and investigated. One effective technique is to add discrete noise-decoupling components or filters into complex CMOS based IC products to decouple, bypass, or absorb the electrical transient voltage (energy) under system-level ESD test [3]. Various types of noise filter networks can be employed to improve system-level ESD stress tests, including capacitor filters, ferrite bead, transient voltage suppressor (TVS), metal oxide varistor (MOV), and 2nd order LC filter or 3rd order π-section filters.

Multi layer ceramic capacitors (MLCC) are employed as an ESD bypass mechanism at the connector pins of electronic control modules. An automotive control module may require the use of a single high-density connector with pin density in excess of 200. In a typical application, a connector may present the designer with a matrix of 4 x 50 (4 rows of 50 pins at each row) in a tightly congested PCB real estate. To accommodate for the ESD protection for each and every I/O pin at the connector of a highly congested PCB real estate, design engineers recommend the use of 0603 style MLC capacitors. In most applications, MLC capacitors used for ESD protection are rated for 100 V stress level. However, post-ESD characteristics of MLCC's are often ignored or misunderstood. In reality, MLCC's exposed to ESD stress exhibit dramatic shift in characteristic impedance behavior. Careful examination of MLCC's reveals a permanent structural damage resulting in excessive low frequency leakage. Post-ESD behavior of MLCC's results in a functional deviation for a control module and it is fundamentally unsafe to use the product for its intended application. It is suggested that the low profile 0603 capacitors should not be used for ESD protection as reported in this paper. Alternative solutions can be met by the use of low profile transient voltage suppressors (TVS) or fast metal oxide varistors (MOV). However, 0805 style MLCC's with high value capacitance (larger than 47 nF) provide a good solution and are safe to be used as an ESD bypass element.

MLCC's as a protective device or mechanism should consider the voltage, peak power and energy as the key

components of an ESD threat. It is thus necessary to fully characterize the amplitude and timing of ESD components. Therefore, protection structure should reduce the voltage, peak power, and energy threats by shunting the stress currents away from fragile portions of the microcontrollers and other ICs [9].

To solve ESD problems, MLC capacitors employed as ESD bypass or filter component on PCB's, must shunt the ESD transient current safely to ground. It is important that MLC capacitor employed as bypass component, absorbs the ESD voltage and current safely and protects the device under test with no degradation. In addition, MLC capacitor must remain within its parametric tolerance if it could be considered as a reliable protection mechanism.

II. MLC CAPACITOR AS AN AUTOMOTIVE ESD PROTECTION DEVICE

Multi layer ceramic capacitors are designed for use where a small physical size with comparatively large electrical capacitance and high insulation resistance is required. General purpose 0603 (1.6 mm x 0.5 mm) class II, type X7R (-55°C -> +125°C) is a popular choice for automotive electronic control module design. Therefore it is a common practice to apply X7R MLCC's as ESD protection component at all I/O pins.
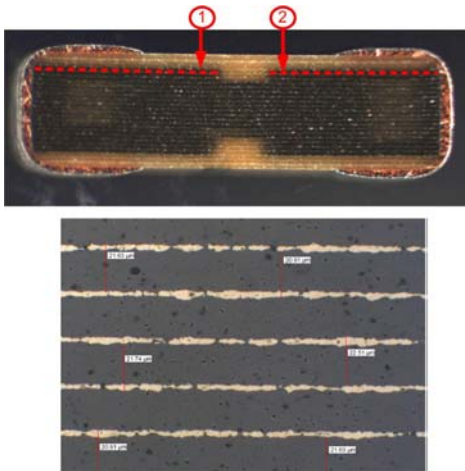

Fig. 1. Standard 0603 MLCC (X 100 Magnification)

Figure 1 illustrates a horizontal grind of 0603 MLCC (magnification X 100) with plates spaced at 21 μm apart for a 10 nF, X7R type II capacitor. It is important to note that in the indicated region, capacitor plates from opposing edge terminals do not overlap. A higher value capacitor is designed with increased number of plates. This will result in a narrow dielectric thickness, a possible drawback for high voltage transients. At the present time (January 2009), capacitor values for a type II X7R 0603 (100 V) range between 180 pF to a maximum value of 39 nF. However, the capacitor value range for the same technology, but larger physical size (0805), varies from 220 pF to a maximum value of 120 nF. This can be an important factor if ESD protection capacitor value is

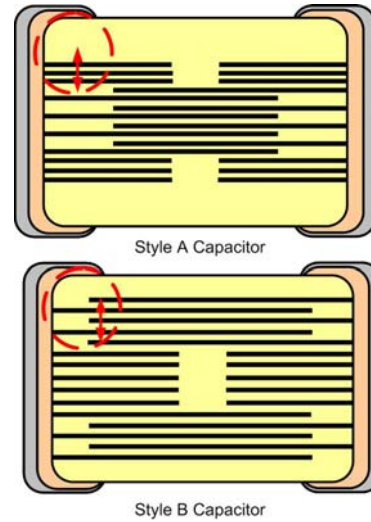determined to exceed the maximum value of 39 nF available in 0603 package.

Fig. 2. 'Standard' vs. 'ESD-Enhanced' 0603 MLCC

Figure 2 illustrates two different styles of MLCC technology with respect to the design of conductive plates. Style A capacitor is a standard MLCC design where the capacitor plates from opposing terminals do not overlap in the upper and lower edges as indicated. A closer examination of post-ESD damage consistently revealed a physical structural damage (crack, bubble or void) in the upper or lower terminal region of MLCC. Capacitor manufacturers recognize the over-voltage stress concern and have provided an ESD-enhanced MLCC product. Fig. 2 demonstrates the style B as an ESD enhanced design. A close examination of Figure 2 (Style B) geometry indicates a design topology, where manufacturers have overlapped the opposing electrodes in the four corners of MLCC terminals. Figure 3 illustrates a horizontal grind of an 'ESD-enhanced' MLCC on a scale of X 100 magnifications.
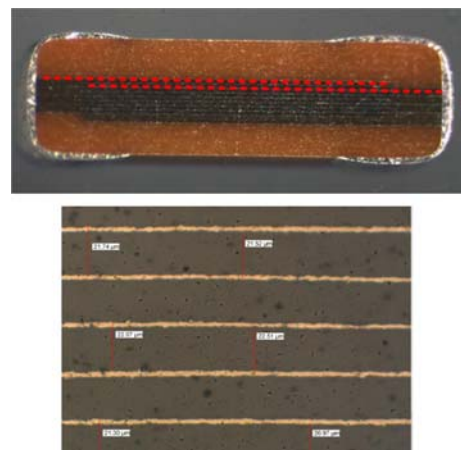

Fig. 3. ESD-Enhanced' 0603 MLCC

Comparison with Fig. 1 demonstrates the differences in plate geometry design. As indicated, plates from opposing electrodes do overlap in four corners of MLCC terminals.

Printed circuit board designers with fundamental EMC trainings, are required to ascertain the optimum mounting strategy for ESD capacitors. EMC engineers verify a "Y-Connection" topology for all of the ESD capacitors, at every I/O pin of the connector. MLCC must be placed in close proximity of the I/O pin (< 1 cm) with a short trace (< 1 cm) to the PCB return plane. In this manner, added PCB parasitic trace inductance and its degradation effect on the effectiveness of ESD bypass capacitor is minimized. The general concern is to limit the added inductance due to PCB mounting inductance, and thus provide a low-impedance path for ESD current flow to return plane.

Another limitation would be to use the lowest value capacitor available, where it is most effective at higher frequencies. ESD would result into an RF current with a bandwidth in excess of 330 MHz. The choice between a 1 nF and 680 pF would easily be reduced to the latter one. However, ESD HBM consists of a 150 pF capacitance, thus a higher value MLC capacitor is preferred. A voltage divider network is established by the combination of HBM capacitor and MLCC. The voltage developed across a larger value MLCC, would lower the voltage developed across an integrated circuit:

$$V_{MLCC} = \frac{C_{HBM}}{C_{HBM} + C_{MLCC}} V_{ESD} \qquad (1)$$

Therefore for $V_{MLCC} \ll V_{ESD}$, it is required that $C_{MLCC} \gg C_{HBM}$.

III. MLC CAPACITOR ELECTRICAL MODEL

Several electrical models of capacitors are available in text books and RF publications used by EMC/RF community to describe the electrical behavior of MLC capacitors. A simple series RLC network is commonly used to provide an accurate behavior for most applications.
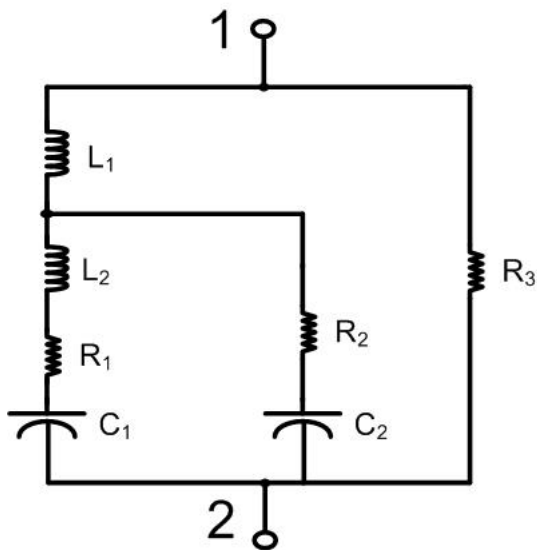

Fig. 4. Improved Electrical Model of MLC Capacitors

However, simple RLC model fails to provide additional technical insight required for the analysis of MLCC's exposed to ESD pulse. The modified model presented in Fig. 4 has additional elements to describe the behavior of MLC capacitors exposed to ESD stress. In fact, the model described here is an accurate electrical description, necessary to account for the various physical attributes found within a capacitor.

1. L_1 is the series parasitic inductance associated with plate connections.
2. L_2 is the equivalent series inductance. It is also known as L_{ESL}.
3. R_1 is the equivalent series resistance (also known as R_{ESR}) and represents the actual Ohmic resistance of the plates. This value is typically very low. It causes a power loss of I^2R_1. Its contribution to the total dissipation factor is $D_1 = \omega R_1 C_1$.
4. C_1 is the nominal capacitance.
5. R_2 is the dielectric loss: A parallel resistance arising from two phenomena; molecular polarization and interfacial polarization (dielectric absorption). Dielectric loss is a complex phenomenon that can change with frequency in most any manner that is not abrupt. Its contribution to the total dissipation factor can be approximated by $D_3 \sim 1/(\omega R_2 C_2)$.
6. C_2 is the parallel dielectric absorption capacitor.
7. R_3 is the leakage resistance, or insulation resistance: A parallel resistance due to leakage current in the capacitor. This value is typically very high. It causes a power loss of V^2/R_3. Its contribution to the total dissipation factor is $D_2 = 1/(\omega R_3 C_1)$.

The impedance characteristics of type II (package 0603, X7R MLC) capacitors for a 680 pF and 10 nF are illustrated in Fig. 5.
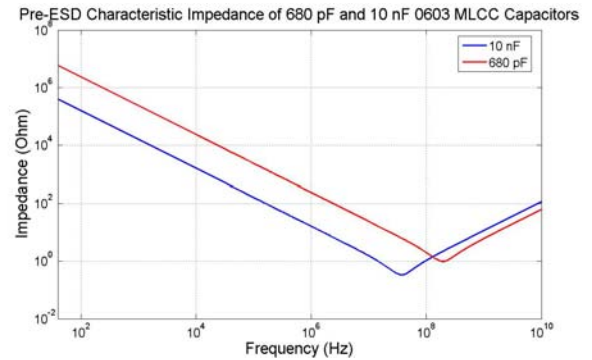

Fig. 5. Pre-ESD Impedance Characteristics

ESD is a high frequency pulse with a rise time of less than 1 ns, resulting in spectral content in excess of 330 MHz. Hence, the choice of ESD capacitor is reduced to a smaller value MLCC, as seen in Fig. 5. Closer examination of Fig. 5 reveals a lower impedance for a 680 pF (1.71 Ω, at f = 330 MHz) compared with a 10 nF (3.97 Ω, at f = 330 MHz). Another consideration may be due to capacitive loading of certain I/O signals, i.e., CAN bus, where a limited capacitance can be added to the communication bus.

TABLE I

MLCC 0603 Capacitor Model Components

NOMINAL VALUES @ 1 kHz	680 pF	10 nF
L1	49 pH	91 pH
L2	931 pH	1.730 nH
C1	680 pF	10 nF
C2	4.10 pF	4.10 pF
R1	5.15 kΩ	0.329 kΩ
R2	753.73 Ω	34.57 Ω
R3	1.471×10^{12} Ω	0.1×10^{12} Ω

The requirements of a lower value ESD capacitor as in the previous paragraph, may suggest the use of the lowest value MLCC available in industry. In addition, there is a third factor that is outlined in Table I, R3 (insulation resistance) that may add additional incentive for the use of the lowest value MLCC. However, further insight is required to distinguish the apparent easy choice.

In Table I, all nominal and parasitic elements for both capacitors are listed as per MLCC supplier A.

It is important to note that the insulation resistor, R3, is an order of magnitude higher in value for smaller value capacitor (Table I). As more plates are stacked up to accommodate for higher value capacitance in the same physical volume of 0603 style package, the dielectric thickness is reduced by a factor of 14.7. Therefore, as a consequence of thinner dielectric material between the capacitor plates, the insulation resistor for higher value capacitor is reduced by the same ratio, (capacitor ratio: 10 nF / 680 pF = 14.7, insulation resistor ratio: 0.1×10^{12} Ω / 14.7×10^{12} Ω = 1/147). It is clear that a higher value capacitor will sustain a dielectric breakdown in lower ESD voltages. It appears by this argument, for ESD applications, only to consider lower-value capacitors with higher insulation resistance in order to protect for dielectric breakdown, i.e., 680 pF vs. 10 nF. Further investigation was required to answer the accuracy of aforementioned statement.

If a smaller capacitor presents a higher insulation resistance as shown above, it is important to examine the behavior of the insulation resistance after ESD tests. It is important to evaluate the impact of ESD stress on 680 pF and 10 nF capacitors by characteristic impedance of post-ESD capacitors for further insight.

IV. HUMAN BODY ESD TEST

ESD tests for automotive applications are derived and based on HBM specified by original equipment manufacturers (OEM) [4,5,6,7,8].

A typical HBM discharge network consists of a 150 pF capacitor with a 2 kΩ resistor. HBM capacitor can be charged up to 25 kV for air-discharge test. The static charge accumulated on the 150 pF discharge network capacitor (charged to 25 kV) would amount to 3.75 μC. ESD is a high-frequency, high-voltage and high current event that can deposit 46.875 mJ of energy in the protection device in a relatively short time duration.

HBM provides much insight into device behavior during an ESD event. Although the HBM stress is characterized by a certain charging voltage, V_{HBM}, the 2 kΩ series resistor of the circuit is usually much larger than the impedance of the device under test, so we think of HBM tester as current sources, with the peak HBM current equal to 12.5 A. (V_{HBM} = 25 kV, air-discharge).

V. PRE-ESD AND POST-ESD MEASUREMENTS

In order to evaluate the impact of ESD stress on 0603 MLCC's two different types of tests were performed. Since a populated electronic control module is the intention of a realistic test, it is important to evaluate the impact of ESD stress as per OEM ESD test techniques. In an another method, an 0603 MLCC network was prepared as shown in Fig. 6 with two short wires (< 1 cm) at each end. Terminal one was connected to a ground plane where an ESD gun return wire would normally be connected. ESD discharge tip was slowly approached to the floating terminal until an air discharge was achieved.

Pre-ESD and post-ESD characteristics of the 0603 capacitor were recorded using an Agilent 4294A impedance analyzer (40 Hz – 110 MHz) with the help of Agilent 16034G test fixture.

Capacitors were removed from test PCB, or ESD network wires and mounted inside the 16034G test fixture for impedance characterization.

It was decided to apply ESD pulse to a fully populated automotive electronic control module as designed with rigorous EMC guidelines. OEM ESD requirements provides guidelines [6,7,8] for remote I/O access ESD stress tests. A HBM model with discharge network as outlined in section IV was calibrated and ESD voltage levels from +/- 4 kV up to +/- 25 kV was applied in successive order. After each discharge, MLCC was removed and analyzed on impedance analyzer as per previous method.
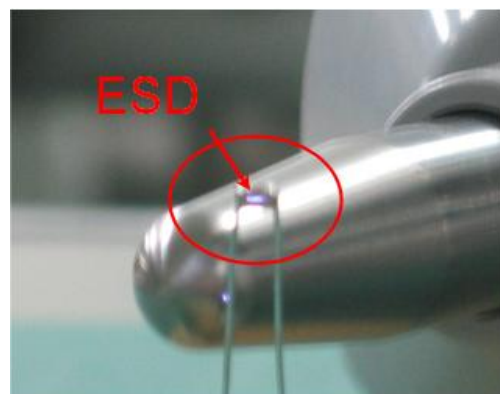

Fig. 6. ESD air-discharge to 0603 MLCC

Figure 7 illustrates the impact of ESD pulse at +/-15kV level for 680 pF capacitor. Figure 8 illustrates the impact of ESD pulse at +/-15kV level for 10 nF capacitor.
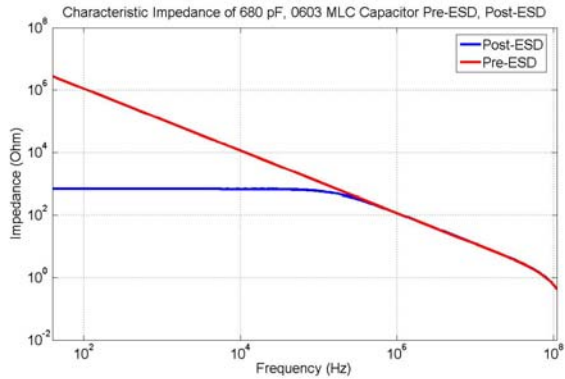

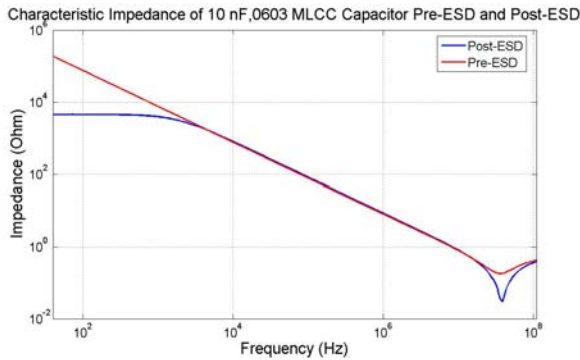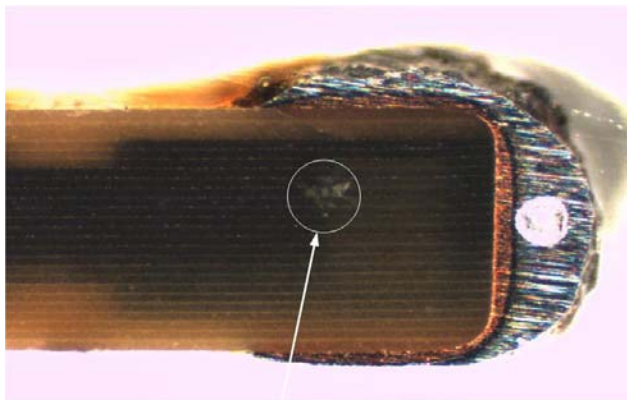Fig. 7. Measured Pre-ESD and Post-ESD (MLCC 680 pF)

Fig. 8. Measured Pre-ESD and Post-ESD (MLCC 10 nF)

ESD Damage to ESD Capacitor SMD 0603 package
(magnification X 100)
"Horizontal Grind"

Fig. 9. Dielectric damage for Post-ESD MLCC

Post-ESD capacitor dielectric damage is illustrated in Fig. 9 (horizontal grind) on a magnification scale of 100.

In Fig. 10, a modified electrical model represented as per Fig. 4, was used for post-ESD effects for both capacitors. In electrical model per Table I, R3 was replaced with a 500 Ω resistor in place of a nominal pre-ESD value provided by MLCC manufactures in Table I (14.7 x $10^{12}\,\Omega$).
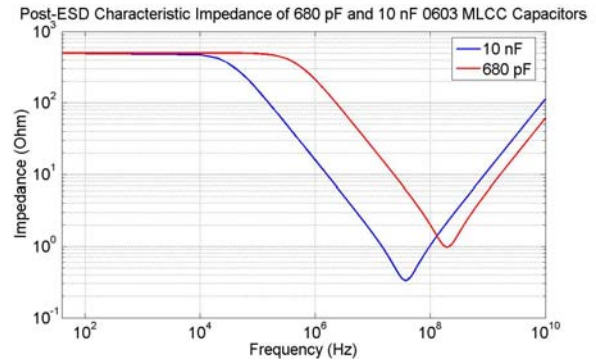

Fig. 10. Simulated Post-ESD Impedance Characteristics, R3 = 500 Ω

It is important to note that 10 nF capacitor has developed a severe leakage from 40 Hz up to 20 kHz, and for 680 pF, the upper frequency is approximately 200 kHz. The impedance of both capacitors registers a 500 Ω resistive value in the aforementioned frequency range. It is thus concluded that ESD has caused a non-recoverable, permanent damage to MLCC's. Post-ESD behavior suggests physical damage to dielectric material due to metallization of capacitor plates. In reference to Fig. 4, it is clear that R3 has shifted from its pre-ESD nominal value as per Table I (for 680 pF, R3 = 1.471 x $10^{12}\,\Omega$ or for a 10 nF, R3 = 0.1 x $10^{12}\,\Omega$ to an extremely low value of 500 Ω.

In order to understand why 680 pF MLCC has a 500 Ω leakage up to 200 kHz, whereas 10 nF shows the ill-effect only up to 20 kHz can be explained as follows: the circuit of Fig. 4 simplifies to the parallel of C1 and R3, at low frequencies, and the knee of the impedance curve appears at a frequency f ~ $1/2\pi R_3 C_1$. For post-ESD, the 680 pF MLCC, is dominated by R3 from DC to ~ 300 kHz, whereas, R3 contributes only up to 20 kHz for the 10 nF capacitor.
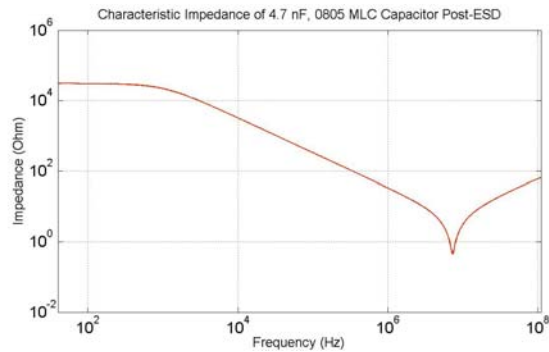

Fig. 11. Measured Post-ESD for 4.7 nF 0805 Capacitor

It is clear that smaller size MLCC will suffer extreme leakage to much higher frequency range. It is recommended to use higher value MLCC's in contradiction to previous recommendations.

As an extension to the exposure of 0603 MLC capacitors to ESD stress, additional ESD tests were performed on modules populated with larger footprints 0805 MLC capacitors. Figure 11 illustrates the impact of +/- 25 kV HBM ESD stress on a 4.7 nF capacitor. It is clear that a 4.7nF, 0805 capacitor would fail the ESD requirements. However, extending the capacitor size (value) to 10 nF in an 0805 package, results in ESD compliance.

VI. CONCLUSION

This study is an examination of the physical damage to the 0603 MLC capacitors exposed to ESD transients. It is shown that permanent damage to dielectric material is resulted for ESD voltages in excess of 15 kV. The use of 0603 MLC capacitors for I/O connector pins, as an ESD bypass mechanism, is not recommended and should be avoided. However, in larger footprints, 0805 MLCC's will meet the ESD stress for 25 kV requirements, provided that capacitor size exceeds 10 nF, and rated for 100 V applications. Throughout this article, it was stressed that lower value MLCC's are preferred with respect to their impedance behavior at higher frequencies. It is clear that one cannot utilize lower values MLCC at will, such as 680 pF due to dielectric degradation, as illustrated in Fig. 7 and Fig. 9. Higher value capacitors exhibit self-resonance phenomena at lower frequencies. Therefore it is also recommended not to exceed the MLCC value indiscriminately. A preferred ESD bypass solution would use a low capacitance transient voltage suppressor (TVS, C_{TVS} < 100 pF) or a fast metal oxide varistor (MOV).

However, I/O pin ESD capacitors in the range of 1 nF to 100 nF are often utilized as an input RF filter at the connector pins. The ESD capacitors provide a bypass element for the induced RF currents on the module harness due to impinging electromagnetic fields. Low value TVS capacitance is insufficient to provide the required filter across the 1 MHz – 200 MHz frequency bandwidth. It is recommended to use a TVS in parallel with a 0603 capacitor (10 nF – 39 nF rated for 50 V) where permissible.

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