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Characterization and modeling of the power delivery networks of memory chips

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Abstract

This paper focuses on the power delivery characterization of high-speed IC memories by means of on-chip measurements. A systematic analysis of the measurement setup, of the effects of chip biasing and of the use of the measured responses to develop models defined by simplified circuit equivalents is given. All the results collected in the paper are based on real measurements carried out on a commercial 90nm flash memory.

Introduction

The modeling of the power delivery system of digital Integrated Circuits (ICs) is of paramount importance for the simulation of the switching noise. Behavioral models based on the characterization of the power delivery networks by responses measured at their ports are the preferred options to cope with the complexity of the problem.

Modeling guidelines for power delivery systems are suggested by the IEC standard Integrated Circuits Electrical Model (ICEM) [1]. Several application papers on the generation of ICEM models of real devices are available, however, most published measurements are based on fixtures that include package and external interconnect and need a complex de-embedding procedure [2]. Besides, the structure of the power distribution system of some devices like digital memories consists of several weakly coupled sub-networks and demand for possible specialized modeling solutions.

In this paper, the characterization and modeling of power delivery systems of high-speed IC memories are specifically addressed. These ICs are particularly significant, because they are widely used in recent System-in-Package (SiP) devices. The paper reports on a set of measurements carried out on an example memory by direct on-chip probing. The measurement setup allows for the dc supply of the device and for the actual reference system that is used in device applications. On-chip probing offers responses free from the effects of the measurement fixture involving the IC package and external interconnects, providing insight on the behavior of the power delivery network on a very wide frequency band. The use of the measured responses to develop models is also shortly discussed.

Example test case

This Section briefly introduces the typical structure of the power delivery network of a digital memory and the example test case considered in this study.

The power delivery system of a memory is composed of different (nearly decoupled) power delivery networks carrying energy to different parts of the device, *i.e.*, to the analog and and/or digital core components and to the output buffers. A simplified schematic of two possible classes of networks and

of their connections to the chip pads is shown in Figure 1. In detail, the two networks are:

- (1) the power rail network (VDDQ-VSSQ) supplying the I/O buffers of the DATA bus (the I/O terminals of the buffers are the DQ n pads in Figure 1).
- (2) the internal network (VDD-VSS) supplying the memory matrix, the digital circuitry and possible additional analog blocks; The substrate is typically connected to VSS.

It is worth noticing that in some memory chips, the VDD-VSS network (2) can be divided into subnetworks supplying the analog and the digital circuitry separately. Also, the number of possible pairs of external pads for each network depends on the chip and is in the typical range of [1-10]. On the other hand, network (1) for the supply of the I/Os consists of two separate rails with a regular distribution of pads, *i.e.*, the VDDQ and the VSSQ pads shown in Figure 1. Besides, a limited number of DQs (in general from one to four) is placed within adjacent pairs of VDDQ-VSSQ pads.

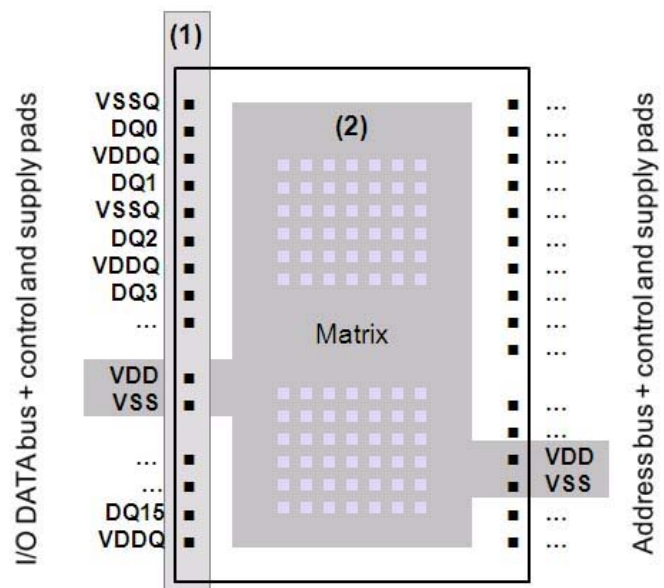


Figure 1. Simplified structure highlighting the three main sub-networks (1) and (2) composing the power delivery network of a digital memory.

All the results presented in this paper are based the measurements carried out on a 512Mb NOR Flash memory in 90nm technology produced by Numonyx., which is representative of a wide class of memory chips. In this device, the reference pads of all networks are wire bonded to the package reference plane, and the power pads are wire bonded to the package supply pins. The reference pads are the only

connections of the die to the package reference plane, as the bottom of the die is insulated. The chip supply networks are also used to bias the semiconductor wells, providing the insulation of the MOS transistors.

Measurement objectives and setup

From a formal point of view, the power delivery system of the chip is an n-port (almost) linear passive network, where the ports are the pairs of chip supply pads and the internal supply terminals of the chip transistors. The internal ports, however, are not accessible to probing and the characterization of the external port responses with simultaneous measurements is hardly feasible. This work, therefore, explores the two-port scattering responses of couples of ports belonging to the same power delivery network or to different ones. External ports not involved in measurement are left open for the RF signal.

Two-port scattering responses can be used to obtain a network matrix for all the external ports of the power delivery system. This characterization, complemented by source terms, can be used to build models for the chip emission caused by the switching activity. On the other hand, this characterization can enable the identification of equivalent circuit models, offering insight in the internal behavior of the networks and possibly enabling the development of models for the assessment of the simultaneous switching noise.

The two-port responses measured in this work are obtained by direct on-chip probing via SG probes, while the G contact connected to the reference pad of the port. Besides, dc supply is provided via DC probes or via the RF probes to mimic the actual biasing conditions. All the measurements reported in this paper have been carried out at the Philips MiPlaza laboratory in Eindhoven by means of a Cascade probing station and a Agilent vector network analyzer.

Figure 2 shows the measurement setup for the characterization of the VDDQ network of the example device. In this setup, the first RF probe (defining the port #1) is connected to the first pair of VDDQ-VSSQ pads on the top left side of the die and the second RF probe (defining the port #2) is connected to another pair of VDDQ-VSSQ pads on the bottom left side of the die of Figure 1. Some dc probes, used to complete the biasing of the device, are also visible in Figure 2. Similar arrangements are used to carry out the two-port scattering measurements needed for the characterization of the VDD network of Figure 1.

Measured responses

This Section collects the measured responses of the example device and discusses the external behavior of the different supply networks.

Responses of the VDD network

Figure 3 shows a selection of two-port measured scattering responses of the VDD network of Figure 1. A setup similar to the one of Figure 2 is used, where the RF probes are connected to two pairs of VDD-VSS pads and the dc probes are suitably connected to supply the chip. The curves in this figure, corresponding to five independent measurements carried out on different dies on the same wafer, highlight the identical behavior of the different dies and the repeatability of the measurement. It is worth noting that the maximum error,

computed as the magnitude of the difference between the scattering responses of different dies is less than -40 dB. Also, the responses in this Figure confirm that the bandwidth of interest is less than 1 GHz (at this frequency, S11 is -1 and the transmission parameter S21 is extremely low).

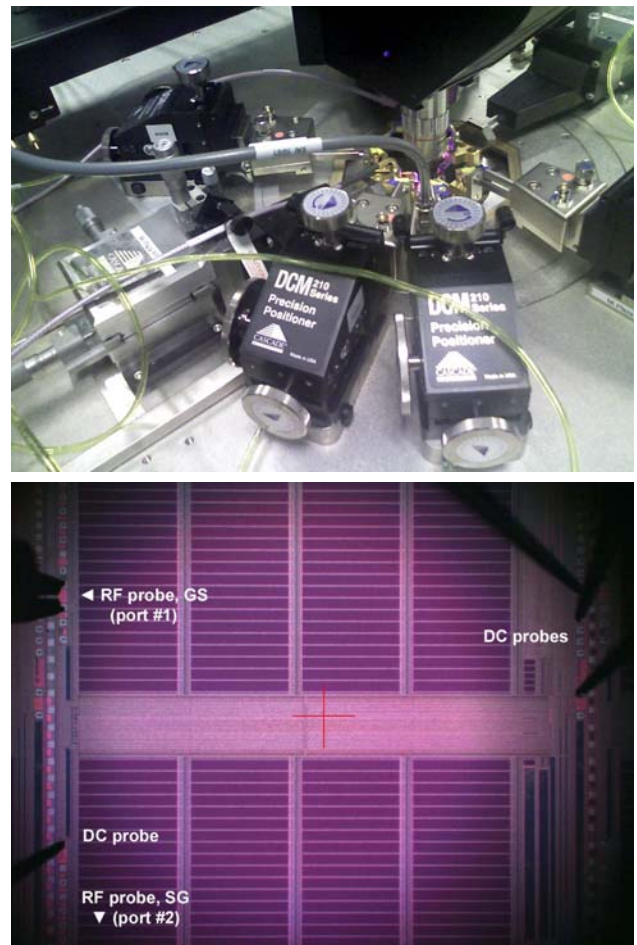


Figure 2. Setup for the collection of the two-port S parameters of the VDDQ network of the example device from on-chip measurements.

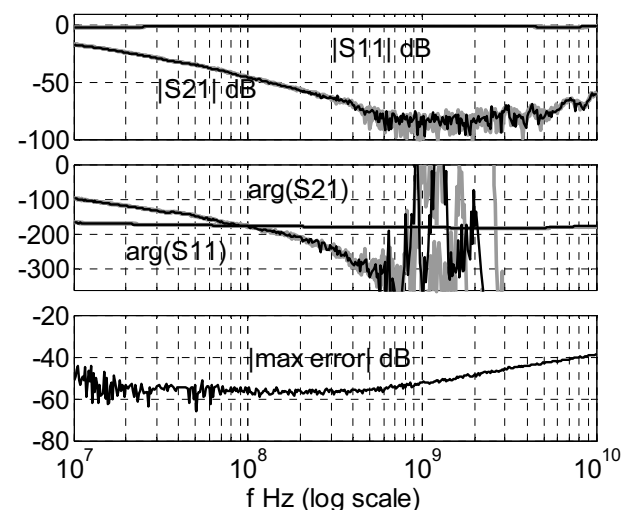


Figure 3. Selection of the scattering responses of the VDD network. Black curve: reference response on a selected die; gray curves: responses of 4 different dies on the same wafer.

In order to assess the effect of the chip biasing, Figure 4 shows the same scattering responses for one selected die either biased via the dc probes or not. The curves in the figure clearly show the same qualitative behavior for the biased and the unbiased case. Besides, the effect of the chip biasing leads to a relatively small shift of the responses only.

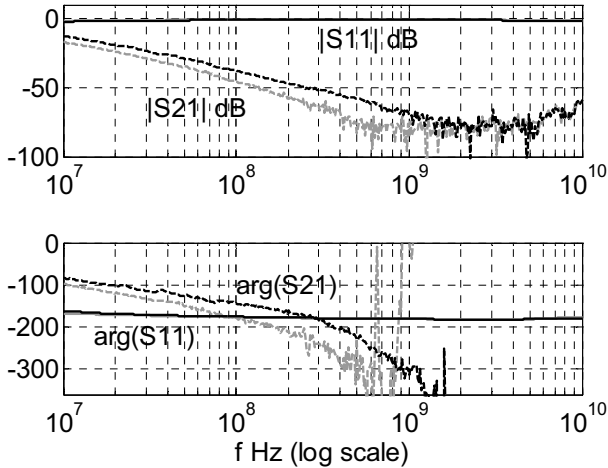


Figure 4. Selection of the scattering responses of the VDD network for a selected die. Black curves: biased die; Gray curves: unbiased die.

Responses of the VDDQ network

Figure 5 shows a selection of the measured scattering responses of the VDDQ-VSSQ power rail, *i.e.*, the longer and the more regular structure among the structures of Figure 1. This first set of responses corresponds to ten measurements carried out on different dies on the same wafer, thus confirming the repeatability of the measurement, the identical behavior of the different dies and the bandwidth of interests. Figure 6 shows the same scattering response for a selected die biased either biased or not via the dc probes. Also for this supply structure, the same qualitative behavior is observed for the biased and the unbiased case.

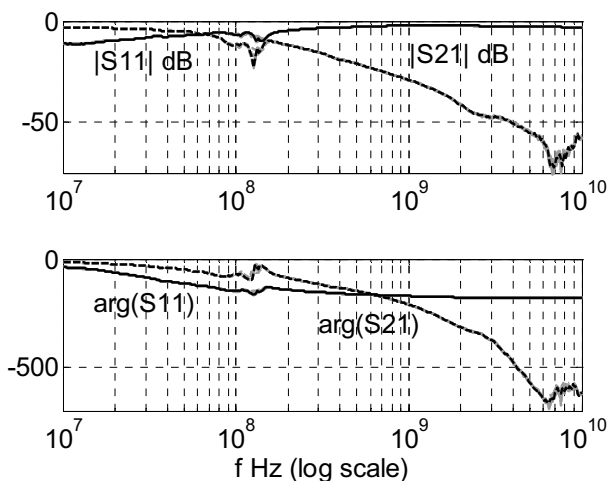


Figure 5. Selection of the scattering responses of the VDDQ network obtained with the two probes connected to the first and the last pair of the supply pads; Black curve: reference measurements on a selected die; Gray curves: responses of nine different dies on the same wafer.

Finally, Figure 7 collects the scattering responses of the VDDQ network obtained by changing the position of the two RF probes. This is done by stepping up the position of the second probe on the bottom left side of Figure 2 (port#2). The very small differences among the curves collected in this Figure (some relevant differences are clear from the phase of the S21 function only), confirm a lumped behavior of the power rail within the bandwidth of interest.

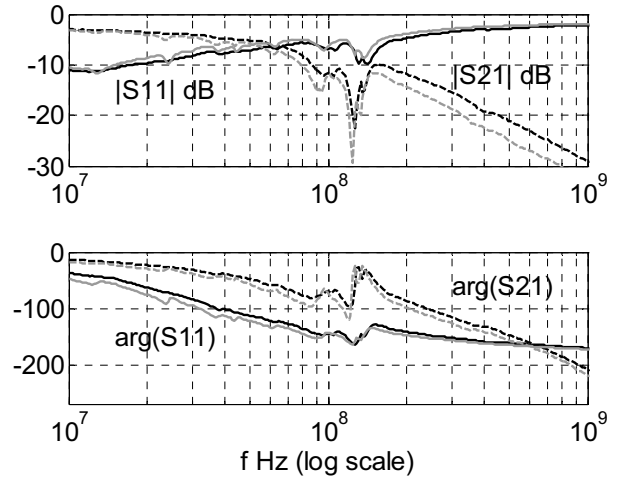


Figure 6. Selection of the scattering responses of the VDDQ network of the selected die with the two probes connected to the first and the last pair of supply pads; Black curves: biased die; Gray curves: unbiased die.

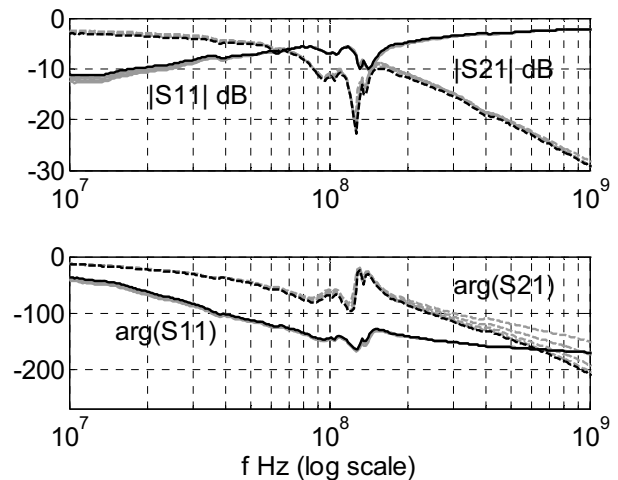


Figure 7. Selection of the scattering responses of the VDDQ network. Black curves: reference responses with the two probes connected to the first and the last pair of supply pads; Gray curves: responses obtained by stepping-up the second probe (*i.e.*, the port #2 of Figure 2).

Modeling

The regular and smooth behavior of the measured responses suggests to address the modeling of the power delivery network of the example device via simplified lumped equivalents.

The assumption to deal with a nearly-lumped device can be clearly verified from the behavior of the responses of the VDDQ network of Figure 7. It is worth noting that the different curves of Figure 7, that are obtained by changing the

spatial position of the two RF probes, lead to very similar responses. The superposition of the different magnitude plots and the small differences in the phases of the S21 parameter (appreciable only at high frequencies) are a clear support for the lumped parameter assumption.

For conciseness, the remaining part of the paper focuses on the VDD network only. However, all the comments and results can be extended to the alternate supply networks. Figure 8 collects a possible set of simplified equivalents that can be used, where the structures (a), (b) are simplified circuit equivalents based on physical insights and on the analysis of the qualitative behavior of the VDD network and structure (c) is a pure black-box equivalent. Once a specific structure is selected, standard techniques are available to compute the parameters of the different structures of Figure 8 from the measured responses.

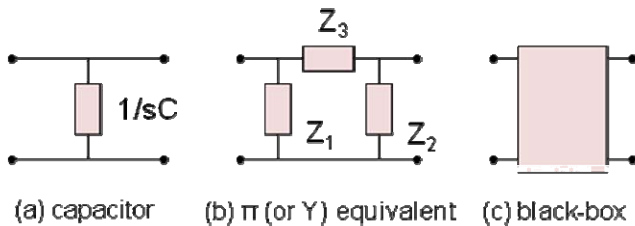


Figure 8 Simplified equivalent structures assumed for the VDD-VSS structure. (a) capacitor; (b) lumped 2-port equivalent ($Z_1 = 1/sC_1$, $Z_2 = 1/sC_2$ and $Z_3 = R_S$) and (c) black-box element defined by a real rational scattering matrix.

As an example, an effective model for the responses of the VDD network can be obtained by using the Π lumped circuit and physical insight. The responses of Figures 3 and 4 have the behavior of a two-pole transmission function. Besides, an RC diffusive behavior is expected from the VDD network and this suggest to identify Z_1 and Z_2 by capacitors and Z_3 by a resistor. Consistently, this equivalent has a two-pole transmission scattering functions and can be fitted to the measured responses very well. The best fit is obtained for $R_S = 3.4 \Omega$ and $C_1 = C_2 = 1.3 \text{ nF}$ and is compared to the measured curves in Figure 9.

Of course, a pure black-box modeling via rational function fitting can offer an improved accuracy [3,4]. For this modeling problem, however, it turns out that unexpectedly large order models are needed to get an accuracy level higher than the one of the Π model. The good performance of the Π model are likely to come from its close relation to the physical structure being modeled, thereby leading to an improved filtering of the measurement error during the model estimation phase.

Conclusions

This work addresses the characterization of the power delivery system of an example memory IC via on-chip two-port scattering parameter measurements. The obtained responses turned out to have a very simple behavior up to frequencies as large as 10 GHz. In contrast to measurements based on fixtures including package and external interconnects, the responses of this work were free from resonant effect. Just one main resonance appeared in the responses of the VDDQ network, that was the structure with

the largest inductive effects. The semiconductor bias turned out to have just a minor effect on the measured responses, whose behavior is maintained regardless of the biasing. Finally, the responses of the VDD network turned out to be very well fitted by simple lumped Π models, thereby supporting the analogy of these models to the physical structure of the modeled networks.

Acknowledgments

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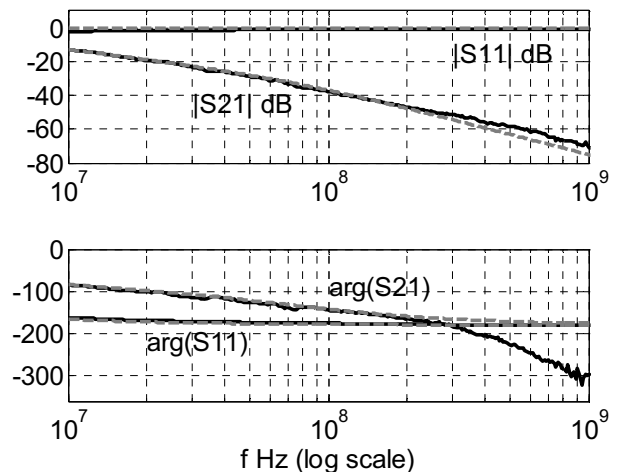


Figure 9 Selection of the scattering responses of the VDD-VSS structure. Solid lines: reference measured responses; dashed lines: responses of Π model (b) of Figure 8 ($Z_1 = 1/sC_1$; $Z_2 = 1/sC_2$; $Z_3 = R_S$; $C_1 = C_2 = 1.3 \text{ nF}$; $R_S = 3.4 \Omega$)

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