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Original
A Fully Differential Digital CMOS Pulse UWB Generator / Casu, M.R., Graziano, M., Zamboni, M.. - In: CIRCUITS SYSTEMS AND SIGNAL PROCESSING. - ISSN 0278-081X. - STAMPA. - 28:(2009), pp. 649-664. [10.1007/s00034-009-9101-z]

Availability:
This version is available at: 11583/2281087 since:

Publisher:
Springer

Published
DOI:10.1007/s00034-009-9101-z

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08 October 2026

A Fully Differential Digital CMOS UWB Pulse Generator

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Abstract

A new fully-digital CMOS pulse generator for impulse-radio Ultra-Wide-Band (UWB) systems is presented. First, the shape of the pulse which best fits the FCC regulation in the 3.1-5 GHz sub-band of the entire 3.1-10.6 GHz UWB bandwidth is derived and approximated using rectangular digital pulses. In particular, the number and width of pulses that approximate an ideal template is found through an ad-hoc optimization methodology. Then a fully differential digital CMOS circuit that synthesizes the pulse sequence is conceived and its functionality demonstrated through post-layout simulations. The results show a very good agreement with the FCC requirements and a low power consumption.

Keywords Ultra-Wide-Band, Impulse-Radio, CMOS

1 Introduction

In 2002 the Federal Communications Commission (FCC) released the spectrum between 3.1 and 10.6 GHz for unlicensed use with Ultra-Wide-Band (UWB) signals, provided that severe average and peak power constraints are respected [22]. According to the FCC regulations an UWB signal is characterized by a bandwidth of minimum 500 MHz or by a fractional bandwidth of at least 20%, regardless of the type of modulation or system of transmission. Since the time of the FCC announcement, an ever increasing number of researchers have been working on the design of integrated circuits for the generation of UWB pulses that comply with the FCC recommendations. In the recent literature two different techniques emerged for the generation of UWB pulses. In the first one a baseband signal of sufficiently large bandwidth is upconverted by mixing with a local oscillator whose frequency coincides with the central frequency of the desired UWB signal [13, 20]. The second one attempts to generate a baseband signal that directly extends over the entire UWB range or a sub-band of it, using an analog approach [3]-[1] or a digital technique [6]-[11]. Our pulse generator belongs to this last category and is characterized by a new fully digital and differential architecture, conceived for a standard CMOS technology. The generated pulse respects the UWB definition, having a -10 dB bandwidth of 1.73 GHz, centered around 4.15 GHz and so a fractional bandwidth of 42%. Unlike [6]-[8], and following an approach similar to [16]-[11], our pulse generator emits UWB signals in 3.1-5 GHz, instead of the full 3.1-10.6 GHz bandwidth, in order to avoid interference with wireless local area networks (WLAN) in 5-6 GHz. Again like in [16, 12, 19, 10], we rely on a safe DLL-based technique in order to generate

precise pulse durations, differently from the approach suggested in [7, 8, 17] of using gate delays which are imprecise, and subject to high variability (a DLL was also used in [17] but with a different purpose). However, our work differs from [16, 19, 10] in that we generate a fully differential signal by using a symmetrical architecture which eliminates the DC component, and from both [17, 19, 10] for a sound theoretical study about the pulse synthesis. Moreover, differently from [19, 10], the circuit is able to meet the FCC specifications without any band-pass filter and using a cheap $0.18\mu m$ technology. Furthermore, unlike [12, 11], a simpler architecture is used and less precise design is required, as fine-tuning of the size of different current sources employed in the referred work to create various pulse amplitudes is unnecessary.

A further technique consists in shaping a preliminary generated pulse by means of a band-pass filter and an UWB antenna so as to respect the FCC specifications. As suggested in [9, 4] the UWB pulse can be obtained co-designing both the pulse generator circuit and an ad-hoc shaping filter. In [8] both the digital technique and the shaping methodology are used to first generate a short rectangular pulse which is then shaped by the conjunction of an off-chip band-pass filter and the antenna. The shaping approach is only apparently simpler and presents also a drawback. In a single-chip perspective, the simplicity is counterbalanced by the fact that the integration of passive devices needed for the band-pass filter might be critical. As for the drawback, it is related to the overall system efficiency: Some of the energy of the generated pulse is filtered out by the band-pass filter and/or the antenna and will not be radiated. From this point of view, a synthetic pulse designed to respect the frequency mask as much as possible without filtering is more efficient.

The present paper is organized as follows. In section 2 we discuss the theoretical aspects that concern our method of pulse synthesis. Then, sections 3 and 4 cover the design aspects and the analysis of performance by means of simulations. Finally, the conclusions are drawn in section 5.

2 Pulse synthesis

The UWB impulse radio transmission requires the use of pulses of sufficiently large bandwidth that occupy a designated spectrum. As previously stated, one technique consists in mixing baseband pulses with a local oscillator (upconversion). Another technique consists instead in generating signals with no DC component that occupy directly the UWB spectrum, without the use of local oscillators. The derivatives of the Gaussian pulse belong to this second category and have been shown to cover the entire spectrum between 3.1 and 10.6 GHz [6, 15]. However, for reasons of flexibility in the use of frequencies, as well as to avoid interferences with WLAN radios around 5.5 GHz, the IEEE group who is working on the standardization of UWB as a physical layer for wireless personal area networks (WPAN) recommends to split that large bandwidth in two sub-bands: the lower one from 3.1 to 5 GHz and the upper one from 6 to 10.6 GHz [23]. As it will be clear later, our pulse generator works in the lower bandwidth. The FCC mask does not give special recommendations for such case of multi-bands. Therefore, in the absence of further regulations for the lower 3.1-5 GHz band, although not strictly necessary, we conservatively adapted the FCC mask around the upper 5 GHz limit, assuming the same 10 dB attenuation of the lower 3.1 GHz bound. Obviously, a

pulse which respects this stricter modified FCC mask also respects the less stringent original mask.

For this particular case of reduced bandwidth, we verified that low-order derivatives of the gaussian pulse, the ones employed for the entire spectrum between 3.1 and 10.6 GHz [6], are no more sufficient, as demonstrated in [15], and that higher order derivatives are necessary. More precisely, we have seen that the 21-st derivative of a Gaussian signal fits the 3.1-5 GHz bandwidth, as the curves in figure 1 show. Generating such signal with analog circuits and filters is a complex task [2]. With the

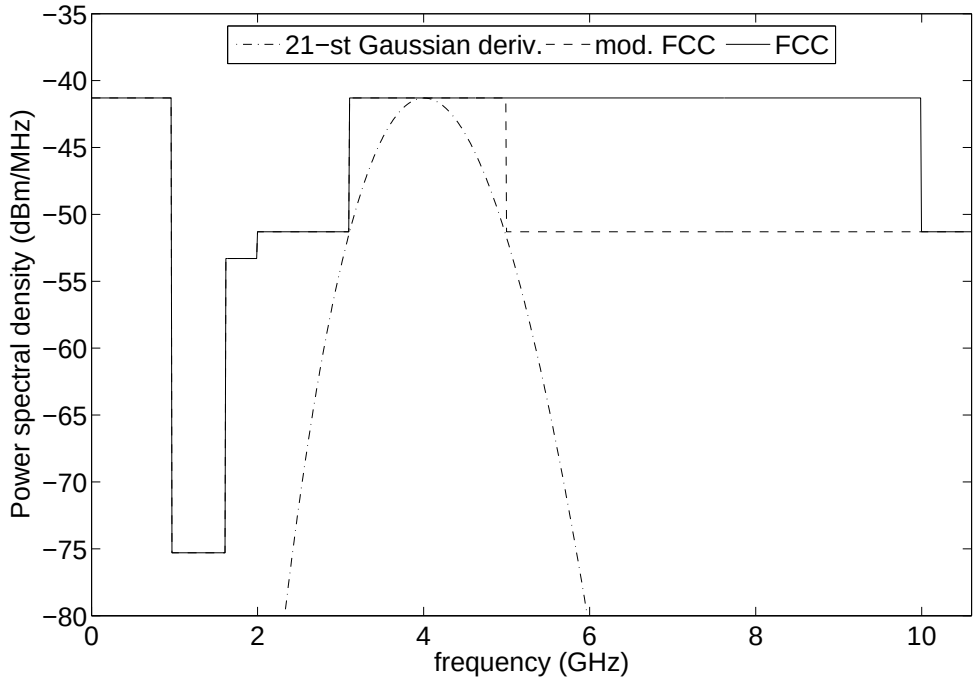


Figure 1: FCC masks, original and modified, and 21-st Gaussian power spectral densities.

aim of reducing the complexity of the pulse generator, we instead decided to resort to digital circuits that generate a sequence of pulses that approximate the signal at

stake. An example of rectangular "digital" pulse $p(t)$ of unitary height and duration $T_p = 1\,\mathrm{ns}$, centered around $t = 0$, is shown in the top plot of figure 2, solid line. The bottom plot, solid line, represents the pulse power spectral density, which is given by the square of the well-known "sinc" function

$$P(f) = T_p^2\,\mathrm{sinc}^2(fT_p) = \frac{\sin^2(\pi f T_p)}{(\pi f)^2}.$$

A limitation with rectangular digital pulses taking only 0/1 values, as can be generated by a CMOS digital circuit, is the strong DC component, as shown by the behavior around f=0 of the spectral plot in figure 2, solid line. In order to remove the DC component, it is necessary to build a signal that takes positive and negative values with respect to a quiescent point. The easiest way consists in an "analog subtraction" of two digital sequences. If two digital signals, say P and N, which get only 0/1 values, are subtracted, their difference $D = P - N$ get ternary values, viz. $(-1, 0, +1)$, as shown in table 1.

Table 1: Correspondence between digital values P and N and difference $D = P - N$.

P	N	$D = P - N$
0	0	0
0	1	-1
1	0	$+1$
1	1	0

An example of two subtracted digital pulses forming a "doublet" pulse is shown in figure 2, dashed lines, where the time-domain waveform and the spectral density are

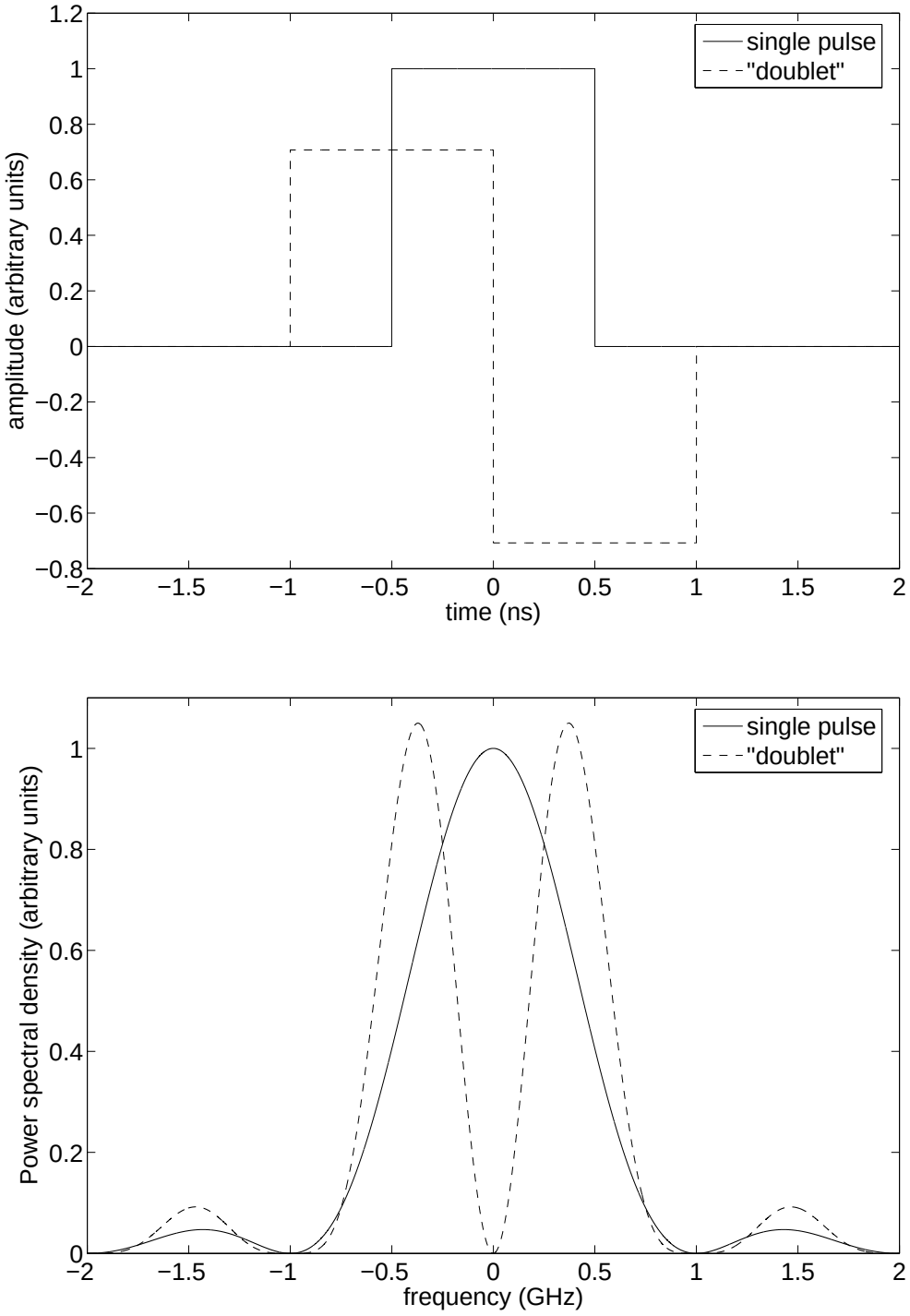


Figure 2: Rectangular pulses in time-domain (top) and their power spectral densities (bottom).

shown in the top and bottom plots, respectively. The figure clearly shows the absence of DC component and the resulting "passband" behavior of the doublet pulse.

Having found a relatively simple way to generate baseband pulses without DC component, the subsequent step is to find a combination of rectangular positive and negative pulses that approximate the 21-st gaussian derivative. We set up an optimization engine that, given a fixed time step, founds the sequence of pulses that approximates the desired signal spectrum in a norm sense. The base signal is the rectangular pulse $p(t)$ shown above. A generic sequence of pulses can be expressed as follows in the time-domain

$$g(t) = \sum_{i=1}^{M} D_i p\Big(t - iT_p + (M+1)\frac{T_p}{2}\Big)$$

and as such in the frequency-domain

$$G(f) = \sum_{i=1}^{M} D_i \frac{\sin(\pi f T_p)}{\pi f} e^{-j2\pi f(iT_p - (M+1)\frac{T_p}{2})}.$$

Amplitudes are quantized as shown above in table 1, i.e. $D_i \in \{-1, 0, +1\}$. The optimizer seeks for the M different amplitude values of D_i that minimize the difference between the sequence of rectangular pulses and the gaussian derivative. If we call the resulting approximating signal $g_a(t)$, with spectrum $G_a(f)$, and $g_{21}(t)$ the 21-st gaussian pulse derivative, whose spectrum is $G_{21}(f)$, the optimization engine minimizes the following error

$$\epsilon_{21,a} = \int_{-\infty}^{\infty} |G_{21}(f) - G_a(f)|^2 \, df.$$

Using a step of 10 ps and a minimum pulse duration of 60 ps, we found a solution which employs a train of 4 positive and 4 negative symmetrical pulses of duration 120, 120, 130 and 60 ps, and which never violates the modified and the original FCC

masks. For a precision of 10 ps, required to discriminate between 120 and 130 ps, is difficult to obtain in practice, we approximated the third pulse duration as 120 ps. This simplification has an impact on the low-frequency behavior of the spectrum: The FCC mask is not respected around 1.3 GHz and requires then little filtering. The slight attenuation necessary to respect the constraint can be simply provided at no additional cost by the UWB antenna designed to work in the selected bandwidth [8]. The plot on top of figure 3 reports both the time-domain version of the 21-st gaussian derivative and its "digital" approximation. The plot at the bottom contains their power spectral densities, the FCC modified mask and two other curves: the frequency-domain behavior of the S_{21} parameter of an UWB antenna [18, 14] and the digital pulse power spectral density "filtered" by such antenna. It is clear that the attenuation of the antenna in the low frequency range allows the FCC mask to be respected.

3 CMOS design

The ultra-short pulses described in the previous section can be created by combining clock edges separated from each other of precisely 60 ps. In other works such clock phases are obtained from a ring oscillator [19, 10] or from differently delayed versions - using gate delays - of the same clock signal [17]. Both approaches are highly sensitive to process as well as voltage and temperature (PVT) variations. For instance, the design in [19] is subject to up to ±30% delay variations over process corners. Contrarily to these approaches, we feed a delay-locked loop (DLL) with a relatively high-frequency clock signal and combine the edges taken from the voltage controlled delay line (VCDL)

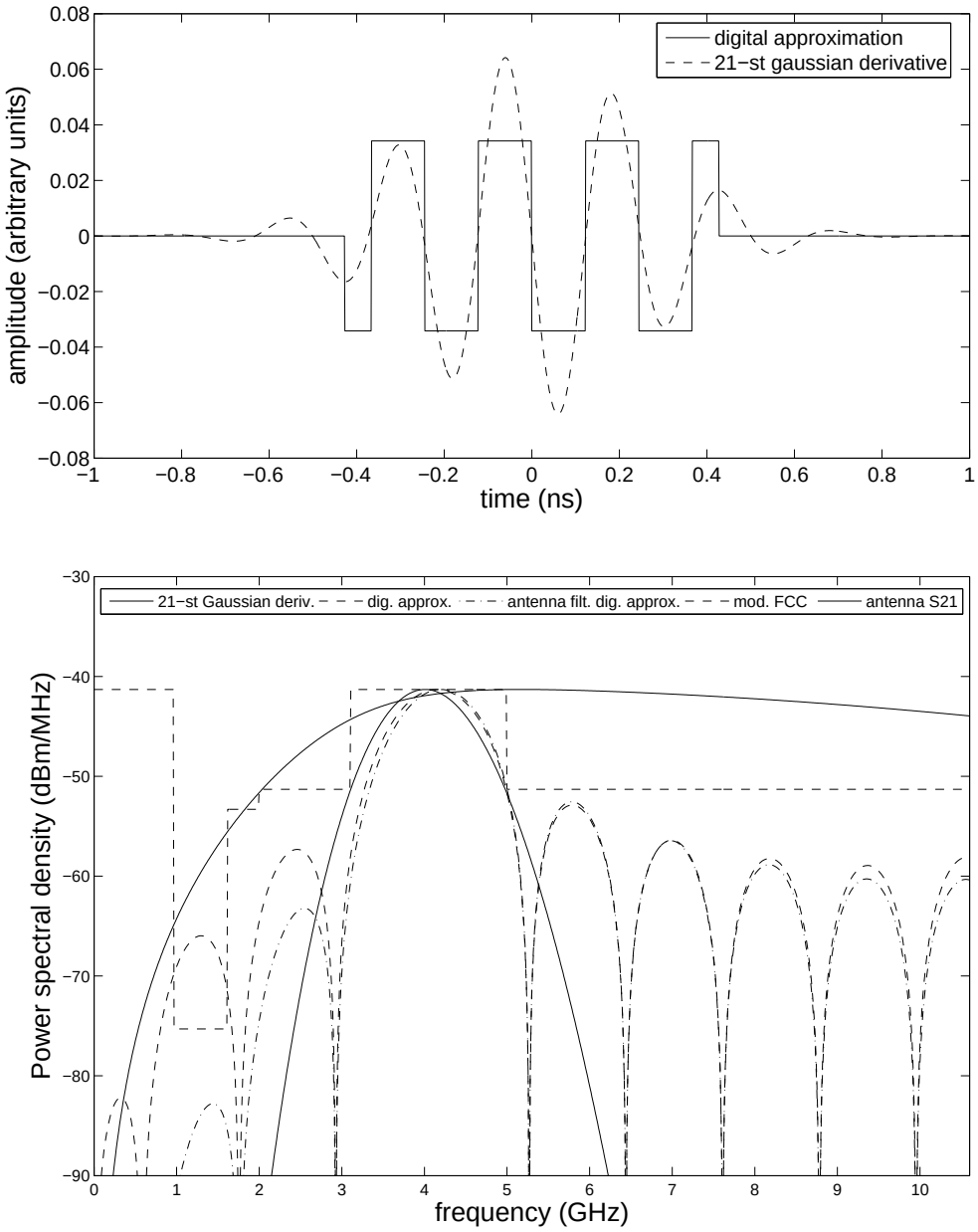


Figure 3: 21-st Gaussian and digital approximation in time-domain (top) and comparison between their spectra with and without antenna filtering (bottom).

of the DLL by means of a special CMOS gate. We will refer in the following to this CMOS circuit as Edge Combiner (EC). In such a way the required precision of 60 ps against PVT variations is guaranteed by the intrinsic properties of the DLL. One of

the problems with our approach is that a huge number of VCDL cells would be needed in order to obtain the 60 ps precision with a DLL locked to a low frequency external clock. In order to limit the number of delay cells, an on-chip produced high-clock frequency is then required. Similarly to the work reported in [17] we used another DLL in combination with another EC that produce a high-frequency signal from an external low-frequency reference clock at 33 MHz. In our work the resulting high-frequency clock runs at around 800 MHz while it was 533 MHz in the cited paper. In [17] the edges of such clock are delayed using gate delays. On the contrary, in our work the high-frequency clock signal is used to lock the DLL that produces the 60 ps separated clocks.

The fact of using a DLL mitigates the effect of PVT variations on the 60 ps delays. Moreover, since such duration is optimal according to the optimization procedure discussed in section 2, residual variations around such optimal point (due for instance to mismatches between NMOS and PMOS speed) will likely have little impact. In order to substantiate this intuition we identified a worst case of delay variation around the exact value which maximizes the power spectral density error. By supposing that delays can vary up to $\pm\Delta T$ it can be shown that a pattern of variations exists which results in the worst error. For instance for $\Delta T = 15$ ps, corresponding to a pessimistic variation of $\pm 25\%$, and referring to the time domain plot in figure 3, the pulse widths of the digital approximation would be from left to right (45 ps, 150 ps, 90 ps, 150 ps, 90 ps, 150 ps, 90 ps, 75 ps) instead of (60 ps, 120 ps, 120 ps, 120 ps, 120 ps, 120 ps, 120 ps, 60 ps). The corresponding power spectral density is in figure 4. The spectrum after antenna still respects the original FCC mask and is almost coincident with the

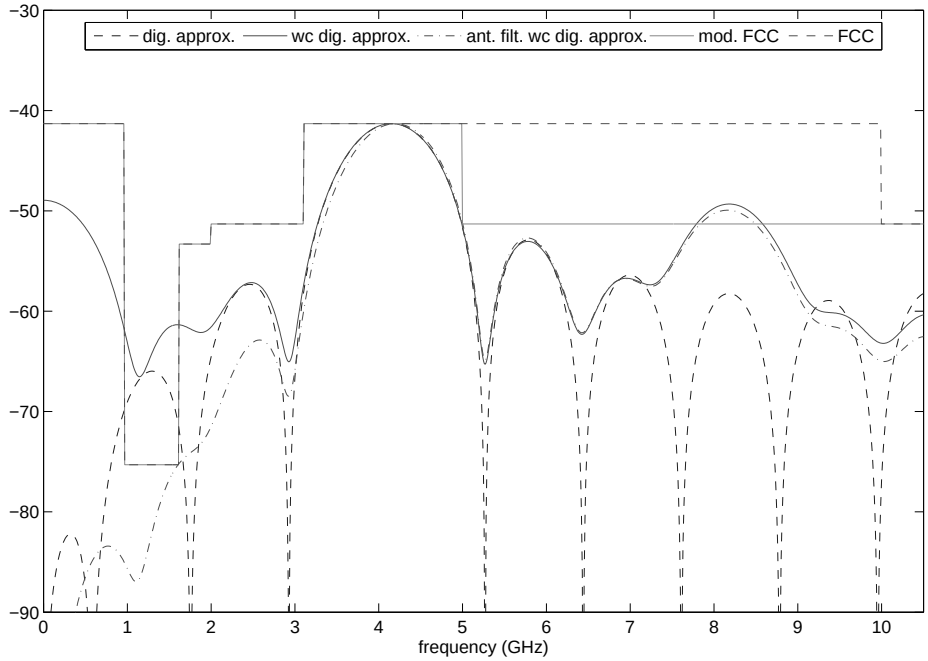


Figure 4: Power spectral densities of a nominal digital approximation and the corresponding worst case due to DLL cell delays variation with and without antenna filtering.

nominal case within the 3.1-5 GHz band. The modified FCC mask is respected except for less then 2 dB around 8 GHz. It must be said that in no way this violation will cause interference problems since the modified FCC mask was only defined in this work just to set a design goal. In addition the 25% delay variation is unrealistic.

From the circuit point of view, the novelty in this work is not in the DLL itself because standard implementations are sufficient, but rather in the EC for which we studied a specific topology. More precisely, the DLL feeds the EC with various clock square waves: ck1, ck2,..., ck15 and their negated values ($\overline{\text{ck1}}$, $\overline{\text{ck2}}$,..., $\overline{\text{ck15}}$). As already said, the distance between ck-i and ck-i+1 edges (and also between their corre-

sponding negated signals) is 60 ps. The EC consists of two identical branches that realize two complex CMOS and-or-invert functions. The outputs of the two EC branches are the positive (P) and negative (N) parts of the pulse sequence whose difference (D) forms the UWB pulse. As specified later, a true subtracter is unnecessary: The differential signal across the two single-ended outputs of the two branches represents the edge combiner output. The three 120 ps positive pulses are built by combining ck2 with $\overline{\text{ck4}}$, ck6 with $\overline{\text{ck8}}$ and ck10 with $\overline{\text{ck12}}$, while the shorter 60 ps positive pulse is obtained as a combination of ck14 with $\overline{\text{ck15}}$. The first negative pulse lasts 60 ps and is formed as a combination of ck1 with $\overline{\text{ck2}}$, while the following three negative 120 ps pulses are obtained by combining ck4 with $\overline{\text{ck6}}$, ck8 with $\overline{\text{ck10}}$ and ck12 with $\overline{\text{ck14}}$. The logic equations that combine all clocks to create the positive and negative signals are the following

$$P = (\text{ck2} \cdot \overline{\text{ck4}}) + (\text{ck6} \cdot \overline{\text{ck8}}) + (\text{ck10} \cdot \overline{\text{ck12}}) + (\text{ck14} \cdot \overline{\text{ck15}})$$

$$N = (\text{ck1} \cdot \overline{\text{ck2}}) + (\text{ck4} \cdot \overline{\text{ck6}}) + (\text{ck8} \cdot \overline{\text{ck10}}) + (\text{ck12} \cdot \overline{\text{ck14}})$$

where "$\cdot$" and "$+$" denote logic *and* and *or* operators. Figure 5, related to the positive part of the EC, shows the clock waveforms and their combinations that produce the 120 ps and 60 ps long pulses as well as the P signal. A similar set of clock waveforms, not reported for the sake of conciseness, are combined to obtain the N signal.

The circuit was designed in a 0.18μm 1.8 V mixed-mode RF CMOS technology chosen as the one guaranteeing a good trade-off between costs and performance. Figure 6 reports the schematic of the two branches of the EC, EC_P and EC_N, fed by the DLL clock signals. As stated above, the differential voltage D across the two single-ended

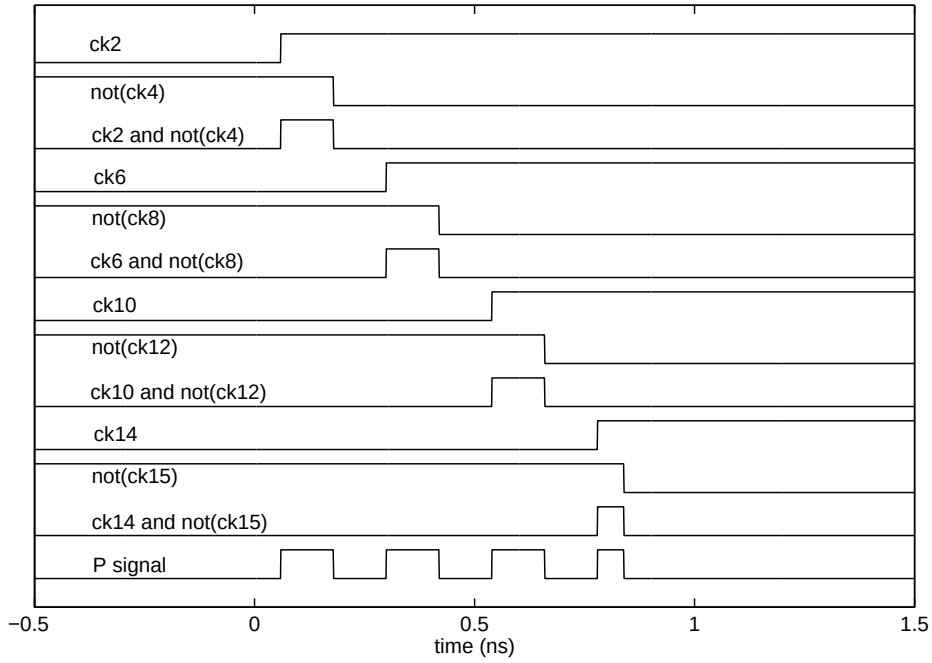


Figure 5: Clocks involved in the generation of P signal.

outputs, P and N, can be interpreted as the difference which represents the digital UWB pulse. Since the two CMOS branches are inverting, the output signal coherent with the previous definition is actually $D = N - P$, as shown in figure by the arrow direction.

Instead of a static CMOS gate with complementary pull-down and pull-up networks, which would slow down the rising edges of P and N signals through a series of many PMOS devices, we used only two PMOS as static pull-up, thus forming a pseudo-NMOS gate [21]. They are always on during normal operation, that is when the UWB signal is being created, and are instead cut-off by an enable signal in other circumstances for the purpose of saving power. As a result of the use of two always-on PMOS, the gate

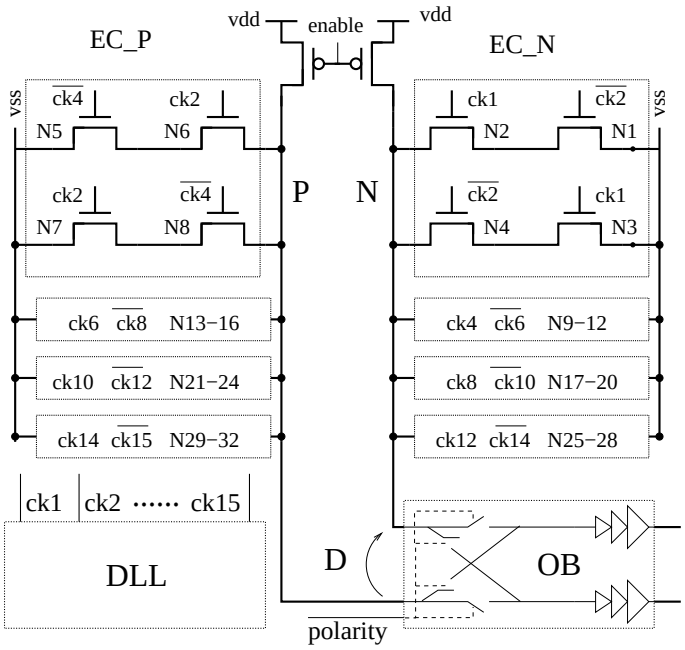


Figure 6: Pulse generator: Delay-Locked Loop (DLL), Edge-Combiner (EC), Output-Block (OB).

is of the ratioed-logic type, thus requiring special care in transistor sizing: The ratio between PMOS and NMOS sizes defines the logic swing, which will not be full rail-to-rail as if a static CMOS gate was used. The employment of only 2 PMOS devices helps switching speed not only because of the PMOS series avoidance, but also thanks to the reduction of the parasitic capacitance added to the EC_P and EC_N outputs. The pull-down NFETs are duplicated and their inputs cross-coupled (e.g. ck1-$\overline{\text{ck2}}$ and $\overline{\text{ck2}}$-ck1 in N1-4) for the sake of balancing the output parasitic capacitance in both rise and fall times. Keeping the parasitic capacitance as low as possible on heavily loaded P and N outputs is crucial and has to be achieved through proper layout of Source/Drain areas and Metal interconnects.

The operation can be described as follows. As shown in figure 5, prior to pulse

generation all clock signals start at low logic level, while their negated values are high. Therefore, none of the pull-down NFETs is active while pull-up PFETs force a high level on both P and N, such that $D = N - P = 0$. When the first signal ck1 rises and with $\overline{\text{ck2}}$ also still high, NMOS N1-4 force a low level on N while P is still high, thus $D < 0$. 60 ps later, when ck2 rises and $\overline{\text{ck2}}$ goes low, N1-4 switch off and pull-up keeps N high. At the same time P goes down through N5-8 by ck2 and $\overline{\text{ck4}}$ still high. As a result, $D > 0$ and the first, negative pulse in figure 3 of duration 60 ps has been generated through the sequence $D = 0$, $D < 0$, $D > 0$. After 120 ps, while D is still positive, ck4 goes high ($\overline{\text{ck4}}$ goes low) such that N5-8 switch off allowing the pull-up keep the P side high, while N9-12 switch on and let N go down. As a result, D switches from positive to negative in such a way that a 120 ps positive pulse is uttered. The sequence of switches proceeds through N13-N32 (not shown in figure 6 but identical to N1-4 and N5-8) until the pulse sequence completes. Key of the operation is that none of the ck1-ck14 signals goes low again before ck15 goes high: This constraint sets a minimum pulse repetition period of about 1.7 ns (maximum repetition frequency 590 MHz). The size of all transistors is W/L=$1.44\mu m/0.18\mu m$, except for NMOS N1-2 and N31-32 that are larger for the sake of speeding up the shorter pulses: W/L=$2.4\mu m/0.18\mu m$.

From this point on, the pulse generator is fully differential. The differential nature of the circuit makes it less sensitive to common-mode variations of quantities like temperature and power supply. The differential output is fed into an output block, OB in figure 6, whose purpose is twofold: It provides $\pm$ polarity, by simply switching the two single-ended outputs of the edge combiner, and drives the two buffers which in turn

drive the off-chip antenna. The circuit that provides polarity changes is detailed in figure 7. Instead of passive transmission gates switches, which revealed being too slow

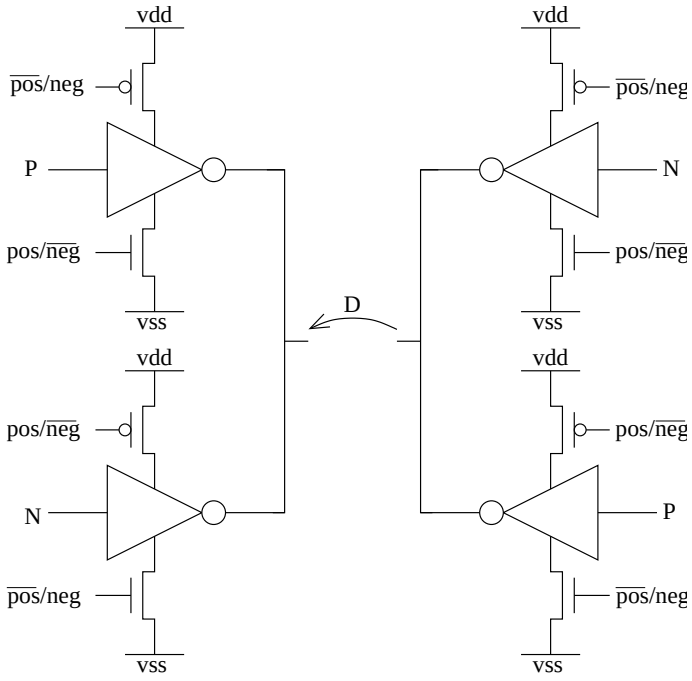


Figure 7: Polarity change block.

for the fast pulses, we used an active solution. The two output shorted three-state inverters on each of the two branches are enabled alternatively based on the polarity information carried by signals pos/$\overline{\text{neg}}$ and $\overline{\text{pos}}$/neg. When pos/$\overline{\text{neg}}$=0 (and so $\overline{\text{pos}}$/neg=1) the P and N signals, inverted, are brought to the left and right output branches, respectively. When instead pos/$\overline{\text{neg}}$=1 ($\overline{\text{pos}}$/neg=0), the opposite occurs and P and N, inverted, are sent respectively to the right and left outputs. In this case we employed lower threshold voltage transistors, available in the technology we used, in order to speed up the circuit operation. The P/N ratio of the inverter transistor widths was $(W_p/L_p)/(W_n/L_n) = (2.88\mu m/0.24\mu m)/(0.64\mu m/0.24\mu m)$, while the PMOS and NMOS driven by the polarity change signals were sized as $12.8\mu m/0.24\mu m$

and $6.4\mu m/0.24\mu m$, respectively (low threshold MOSFET's design rules required channel lengths longer than minimum). Polarity change can be used for binary phase shift keying (BPSK) modulations or for smoothing the spectrum in pulse-position modulations (PPM).

Particular care has been taken in the layout design. Pre-layout simulations showed that the most critical point in the whole design was the generation of the ultra-short 60 ps pulses. The effect of the source/drain-to-substrate and gate-to-drain capacitances of all FET's connected to the EC outputs tends to filter out the shortest pulses which may not have sufficient time to rise and fall (or viceversa). It was thus necessary a layout in which the source/drain diffusions were reduced as much as possible. Care was also given to reducing interconnect lengths in order not to add further metal capacitances. Figure 8 shows the layout of the P side of the edge combiner. The N side is symmetrical. The figure allows to appreciate the larger size of the NMOS transistors involved in the generation of the 60 ps long pulses, driven by ck14 and $\overline{\text{ck15}}$ (in the negative side their role is played by transistors connected to ck1 and $\overline{\text{ck2}}$. This precaution was necessary because using the same smaller size of the transistors that generate the 120 ps longer pulses would have not allowed a sufficient swing for the shorter ones. The sizing is the result of a compromise between current drive and parasitic capacitance: Both increase as MOS size grows.

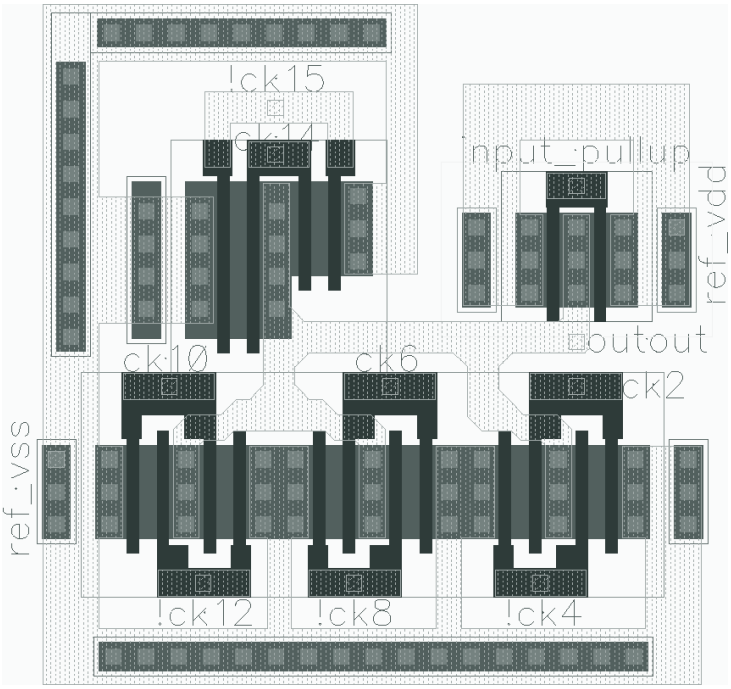


Figure 8: Optimized layout of the positive edge combiner branch.

4 Simulation results

We simulated the pulse generator at both schematic and post-layout level. We did not observe any degradation in post-layout extracted simulations, because we had conservatively estimated the parasitic capacitances in nodes P and N prior to layout design. Figures 9 and 10 reports post-layout time and frequency-domain simulations of the signal emitted by the output block. Although the ratioed-logic nature of the edge combiner does not permit the full Vdd-Vss swing, the output block, designed in a full CMOS style, regenerates the signal as much as possible. As a result, the transient waveform shows that the 120 ps long pulses reach the maximum allowed voltages of 1.8 V and -1.8 V while the 60 ps pulses are not able to reach the full swing. This limitation was given by the 0.18 μm technology we have used, whose transistors were not fast enough. However, this does not come to the detriment of the UWB signal which,

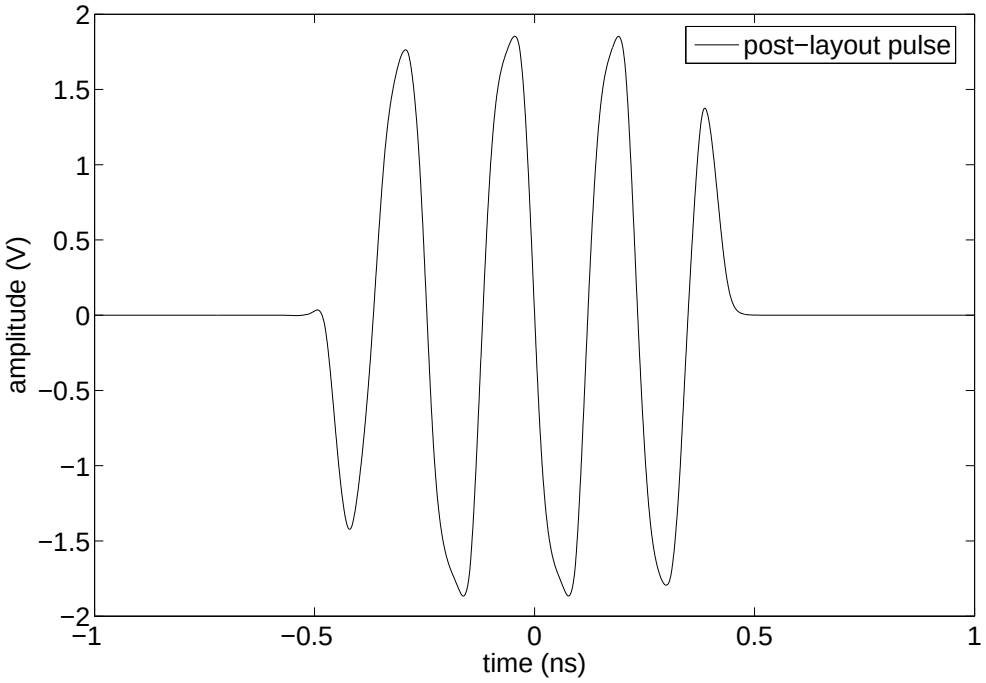


Figure 9: Post-layout emitted pulse in time-domain.

on the contrary, resembles even better the original 21-st gaussian derivative. Compared with the ideal spectrum of figure 3, the behavior at low frequency and in-band perfectly overlaps the ideal digital template and is even better at high frequency, due to the smoother shape of the waveform. The resulting -10 dB bandwidth of the UWB signal is 1.73 GHz, centered around 4.15 GHz. The fractional bandwidth is $100 \cdot 1.73/4.15 = 42\%$. The generated pulse then perfectly complies with the FCC definition of UWB signal. The unfiltered signal slightly violates the mask around 1.3 GHz, like the ideal digital pulse. However, the post-layout antenna filtered curve shows that the FCC mask is perfectly respected once the effect of the antenna is accounted for.

These results must be validated considering the possible effects of process, voltage and temperature variations (PVT). The structure has been simulated taking into ac-

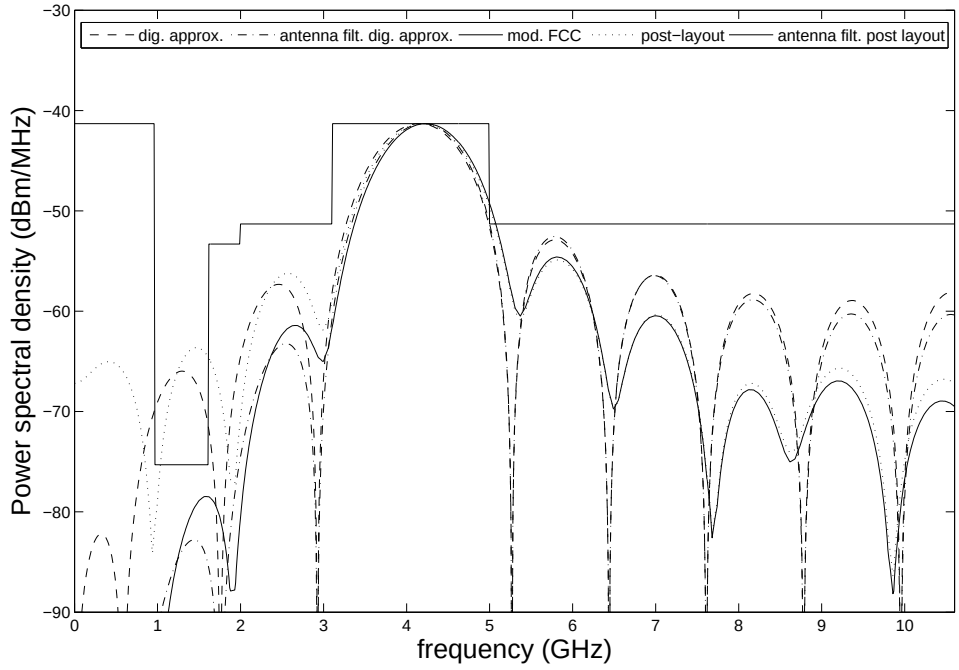


Figure 10: Power spectral density of post-layout emitted pulse, with and without antenna filtering, compared with the ideal digital approximation.

count the typical, slow and fast process corner for all transistors. Furthermore, the speed of NMOS vs. PMOS has been differentiated so that all possible mismatches between rise and fall times are included in the simulations. Finally, $\pm 10\%$ power supply variations as well as temperature corners (0°C, 25°C, 85°C) have been considered. The various power spectral density obtained in all possible combinations of the PVT values are plotted in figure 11 in which the typical and the overall worst and best cases are highlighted. All cases respect the original FCC mask. As for the modified mask there is a violation around 5 GHz. The same remark made for the DLL delays variations holds in this case as the modified FCC mask was just set as a design reference and therefore no interference issues will arise as long as the original mask is respected. The only

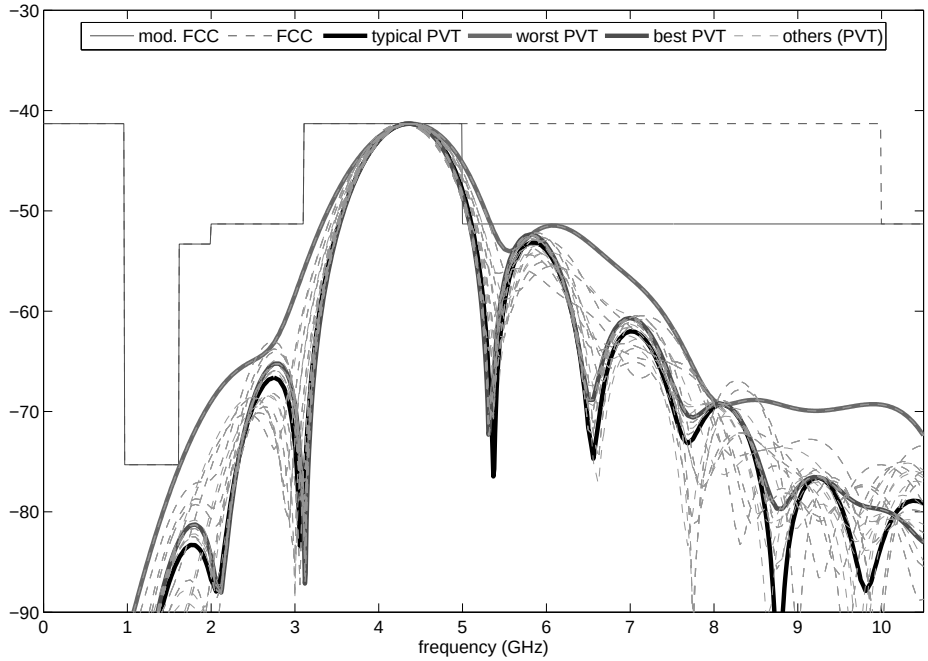


Figure 11: Power spectral densities of post-layout emitted pulse with PVT variations and antenna filtering.

drawback, from the receiver point of view, is that some of such out-of-band transmitted energy will not be captured in case a WLAN interference filter is used. Anyway, such energy is negligible compared to the whole useful energy between 3.1 GHz and 5 GHz.

We measured by simulation the current drawn from the 1.8 V power supply during the pulse generation. The energy necessary for a single pulse is 2 pJ which corresponds, for instance, to a power dissipation of 200 μW for a pulse repetition rate of 100 MHz. The power consumption is then sufficiently low for the use in low data-rate sensor networks or other WPAN applications, where extended battery lives are key requirements [23].

5 Conclusion

In this paper we presented a new pulse generator for UWB impulse radio based on a 0.18 μm CMOS technology. Its main features are a fully differential and digital architecture. The generated pulse occupies the UWB spectrum between 3.1 and 5 GHz with a -10 dB bandwidth of about 1.73 GHz and a fractional bandwidth of 42%, which is perfectly compliant with the definition of ultra-wideband signal given by the Federal Communications Commission. Its low power consumption makes it suitable for battery operated devices employed in applications like sensor and wireless personal area networks. We are currently working on the design of a CMOS low power/low cost receiver that we expect to integrate with the present pulse generator in a single chip UWB transceiver.

References

[1] Y. Bachelet *et al.*, " Fully integrated CMOS UWB pulse generator", Electronics Letters, Vol. 42, n. 22, 2006.

[2] S. Bagga et al., "Codesign of an Impulse Generator and Miniaturized Antennas for IR-UWB," IEEE Trans. Microwave Theory Tech., Vol. 54, No. 4, April 2006.

[3] D. Barras *et al.*, "Low-Power Ultra-Wideband Wavelets Generator With Fast Start-Up Circuit David Barras", IEEE TRAN on microwave theory and techniques, vol 54, n. 5 May 2006.

[4] C. Buccella *et al.*, "Pulse-Shaping Numerical Procedures for Ultrawide Bandwidth Systems", IEEE Transactions on Magnetics, Volume 43, Issue 4, April 2007 pp. 1549 - 1552

[5] J.R. Fernades *et al.* "A pulse Generator for UWB-IR Based on a Relaxation Oscillator", IEEE Transaction on Circuit and Systems II: Express Briefs, March 2008, Vol 55, N.3, pp. 239-243

[6] H. Kim et al., "All-digital low-power CMOS pulse generator for UWB system," Electronics Letters, Vol. 40, No. 24. Nov. 2004.

[7] H. Kim *et al.*. "Digitally Controllable Bi-Phase CMOS UWB Pulse Generator", IEEE 2005 International Conference on Ultra-Wideband, Sept. 2005 pp. 109 - 112.

[8] J. Lee et al., "System-on-Package Ultra-Wideband Transmitter Using CMOS Impulse Generator," IEEE Trans. Microwave Theory Tech., Vol. 54, No. 4, April 2006.

[9] G. Lu *et al.*, Antenna and pulse designs for meeting UWB spectrum density requirements, IEEE Conference on Ultra Wideband Systems and Technologies, 16-19 Nov. 2003 pp. 162 - 166

[10] P.P. Mercier *et al.*, "Ultra-low-power UWB for sensor network applications", IEEE International Symposium on Circuits and Systems, 2008, 18-21 May 2008, pp. 2562 - 2565.

[11] O. Mi-Kyung *et al.* "Digitally-Controlled UWB Pulse Generator for IEEE 802.1 5.4a systems", International Conference on Consumer Electronics, 2007. 10-14 Jan. 2007.

[12] T. Norimatsu *et al.*. "A UWB-IR Transmitter With Digitally Controlled Pulse Generator" IEEE Journal of Solid-State Circuits, Volume 42, Issue 6, June 2007, pp. 1300 - 1309.

[13] J. Ryckaert *et al.*, "Ultra-wide-band transmitter for low-power wireless body area networks: Design and evaluation," *IEEE Trans. Circuits Syst. I*, vol. 52, no. 12, pp. 2515–2525, 2005.

[14] H. G. Schantz, "Planar elliptical element ultra-wideband dipole antennas," in IEEE APS Int. Symp. Dig., vol. 3, Jun. 2002, pp. 16-21.

[15] H. Sheng*et al.* "On the spectral and power requirements for ultra-wideband transmission", Proceedings of IEEE Int. Conf. on Communications, Anchorage, AL, USA, March 2003, pp. 738-742"

[16] L. Smaini et al., "Single-Chip CMOS Pulse Generator for UWB Systems," IEEE J. Solid-State Circuits, Vol. 41, No. 7, July 2006.

[17] L. Stoica *et al.*, "An Ultrawideband System Architecture for Tag Based Wireless Sensor Networks," *IEEE Trans. Veh. Technol.*, vol. 54, no. 5, pp. 1632–1645, 2005.

[18] S. B. T. Wang *et al.*, "Circuit Modeling Methodology for UWB Omnidirectional Small Antennas," IEEE J. Selected Areas in Comm., vol. 24, no. 4, April 2006, pp. 871-877.

[19] D.D. Wentzloff *et al.*, "A 47pJ/pulse 3.1-to-5GHz All-Digital UWB Transmitter in 90nm CMOS", IEEE International Solid-State Circuits Conference, 2007. 11-15 Feb. 2007 pp. 118 - 591

[20] D. D. Wentzloff and A. P. Chandrakasan, "Gaussian Pulse Generators for Subbanded Ultra-Wideband Transmitters," IEEE Trans. Microwave Theory Tech., Vol. 54, No. 4, April 2006, pp. 1647-1655.

[21] N. H. E. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective,* 3rd edition, Addison Wesley, 2005, Chap. 6.

[22] "Revision of part 15 of the commission's rules regarding ultra-wideband transmission systems," Report and order, adopted February 14, 2002, released July 15, 2002, FCC.

[23] IEEEn 802.15 wpan low rate alternative phy task group 4a (tg4a). [Online]. Available: http://www.ieee802.org/15/pub/TG4a.html

Figure captions

Figure 1. FCC masks, original and modified, and 21-st Gaussian power spectral densities.

Figure 2. Rectangular pulses in time-domain (top) and their power spectral densities (bottom).

Figure 3. 21-st Gaussian and digital approximation in time-domain (top) and comparison between their spectra with and without antenna filtering (bottom).

Figure 4. Power spectral densities of a nominal digital approximation and the corresponding worst case due to DLL cell delays variation with and without antenna filtering.

Figure 5. Clocks involved in the generation of P signal.

Figure 6. Pulse generator: Delay-Locked Loop (DLL), Edge-Combiner (EC), Output-Block (OB).

Figure 7. Polarity change block.

Figure 8. Optimized layout of the positive edge combiner branch.

Figure 9. Post-layout emitted pulse in time-domain.

Figure 10. Power spectral density of post-layout emitted pulse, with and without antenna filtering, compared with the ideal digital approximation.

Figure 11. Power spectral densities of post-layout emitted pulse with PVT variations and antenna filtering.

Table captions

Table 1. Correspondence between digital values P and N and difference $D = P - N$.

Table 1

P	N	$D = P - N$
0	0	0
0	1	-1
1	0	$+1$
1	1	0

Figure 1

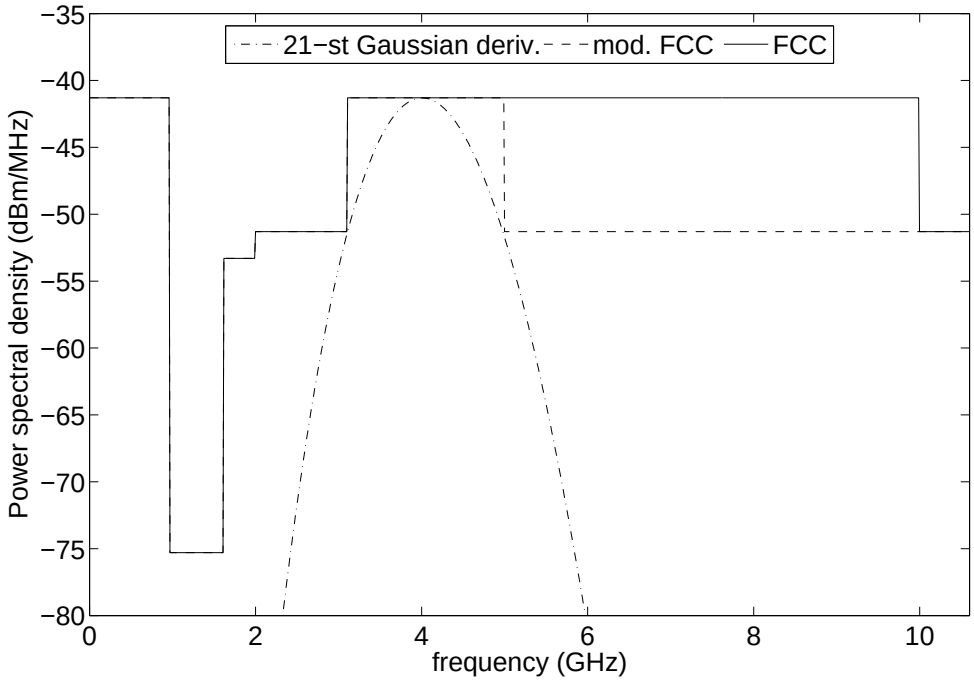
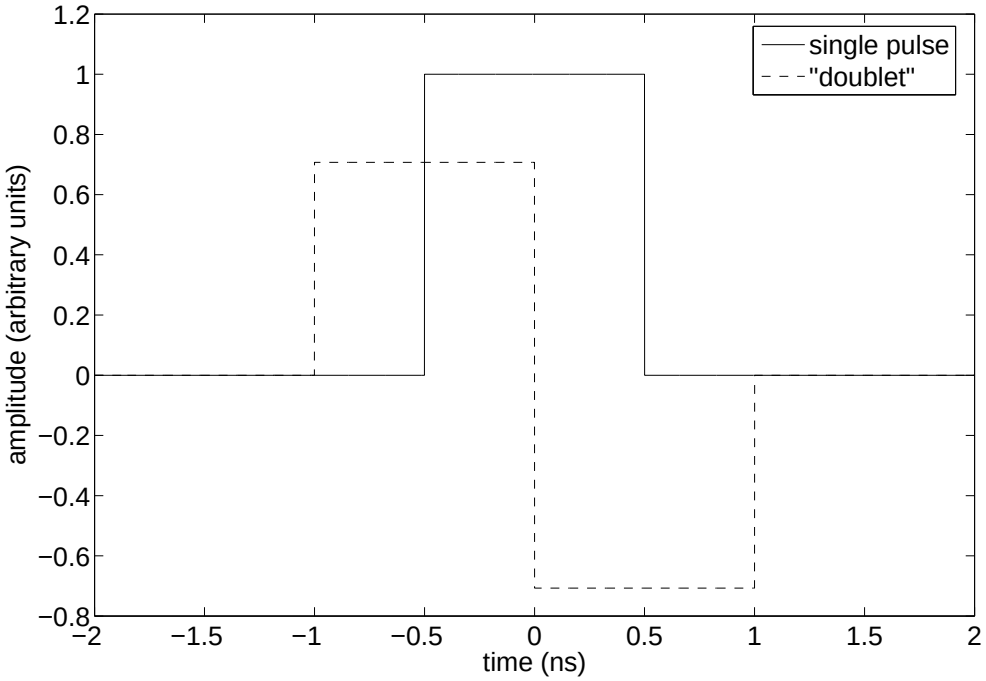

21−st Gaussian deriv.
mod. FCC
FCC
Power spectral density (dBm/MHz)
frequency (GHz)
−35
−40
−45
−50
−55
−60
−65
−70
−75
−80
0
2
4
6
8
10

Figure 2


single pulse
"doublet"
amplitude (arbitrary units)
time (ns)
1.2
1
0.8
0.6
0.4
0.2
0
−0.2
−0.4
−0.6
−0.8
−2
−1.5
−1
−0.5
0
0.5
1
1.5
2

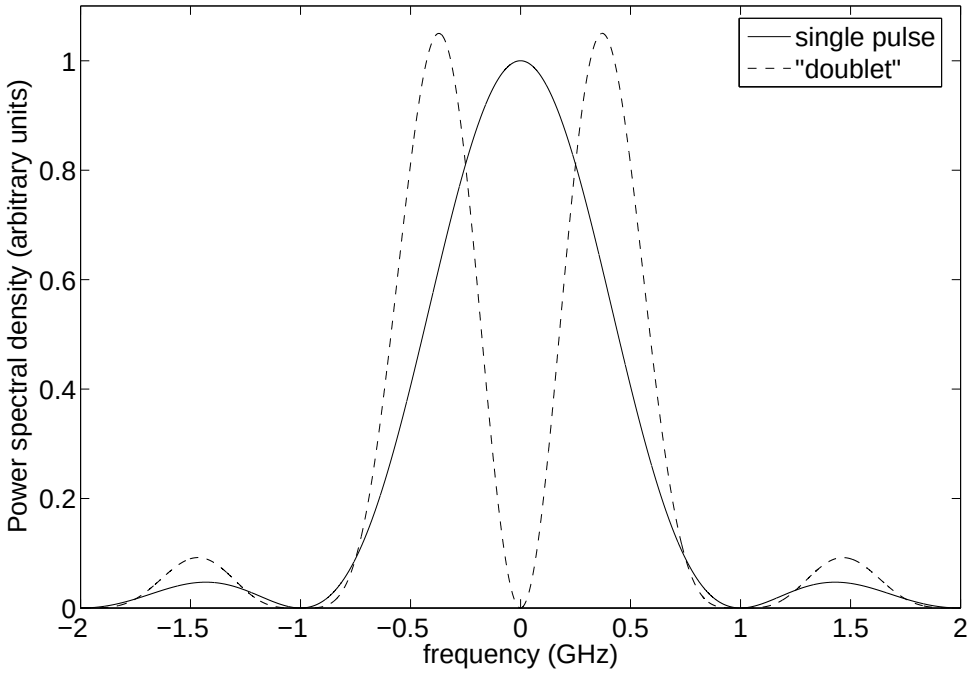
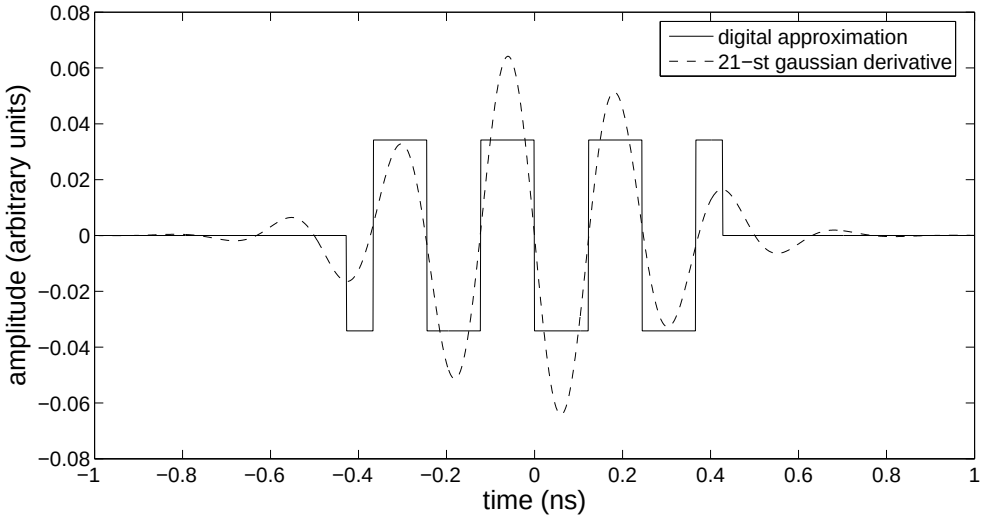

single pulse
"doublet"
Power spectral density (arbitrary units)
frequency (GHz)
1
0.8
0.6
0.4
0.2
0
−2
−1.5
−1
−0.5
0
0.5
1
1.5
2

Figure 3


digital approximation
21−st gaussian derivative
amplitude (arbitrary units)
time (ns)
0.08
0.06
0.04
0.02
0
−0.02
−0.04
−0.06
−0.08
−1
−0.8
−0.6
−0.4
−0.2
0
0.2
0.4
0.6
0.8
1

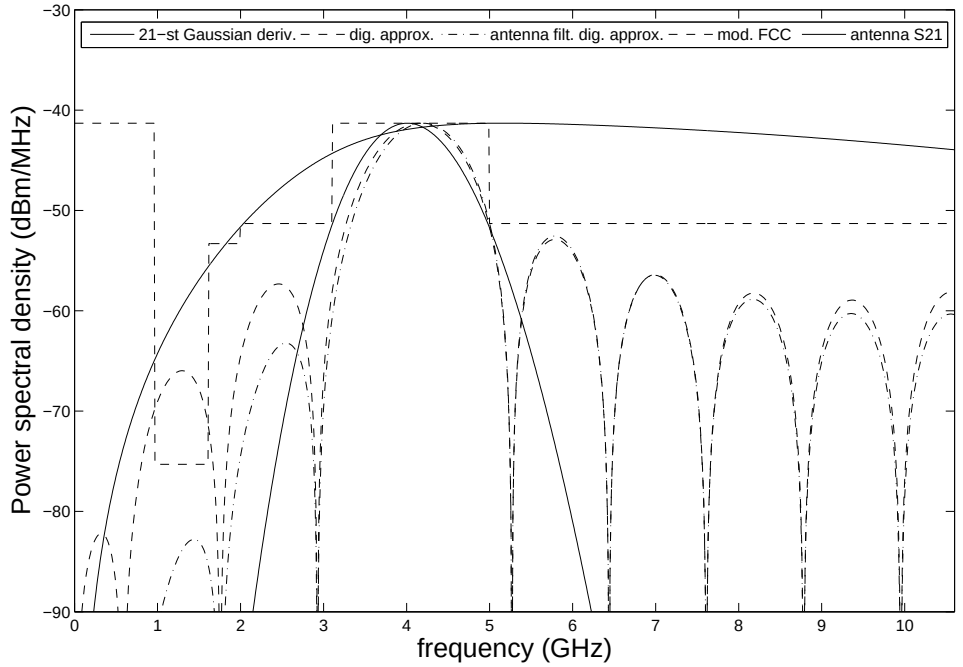

21−st Gaussian deriv.
dig. approx.
antenna filt. dig. approx.
mod. FCC
antenna S21
Power spectral density (dBm/MHz)
frequency (GHz)
−30
−40
−50
−60
−70
−80
−90
0
1
2
3
4
5
6
7
8
9
10

Figure 4

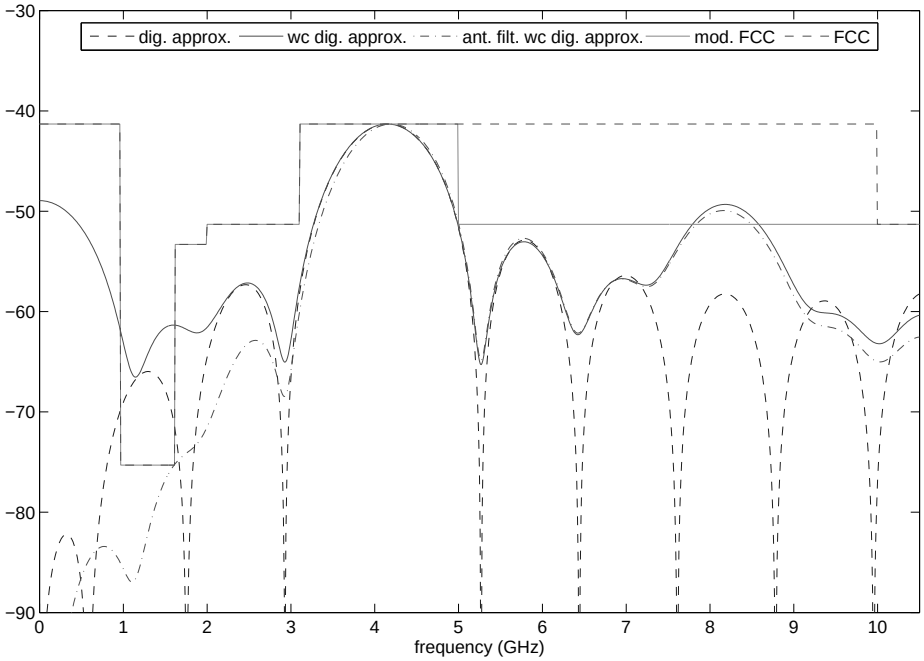

dig. approx.
wc dig. approx.
ant. filt. wc dig. approx.
mod. FCC
FCC
−30
−40
−50
−60
−70
−80
−90
0
1
2
3
4
5
6
7
8
9
10
frequency (GHz)

Figure 5

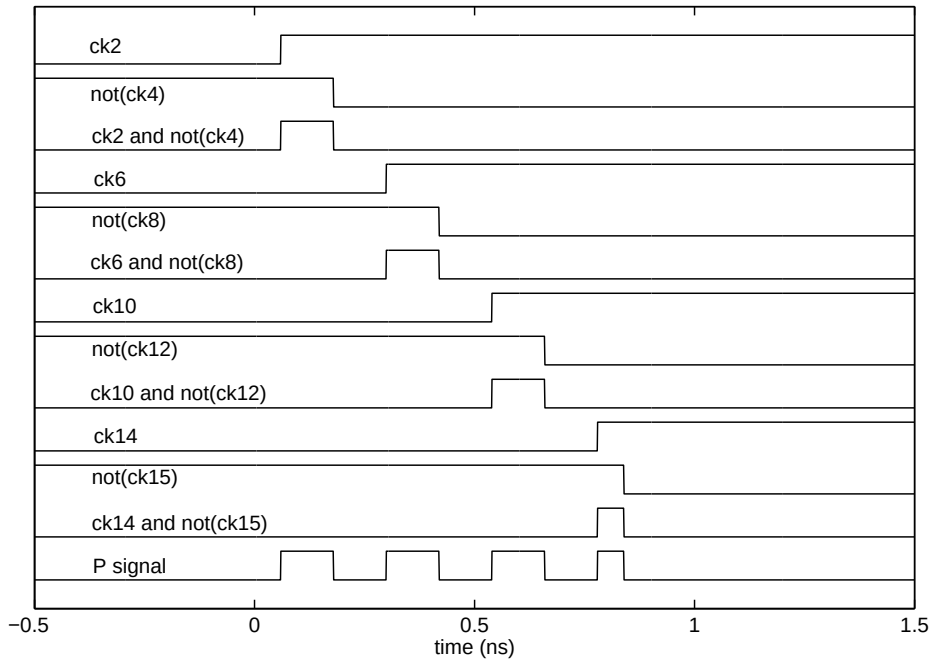

ck2
not(ck4)
ck2 and not(ck4)
ck6
not(ck8)
ck6 and not(ck8)
ck10
not(ck12)
ck10 and not(ck12)
ck14
not(ck15)
ck14 and not(ck15)
P signal
−0.5
0
0.5
1
1.5
time (ns)

Figure 6

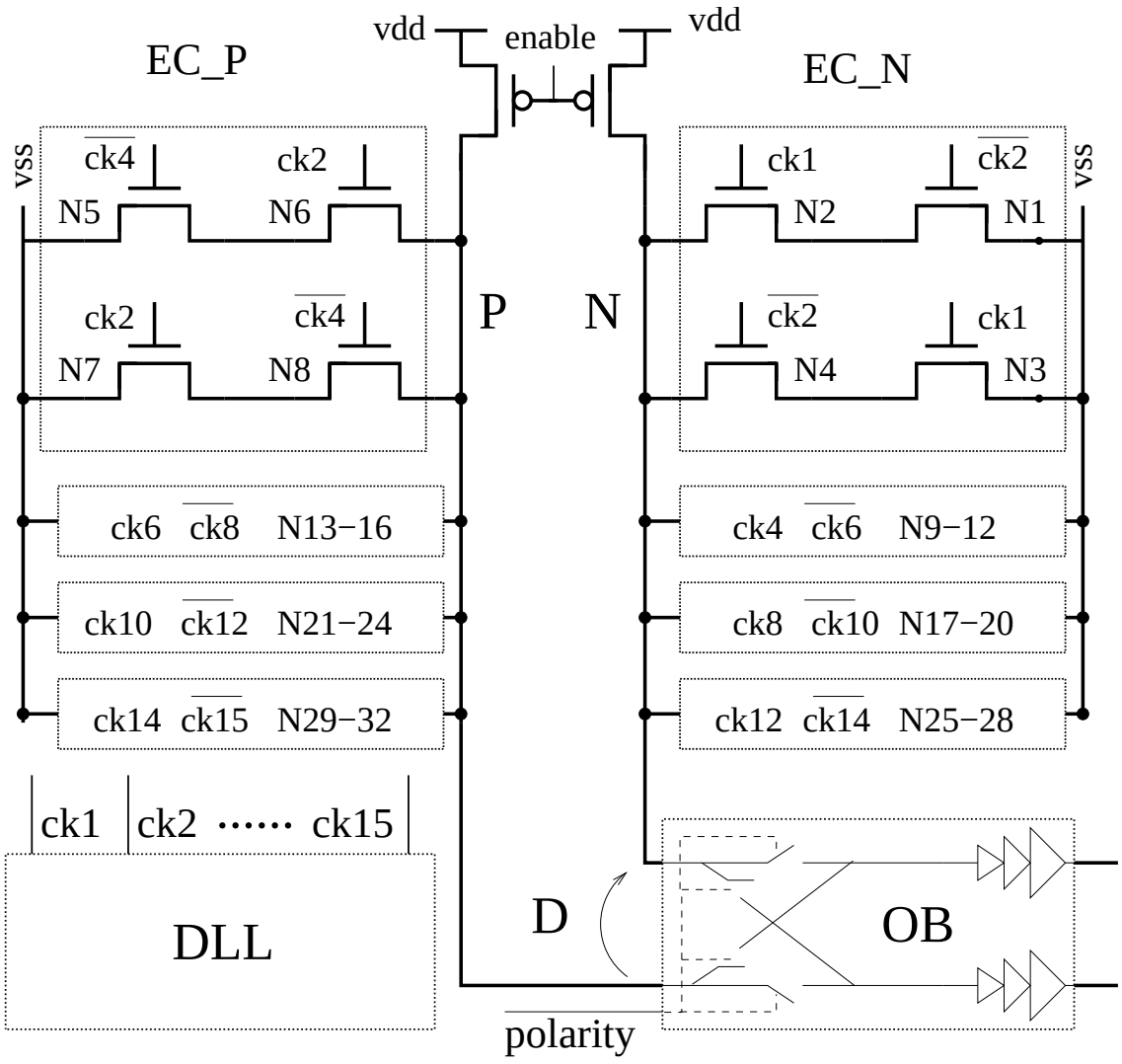

vdd
enable
vdd
EC_P
EC_N
vss
ck4
ck2
N5
N6
ck1
ck2
N2
N1
ck2
ck4
N7
N8
P
N
ck2
ck1
N4
N3
ck6 ck8 N13−16
ck4 ck6 N9−12
ck10 ck12 N21−24
ck8 ck10 N17−20
ck14 ck15 N29−32
ck12 ck14 N25−28
ck1 ck2 ····· ck15
DLL
D
OB
polarity

Figure 7

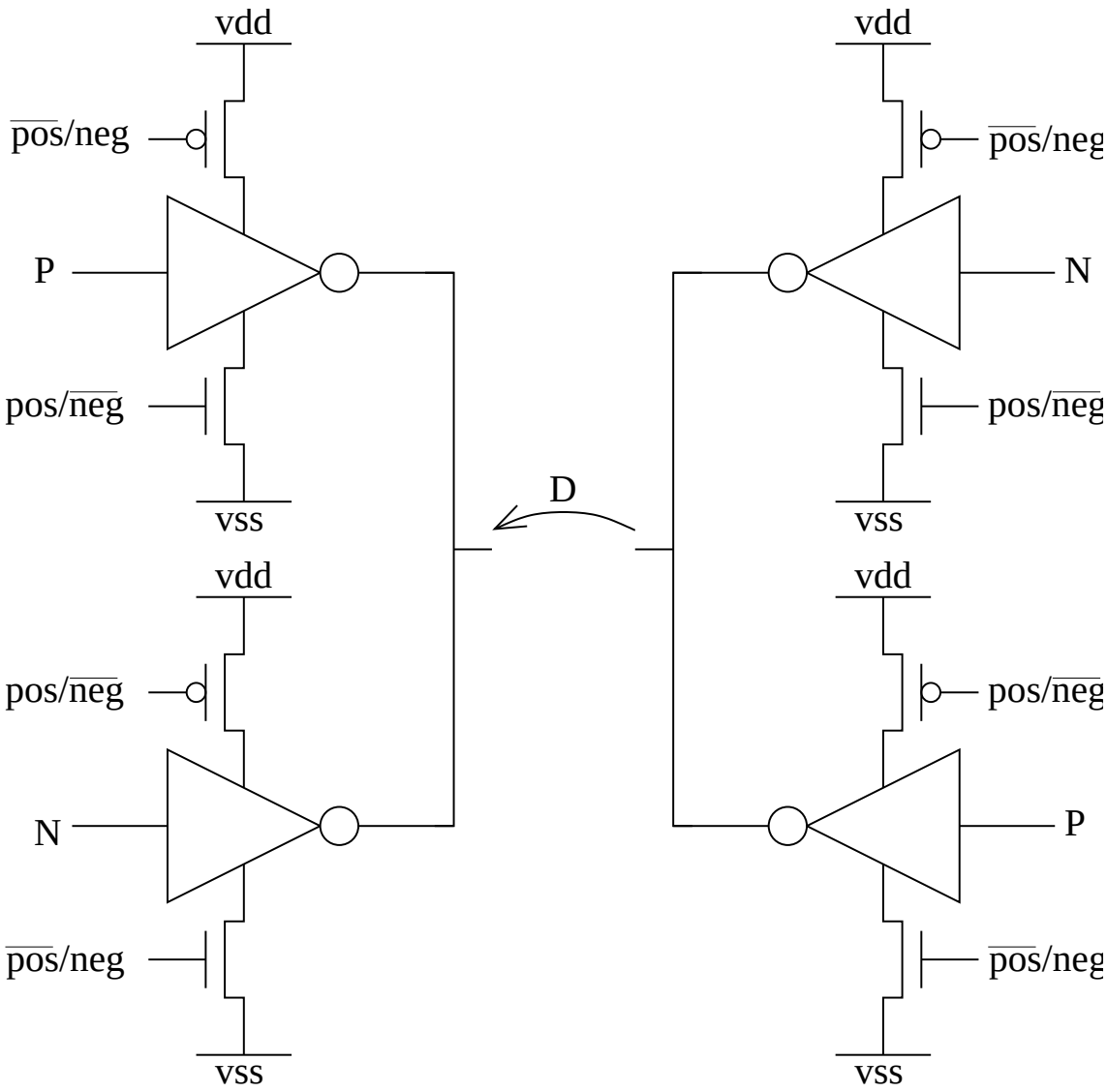

vdd
pos/neg
P
pos/neg
vss
vdd
pos/neg
N
pos/neg
vss
D
vdd
pos/neg
N
pos/neg
vss
vdd
pos/neg
P
pos/neg
vss

Figure 8

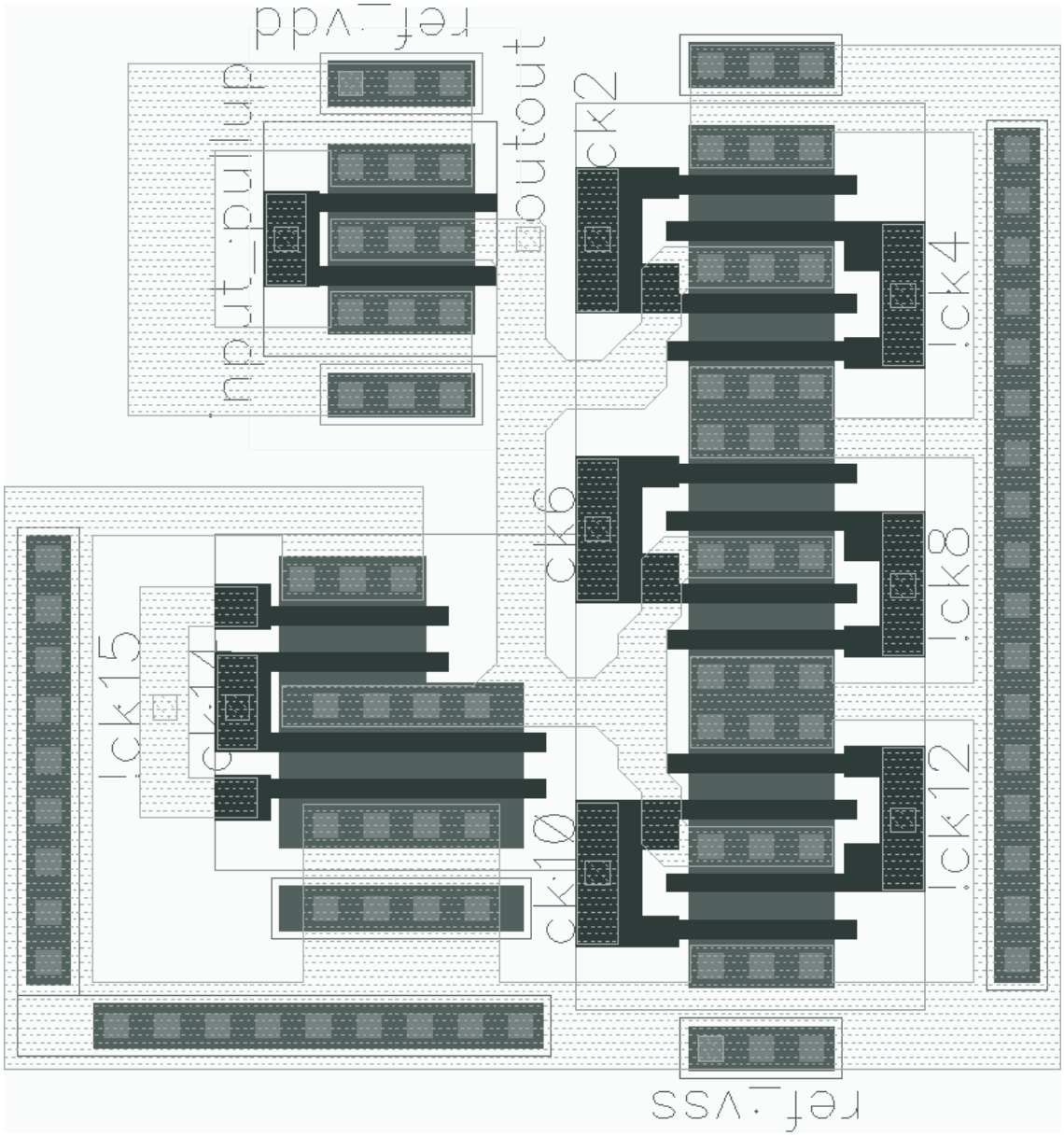

ref_vdd
output_pullup
boutout
ck2
ck4
ck6
ck8
ck10
ck12
ck14
ck15
ref_vss

Figure 9

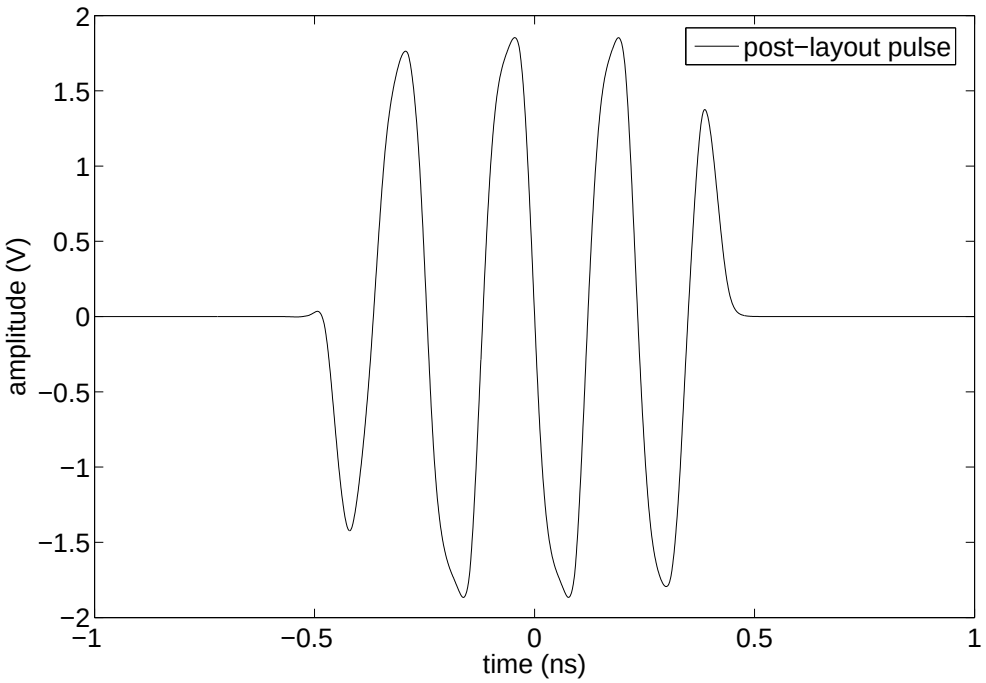

post−layout pulse
amplitude (V)
time (ns)
2
1.5
1
0.5
0
−0.5
−1
−1.5
−2
−1
−0.5
0
0.5
1

Figure 10

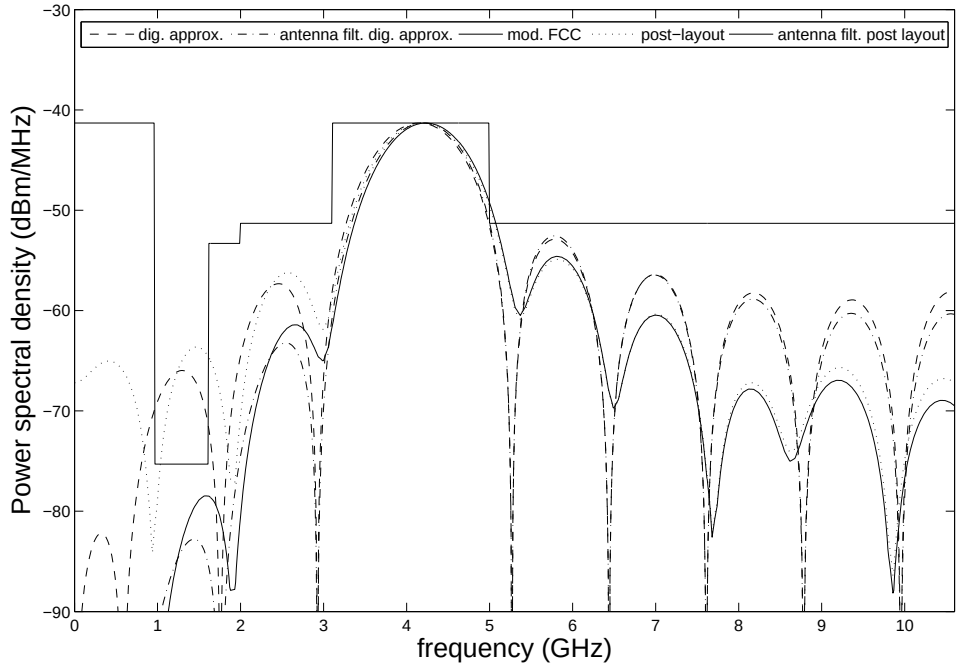
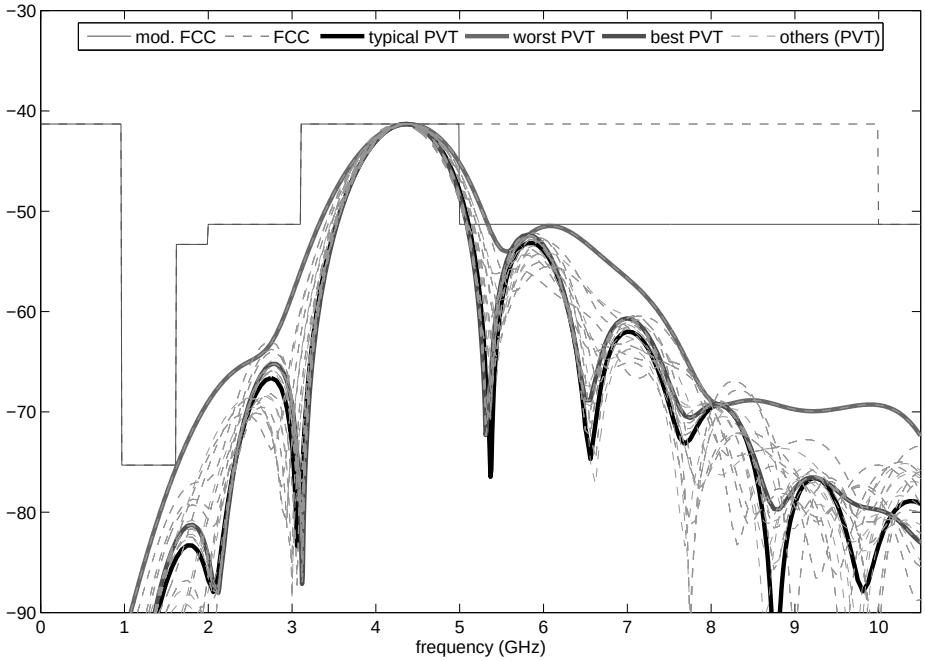

dig. approx.
antenna filt. dig. approx.
mod. FCC
post−layout
antenna filt. post layout
Power spectral density (dBm/MHz)
frequency (GHz)
−30
−40
−50
−60
−70
−80
−90
0
1
2
3
4
5
6
7
8
9
10

Figure 11


mod. FCC
FCC
typical PVT
worst PVT
best PVT
others (PVT)
−30
−40
−50
−60
−70
−80
−90
0
1
2
3
4
5
6
7
8
9
10
frequency (GHz)