Behavioral Macromodels of Digital Integrated Circuits for RF Immunity Prediction

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***Abstract* — This paper addresses the generation of accurate macromodels of digital ICs accounting for both the functional and the out-of-band behaviour of devices. The proposed models that can be effectively used for immunity predictions are obtained from port transient responses only and can be implemented in any commercial tool based on SPICE or mixed-signal hardware description languages. The approach is demonstrated on a real test board by injecting a RF noise disturbance into a digital IC: a systematic study comparing actual measurements and simulation predictions is carried out.**

I. Introduction

Nowadays, the development of modern high-end electronic equipments requires the assessment of system performance at the early stages of their design. Many ICT systems like mobile phones or safety equipments mounted on vehicles, airplanes and trains are immersed in a noisy EM environment and must satisfy severe reliability constraints in terms of signal integrity and electromagnetic compatibility. In the above electronic systems, the most critical elements are the digital devices that may poorly operate in the presence of EM disturbances.

In this paper, we propose a systematic study of the effects of RF noise directly or indirectly coupled to digital systems. This study will lead to the generation of accurate and efficient macromodels of digital devices, accounting not only for their functional behaviour, but also providing insights on their RF immunity. Predictions obtained by means of the proposed IC macromodels and SPICE simulations are compared to actual measurements carried out on a real test board.

II. Test Board

The study is conducted on a data communication link composed by two digital devices interconnected by a PCB trace. In order to inject the RF noise into the system, the test board shown in Fig. 1 has been designed as suggested by [1]. The board implements the idea of injecting a disturbance through a long coupled interconnected structure. The two devices, i.e., a driver on the right side in Fig. 1 and a receiver on the left, are connected to terminals 4 and 2 of the coupled structure, respectively. A RF generator is connected to the terminal 3 and a 50 Ω matching resistor to terminal 1. The interconnection, that has a length of 25 cm, is designed to maximize the coupling between the signal communication line and the aggressor trace carrying the RF disturbance. In this study, the two digital ICs in Fig. 1 are simple inverter gates (TI SN74AUC1G04DBVR), optimized for 1.8-V operation. This simplified structure and the two inverters are considered to avoid the complexity of real ICs mounted on an application board and thus allowing to completely understand and model the RF immunity of a digital circuit.

In this work, all the parts composing the complete system in Fig. 1, i.e., the coupled interconnect and the two devices are modeled by means of a suitable set of modeling methodologies, as suggested in [2]. All the models are then implemented in SPICE in order to simulate the complete interconnected structure.

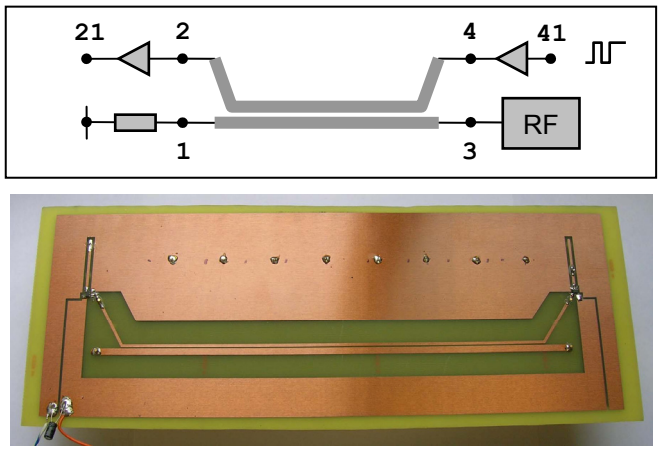

Fig. 1. Ideal setup designed to inject the RF noise into a digital IC (top panel). Test board (bottom panel).

In particular, the macromodels for the two digital devices are obtained by means of the state-of-the-art Mπlog (Macromodeling via Parametric Identification of Logic Gates) methodology [3-6]. A brief overview of the basic Mπlog technique and the new enhancements of the basic structure of the models to account for the immunity effects are provided in Section III.

In this study, the coupled line structure on the board was characterized by means of a two-port network analyzer that has provided a complete set of S parameters up to 2 GHz. These measurements were used to generate a model of the linear interconnect, by means of the IdEM (Identification of Electrical Macromodels) methodology [4]. IdEM is a modeling technique based on the estimation of a reduced order rational approximation reproducing the port behaviour of a complex linear structure from their port responses. The approximation is performed via the powerful and well-known Vector Fitting (VF) algorithm [7], with an a-posteriori

correction to assure the passivity of the obtained rational model [8]. Fig. 2 shows a selection of port frequency responses; the comparison of measurements and fitting highlights the excellent accuracy of the obtained model to reproduce the real measurements.

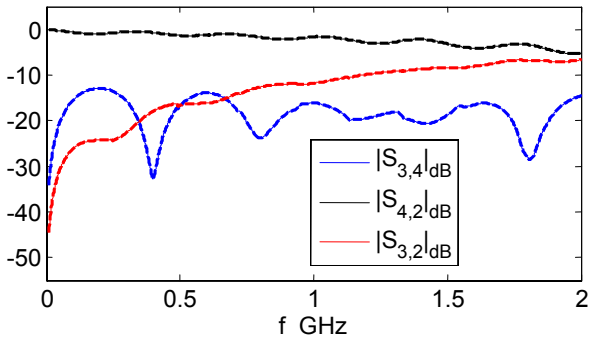

Fig. 2. Selection of S parameters of the test board in Fig. 1. Solid lines: measured parameters; dashed lines: model responses.

III. IC MACROMODELS

This Section reviews the Mπlog methodology and presents the enhancements of the basic model structures to account for the effects of RF disturbances feeding the device ports.

Briefly speaking, the Mπlog approach amounts to define a suitable set of parametric relations approximating the nonlinear dynamical behavior of devices [3-6]. The model parameters are computed by fitting the model responses with the device port transient signals that are obtained by stimulating the devices with properly-designed voltage sources. These sources are devised to excite every possible dynamical behavior of the port within a predefined bandwidth, thus allowing the obtained models to account for both the functional and the out-of-band behavior of devices. The proposed models that are expressed as mathematical relations hiding the internal structure of devices can be readily implemented according to standard industrial simulation tools like SPICE and VHDL-AMS. In addition, such already-mentioned SPICE and VHDL-AMS implementations are completely compatible with the multilingual extension of IBIS (Input/output Buffer Information Specification), which is the most established standard for the behavioral description of IC ports. In fact, ver. 4.1 of IBIS specification [9] is an extension, recently devised to overcome some limitations of the original standard, allowing for more general models not necessarily based on simplified circuit interpretations.

For the sake of simplicity, the discussion is based on the two single-ended devices in Fig. 1, i.e. the driver and the receiver circuits. In addition, the model structures are provided with the simplifying assumption of constant power supply voltages. Previous results on the extension of the proposed models to account for the fluctuations of the power supply can be found in [3] and estimation of parametric models from measured transient responses is demonstrated in [5]. The output buffer constitutive relation for the driver in Fig. 1 is sought as a dynamic nonlinear parametric two-piece model of the form [3]

$$i_4(t) = w_H(t)\, i_H(v_4(t), d/dt) + w_L(t)\, i_L(v_4(t), d/dt) \qquad (1)$$

where v_4 and i_4 are the port voltage and current signals at pin 4, i_H and i_L are parametric submodels describing the port behaviour in the high and low logic states, respectively, and $w_H(t)$ and $w_L(t)$ are weighting coefficients describing state transitions. It is worth noting that a possible RF disturbance at the output pin of a driver (pin 4 in Fig. 1) weakly affects the signals at its input pin (pin 41 in Fig. 1) and that equation (1) can be proven to accurately describe the output port behavior even for out-band signals.

On the other hand, the conventional model representation for receiver circuits, like the one in Fig. 1, writes [6]

$$\begin{cases} i_2(t) = i_{IN}(v_2(t), d/dt) \\ v_{21}(t) = g(v_2(t), d/dt) \end{cases} \qquad (2)$$

where i_{IN} is a dynamical parametric relation accounting for the input port behavior and $g(\cdot)$ is the input-output constitutive relation of the receiver that accounts for the transmission of the voltage signals between its input and output pins. Previous results on the modeling of receiver circuits, including the detection mechanism and the effects of power supply voltage fluctuations, are reported in [6]. The above paper provides a simple but effective solution for the second equation in (2) that can be effectively used when the devices operate in normal condition only. Here we suggest to improve the model in [6] by using for $g(\cdot)$ a block structure defined by the series connection of a static block followed by a dynamic one. For the static part, the input-output DC characteristic is used. For the alternate dynamic part, the same class of parametric relations used for the submodels in (1) are used.

The Mπlog modeling procedure outlined in this Section is applied to build the macromodels for the two ICs mounted on the test board of Fig. 1. For this study, the models are obtained from the responses of detailed transistor-level descriptions of the devices that are freely available from the official website of the vendor and are implemented as SPICE subcircuits. The macromodels are computed for a power supply voltage of 1 V, which will be hereinafter used for carrying out our study. This supply level, which is close to the lower limit indicated by the manufacturer, was adopted since it is representative of the most critical bias conditions of the device for its noise immunity.

The obtained models of the devices in Fig. 1 are first validated by comparing their responses to the responses of the detailed transistor-level descriptions of devices. As an example, Fig. 3 shows the comparison of the reference and the macromodel responses of the receiver circuit for different voltage signals feeding its input port. Three cases are considered, with different amplitudes of a possible RF disturbance corrupting the functional signal (see top panel of Fig. 3). The predicted signals at the receiver output (bottom panel) highlight a very good accuracy of the proposed models.

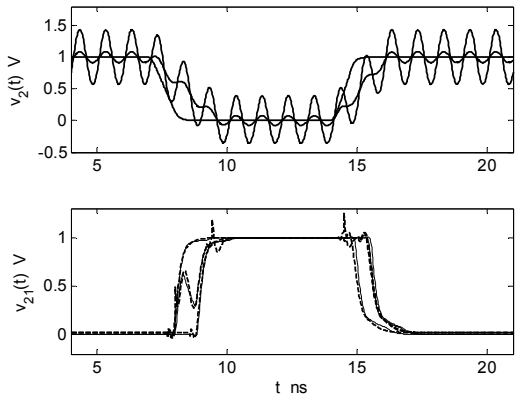

Fig. 3.Voltage sources $v_2(t)$ applied to the input port of the receiver (top panel) and detected signals $v_{21}(t)$ at the output pin of the receiver; solid lines: reference transistor-level model, dashed curves: macromodel (bottom panel).

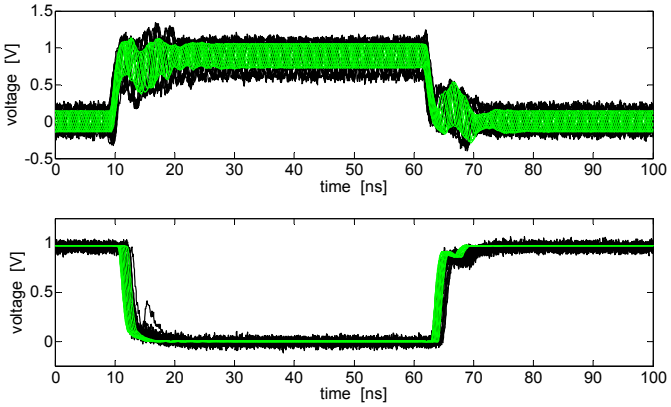

Fig. 4. Voltage signals at input port (top panel) and output port (bottom panel) of the receiver for an injected RF noise level of 10 dBm. Black lines: measurements; green lines: simulations.

The Mπlog models are then used to simulate the complete structure in Fig. 1 and the obtained responses are compared to measurements carried out on the real board. In the absence of any RF noise (i.e., the RF source is not connected and is replaced by a matching resistor of 50 Ω) the model results are in excellent agreement with measurements, as already documented in the literature [3,5] (detailed results are not reported here for lack of space).

IV. Device Immunity

In this Section, the test board shown in Fig. 1 is used to perform a systematic set of measurements aimed at the assessment of the immunity of the receiver circuit mounted on the left side of the board. As already outlined in the introduction, a RF generator with 50Ω internal impedance and a variable frequency and power is used to inject a disturbance into the communication system. The RF noise, which couples with the functional signals transmitted on the communication line, is increased to verify the receiver immunity thresholds. For this reason, the voltage signal at input terminal 2 of the receiver and the transmitted voltage at terminal 21, i.e., the data processed by the receiver circuit, are monitored to verify possible communication errors. It is worth to remark that the noise immunity of the driver is not considered since, for technology reasons, the internal circuitry of a driver is much more immune to a disturbance injected into its output port. In this experiment, the RF generator produces a 267 MHz sinusoidal waveform and its power is varied between 10 and 23 dBm. The input terminal 41 of the driver circuit is instead connected to a waveform generator producing a square wave signal, i.e. a 010 cyclic bit stream, with a period of 100 ns. A digital scope (Lecroy WavePro 7000A Series) and passive voltage probes (Tektronix P6114B) with a bandwidth of 3 GHz are used to record the voltage signals along the propagation path.

In order to verify the feasibility of the proposed modeling approach to predict the immunity effects of devices, the agreement between real measurements and simulations is assessed. The macromodels obtained for both the devices and the coupled line are used together in a SPICE environment to simulate the complete interconnected structure of Fig. 1. It is worth adding that the lumped equivalents of the voltage probes, as provided by the supplier, are included in the simulation setup to reproduce the real measurements.

Fig. 4 shows an example of a comparison between measured and predicted responses for the voltage signal at the input (terminal 2) and at the output (terminal 21) ports of the receiver when the power of the RF generator is 10 dBm. The plots are obtained by wrapping in time twenty different periods of the receiver port voltage responses. This comparison highlights that the accuracy of signals predicted by the macromodels are in very good agreement with actual measurements. Besides, the differences between measurements and simulations are mainly due to the model that has been generated from the transistor-level description of devices. Better results could be obtained for models generated from measured data as suggested in [5]. It is also worth to notice that, in this case, the power of the injected disturbance is not sufficient to generate errors in the transmission of the functional signal, even if the input voltage of the receiver has a quite large amount of noise superimposed to the functional part of the signal.

The power of the injected RF signal is then increased to verify potential errors of the received bit at terminal 21. Table I collects the main results of the study and provides in a compact form the information for both the received data 0 (output of the receiver at low state) or 1 (output of the receiver at high state). Each cell compares the possibility of receiver

TABLE I
RF Immunity of the Receiver at High and Low States

RF power level (dBm)	errors @ receiver output - V21 (measurements / simulations)	
	HIGH state	LOW state
10	no / no	no / no
13	no / no	possible / possible
16	no / no	yes / possible
20	possible / possible	yes / yes
23	yes / yes	yes / yes

errors estimated from measurement or simulation. Apart from the classical indications (*yes* and *no*), a third keyword (*possible*) is used in this table: it means that some glitches in the corresponding H or L states exist and, consequently, error detections at the output of the receiver are possible, depending upon the sampling time. An example of this behaviour is the simulation curves reported in the bottom panel of Fig. 4, where results of the RF injection of 16 dBm are shown. In this case, the low state is perturbed just after the switching by some spurious transitions which can generate faults in the data communication link.

Moreover, the 16 dBm test case shows an asymmetric behaviour of the device immunity for the two logic states: the H state is more robust than the L one. In fact (see Table I), a RF level of 23 dBm must be injected in the system for inducing regular faults in the high state, whereas a noise power of 13 dBm may already provoke errors in the low state.

Even in such a critical situation of asymmetry, the Mπlog approach proves its capabilities, thanks to the two-piece structure (see Eq. 1). Only in the L logic state of the test employing a power of 16 dBm, a discrepancy between the model and the measurements can be noticed in the bottom panel of Fig. 5: the output of the real receiver is perturbed by spurious transitions whatever the sampling time is, while the Mπlog predicts them only just after the switching. This discrepancy can be explained by analyzing the top panel of the same Fig. 5 reporting the voltage at the input port of the receiver (terminal 2): it highlights differences between measurement and simulation results on the amplitude of the oscillations, especially for the H input state. This leads to suspect a non-optimal transistor-level description of the device input port and confirms the need of an Mπlog macromodel extraction from ad-hoc measured data.

Finally, when the injected power reaches 23 dBm (Fig. 6), the receiver is no longer able to reproduce at its output port the functional signal, both for the L and the H state, but such signal is so distorted that it appears to be almost a replica of the injected noise disturbance. Also in this case, the Mπlog models (even if extracted from transistor-level descriptions) ensure good quality predictions of the out-of-band and out-range behaviour of the devices, both in terms of amplitude level and of waveform shape.

V. Conclusions

This paper addresses the generation of digital IC macromodels accounting for both the functional and the noise immunity behavior of the devices. The feasibility of the proposed approach has been verified on a real point-to-point interconnect by comparing measurements and simulations. Next steps towards the generation of a complete IC macromodel will have to focus on the injection of RF noise into the power supply net of the device and on the modeling of these effects.

References

[1] J. S. Bazzoli, B. Démoulin, M. Cauterman, P. Hoffmann, "Susceptibility of integrated circuits connected to wiring systems", *Proc. of IEEE Symposium on Embedded EMC (2EMC),* Rouen, France, Sep. 2005.

[2] F. G. Canavero, S. Grivet-Talocia, I. A. Maio, I. S. Stievano, "Linear and nonlinear macromodels for system-level signal integrity and EMC assessment", *IEICE Transactions on Communications - Special Issue on EMC*, vol. E88-B, no. 8, pp. 1121-1126, Aug. 2005.

[3] I. S. Stievano, I. A. Maio, F. G. Canavero, "Mπlog, macromodeling via parametric identification of logic gates", *IEEE Transactions on Advanced Packaging*, vol. 27, n. 2, pp. 15-23, Feb. 2004.

[4] Modeling tools of the EMC group available at http://www.emc.polito.it.

[5] I. S. Stievano, I. A. Maio, F. G. Canavero, "Behavioral models of I/O ports from measured transient waveforms", *IEEE Transactions on Instrumentation and Measurement*, vol. 51, no. 6, pp. 1266-1270, Dec. 2002.

[6] I. S. Stievano, F. G. Canavero, I. A. Maio, "Behavioral macromodels of digital IC receivers for analog-mixed signal simulations", *Electronic Letters*, 2005.

[7] B. Gustavsen, A. Semlyen, "Rational approximation of frequency responses by vector fitting", *IEEE Transactions on Power Delivery*, vol. 14, pp. 1052-1061, July 1999.

[8] S. Grivet-Talocia, "Passivity enforcement via perturbation of Hamiltonian matrices", *IEEE Transactions on CAS-I*, vol. 51, n. 9, pp. 1755-1769, Sept. 2004.

[9] "I/O Buffer Information Specification (IBIS) Ver. 4.1", on the web at http://www.eigroup.org/ibis/ibis.htm.

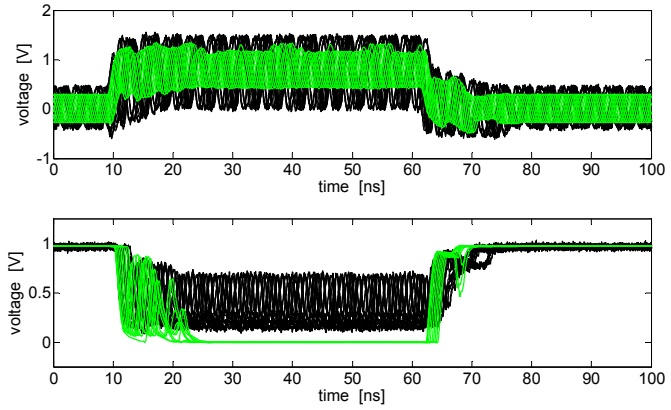

Fig. 5. Voltage signals at input port (top panel) and output port (bottom panel) of the receiver for an injected RF noise level of 16 dBm. Black lines: measurements; green lines: simulations.

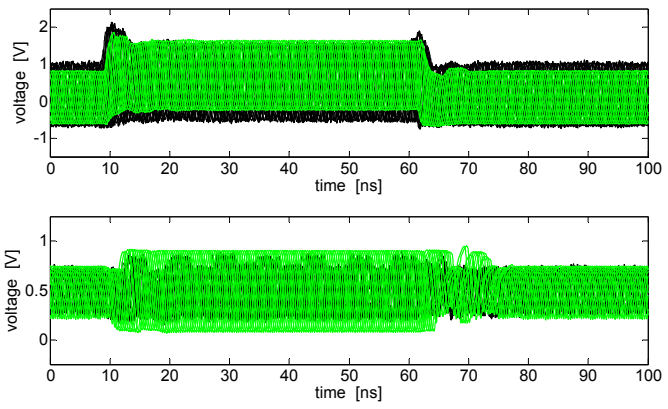

Fig. 6. Voltage signals at input port (top panel) and output port (bottom panel) of the receiver for an injected RF noise level of 23 dBm. Black lines: measurements; green lines: simulations.