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# On Integrating a Proprietary and a Commercial Architecture for Optimal BIST Performances in SoC

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# ON INTEGRATING A PROPRIETARY AND A COMMERCIAL ARCHITECTURE FOR OPTIMAL BIST PERFORMANCES IN SOCS

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## Abstract

*This paper presents the integration of a proprietary hierarchical and distributed test access mechanism called HD<sup>2</sup>BIST and a BIST insertion commercial tool. The paper briefly describes the architecture and the features of both the environments and it presents some experimental results obtained on an industrial SoC.*

## 1. The HD<sup>2</sup>BIST architecture

HD<sup>2</sup>BIST (Hierarchical-Distributed-Data BIST) is a proprietary architecture that supports the integration of embedded cores with different test requirements, as Full Scan cores, Partial Scan cores or BIST-ready cores. HD<sup>2</sup>BIST allows adding to the SoC design a high degree of reusability and flexibility in terms of:

- *Test structure*: the hardware inserted to manage the different test strategies of the embedded cores is customizable on a trade-off among routing, area, and test length;
- *Scheduling*: the HD<sup>2</sup>BIST structure allows to apply and/or activate and check the test procedures of each core of the system in any possible order, also resorting to complex scheduling control flow mechanisms as “wait” and conditional operations;
- *Test Access Protocol*: the approach defines a unified Test Access Method (TAM) to the different cores of the system, independent from their built-in test access protocols;

- *Hierarchy*: the HD<sup>2</sup>BIST is completely reusable during different phases of the product life cycle (horizontal reuse), and at different levels of integration (vertical reuse).

The main goal of the HD<sup>2</sup>BIST architecture is to maximize and simplify the reuse of the built-in test architectures, giving the chip designer the highest flexibility in planning the overall SoC test strategy. HD<sup>2</sup>BIST defines a Test Access Method (TAM) able to provide a direct “virtual” access to each core of the system. It can be conceptually considered as a powerful complement to the P1500 standard (**Error! Reference source not found.**), whose main target is to make the test interface of each core independent from the vendor.

The key idea of HD<sup>2</sup>BIST is to distribute test data to each core through a *Test Bus (TBUS)*. Each core uses the bus to gather the test data inputs and to send out the test data outputs. Each core is connected to the TBUS through an ad-hoc interface called *Test Block (TB)*.

A detailed technical description of the HD<sup>2</sup>BIST architecture can be found in [1] and in [2].

## 2. Integration of HD<sup>2</sup>BIST within a commercial BIST insertion tool environment

The aim of the proposed integration is to merge the flexibility of the HD<sup>2</sup>BIST bus-based test access mechanism with the indispensable reliability of commercial BIST insertion tool environment. The management of the BIST controllers is demanded to

HD<sup>2</sup>BIST structures, leaving the generating the proper BIST structures to the BIST insertion tool.

The integration allows exploiting the HD<sup>2</sup>BIST test access mechanism, ad-hoc defined to effectively deal with system hierarchy and reusability. The HD<sup>2</sup>BIST task is twofold: on one hand it permits the access of each BIST controller with the Test Bus (TBUS) and on the other hand, it relieves the external ATE of the BIST controllers management thanks to the scheduling capability of the Test Processors.

To perform the integration, the system to be tested is first processed for BIST controller generation. A collar and a BIST controller are generated for each core as well as a BIST controller for the glue logic. Then, a HD<sup>2</sup>BIST TB is designed for each generated BIST controller, and a HD<sup>2</sup>BIST TP is designed for each hierarchical level present into the original system. At top level, a HD<sup>2</sup>BIST TLTP is designed to make the structure accessible from outside.

### 3. The test case

A case study has been used to evaluate the integration of BIST controllers generated by a commercial tool in the HD<sup>2</sup>BIST environment and to gather experimental results. The circuit, named VC12AD, is a part of a telecommunication ASIC designed by Italtel SpA. Both Italtel SpA and Siemens ICN have already used the circuit as a benchmark for evaluating commercial BIST Insertion Tools.

The target circuit is described in VHDL and has been synthesized using the *G10 LSI Logic™ library* [3], which provides a set of SRAMs of different sizes. The VC12AD counts up to 860K Synopsys™ equivalent gates (excluding RAMs), plus 36 small-sized SRAMs, for a total of 14,704 bits.

#### 3.1. Test case after BIST insertion

The commercial tool inserted eight RAM BIST controllers plus an additional logic BIST controller to test the glue logic connecting the RAMs. The TAP controller can manage the BIST controllers and the Boundary Scan cells available on VC12AD.

The HD<sup>2</sup>BIST structure inserted in VC12AD lies on two hierarchical levels: a lower level ring to manage the BIST controllers of SYNDES modules and a top level ring to manage the other BIST controllers and the lower chain Test Processor (see Figure 1).

#### 3.2. Area and test time overhead

The area (in Synopsys equivalent gate [4]) obtained synthesizing the HD<sup>2</sup>BIST structures generated for the VC12AD. The technology library adopted is the G10 LSI Logic library.

The area overhead of the HD<sup>2</sup>BIST structure w.r.t. the VC12AD with BIST controllers is about 3%. The time overhead is negligible; it includes the configuration of the different test blocks before starting the test session, and the time to collect the test results when the test is concluded.

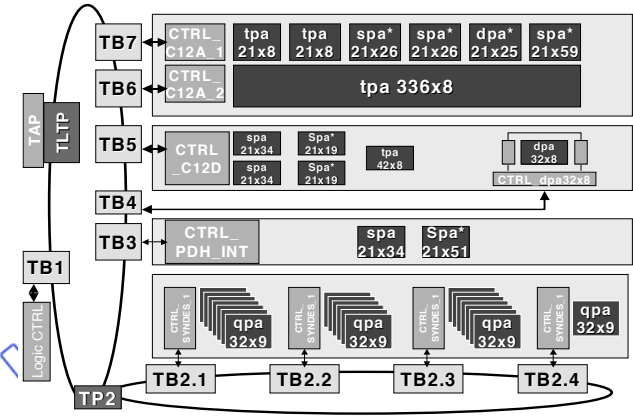


Figure 1: HD<sup>2</sup>BIST structure in VC12AD

### 4. Conclusions

This paper proposed the integration of a commercial tool with a proprietary bus-based test access mechanism called HD<sup>2</sup>BIST [BDCP00] in testing complex SoC. The commercial tool was used to generate BIST controllers for testing each core while HD<sup>2</sup>BIST to access and manage all of them. The proposed approach has been validated using as a test case an industrial design by Siemens ICN, and implemented in *LSI Logic G10* technology.

### 5. References

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