On the Substrate Thermal Optimization in SiC-Based Backside-Mounted High-Power GaN FETs

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Federica Cappelluti, *Member, IEEE*, Mauro Furno, Annamaria Angelini, *Student Member, IEEE*, Fabrizio Bonani, *Senior Member, IEEE*, Marco Pirola, *Member, IEEE*, and Giovanni Ghione, *Fellow, IEEE*

***Abstract*—This paper presents a discussion on the substrate thermal design of backside-mounted power GaN high-electron mobility transistors. After a review on the thermal properties of the relevant materials and their temperature dependences, design guidelines are proposed on the basis of 3-D thermal simulations; the results presented suggest that in SiC-based devices, substrate thinning does not typically improve the thermal resistance or the dynamic thermal behavior. Contrary to what happens in III–V GaAs- or InP-based discrete or integrated devices, therefore, microstrip design on a thinned substrate (as opposed to coplanar design on a comparatively thick substrate) is generally not thermally superior. This should make possible, from the thermal standpoint, the realization of coplanar multifunctional GaN-based monolithic microwave integrated circuits integrating, e.g., low-noise and power stages and avoiding the use of via holes.**

***Index Terms*—GaN, power modulation-doped field-effect transistors (MODFET), semiconductor device thermal factors, SiC.**

I. Introduction

THE RADIO frequency power density of AlGaN/GaN high-electron mobility transistors (HEMTs) has increased steadily during the last few years, recently reaching in field-plate devices values as large as 40 W/mm [1]. The related heat dissipation issues clearly make thermal design a key point in the successful development of power GaN FETs.

Backside mounting (BS) of GaN-based devices grown on SiC or Si substrates is probably now the most popular thermal management solution, which is applicable to both discrete (hybrid) and integrated monolithic microwave integrated circuit (MMIC) devices; in the BS case, heat dissipation mainly occurs through a two-layer medium (semiconductor substrate and metal mounting). Taking into account that the design of the thin AlGaN–GaN surface layer is dominated by electrical and other technological constraints, the degrees of freedom that are left for thermal optimization are the layout (to some extent) and the substrate-mounting structure.

The thermal optimization of the semiconductor substrate is often carried out in conventional III–V technologies (GaAs or InP based) through substrate thinning; this excludes the coplanar approach in power devices and circuits, with only microstrip circuits allowing for thin substrates without compromising the electrical performances. Moreover, the via-hole technology that is exploited for device grounding in a microstrip approach may also be made easier by substrate thinning.

For SiC-based GaN devices, however, a markedly different scenario can arise when compared to standard III–V-based devices. In fact, the minimization of the thermal resistance of the two-layer (semiconductor and mounting) medium supporting the GaN epitaxial layer is based on two contrasting strategies according to whether the top layer is a worse or better thermal conductor, respectively, than the bottom layer. In the first case (common in conventional III–V technology), the overall thermal resistance increases as a function of the top layer thickness, and in the second (often more appropriate for GaN-based devices) it may decrease (see for a more detailed discussion Section III), making substrate thinning useless or even detrimental. In such a condition, therefore, coplanar-mounted devices on thick substrate may have, in principle, better thermal performances than microstrip-mounted devices on thin substrates. Notice, moreover, that substrate thinning down to 100 μm or less can be considered at present somewhat mandatory in microstrip circuits based on SiC substrates, owing to the technological problems encountered in etching deep via holes in this material [2], [3].

Inspection of the thermal conductivity of substrate materials (sapphire, Si, 4H-SiC, and 6H-SiC) and mounting metals (Mo, W, and Cu, shown as limiting cases of representative alloys), see Fig. 1, suggests that both 4H-SiC and 6H-SiC are thermally superior to CuMo (CuW) alloys at room temperature, whereas sapphire and Si typically exhibit poorer conductivity. However, the semiconductor thermal conductivity is known to severely drop with increasing temperature, whereas the metal thermal conductivity does not; this implies that with increasing power densities, the SiC thermal conductivity will ultimately fall below the metal mounting conductivity. The same remarks apply, of course, if the heat sink temperature is raised over 300 K. For SiC-based GaN devices with a given heat sink temperature, a break-even dissipated power therefore exists, below which the SiC substrate should be made thicker (rather than thinner) to improve dissipation. Owing to the material thermal nonlinearity, such a break-even power should be identified with the help of numerical simulations.

In this paper, we provide a comparative analysis of coplanar and microstrip-like BS mountings, choosing as a case study typical X-band layouts, and derive thermal design guidelines; particular attention is devoted to the uncertainty affecting the

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The authors are with Dipartimento di Elettronica, Politecnico di Torino, 10129 Torino, Italy (e-mail: federica.cappelluti@polito.it).

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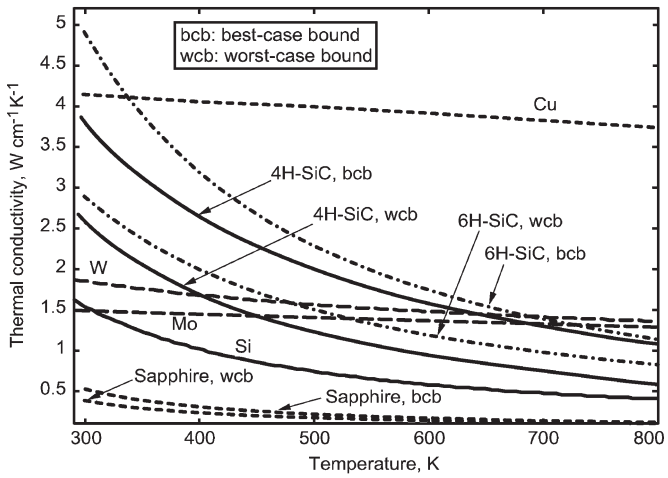

Fig. 1. Si thermal conductivity model; worst-case and best-case thermal conductivity models for 6H-SiC, 4H-SiC, and sapphire; Cu, Mo, and W thermal conductivity models are also shown. The Si conductivity model is standard [4] and shown for comparison.

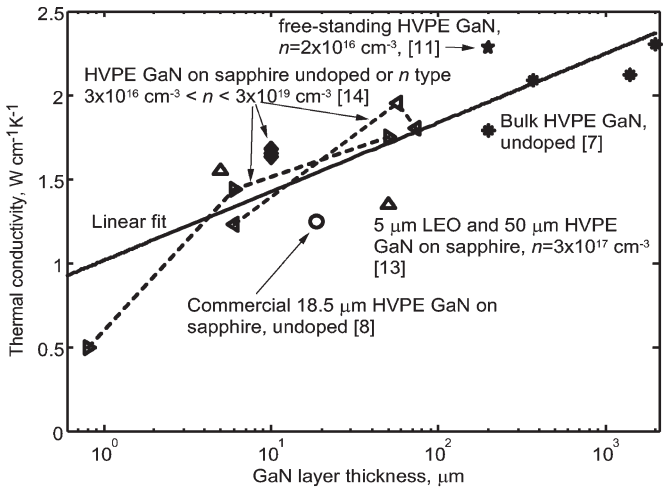

Fig. 2. Room-temperature GaN thermal conductivity as a function of layer thickness. Symbols: values from [9], [10], [13], [15], and [16]. Solid line: least square fit.

SiC thermal parameters. This paper is structured as follows: Section II presents a comprehensive review of the thermal parameters of GaN, SiC, and metal mountings, introducing best-case and worst-case conductivity models on the basis of literature data. Thermal design guidelines of backside-mounted GaN FETs are derived on the basis of 3-D simulations (continuous wave (CW) and transient) in Section III, leading to the conclusion that substrate thinning does not typically provide an improvement of thermal performances in CW or pulsed operation. Preliminary experimental data on thinned versus unthinned devices are finally discussed, whose trend appears to confirm the aforementioned remarks.

II. Thermal Models

The channel temperature and thermal resistance of BS FETs can be evaluated through a number of well-known fully or partly numerical approaches [5]. In the present discussion, the temperature dependence of the thermal conductivity plays a discriminating role; also considering the multilayered substrate, this excludes the use of linear tools coupled to the Kirchhoff transformation (only approximate in a multilayered environment, see [6]). A standard finite-element method-based 3-D code with constant injected power and temperature averaged over the injection region will be exploited in all the simulations presented to define the temperature-dependent thermal resistance.

On the other hand, the accuracy of simulation results strongly depends, as obvious, on the accuracy of thermal conductivity models. Unfortunately, available literature data on the thermal properties of GaN and SiC are affected by a large spread, probably due not only to the measurement uncertainty but also to technological and material issues. To make a meaningful choice at a modeling level, we will introduce for SiC (which turns out to be more critical from a design standpoint) a worst-case-bound (wcb) model and a best-case-bound (bcb) model. This immediately allows to provide worst-case and best-case estimates for the device thermal resistance as a function of the geometry. A review of thermal material parameters is provided in the following sections.

A. GaN Conductivity Model

The room-temperature thermal conductivity k_{GaN} of ideal GaN crystals was estimated to be as high as 4.1 W cm^{-1} K^{-1} [7], [8]; experimental data are much lower and strongly depend on crystal quality and growth method. Record reported measured conductivities are 2.3 W cm^{-1} K^{-1} for Fe-doped 2-mm-thick GaN on sapphire samples grown by hybrid vapor phase epitaxy (HVPE) [9] and 2.25 W cm^{-1} K^{-1} for undoped 200-μm free-standing GaN samples grown by HVPE [10]. Exceptionally high k_{GaN} values are also reported on lateral epitaxial overgrown (LEO) GaN/sapphire samples [11]. A number of literature works theoretically demonstrate that k_{GaN} is limited by material defects and impurities (acting as phonon scatterers), namely threading dislocations [12], unintentional residual impurities (oxygen, hydrogen, carbon, and silicon) [13], and dopants [14].

Recently reported k_{GaN} values for undoped or moderately doped samples are shown in Fig. 2 as a function of the GaN layer thickness [9], [10], [13], [15], [16]. A general trend of decreasing k_{GaN} with decreasing thickness may be observed, which is consistent with an increase in defect density [9]. However, all measured values refer to GaN samples grown on sapphire by HVPE or LEO; no data were found in the literature for films grown by MBE or conventional MOCVD, i.e., the epitaxial growth methods typically employed in GaN-based FET technology. Furthermore, the thickness of the measured samples is in the range of 5 μm to 2 mm, which is much greater than the thickness of GaN layers in GaN-based FETs (except from the lowest thickness sample in Fig. 2, whose doping concentration is, however, on the order of 3×10^{19} cm^{-3}). Least square extrapolation of the collected values (solid line in Fig. 2) leads to $k_{\mathrm{GaN}} = 1$ W cm^{-1} K^{-1} at room temperature for a 1-μm-thick GaN layer.

Concerning the temperature dependence of k_{GaN}, a T^{-1} dependence is theoretically calculated in [14] for low-defect

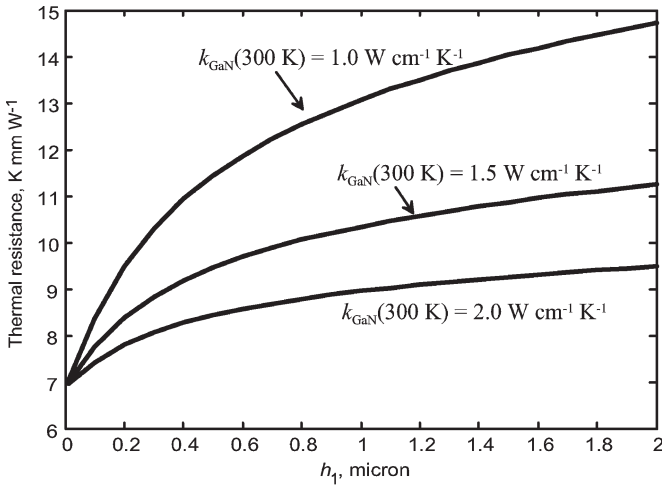

Fig. 3. Variation of 2-D thermal resistance of a two-layer GaN–SiC as a function of the GaN layer thickness; different values of the 300 K GaN thermal conductivity are assumed. The SiC thermal conductivity was assumed as in (5), and the SiC layer thickness h_2 is 300 μm.

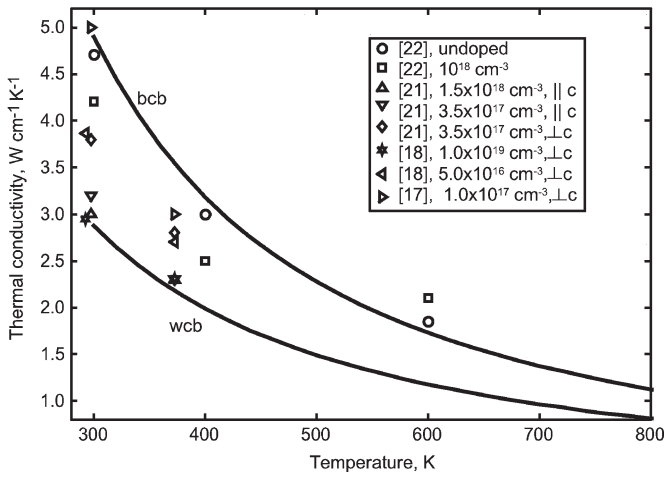

Fig. 4. Temperature dependence of the thermal conductivity of n-doped 6H-SiC. Comparison of experimental thermal conductivity data and wcb and bcb models for 6H-SiC. Experimental data are from [19], [20], [23], and [24].

density samples (whose behavior is dominated by Umklapp scattering); high-quality free-standing samples follow this law (see [10], for example). For samples with higher density of point defects and dislocations, the thermal conductivity is calculated to approach $T^{-0.5}$ [14]. In [17], a $\propto T^{-0.67}$ dependence is extracted from data measured on a commercial 18.5-μm HVPE-grown GaN/sapphire sample. For comparison, it is worth noticing that polycrystalline GaN samples in [18] exhibit $T^{-0.26}$ and $T^{-0.46}$ dependences. In the following discussion, we will assume an approximate $T^{-0.5}$ dependence for 1-μm-thick conventionally grown GaN layers; the resulting conductivity model will therefore be

$$k_{\mathrm{GaN}}(T) = 1.0 \times \left(\frac{T}{300}\right)^{-0.5} \ \mathrm{W\ cm^{-1}\ K^{-1}}. \qquad (1)$$

Thin (micrometer order of magnitude) surface GaN layers are often neglected in large-scale thermal simulations.[1] Their impact on the total thermal resistance is, however, far from being negligible (see the results in Fig. 3), where the per-unit-length thermal resistance of a 0.6-μm heat source located on a two-layer GaN on 6H-SiC substrate, backside mounted on the heat sink, is shown for different values of the GaN conductivity. The GaN thickness is h_1, the SiC thickness is $h_2 = 300$ μm, and the SiC conductivity is from (5). Already for $h_1 = 1$ μm, neglecting the GaN layer severely underestimates the thermal resistance. However, owing to the reduced GaN layer thickness and proximity to the heat source, we can assume that its conductivity, while influencing the absolute value of the overall thermal resistance, does not affect other geometry and material trends, which are the object of the following discussion. In the rest of this paper, the model in (1) will be assumed as an approximation.

[1]These also include a GaN–AlGaN heterostructure and a very thin AlGaN layer that we neglect in the analysis despite its inferior thermal properties versus GaN—see [17]—also because the heat source is approximately located at the GaN–AlGaN interface.

B. 6H-SiC and 4H-SiC Thermal Conductivity Models

Silicon carbide (6H and 4H polytypes are considered here) exhibits exceptionally high 300 K thermal conductivity ($3-5$ W cm^{-1} K^{-1}), which is comparable or superior to many metals. Measurements of the 6H-SiC thermal conductivity are reported in [19] and [20] and, more recently, in [21]–[23] (CREE Research, Inc.) and [24], pointing out a strong decrease of the conductivity with temperature, as well as with increasing doping impurity concentration; anisotropy effects amounting to a 10% increase in thermal conductivity perpendicular to the c-direction are also observed on CREE samples at room temperature. The temperature dependence of the thermal conductivity was compared with theoretical models in [25] and [26]; in fact, whereas room-temperature conductivity is similar in SiC and many metals, SiC heat transport is dominated by phonons, not by electrons as in metals, thus leading to a far stronger decrease with temperature. The main scattering processes responsible for the diminution of 6H-SiC thermal conductivity at high temperatures should be a combination of four-phonon and Umklapp processes, yielding a theoretical dependence of the form $T^{-\beta}$, with $1 < \beta < 2$.

Various models for the temperature behavior of 6H-SiC have been proposed in the literature [21], [25], [27]–[29]; due to the spread of available experimental data, we introduce equivalent isotropic wcb and bcb models for the 6H-SiC $k_{\mathrm{SiC}}(T)$ to be exploited in simulations. The model from Müller *et al.* [21] is used as wcb, i.e.,

$$k_{\mathrm{6H\text{-}SiC,wcb}}(T) = 4.517 \times 10^3 \times T^{-1.29} \ \mathrm{W\ cm^{-1}\ K^{-1}}. \quad (2)$$

The bcb model is taken from [29] and reads as follows:

$$k_{\mathrm{6H\text{-}SiC,bcb}}(T) = 4.9 \times \left(\frac{T}{300}\right)^{-1.5} \ \mathrm{W\ cm^{-1}\ K^{-1}}. \qquad (3)$$

The models are compared with the experimental data in Fig. 4.

Concerning 4H-SiC, the only currently available experimental data from [22] and [23] (CREE Research, Inc.) are depicted

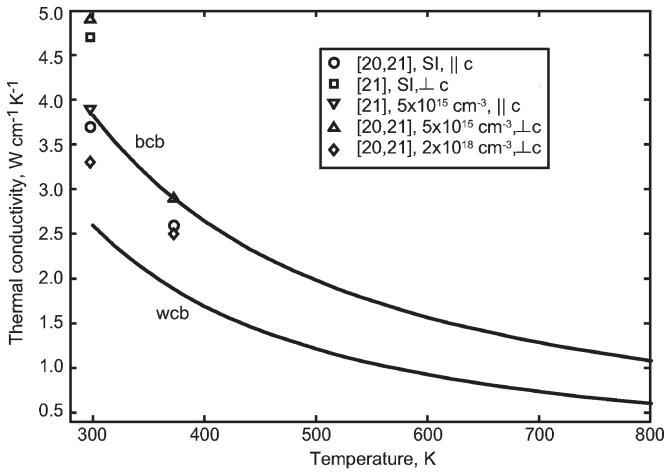

Fig. 5. Temperature dependence of the thermal conductivity of SI and n-doped 4H-SiC and wcb and bcb models for 4H-SiC. Experimental data are from [22] and [23].

in Fig. 5. The reported values are slightly lower than those for 6H-SiC, but the same strong decrease of the thermal conductivity with increasing temperature and doping concentration can be observed. The conductivity of semi-insulating (SI) substrates lies between high and low doping values, probably due to the high degree of compensation from vanadium impurities (in the 10^{17}–10^{18} cm^{-3} range) [30] that is necessary to ensure SI properties to SiC substrates. The thermal conductivity of 4H-SiC is also experimentally determined to be about 20% lower for heat conduction along the c-axis with respect to the perpendicular plane.

The collected approximated thermal conductivity models are depicted in Fig. 5. By comparing them with experimental data, it seems that all the published models are referred to heat conduction along the c-axis direction. For the purpose of electrothermal simulations, wcb and bcb isotropic models are proposed, as in the case of 6H-SiC. The wcb thermal conductivity model chosen for 4H-SiC is as follows [31]:

$$k_{4\mathrm{H-SiC,wcb}}(T) = 2.6 \times \left(\frac{T}{300}\right)^{-1.49} \ \mathrm{W\ cm^{-1}\ K^{-1}}. \quad (4)$$

The bcb model was taken from [32]

$$k_{4\mathrm{H-SiC,bcb}}(T) = 3.95 \times \left(\frac{T}{293}\right)^{-1.29} \ \mathrm{W\ cm^{-1}\ K^{-1}}. \quad (5)$$

Indirect estimates of the SiC conductivity were finally attempted in the literature through comparison between thermal data derived from the simulation of GaN FETs and thermal resistance or temperature measurements. For instance, in [33], a best fit value of 4.08 W cm^{-1} K^{-1} was obtained, which is similar to the one derived by the present authors through comparison with photocurrent-based measurements by Regoliosi *et al.* [34] (see [35] and [36]). Owing to the combined uncertainities of modeling and measurements on complex structures (where additional contact and package thermal resistances, which are difficult to estimate, also are present), such an approach is useful to obtain simulations that are consistent with measurements for a given technology, with some predictive capability in terms of optimization, but can hardly be assumed to provide reference data also because the parameter uncertainty is likely to be (at least in part) technology dependent.

C. Mounting Metal Conductivity Models

Models for the temperature dependence of copper (Cu) [37], molybdenum (Mo) [38], and tungsten (W) [37] thermal conductivities were also developed from the given references. Thus

$$k_{\mathrm{Cu}}(T) = 4.13 - 5.17 \times 10^{-4} T \ \mathrm{W\ cm^{-1}\ K^{-1}} \quad (6)$$

$$k_{\mathrm{Mo}}(T) = 1.5 - 4.24 \times 10^{-4} T \ \mathrm{W\ cm^{-1}\ K^{-1}} \quad (7)$$

$$k_{\mathrm{W}}(T) = 1.29 \times \left(\frac{T}{300}\right)^{-0.5} + 0.49 \ \mathrm{W\ cm^{-1}\ K^{-1}}. \quad (8)$$

The conductivity variation is found to be almost negligible on a wide temperature range. CuMo and CuW were selected as cases of representative compound metal heat sinks, although other materials are available. In what follows, CuMo and CuW compounds will be characterized by a temperature-independent conductivity.

D. Comparison

Conductivity models for 6H-SiC, 4H-SiC, Cu, Mo, and W are plotted together in Fig. 1, where, for completeness, the sapphire and Si data are also shown; for sapphire, bcb and wcb models were extracted on the basis of the data in [39] and [40], with room-temperature thermal conductivities ranging from 0.35 (wcb) to 0.52 (bcb) W cm^{-1} K^{-1}; $(T - T_r)^{-1}$ (T_r = 159 K) temperature dependences were exploited (see also [35]). We clearly notice that the metal thermal conductivity is almost T independent; k_{Cu} is almost always larger than k_{SiC} for any possible model, whereas the 6H-SiC and 4H-SiC conductivities are larger than for Mo and W (and similarly for CuMo and CuW alloys) at room temperature and for a significantly wide temperature range extending above 400 K. However, increasing the heat dissipation, and therefore the channel temperature, will ultimately degrade the SiC conductivity to values below the mounting metal conductivity.

III. Thermal Design Guidelines of Backside-Mounted GaN FETs

Optimum die-level thermal design of backside-mounted conventional compound semiconductor (GaAs or InP) hybrid or MMIC FETs is based, as already recalled, on well-known recipes, such as substrate thinning and increasing the gate-to-gate spacing. Increasing the gate width improves the thermal resistance R_{th} only if the power density is correspondingly decreased, but in what follows, we will consider design at constant dissipated power density. It should be considered, however, that the layout degrees of freedom are indeed reduced for a given frequency range since the total (side to side) device width in a multifinger layout has to be small with respect to the operating wavelength and the gate width should be less than 100 μm in the X-band (for a discussion, see, e.g., [41, p. 23]). In X-band

applications, typical gate-to-gate spacings are on the order of 50 μm. Therefore, only substrate engineering remains as a tool to control $R_{\rm th}$; in GaAs and InP technologies, decreasing the substrate thickness also leads to excluding the coplanar solution for power circuits, owing to the resulting parasitic coupling with a closely spaced lower conducting plane. Conversely, the microstrip solution with the related via-hole technology is compatible with substrate thinning.

To have some insight on how this scenario changes when SiC is exploited as a substrate, let us first consider some typical $R_{\rm th}$ trends when varying the thickness of the semiconductor substrate layer that is placed on a metal mounting connected in turn to the heat sink. As a case study, we consider a three-layer structure with a top GaN 1.2-μm layer grown on top of a 4H-SiC layer of thickness varying between 50 and 400 μm and glued (zero interface resistance assumed) to a 1-mm-thick metal dissipator. For the 4H-SiC conductivity, the bcb model was selected, also corresponding to an average value for 6H-SiC. We consider the resistance of a 3-D system made of a periodic arrangement of gate strips (spacing of 50 or 400 μm) with constant heat source of width $W = 1$ μm and length $W = 100$ μm, normalized over 1-mm total gate periphery. The largest finger spacing approximately corresponds to thermally decoupled fingers. Furthermore, as a metal dissipator, we exploit Cu (as a bcb) and the alloy $Cu_{15}Mo_{85}$ with a conductivity of 1.79 W cm^{-1} K^{-1}. The metal conductivity is assumed as constant with temperature, whereas the semiconductor conductivity decreases with temperature according to (5).

In general, the thermal resistance of a 3-D planar, finite-size uniform heat source on a uniform layer, backside mounted on the heat sink, increases as a function of the layer thickness, asymptotically saturating for infinite thickness to a value $R_{\rm th} \approx 1/k\sqrt{2\pi A}$, where k is the layer conductivity and A is the heat source area (see [42] and references therein). For a two-layer medium (representative, e.g., of the SiC layer and metal mounting), relevant behaviors can be derived, e.g., by exploiting the closed-form approximations presented in [42] for a 3-D analog electrostatic problem. It is found that if the conductance k_1 of the upper layer (closer to the heat source, thickness h_1) is smaller than the conductance k_2 of the bottom layer of thickness h_2, the total thermal resistance $R_{\rm th}$ increases (as it could be expected) with h_1. This behavior is confirmed in Fig. 6, which shows the thermal resistance for a 4H-SiC device on Cu as a function of the SiC layer thickness and for different power levels. Since Cu is a better conductor than SiC already at ambient temperature (let alone at higher temperature), the only way to reduce the thermal resistance in this case is substrate thinning.

On the other hand, when $k_1 > k_2$, $R_{\rm th}$ decreases versus h_1 for small h_1; for $h_1 \to \infty$, $R_{\rm th}$ ultimately saturates with negative or positive slope (according to the parameter values); in the latter case, $R_{\rm th}$ exhibits a minimum versus h_1. In practice, already for moderate values of $k_1/k_2 > 1$, we observe that $R_{\rm th}$ exhibits a substantially constant (initially slowly decreasing) behavior with increasing h_1 on the whole range corresponding to realistic h_1 values. According to physical interpretation, the decreasing behavior corresponds to the better heat spreading allowed for by the top layer, which decreases the thermal resistance of the bottom layer, thus compensating for the increase of the top layer resistance. This is indeed the case for a GaN FET on 4H-SiC with a $Cu_{15}Mo_{85}$ metal dissipator, whose conductivity at 300 K is worse than the 4H-SiC conductivity. Figs. 7 and 8 show the thermal resistance as a function of the substrate thickness for different values of the dissipated power per millimeter and for two heat sink temperatures (27 °C = 300 K and 80 °C). Due to the nonlinear behavior of SiC, we see that for dissipated powers up to about 20 W/mm (15 W/mm) for heat sink temperature of 27 °C (80 °C), the thermal resistance slowly decreases or is substantially constant as a function of SiC thickness. For larger dissipated power, the behavior is reversed due to the deterioration of 4H-SiC conductivity with increasing temperature; however, this occurs at average dissipated powers leading to junction temperatures far beyond the acceptable range.

In Figs. 9 and 10, the computation is repeated for a larger gate-to-gate spacing. Increasing the gate spacing up to the

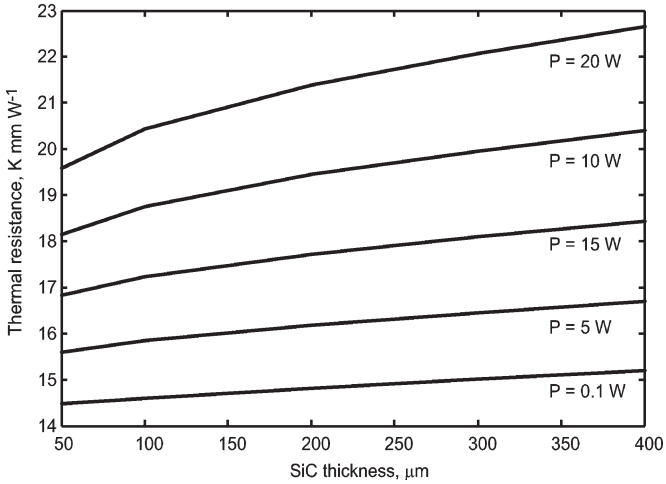

Fig. 6. Thermal resistance of 4H-SiC-grown GaN FET as a function of the SiC layer thickness for a heat sink temperature of 27 °C and different dissipated powers (from 0 to 20 W/mm). The 1-mm-thick heat sink is Cu. The gate spacing is 50 μm.

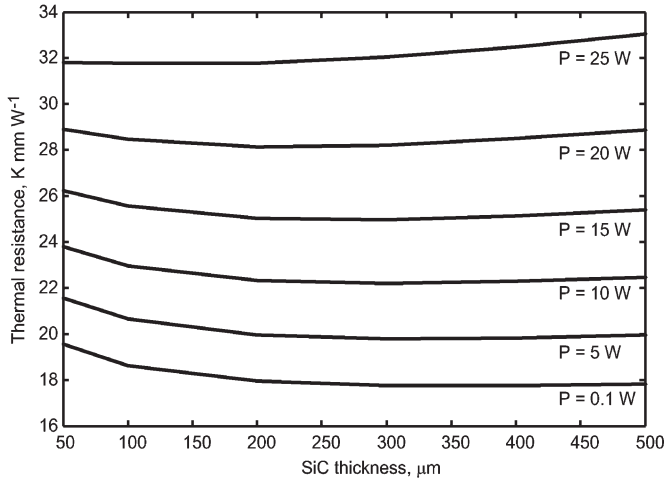

Fig. 7. Thermal resistance of 4H-SiC-grown GaN FET as a function of the SiC layer thickness for a heat sink temperature of 27 °C and different dissipated powers (from 0 to 25 W/mm). The 1-mm-thick heat sink is $Cu_{15}Mo_{85}$. The gate spacing is 50 μm.

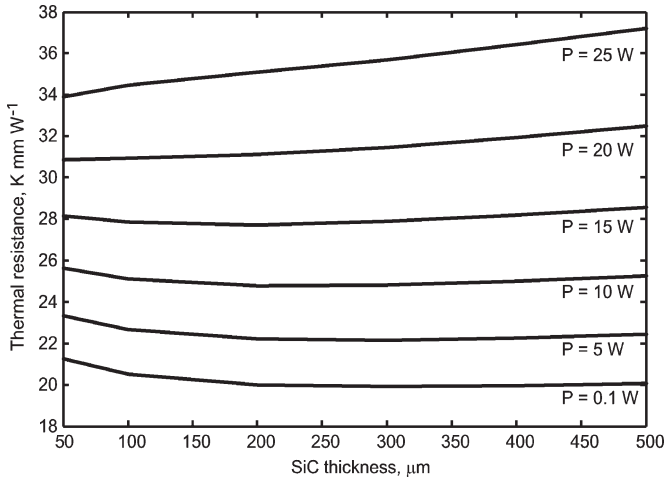

Fig. 8. Thermal resistance of 4H-SiC-grown GaN FET as a function of the SiC layer thickness for a heat sink temperature of 80 °C and different dissipated powers (from 0 to 25 W/mm). The 1-mm-thick heat sink is $Cu_{15}Mo_{85}$. The gate spacing is 50 μm.

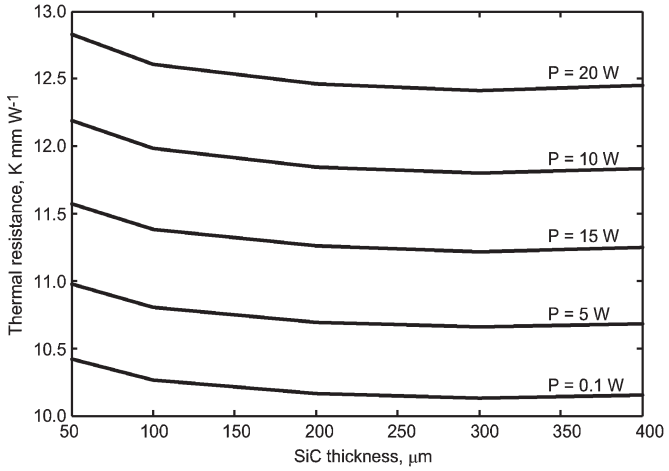

Fig. 9. Thermal resistance of 4H-SiC-grown GaN FET as a function of the SiC layer thickness for a heat sink temperature of 27 °C and different dissipated powers (from 0 to 20 W/mm). The 1-mm-thick heat sink is $Cu_{15}Mo_{85}$. The gate spacing is 400 μm.

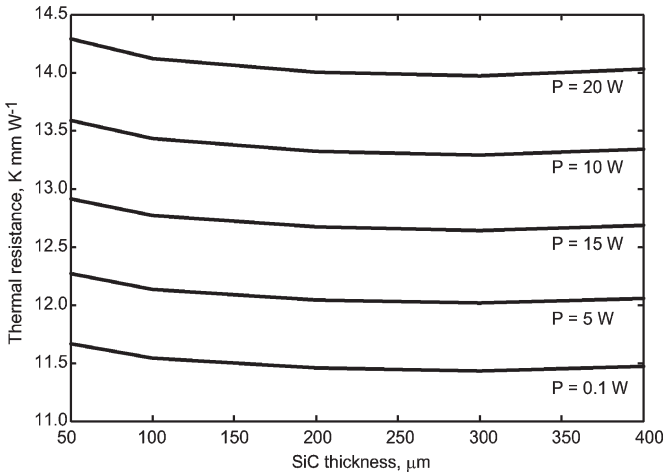

Fig. 10. Thermal resistance of 4H-SiC-grown GaN FET as a function of the SiC layer thickness for a heat sink temperature of 80 °C and different dissipated powers (from 0 to 20 W/mm). The 1-mm-thick heat sink is $Cu_{15}Mo_{85}$. The gate spacing is 400 μm.

substrate thickness (or, as a rule of thumb, up to two times the substrate thickness to allow for full lateral heat spreading) changes the heat conduction pattern into full 3-D, thus significantly decreasing the thermal resistance and the effect of substrate thickness increase. Notice that the $R_{\rm th}$ behavior is now always slowly decreasing; furthermore, the improvement in $R_{\rm th}$ obtained by a larger gate-to-gate spacing is far more impressive than the one due to substrate thickness variation.

We can therefore conclude that if the substrate conductivity is worse or marginally better at room temperature than the mounting metal conductivity, the thermal resistance is improved by thinning (as in sapphire or Si-based device on most mountings or as in SiC-based device on Cu or even better—e.g., diamond—mountings). However, the situation is more complex for SiC-based devices on CuMo or CuW mounting alloys. In this case, for a given heat sink temperature, the thermal resistance somewhat improves by increasing the SiC thickness up to a certain dissipated power, which decreases with increasing heat sink temperature. For realistic dissipated power values, increasing the SiC substrate thickness leads to an (albeit small) decrease of the thermal resistance for most typical mounting metals. Substrate thinning, therefore, does not typically allow for better thermal management, and, as a consequence, microstrip mounting turns out to be less effective than coplanar mounting from a thermal standpoint.

Such conclusions are further supported by a full 3-D case study in which a ten-finger GaN HEMT based on SELEX-SI technology is considered. The device includes a GaN epilayer of 1.2 μm on top of a 4H-SiC substrate with or without substrate thinning (or, in other words, with microstrip or coplanar mounting). The gate width is 100 μm, and the gate-to-gate spacing is 50 μm; the mounting alloy is $Cu_{20}W_{80}$ with a conductivity of 2.22 W cm^{-1} K^{-1}, and the mounting (package bottom layer) thickness is 381 μm. The SiC substrate is glued to the mounting through a layer of silver-filled epoxy resin (EPO-TEX H20E) with a thickness of 70 μm [44] and a conductivity of 0.29 W cm^{-1} K^{-1} [45]. We analyze two structures.

1) The 400-μm 4H-SiC substrate is backside mounted to the CuW mounting on an ideal heat sink (coplanar mounting).
2) The substrate is thinned down to $h_{\rm SiC} = 70$ μm and backside mounted to the CuW mounting on an ideal heat sink (microstrip mounting).

For each structure, we evaluate the average temperature of the central (hottest) fingers through the bcb and wcb approaches for dissipated power densities up to 20 W/mm. The thermal resistances are shown in Fig. 11; for the bcb model, the heat sink is kept at $T_0 = 27$ °C or 80 °C, whereas for the wcb model, only $T_0 = 27$ °C is considered.

From the aforementioned results, we conclude that the unthinned substrate (coplanar) mounting is thermally superior to the thinned substrate (microstrip) mounting for the bcb 4H case (also corresponding to an average for 6H, as already remarked) for heat sink temperatures up to 80 °C. In all cases, the microstrip mounting shows an increase of thermal resistance of about 20%, which is larger than what is expected from the results presented in Figs. 7 and 8. From a physical viewpoint,

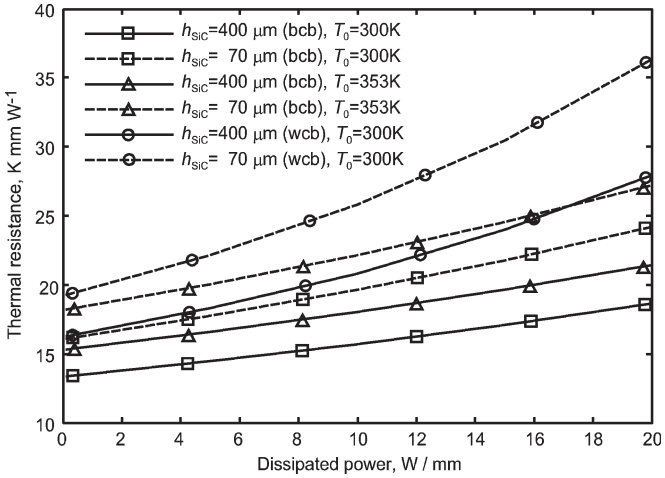

Fig. 11. Thermal resistance for several GaN FET on 4H-SiC BS coplanar or microstrip-like mountings and k models as a function of dissipated power. The 381-μm-thick heat sink is $Cu_{20}W_{80}$.

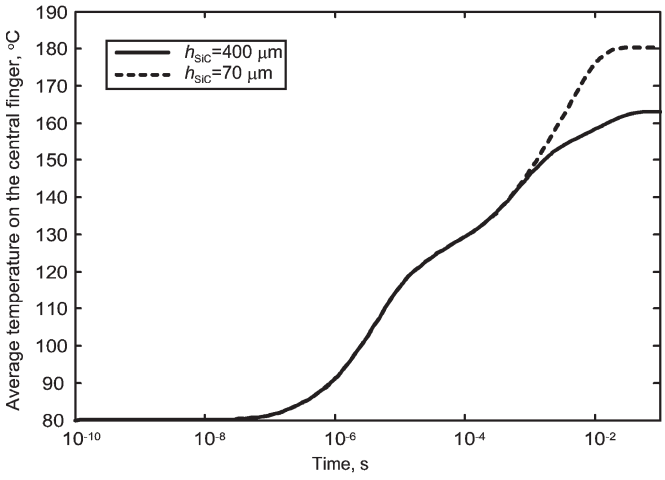

Fig. 12. Maximum temperature step response to a dissipated power step of 5 W: coplanar mounting (continuous line) and microstrip mounting (dashed line). A 4H-SiC bcb substrate is assumed with $T_0 = 80\,^{\circ}$C. The 381-μm-thick heat sink is $Cu_{20}W_{80}$.

such degradation is due to the presence of the epoxy resin whose thermal conductivity is almost one order of magnitude lower than the mounting conductivity, thus enhancing the effectiveness of heat spreading through the SiC layer. Similar conclusions may be drawn also for the wcb 4H case.

Finally, we have simulated the transient behavior of thinned versus unthinned substrates (see Fig. 12). The exploited T-independent specific heat values were 690, 490, 181, and 211 J kg^{-1} K^{-1} for SiC [27], [28], GaN [43] CuW [37], and EPO-TEX H20E [46], respectively. The maximum channel temperatures in the two cases are almost equal in the fast transient, whereas in the slow transient, the thinned substrate exhibits, as it could be expected, a slightly faster response; differences are, however, below 10%. It can be concluded that substrate thinning does not substantially alter or improve the dynamic thermal response, which implies that no advantages arise with microstrip mounting not only in CW but also in pulsed operation.

Such remarks are confirmed by experimental data on thinned versus unthinned devices (the device layout and structure is similar to the one analyzed in this paper; see Fig. 11): On-wafer pulsed current–voltage characterization carried out on the same SELEX-SI device before and after substrate thinning shows a significant increase of self-heating effect in thinned devices [47].

Moreover, a preliminary characterization of packaged SELEX-SI devices through the photocurrent method described in [36] yields thermal resistance values on the order of 10 °C/W for unthinned devices, whereas thinned devices exhibit significantly higher values (14.3, 17.1, and 26 °C/W according to slightly different layout choices; an averaged value is exploited over the device area) [48]; such results can be compared with simulated data, allowing a thermal resistance spread from 13 °C/W (unthinned substrate, bcb model) to 20 °C/W (thinned substrate, wcb model). It can be concluded that while the agreement between measured and simulated data can be probably improved, the experimental evidence seems to confirm that substrate thinning does not lead to any improvement in the thermal behavior of packaged devices.

IV. Conclusion

The thermal behavior of backside-mounted power GaN on SiC HEMTs is discussed when varying the SiC substrate thickness. After a review of the thermal properties of the relevant materials, a comparison is carried out between devices on thinned substrates (microstrip mounting) and unthinned substrates (coplanar mounting) exploiting 3-D thermal simulations. As a conclusion, it is found that coplanar mounting is at least thermally equivalent (and probably superior for high-quality 4H- or 6H-SiC substrates) both in CW and in pulsed operation to microstrip mounting for realistic power levels and channel temperatures. Preliminary experimental data appear to confirm the aforementioned trends.

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Federica Cappelluti (S'02–M'03) was born in Ortona, Italy, in 1973. She received the Laurea degree in electronic engineering and the Ph.D. degree in electronic and communications engineering from Politecnico di Torino, Torino, Italy, in 1998 and 2002, respectively.

She is currently a Research Assistant in the Dipartimento di Elettronica, Politecnico di Torino. Her main research interests concern the system-level and physics-based modeling and simulation of microwave and optoelectronic devices.

Mauro Furno was born in Ivrea, Italy, in 1977. He received the Laurea degree (*cum laude*) in materials engineering from Politecnico di Torino, Torino, Italy, the Diplôme d'Ingénieur from the Institut National Polytechnique de Grenoble, Grenoble, France, in 2002, and the Ph.D. degree in electronic devices from Politecnico di Torino, in 2007.

He is currently a Postdoctoral Fellow in the Dipartimento di Elettronica, Politecnico di Torino. His research interests concern the physics-based simulation of wide-bandgap power and microwave devices. He is also involved in the modeling of the physical and electronic properties of advanced semiconductor materials.

Annamaria Angelini (S'05) was born in Casale Monferrato, Italy, in 1975. She received the electronic engineering degree from Politecnico di Torino, Torino, Italy, in 2004. She is currently working toward the Ph.D. degree at the Dipartimento di Elettronica, Politecnico di Torino.

Her research interests concern the modeling and measurement of high-power devices. She is also involved in research on power microwave devices and circuits, with an emphasis on electrothermal modeling issues.

Fabrizio Bonani (S'89–M'91–SM'02) was born in Torino, Italy, in 1967. He received the Laurea degree (*cum laude*) and the Ph.D. degree in electronic engineering from Politecnico di Torino, Torino, in 1992 and 1996, respectively.

From October 1994 to June 1995, he was with the ULSI Technology Research Department, Bell Laboratories, Murray Hill, NJ, as a consultant, where he worked on physics-based noise modeling of electron devices. Since 1995, he has been with the Dipartimento di Elettronica, Politecnico di Torino, first as a Researcher and, since 2001, as an Associate Professor of electronics. His research interests are mainly devoted to the physics-based simulation of semiconductor devices, with special emphasis on the noise analysis of microwave field-effect and bipolar transistors, and to the thermal analysis of power microwave circuits. Part of his research concerns the analysis and simulation of nonlinear dynamical systems.

Marco Pirola (M'97) was born in Velezzo Lomellina, Italy, in 1963. He received the Laurea degree in electronic engineering and the Ph.D. degree from Politecnico di Torino, Torino, Italy, in 1987 and 1992, respectively.

In 1992 and 1994, he was a Visiting Researcher in the Microwave Technology Division, Hewlett Packard, Santa Rosa, CA. Since 1992, he has been with the Dipartimento di Elettronica, Politecnico di Torino, first as Researcher and, since 2000, as an Associate Professor, where his research concerns the simulation, modeling, and measurements of microwave devices and systems.

Giovanni Ghione (M'87–SM'94–F'07) was born in Alessandria, Italy, in 1956. He received the electronic engineering degree (cum laude) from Politecnico di Torino, Torino, Italy, in 1981.

In 1990, he joined the University of Catania, Catania, Italy, as a Full Professor of electronics, and since 1991, he has covered the same position again in the II Faculty of Engineering, Politecnico di Torino. His current research interests concern the physics-based simulation of active microwave and optoelectronic devices, with particular attention to noise modeling, thermal modeling, and active device optimization. His research interests also include several topics in computational electromagnetics, including coplanar component analysis.

Prof. Ghione is a member of the Associazione Elettrotecnica Italiana. He is also a member of the Editorial Board of the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES.