# An effective AMS Top-Down Methodology Applied to the Design of a Mixed-Signal UWB System-on-Chip

# An effective AMS Top-Down Methodology Applied to the Design of a Mixed-Signal UWB System-on-Chip

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## Abstract

*The design of Ultra Wideband (UWB) mixed-signal SoC for localization applications in wireless personal area networks is currently investigated by several researchers. The complexity of the design claims for effective top-down methodologies. We propose a layered approach based on VHDL-AMS for the first design stages and on an intelligent use of a circuit-level simulator for the transistor-level phase. We apply the latter just to one block at a time and wrap it within the system-level VHDL-AMS description. This method allows to capture the impact of circuit-level design choices and non-idealities on system performance. To demonstrate the effectiveness of the methodology we show how the refinement of the design affects specific UWB system parameters such as bit-error rate and localization estimations.*

## 1. Introduction

Ultra-Wideband (UWB) impulse-based communication received recent attention since the Federal Communications Commission released the spectrum between 3.1 and 10.6 GHz for unlicensed use in 2002. Sub-nanosecond base-band UWB pulses can be directly sent to a wideband antenna without carrier modulation. Among the others, perhaps the most attractive feature of UWB is the locationing capability, enabled by the possibility of isolating the first echo of the signal received through a multipath channel. The large bandwidth, and the corresponding short time duration, is the key for such accurate time-domain resolution, which translates into an accurate distance measurement [3]. Providing UWB transceivers with locationing capabilities may open the way to a number of applications within the WPAN field (e.g. package tracking, search-and-rescue functions). An IEEE standardization task group is currently working toward an alternative physical layer of the 802.15.4 standard with the aim of enabling high precision localization (on the order of 1 meter) [4]. The final goal is the complete integration of UWB transceivers with locationing functions in the same System-on-Chip (SoC), possibly using a standard CMOS technology. This paper thus deals with the design, modeling and simulation of UWB Mixed-Signal Systems-on-Chip (SoC).

Recent papers discuss UWB design topics [7][10][9][11], however none of them focus on the interaction between system-level issues and circuit-level design and on the importance of using a uniform methodology. With the aim of closing this gap, we proposed the use of VHDL-AMS as a common description language used at both levels [1][2]. While not new as an approach to the description of telecom SoC [8][5], we applied it for the first time in the UWB context.

However, once we pass from modelization to CMOS transistor-level design, VHDL-AMS is no more sufficient, and using Spice-like netlists and complex MOSFET models becomes mandatory. The risk when dealing with such fine-grain details is that of losing the system-level view and the impact that specific choices taken at this lower level may have on it. In this work we focused then on a methodology which permits the evaluation of the effect on system-level parameters, like bit-error rate (BER) or localization accuracy, of MOS-level design choices of relevant blocks of a UWB device based on the "energy detection" principle. We first summarize in section 2 the architecture of a UWB transceiver to which the simulation and design methodology, described next in section 3, has been applied. Section 4 presents the design of a relevant block in a CMOS technology. Then we show in section 5 how system-level parameters are affected by design choices and second-order effects by comparing pure VHDL-AMS results with mixed VHDL-AMS and Spice simulations. Finally section 6 summarizes the paper achievements and indicates future works in this field.

## 2. UWB receiver architecture

The architecture of the transceiver based on energy detection of a 2-PPM modulated train of UWB pulses is de-

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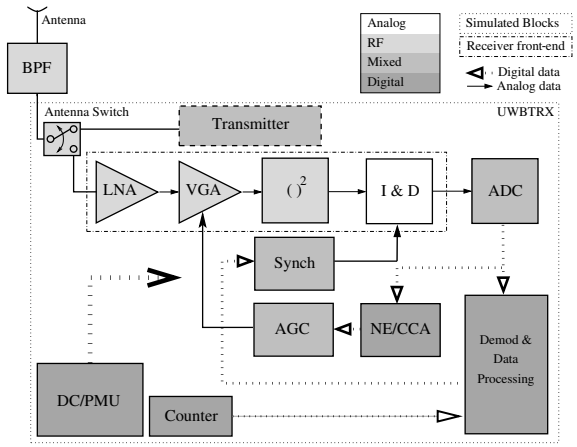


**Figure 1. Architecture of the UWB transceiver. Gray shading is used to distinguish between analog, RF, mixed-signal and digital blocks.**

scribed by the block diagram in figure 1. The chosen modulation scheme and the energy detection approach, also in accordance with the IEEE standardization task group, seem very appropriate for low data-rate WPAN localization applications [4]. The details of the operation of each block in figure can be found in [2]. Here we summarize the behavior of the relevant ones for the scope of this paper. In a 2-PPM modulated signal the symbol repetition period $T_s$ is divided in two slots of duration $T_s/2$. In case of a transmission of a '0', the UWB pulse appears in slot $[0, T_s/2]$, in case of a '1', the pulse lays in $[T_s/2, T_s]$. The demodulation of the received signal through energy detection consists in evaluating the energy in the first and in the second half of $T_s$ and deciding which one is larger. The energy is calculated by squaring the signal, $()^2$ in figure, and by "integrating and dumping" (I&D) the squared value two times in each symbol period. The integrated values are converted in a digital format by an ADC and compared using a digital circuitry. The front-end is a low-noise amplifier, LNA, followed by a variable gain amplifier, VGA, which plays a crucial role because its duty is to adapt the signal gain in such a way that the input dynamics of the ADC is fully exploited. Its gain is controlled in steps using a DA converter within the *Automatic Gain Control* (AGC) block. The I&D timing is given by the *Synchronizer* which locks on the received signal clock helped by a proper non-modulated preamble sequence (i.e. all UWB pulses located in the same slot) which precedes the modulated data. There is a very first phase before synchronization which consists in sampling the channel energy from time to time in order to evaluate whether a preamble is being transmitted. This phase is split into two subphases, *noise estimation* and *preamble sense* (NE/PS).

The transmitter branch contains a pulse generator and a modulator which formats transmitted data according to a packet structure made of a non-modulated sequence of pulses, i.e. the preamble, followed by the modulated data, i.e. the payload.

The counter block is used for the so called *Two-Way Ranging* operation discussed in section 5.

As clear from the figure, which highlights by a gray shading coloring the digital, analog, mixed-signal and radio-frequency blocks, and from the discussion above, the UWB transceiver is clearly a complex Mixed-Signal SoC which requires a proper description, simulation and design methodology. Depending on the accuracy required by these processes, VHDL for the digital parts, VHDL-AMS for the analog and RF parts and Spice-like netlists will be required, as clarified in the following section. In particular, the possibility to co-simulate all blocks within a single environment, even in the presence of differently described components, e.g. VHDL and Spice, is of momentous importance when the SoC designer needs to evaluate their reciprocal impact.

## 3. Design methodology

The VHDL-AMS language, a superset of VHDL, has been conceived for modeling analog and mixed-signal circuits, as it supports the use of digital constructs together with electrical quantities and differential equations. Furthermore, it allows the hardware description with different levels of abstraction, then making viable a top-down design methodology in which a preliminary behavioral description of the blocks allows a coarse functionality test of the system, while a progressive refinement defines the real circuit performance. This aspect is further enhanced as current commercial tools, like ADMS by Mentor Graphics, allow to co-simulate VHDL and VHDL-AMS constructs together with Spice-like netlists (ELDO) within a unique environment [12]. Such a flexibility allows the designer to transfer system constraints on circuit level parameters, and to evaluate the impact of circuit non-idealities reflected on the system performance. We think that these characteristics are markedly significant when designing complex telecommunications SoC, especially considering that traditional design and simulation methods deceive these objectives: In fact, on the one hand, coarse system level descriptions are unsuited to assure the accuracy needed for the design of analog and mixed-signal circuits, on the other hand, using transistor-level simulations for the evaluation of performance of an entire system is impractical because of the unacceptably long simulation time.

We exploit the possibility to hierarchically describe an architecture adopting a top-down methodology organized in four steps as shown in figure 2.

**Phase I.** In this phase, described in [1], the structure of the UWB transceiver was behaviorally modeled, the system

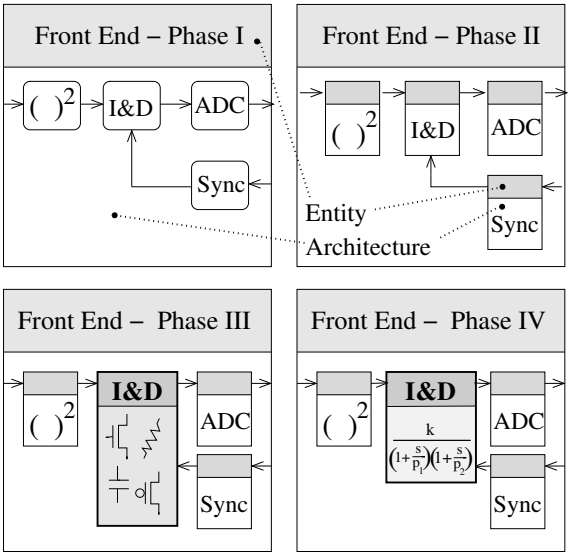


**Figure 2. Design flow phases using VHDL-AMS, ADMS and Eldo.**

level functionalities were tested, and the coherence with another high level description language (Matlab) was checked. In particular, the bit-error rate (BER) were evaluated varying the signal-to-noise ratio (SNR) at the receiver input. At this stage, the level of abstraction is similar to Matlab: The analog input is squared, the integration is performed using a behavioral "integrate and dump" process, activated by a control signal forced by an ideal synchronizer. Then, the integrated analog signal is converted to a digital signal by an ideal ADC. Figure 2, *Phase I*, shows a unique entity and architecture which includes all the behavioral equations used for modeling the analog and RF units. Using this description, detailed in [1], we obtained BER curves which perfectly overlapped the Matlab ones.

**Phase II.** In this *architectural phase* we built the entire architecture in VHDL-AMS, including synchronization, preamble sense and AD conversion. A functional partition among the main building blocks was performed for reaching a more hardware-oriented description: Appropriate *entities* and *architectures* from the processes given in the previous listing were created (see figure 2). Internally, every block was still described using abstract VHDL-AMS statements so that their behavior can be considered as "ideal". Non-linear effects, offsets, bandwidth limitations are excluded from this simulation, the goal being to demonstrate the functionality of the entire transceiver. Nonetheless effects which have a relevant impact on the system-level performance have been modeled (quantization effects of the ADC and of the DAC controlling the AGC and saturation in the various stages). The results of system-level simulations obtained at this stage are reported in [2].

**Phase III**. Once the architectural details have been defined through extensive simulations in *Phase II*, the blocks description should reach the circuit-level characteristics. Even if the language semantics is rich enough for this purpose, the CPU cost would be relevant if the entire architecture had to be simulated. ADMS offers the possibility to adopt a *substitute-and-play* approach: Single blocks description can be changed, and a transistor-level netlist can be imported, without having to modify the environment (see figure 2), provided that input/output terminals are electrically compatible [12]. This possibility is extremely powerful, as the system-level testbenches can be used to evaluate the impact of a single block on the entire system, by comparing *Phase II* and *Phase III* results. In this work we selected the "Integrate and Dump" as the best candidate to show the effectiveness of the methodology: Its design and specific behavior are reported in section 4, while its impact on system level performance is discussed in section 5.

**Phase IV**. The *substitute-and-play* philosophy suggests then to proceed with the design of the other blocks as in *Phase III*. Anyway, "non-ideal" effects derived from the already detailed blocks cannot be neglected when designing and simulating new blocks. On the other side, the CPU time needed for a system level simulation carried on as in *Phase III* can be relevant, if the transistor level circuit has to be kept for all the blocks. The way we propose to solve the conflict is to *characterize* the detailed block and to *model* it, so that corrections can be imposed to the behavioral description of the block, and, in the same time, still a light system simulation can be performed in terms of CPU time: The input/output terminals are electrically compatible (see figure 2), the architecture description does not include a transistor netlist, but the transistor-level effects are included in the description. The *Phase IV* results in the case of the "Integrate and Dump" are discussed in sections 4 and 5.

## 4. CMOS integrator implementation

The Integrate and Dump unit (I&D) is crucial for an UWB energy detection receiver, especially for the synchronization and ranging phases, and requires special design care in order to guarantee a sufficiently high gain-bandwidth product. Differently from a recent implementation using a BiCMOS technology [10], our target was to develop a lower cost standard-CMOS integrator.

In the literature, the typical CMOS integrator is the $G_mC$ one, which consists of an open-loop Operational Transconductance Amplifier (OTA) loaded with a capacitor. Ensuring high gain-bandwidth products requires voltage mode networks avoidance: A current mode circuit [6] was thus chosen (figure 3). Apart from the bias circuit, the I&D unit includes three parts: the Integration Switches circuitry, the CMFB (Common Mode FeedBack) network and the transconductance amplifier. It needs two signals *Controlp*

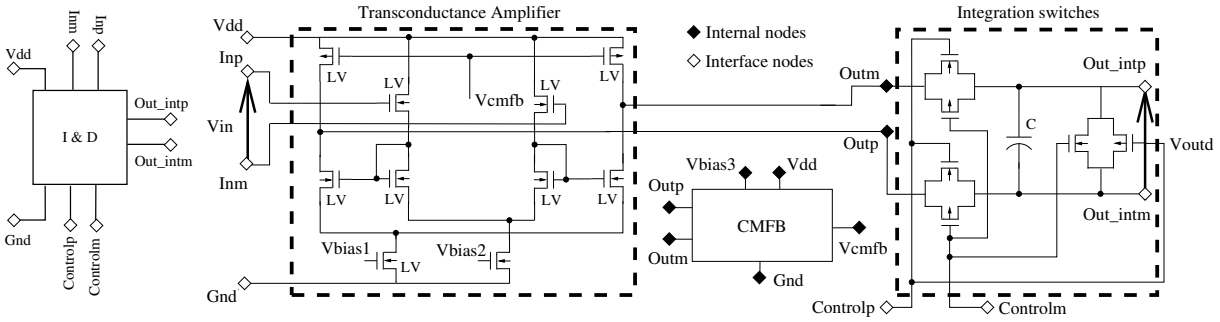


**Figure 3. Integrate and Dump circuit structure**

and *Controlm* which control the integration and dumping process. It has a fully differential architecture so as to reject common mode noise, especially coming from the substrate.

The biasing circuit, not shown in figure for brevity, consists of two auto-biasing networks which give the references for the remaining parts of the circuit. The Integration Switches consist of a couple of transmission gates which connect the OTA outputs to the integrating capacitor and of an additional transmission gate whose aim is to reset the accumulated charge prior to restart integration. The CMFB block, again not reported for space reasons, is fundamental because the output nodes of the transconductance amplifier have a high impedance and are subject to temperature and power supply voltage variations causing the output to float. The transconductance amplifier consists of a source-follower differential input stage whose currents are mirrored and amplified into the output stage, resulting in an output current proportional to the input voltage.

The input stage nMOS aspect ratio on the order of 20 allows a high gain, while the output stages mirroring MOS aspect ratio of about 2 permits a high bandwidth. In addition, this circuit includes LV (low threshold voltage) transistors, that allow a large overdrive voltage and compensation the threshold variations due to both body-effect and noisy bulk voltages coming from the substrate. Some of the integrator design constraints such as slew rate and bandwidth, have been extrapolated from the analysis of 100 UWB TG4a CM1 waveform realizations [4]. The process employed is UMC mixed mode 0.18 $\mu$m 1.8 V. The DC input linear range is around 100 mV and the output swing is 1.6 V because the output stage does not include any cascode structure. The load capacitor $C$ is nominally 1 pF. The operating temperature range is from 0 to 90 °C; at 30 °C the small-signal CMRR measured at 100 Hz is 162 dB while the small-signal PSRR measured at the same frequency is 127 dB.

The AC response of the integrator simulated with Eldo (Spice model level-57) is shown in figure 4 ($V_{dd} = 1.8V$, $T = 30°$C) where *Voutd* and *Vin* are the differential voltages defined in figure 3. The circuit approximates an ideal

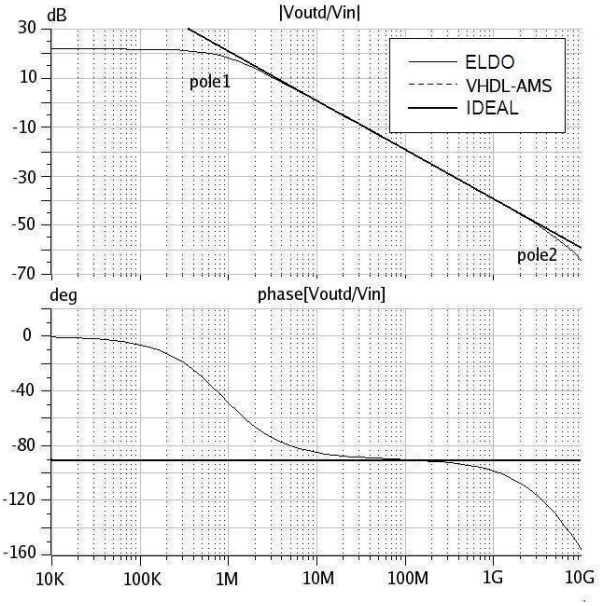


**Figure 4. Integrator AC response**

integrator in the frequency range from 10 MHz to 1 GHz, which is sufficient for an UWB signal rectified by the squarer unit in figure 1. The low-pass behavior at low frequencies is due to the finite output resistance of the final stage, resulting in a pole at $f_{pole1} = 0.886$ MHz and in a DC gain of 21 dB, while the effect of the parasitic capacitors results in a pole at $f_{pole2} = 5.895$ GHz.

According to the methodology step presented in section 3, *phase IV*, a proper VHDL-AMS model of the integrator through its transfer function is needed to save simulation time at system level. At the time of writing the model simply consists of two coupled differential equations which define the two poles and the DC gain, as it will be shown in the next section. As shown in figure 4, this model, even if not refined, perfectly overlaps the AC response simulated with Eldo. The behavior in the transient regime is discussed in the following section.

## 5. System simulations

We report here the simplified VHDL-AMS listings derived from phase II, III and IV of our methodology. For the ELDO netlist, the component instantiation defines a VHDL-AMS/ELDO co-simulation.

```
-- IDEAL -- PHASE II
if sel='1' use vo'Dot==vin*K; else vo==0.0; end use;
-- SPICE (ELDO) -- PHASE III
component int_spice
  port ( terminal Inp, Inm: electrical;
         terminal Controlp, Controlm, Vdd,
                  Gnd, Out_intp, Out_intm: electrical);
end component;
ATTRIBUTE Eldo_device OF int_spice:
                          COMPONENT IS Eldo_subckt;
-- BEHAVIOURAL VHDL-AMS -- PHASE IV
if sel='1'use
  vin-1.0/(2*3.14*0.8e6)*vo_q'Dot-vo_q==0.0;
  10**(21.8/20)*vo_q-1.0/(2*3.14*5.9e9)*vo'Dot-vo==0.0;
else vo_q==0.0; vo==0.0; end use;
```

In this example, the ideal integrator with its corresponding differential equation and gain *K* is shown as first. The ELDO integrator, which includes 31 transistors, is specified simply by instantiating the component with the same terminal names as shown in figure 3. The VHDL-AMS behavioral model is specified through two differential equations which model the two poles and the DC gain. In both the first and the third cases *Vo* is the integrated output voltage, *Vin* is the input voltage from the squaring unit and *sel* is the integration control signal.

A significant result is presented in figure 5 in which the system transient responses for the three implementations are shown. In this example the input signal is integrated, then held for the required time for an ADC conversion, and successively the integration voltage is reset. The VHDL-AMS model output is slightly different from the ELDO transient response, notwithstanding the perfect overlapping of AC figures underlined before: This mismatch is due to distortions caused by the limited linear input range of the circuit not contemplated in the model. This discrepancy evidences the limits of the simple model chosen, as it includes only the poles and the gain as non ideal effects. Anyway, it is adequate to show the effectiveness of the proposed methodology, as the following results will demonstrate.

Table 1 shows the required CPU times for a system simulation lasting 30 $\mu s$. The simulations are run (IBM-Xeon, 4GB RAM, 3.0 GHz processor) with a fixed time step of 0.05 ns, an accuracy $EPS = 10^{-6}$ and the Newton/Raphson solving algorithm. The CPU time with the ELDO netlist is 3 times larger than the time required using the VHDL-AMS model and 6 than the IDEAL one. These results emphasize how it would be unfeasible, in terms of CPU time, to proceed with the design of the other receiver blocks and simulate the whole architecture keeping a transistor-level netlist for all the components. On the other side, the promising CPU time improvement achieved while including the VHDL-AMS model confirms that *Phase IV* is unavoidable, if one aims at capturing the real circuits behavior while keeping under control the time budget to complete the design.

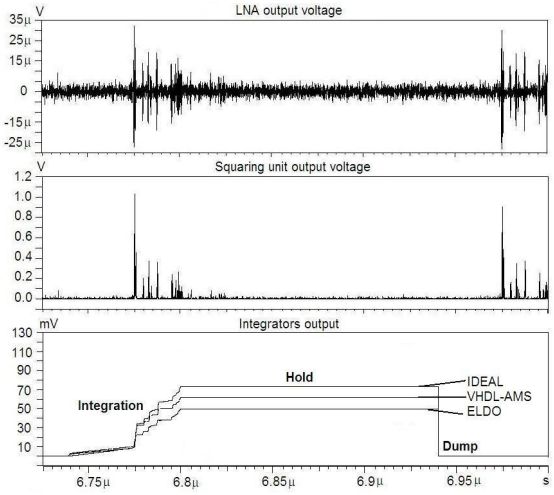


**Figure 5. Integrators transient responses**

**Table 1. CPU time comparison**

| Model | CPU Time | Simulation time |
|---|---|---|
| ELDO | 59 m 33 s | $30\mu s$ |
| VHDL-AMS | 20 m 37 s | $30\mu s$ |
| IDEAL | 9 m 11 s | $30\mu s$ |

It is now interesting to discuss the results on system level parameters like BER and Two-Way Ranging (TWR). We compare only the ideal to the SPICE results: The VHDL-AMS model of the I & D unit, as evident from the above comments to figure 5, needs further improvements to better adhere to the transistor level model. The BER curves in figure 6 show a performance improvement of the real integrator at higher $E_b/N_0$ values, imputable to the noise shaping effect of the second pole at high frequencies.

The TWR consists in a distance estimation through the Round-Trip-Time (RTT) of UWB signals exchanged between two transceivers [2]. A request packet is sent by a first transceiver and is replied by a second after a known processing time (PT). The replied packet is received again by the first transceiver which estimates the RTT by subtracting the PT. The results of 10 TWR iterations at a single distance point (9.9 m) for the ideal and mixed VHDL-AMS/ELDO system are presented in table 2. Here the TG4a UWB channel model employed is the CM1 LOS (Line-Of-Sight) with the recommended path loss. All the simulations have been run with the remaining ideal parts of the circuit described as in section 3, phase II.

With respect to the ideal system two important aspects

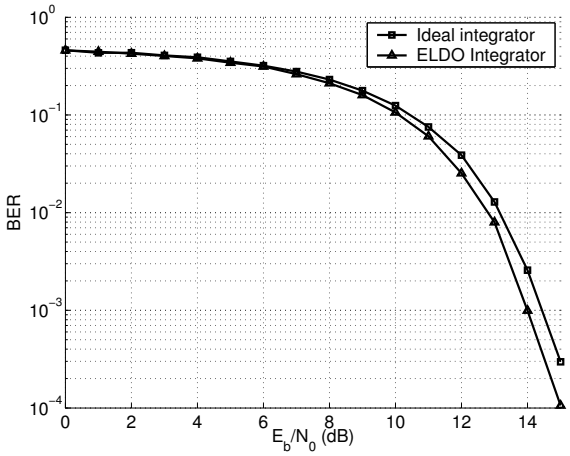


**Figure 6. Comparison between BER curves with ideal and SPICE integrators**

**Table 2. TWR simulation results @ 9.9m with IDEAL and ELDO integrator**

| IDEAL integrator | | ELDO integrator | |
|---|---|---|---|
| **Mean** | **Variance** | **Mean** | **Variance** |
| 10.10 m | 0.49 m | 11.16 m | 0.10 m |

must be underlined: The lower distance estimation variance and the larger offset contribution (1.36 m vs. 20 cm). The first effect is due to the noise shaping which results in an equivalent signal to noise ratio increase at a given distance as cleared in figure 6. The second is due to architectural issues: The AGC cannot ensure both amplitude matching for the integrator input range and energy matching for the ADC input range because of the limited gain of the integrator and input range. In other words, the UWB signal amplified by the AGC causes the squared signal to be out of the integrator input range resulting in a lower output voltage.

These results enhance two crucial points confirming the effectiveness of the proposed methodology. First, we are able to precisely evaluate the impact on system level parameters of a single component, and thus to trim the block design specification (and this is done early in the design flow with respect to the traditional methodologies). Second, adjustments to the architecture are suggested which would not have been detected without the simulation based on the coexistence of both architectural and transistor layers.

In this case, a possible solution consists in modifying the AGC unit including in its description two gain control stages: a first one, at the front-end beginning which controls the signal amplitudes so that saturation at the input is avoided and a second one, which amplifies the integrator output in order to adjust the integrated energy for the ADC input range.

## 6. Conclusions

In this paper we discussed the application of a top-down methodology, which exploits the flexibility of VHDL-AMS, to the design of a UWB mixed-signal SoC. We demonstrated the effectiveness of the methodology in capturing architectural deficiencies and coarse component specifications discovered only after circuit design with a practical and real-life example. Our approach helps limit the risk of traditional methods by letting emerge the impact of fine-grain circuit-level details on system parameters in early design stages. As a result, the unavoidable iterations from system to circuit and back to system are shortened. Given the achieved results, we plan to use the methodology to complete the design of the entire UWB receiver. Special care will be necessary when refining the VHDL-AMS models of the transistor-level blocks (in *phase IV*) so as to avoid excessive CPU time while not losing the needed accuracy.

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