On-the-fly Estimation of IC Macromodels

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I.S. Stievano, I.A. Maio and F.G. Canavero

The development of integrated circuits output buffer macromodels for assessment of signal integrity and electromagnetic compatibility effects in high-speed digital circuits is addressed. The approach is based on the estimation of suitable parametric relations from simulated or measured responses recorded during regular operation of devices, thus not requiring a specific modelling setup and test fixtures.

Introduction: Nowadays, the design of high-speed digital systems along with the time-to-market constraints require assessment of signal integrity and electromagnetic compatibility effects in the early stages of the design process. Such an assessment, achieved by the simulation of signals propagating on critical interconnect structures, relies on the availability of accurate and efficient macromodels of the ports of digital integrated circuits that act as the nonlinear terminations of interconnects. As an example, a macromodel for the output buffer in Fig. 1 is represented by a suitable nonlinear dynamic relation between voltage v and current i of the device port.

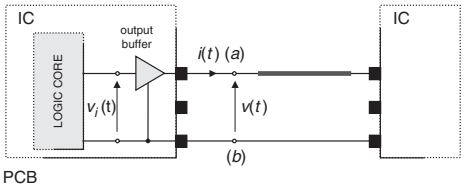

Fig. 1 *Typical interconnect structure with main IC blocks and relevant electrical variables*

Different approaches are in use to obtain IC port macromodels. The most common approach is based on simplified equivalent circuits derived from a conventional internal structure of the modelled devices. This approach leads to the I/O Buffer Information Specification [1], that is widely supported by EDA tools. More recent approaches are based on the use of parametric relations to approximate the device port equations, and on the identification of their parameters from device responses [2]. These approaches offer enhanced modelling capabilities, that facilitate and improve the modelling of recent devices, such as pre-emphasis drivers.

For both approaches, however, the generation of macromodels requires the availability of transistor-level models of the device, or the capability to control the device operation, i.e. the use of dedicated test fixtures to stimulate and measure specific device behaviours. As an example, the estimation of parametric models for the output buffer in Fig. 1 exploits port responses recorded while the buffer is forced (e.g. through the internal logic signal v_i) in a fixed logic state or is forced to perform complete state switchings on suitable test loads [2]. In real devices with complex logic cores, output buffer states can be hardly controlled and model generation from measured data becomes unpractical.

We propose a new technique for the generation of macromodels from actual measurements, avoiding the need of dedicated test fixtures and device control. Macromodels are obtained from device port transient responses measured on devices mounted directly on the board and operating in normal conditions as in the simplified scheme of Fig. 1.

Model structure, estimation and validation: Parametric macromodels of the output buffers of digital ICs exploit the following two-piece parametric relation

$$i(t) = w_H(t) i_H(v, d/dt) + w_L(t) i_L(v, d/dt) \quad (1)$$

where w_H and w_L are switching signals accounting for the device state transitions and playing the same role of the internal voltage v_i in Fig. 1, and i_H and i_L are nonlinear parametric relations accounting for the device behaviour in fixed logic high and low states, respectively [3]. More details on the model representation (1) and on the use of parametric relations for the modelling of IC ports can be found in [2] and references therein.

The estimation of model (1) amounts to computing the parameters of submodels i_H and i_L and the weighting signals w_H and w_L from suitable port voltage $v(t)$ and current $i(t)$ responses. Model parameters are computed by minimising error functions (e.g. the mean square error) between the model responses and the measured port responses, that are used as references to be fitted [3, 4].

The problem addressed in this Letter is how to obtain device responses useful for model parameter estimation while the device is mounted on an application board and operates in normal mode. The estimation of submodels i_H and i_L, and of the weighting functions w_H and w_L, require transient responses containing information on the port behaviour in high and low logic states, and on state switching, respectively. The information on state switching can be extracted from switching responses of the device mounted on the board. On the other hand, the estimation waveform for i_H and i_L must be obtained by perturbing the port variables while the device is in fixed logic state. This can be achieved by shunting the device output port with a perturbing element during normal operation and by using those segments of the responses occurring while the device is in high or low state. The simplest perturbing element that causes transient responses exploring a wide range of the output voltage and current variables is a mismatched stub. Alternatively, different (possibly active) perturbing elements can be devised.

For simplicity, the example of this Letter is based on the output port of a commercial Texas Instruments transceiver, the HSPICE transistor-level description of which is available from the vendor official website. The example device is an 8-bit bus transceiver with four independent buffers (model name SN74ALVCH16973, power supply voltage VDD = 1.8 V), operating at 167 Mbit/s (i.e. the bit time is 6 ns). The HSPICE simulations of the transistor-level model of this example driver (set to produce a 2048 long pseudorandom bit stream) are assumed as the reference curves hereafter.

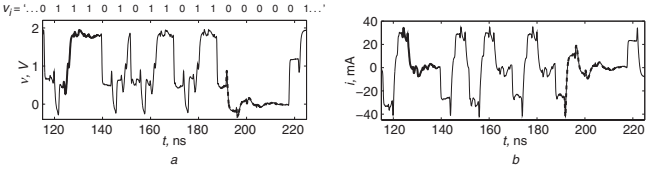

Fig. 2 *Output port voltage v(t) and current i(t) responses computed for example driver of Fig. 1 with mismatching stub placed between terminals (a) and (b)*

a $v(t)$
b $i(t)$
Shown waveforms represent an excerpt of 2048-long pseudorandom bit stream generated by IC of Fig. 1.Thick segments of $v(t)$ and $i(t)$ signals are the waveforms used for estimation of submodels i_H and i_L in (1) (see text for details)

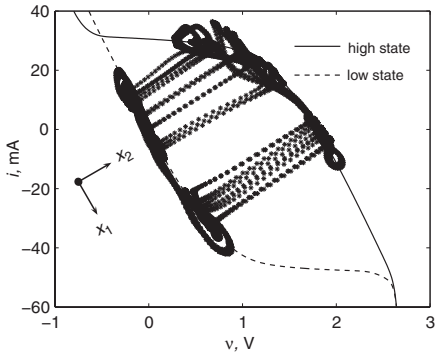

Fig. 3 *Static characteristics of example driver in fixed high state and low state superimposed to samples {v(t), i(t)} of port transient responses in Fig. 2 (stars)*

Fig. 2 shows the port responses obtained with a perturbing stub connected in parallel to terminals (*a*) and (*b*) in Fig. 1. For this simulation, the stub is modelled as an ideal transmission line (characteristic impedance $Z_0 = 50\ \Omega$, time delay $T_d = 2$ ns) loaded by a 10 pF capacitor. The voltage and current time sequences of Fig. 2 are represented as trajectories in the (v, i) plane in Fig. 3. This cloud of points (equispaced in time by 20 ps) are superimposed to the device static characteristics computed when the device is in the high (low) logic state. Fig. 3 highlights that the transient responses obtained with the stub can densely explore the portion of voltage and current plane around the device static

output characteristics. Hence they are good candidates for the identification of model parameters. This example suggests the following two-step procedure for the estimation of model (1).

(i) Estimation of submodels: As in [2], the parametric models used for i_H and i_L in (1) are discrete-time parametric representations based on sigmoidal expansions [3], the parameters of which can be estimated by standard algorithms as in [4]. The estimation waveforms for submodel i_H (i_L) must be voltage and current transient responses of the device in high (low) logic state. For the example device, the estimation waveforms of i_H can be obtained from the solid thick parts of the signals $v(t)$ and $i(t)$ of Fig. 2. These signals are obtained by considering the slice of the port responses recorded while the device is in the high state for some consecutive bit intervals. Similarly, the estimation waveforms of submodel i_L can be obtained from the dashed thick parts of Fig. 2.

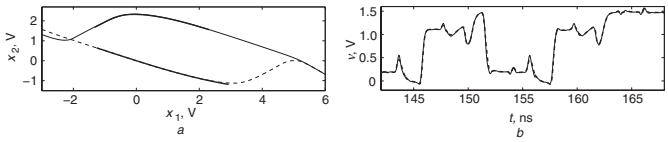

Fig. 4 *Static characteristics of submodels i_H and i_L in (1) (solid thick curves) superimposed to actual characteristics of example driver in fixed high state (solid line) and low state (dashed line) (Fig. 4a); port voltage v(t) response computed for example driver connected to a validation load (ideal transmission line with characteristic impedance $Z_0 = 50\ \Omega$, time delay $T_d = 1$ ns terminated by shunt 100 Ω resistor and 5 pF capacitor) (Fig. 4b)*

The modelling process is facilitated if the following variable transformation is adopted:

$$\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} 1 & -50 \\ 1 & 50 \end{bmatrix} \begin{bmatrix} v \\ i \end{bmatrix} \tag{2}$$

where the new input and output variables (x_1, x_2) have the effect of simplifying submodels i_H and i_L, thereby facilitating estimation of their parameters. The above transformation also implies that the submodels are always defined for every value of the new input variable occurring in regular operation.

(ii) Computation of weighting signals: The weighting signals w_H and w_L are computed after estimation of submodels i_H and i_L from port responses occurring during state switchings. In our problem, we use the simplifying assumption $w_L = (1 - w_H)$ and compute w_H as a solution of (1) when v and i are the waveforms of a single state transition event. These waveforms are extracted from the edges of $v(t)$ and $i(t)$ measured during ordinary data transmission without the perturbing stub connected. In this procedure, use of switching waveforms for two different device loads, in order to compute both w_H and w_L, turned out to be scarcely effective. This is due to errors from both measurements and submodel estimation, as well as to inter-symbolic interference noise affecting the edges of pulses transmitted in ordinary operation, that penalise the two switching waveforms approach.

Once all model parameters are computed, the model equations are converted into a macromodel to be plugged in a standard simulation environment, e.g. SPICE or any hardware description language allowing for analogue parts. Implementation details are described in [2].

The proposed modelling procedure has been applied to the example device, obtaining a model with i_H and i_L composed of two and three sigmoidal functions, respectively, and with a dynamic order equal to 3 [2]. The ability of the proposed procedure to extract the static behaviour of the modelled device is demostrated by Fig. 4*a*, comparing the static characteristics of the original device and of its model. The accuracy of the dynamic response of the model can be appreciated in Fig. 4*b*, that compares the output voltage waveform $v(t)$ of the original device and of the model when they drive a load different from the one used for the estimation process. In conclusion, the proposed modelling approach enables generation of accurate parametric models from measurement carried out on devices operating in their application environments.

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