Behavioural Macromodels of Digital IC Receivers for Analogue-Mixed Signal Simulations

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I.S. Stievano, F.G. Canavero and I.A. Maio

A behavioural multiport macromodel for the input buffers of digital integrated circuits is presented, including the bit detection and the effects of power-supply fluctuations. The model is given in terms of mathematical expressions, thus preserving proprietary information of designers, and offers comparable accuracy and improved efficiency compared with transistor-level models. It is also completely compatible with SPICE, VHDL-AMS and IBIS implementations.

Introduction: Data transmission in modern information and communication devices requires higher and higher bit rates, and the analogue nature of transmitted digital data on interconnects becomes increasingly important. This trend involves any integration scale, from chip to system level, and reproduces at smaller scales those transmission problems typical of traditional data links. Thus, the designers need to worry more and more about the analogue signals reaching the input port of buffers and of the corresponding signals processed inside the receivers and forwarded to the digital core of integrated devices.

During the design of a system, the control of critical effects, such as jitter, intersymbol interference, crosstalk, etc., is normally done by the analogue generation of eye diagrams of very long bit patterns, which in turn require efficient models of interconnects, drivers and receivers. In this Letter, we concentrate on the efficient modelling of receivers, which represent critical elements for the simulation of data links. It is insufficient to consider receivers as simple one-port mostly linear buffers showing a capacitive behaviour, as commonly done in the past. Receiver buffers, in fact, process the received signal, degraded by its propagation along the data channel, and reshape the original bit pattern by making the transitions more regular, and flattening the high and low levels. This detected signal, still analogue but much closer to a digital sequence, is then forwarded to the internal stages of the logic device, where the processing of information takes place. A very accurate prediction of such a detected signal is needed, since the designer wants to make sure that no bit errors arise inside the entire chain. In addition, the final bit pattern output by the receiver buffer is not insensitive to the switching noise present on the power supply pin, which may act on the device thresholds, and alter the bit detection. The previous considerations motivate us to seek a multiport model of receivers, where the dynamic (and possibly nonlinear) load that the device presents to the incoming signal is accounted together with the bit detection, and both processes are coupled with the power supply pin.

The work presented in this Letter, extending a simple one-port model discussed in [1], is aimed at building a fully-coupled three-port model in terms of mathematical expressions, relying on the well established theory of system identification for the estimation of parametric models from systems port responses [2, 3]. The great advantage of the approach advocated is its ability to hide the internal structure of the device, thus preserving the founder proprietary information, and the full compatibility with IBIS version 4.1 [4], which allows, via its multilingual extension, the coexistence of traditional IBIS models with externally-defined models implemented in SPICE or VHDL-AMS code. This is particularly important, since nowadays most signal integrity (SI) and electromagnetic compatibility (EMC) simulations are carried out by specialised IBIS-compliant commercial tools, for which large component libraries and powerful utilities are available.

Model structure: Fig. 1 shows the basic structure of a receiver circuit with its relevant electrical and 'digital' variables of interest: v_A and i_A are the input port voltage and current, v_{ds} and i_{dd} are the voltage and current of the power-supply port, and voltage v_D is the analogue output of the first receiver stage. Today's macromodels usually consist of a single port, relating v_A and i_A variables, only. However, the inclusion of signal v_D has two great advantages, i.e. it includes the threshold detection carried out by the receiver, and it carries additional information on the effects of the power supply noise and of electromagnetic interference as they reach the logic core of the receivers. A complete behavioural model of a receiver circuit must therefore relate the voltage and current variables of all ports. In actual receivers circuits, the state transitions of the detected signal $v_D(t)$ are triggered by the analogue input voltage v_A. This is mainly due to the strongly nonlinear nature of the v_D–v_A static characteristic and to possible enhanced detection mechanisms of the receiver input stages. Besides, the activity of the logic core weakly influences the behaviour of the analogue part (i.e. the shape of the $v_D(t)$ edges is independent of the shape of $v_A(t)$). From these general considerations, the complete receiver macromodel can be cast as the composition of two submodels: one for the analogue part and the second one for the detected signal (i.e. for the transmission from the analogue to the 'digital' part), as illustrated by the vertical separation of Fig. 1.

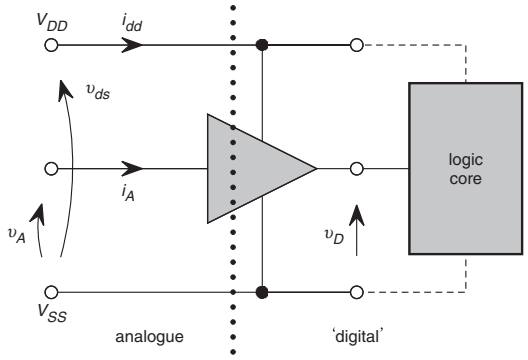

Fig. 1 *Structure of input buffer of digital integrated circuit with relevant blocks and electrical variables of interest*

The conventional model representation for the receiver analogue port is obtained as a sum of a static and a dynamic part, as follows:

$$i_A(t) = f_s(v_A,\ v_{ds}) + f_d(v_A,\ v_{ds},\ d/dt) \tag{1}$$

where submodel f_s is the two-dimensional static characteristic of the input port of the receiver and submodel f_d is a general nonlinear dynamic model. A similar representation holds for current i_{dd}. The splitting of static and dynamic contributions is justified by the discussion of a similar case provided in [5].

Without loss of generality, for the device under modelling presented in this work, the static surface f_s is approximated via a linear interpolation of the static characteristics v_A–i_A computed for two different values of the power supply. For submodel f_d, a nonlinear parametric model based on sigmoidal expansions is used to approximate the nonlinear dynamic behaviour of receivers [3]. A detailed discussion of the model estimation, based on device port responses is outside the scope of this Letter and the reader is referred to [2, 3].

The transmission between the receiver input and output ports is represented as a controlled voltage source $\hat{v}_D$ obtained by juxtaposition in time of some elementary up and down state transitions of voltage v_D, consequent to up (or down) state transitions of the receiver input voltage v_A. Such state transitions are triggered when v_A crosses a suitable threshold value (or more than one for a receiver with hysteresis) and the shape of the edges is independent of the shape of $v_A(t)$. It is worth noting that each elementary transition includes the delay between the v_A and the v_D state transitions. If necessary, the dependency of the delay on external parameters, like the temperature or the v_A slope in the threshold region, can be readily included. Also, it should be mentioned that the elementary transitions are recorded for nominal power supply values V_{DD} and V_{SS}, and the effect of the power supply voltage variation is included in the model by a linear correction, as follows:

$$v_D(t) = \hat{v}_D(t)\left(\frac{v_{ds}(t)}{V_{DD}}\right) \tag{2}$$

since we assume that $v_D(t)$ is roughly proportional to the power supply voltage $v_{ds}(t)$.

A final comment on possible alternatives to model (2) is in order here. A simplified model consisting of a cascade of a static mapping and a linear dynamic system may suffer from non-causality problems (variable transmission delay inside the receiver may misalign the juxtaposition of up and down transitions). On the other hand, more complex neural-network types of model are heavy in terms of simulation time, without significantly improving the accuracy of the advocated model (2), which already provides good results, as demonstrated in the following Section.

Application: To validate the proposed macromodel and assess its performance, we use a high-speed IBM CMOS transceiver ($V_{DD} = 1.8$ V), for which a transistor-level description is available; additional details of this transceiver can be found in [1]. A macromodel of this device used as a receiver has been derived from the responses collected by simulations of the transistor-level model, according to the model structure described in the previous Section. The macromodel equations are interpreted as circuit equivalents (see [1] for details), and has been implemented as a SPICE-like subcircuit. Alternatively, the model equations can be directly implemented via metalanguage descriptions, like VHDL-AMS. The validation setup is a typical data link consisting of a driver and a receiver (both realised by means of the same transceiver), connected via a 8 cm-long MCM trace, modelled as a lossy and dispersive transmission line. The data pattern sent on the interconnection is a random sequence of 256 bits with 1 ns duration. The power supply network connected to both driver and receiver is modelled by a lumped equivalent.

All simulations are carried out by means of PowerSPICE and the following simulation strategy has been adopted: a set of reference waveforms is computed by using the transistor-level description for the driver and the receiver; then, two sets of waveforms are generated by replacing the receiver with a macromodel using: (i) a simplified linear parametric approximation of the dynamic term (macromodel **M1** in the following); and (ii) the sigmoidal parametric model (macromodel **M2**).

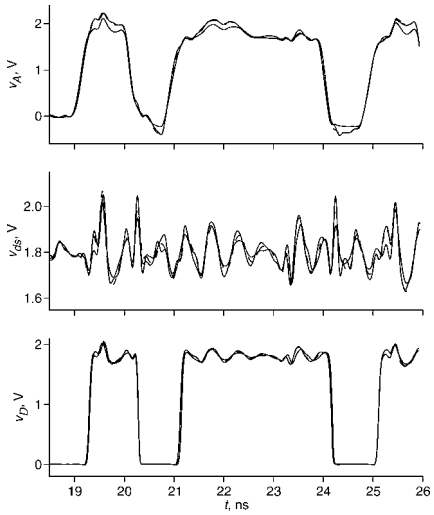

Fig. 2 *Voltage waveforms $v_A(t)$, $v_{ds}(t)$ and $v_D(t)$ for example test case*
—— reference —— approximate macromodel **M1** – – – **M2**

Fig. 2 shows a comparison of the voltage waveforms $v_A(t)$, $v_D(t)$ and $v_{ds}(t)$ computed by means of the reference and predicted by the macromodels. The comparison highlights that macromodel **M2** accurately reproduces the extreme over/undershoots of voltage v_A, which are only roughly approximated by the simplified macromodel **M1**. In addition, it is worth noting that the timing errors introduced by both models are always less than 30 ps (3% of bit time) and that **M1** is sufficient for an accurate prediction of the detected signal $v_D(t)$. In terms of efficiency, in the computation of curves for the complete 256 bit-long sequence, the speedup factor introduced by the macomodels is of the order of 37 for **M1** and 33 for **M2**.

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