A comprehensive class A to B power and load-pull characterization of GaN HEMTs on SiC and sapphire substrates

A Comprehensive Class A to B Power and Load-Pull Characterization of GaN HEMTs on SiC and Sapphire Substrates

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***Abstract*— An extensive power characterization of devices fabricated on GaN grown on SiC and sapphire substrates has been carried out, including power sweep and load-pull measurements in different bias conditions from class A to class B. An active load-pull bench optimized for high voltage and high power measurements allows to extend the load-pull characterization to the whole Smith chart, and to localize the optimum load conditions even for devices with almost reactive optimum terminations. The characterization procedure allows to verify scaling rules and the effects of defects and thermal degradation on the device power performances. The results of the SiC and sapphire-based devices show that, on one side, SiC-based devices exibit state-of-the-art performances in Class A, and, on the other side, low-cost sapphire-based devices, when biased in high efficiency classes, can be viable candidates for medium power applications, despite the higher thermal resistivity of sapphire compared with the one of SiC.**

I. Introduction

HEMT devices fabricated on GaN are presently attracting growing attention for their promising high power capabilities, due to the excellent intrinsic GaN material properties. The wide band gap energy and high breakdown electric field strengths, several times larger than in both silicon and GaAs [1], allow for high voltage operation. Furthermore, the AlGaN/GaN heterostucture induces a very high electron density in the HEMT channel, compared to standard AlGaAs/GaAs HEMT devices; this, in combination with the high saturated electron drift velocity, leads to an even increased output power [2], [3]. Despite promising performances have already been demonstrated, GaN HEMTs still need technological improvements to be developed, in order to be exploited in industrial production. Defects play a major role in limiting the state-of-the-art device output power, while the extremely high power density reached in the large periphery devices poses thermal degradation and reliability problems as further limiting factors to be investigated. Therefore, power characterization, together with reliability assessment, is becoming the key step in evaluating the various technologies and driving the design engineers towards high power and high efficiency PA design.

This paper presents a complete characterization campaign of GaN devices fabricated by Selex on both SiC and sapphire substrates from Qinetiq Ltd [4], [5]. Devices from the same technology (SiC or sapphire) are measured in different bias conditions, from class A to class B, and compared, in order to verify their output power scaling and thermal effects with varying gate periphery. Finally, the maximum output power reached in 1 mm devices on SiC and sapphire substrates are compared to draw conclusions on the possible exploitation of the two technologies. Globally, Selex GaN HEMTs show performances well within the state-of-the-art.

II. Active Load-Pull Characterization

Load-pull characterization at the fundamental frequency [6], and at the harmonics [7], has been demonstrated to be the most straightforward way to extract the maximum power deliverable by a given device, and is therefore a valuable technique to directly evaluate the effects of technology improvements on the device power performances. Challenges in the load-pull characterization arise in the particular case of GaN devices and require dedicated measurement set-ups. In particular, devices with small gate periphery are often used as a technological test to determine the power capabilities, thus avoiding thermal effects. These devices pose characterization problems, since the power optimum load termination is highly reflective due to the high bias voltages associated with a relatively small drain current, and to the small reactive part involved. The typical optimum output reflection coefficient for this kind of periphery can be easily in magnitude even greater than 0.9, making its synthesis extremely awkward using conventional passive load-pull systems, where the maximum attainable reflection coefficient is limited by the losses: for this reason an active load-pull system appears to be the best choice [8]. The active load-pull bench developed at Politecnico of Torino, operating in the 0.5-18 GHz frequency range, is shown in Fig. 1.

The incident and reflected power waves (port 1 and port 2) are measured (sampler 1 and 2) with a VNA. The VNA calibration implements both conventional, and power correcting algorithms, required for the non-linear characterization, able to set the reference planes at the probe tips, on the wafer. The bench, besides conventional multi-bias S-parameters, allows for load and source pulling (fundamental frequency and harmonics), with simultaneous real-time measurements of input reflection coefficients, P_{in}, P_{out}, Gain, PAE, and IMPs. For high power and high reflectivity GaN devices, the active load-pull set-up has been further improved with new ad-hoc features: high power bias tees, low-loss directional couplers [9], and fast current shutter to protect the probe from damage in case of device failure. Finally, for large periphery devices, and on-wafer characterization, the dissipated power can be so high to increase the probe station chuck temperature during measurements, compromising the accuracy of the experimental

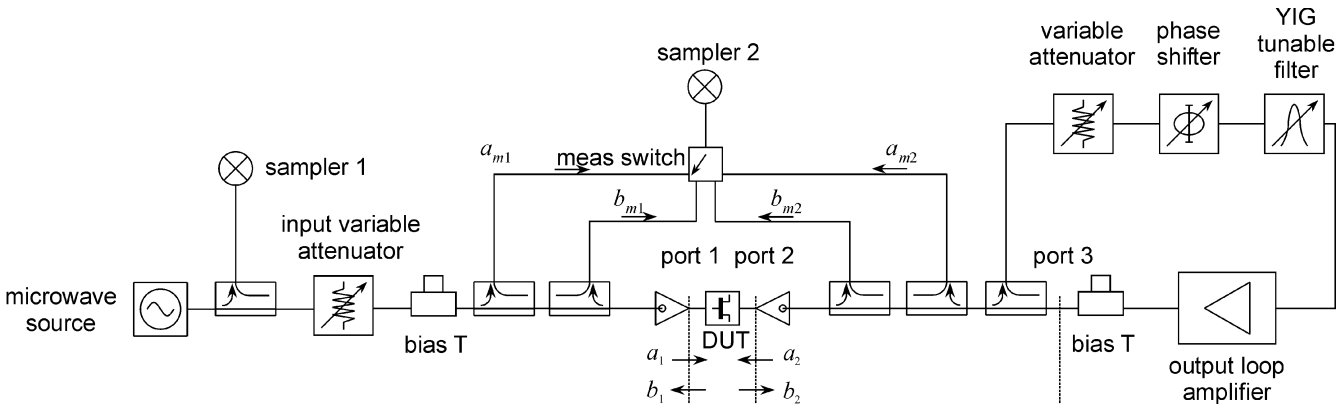

Fig. 1. A simplified scheme of Politecnico di Torino real-time active load-pull system.

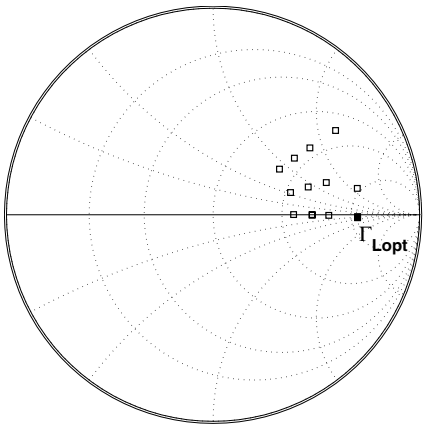

Fig. 2. Load-pull map of a $2 \times 100\mu$m device on SiC technology operating at 2 GHz, and biased in class A ($50\%I_{DSS}, V_{DS} = 30$ V). The marker shows the location of the optimum load.

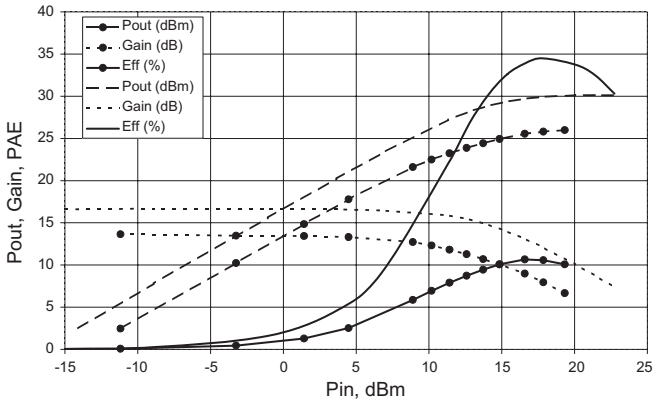

Fig. 3. Power performances of the SiC $2 \times 100\,\mu$m device operating at 2 GHz, and biased in class A ($V_{DS} = 30$ V) on a 50 Ω load (circle markers), and on the optimum load.

data; in our set-up, a chuck temperature control has been implemented using a forced liquid cooling system.

III. Results

The measurement campaign has been carried out on HEMT devices fabricated both on SiC and sapphire substrates with Contact Lithography (CL) technique, allowing for a gate length of $1\,\mu$m. This limitation will be relieved in next generation devices, either by improving the CL technology itself or by using the Electron Beam Lithography. At the present moment, the device transition frequency is relatively low, and therefore the charaterization process has been carried out at 2 GHz. Both in the case of SiC and sapphire substrates, devices available for on-wafer measurements are characterized by increasing the gate periphery: $w = 2 \times 25\,\mu$m (two fingers of $25\,\mu$m), $w = 2 \times 100\,\mu$m (two fingers of $100\,\mu$m) and a millimeter gate device ($100\,\mu\text{m} \times 10$ fingers). The sapphire fabrication technology is of more recent generation than the one on SiC, therefore, devices with the same layout, but grown on the two different substrates, cannot be directly compared.

Let us first consider the SiC based technology. Devices have been biased in class A ($50\%I_{DSS}$) in order to achieve the maximum output power, although the efficiency is low. The drain voltage has been set to 30 V, which is slightly less than the theoretical optimum drain bias in class A that, with an estimated breakdown voltage of 80 V, corresponds to 40 V. We have decreased the drain voltage in order to lower DC power dissipation, and therefore reduce thermal degradation effects. It will be shown below that, by varying the drain bias between 30 and 40 V, while keeping the gate voltage unchanged, the effect of thermal degradation partially compensates the improvement, thus leading to power performances only slightly better, while the PAE is worsened. Therefore we have chosen a drain bias of 30 V as the best compromise to achieve both high output power and efficiency.

Fig. 2 shows a typical result from load-pull characterization, *i.e.* a load-pull map, for the $2 \times 100\,\mu$m devices on SiC, operating at 2 GHz, abd biased in class A . The optimum load is found to be (see again Fig. 2) $\Gamma_L = (0.7, 0°)$. Fig. 3 shows the behaviour of output power, gain, and PAE, as a function of the input power, for the same device in class A. The figure compares the performances on a 50 Ω load, and on the optimum load. In this device, the 50 Ω load is far from the optimum load condition (see again Fig. 2), and therefore all the performances show a significant inprovement from 50 Ω to the optimum load. Concerning the output power, at 5 dB gain compression the $2 \times 100\,\mu$m device is capable of 30.5 dBm (5.7 W/mm). The PAE efficiency in this case is limited to 35 % due to the choice of the class A operation. The scaling properties of devices in this technology will be adressed below, by comparing these results on measurements on 1 mm device.

In fact, similar characterization has been performed on the 1 mm device from the same technology, again in class A

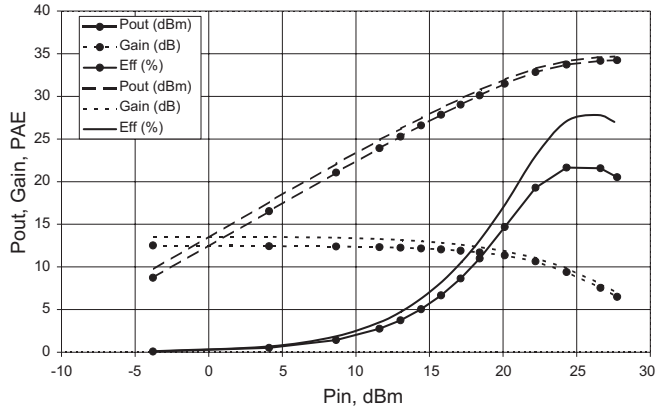

Fig. 4. Power performances of the SiC 1 mm device operating at 2 GHz, and biased in class A ($V_{\mathrm{DS}} = 30$ V) on a 50 Ω load (circle markers), and on the optimum load.

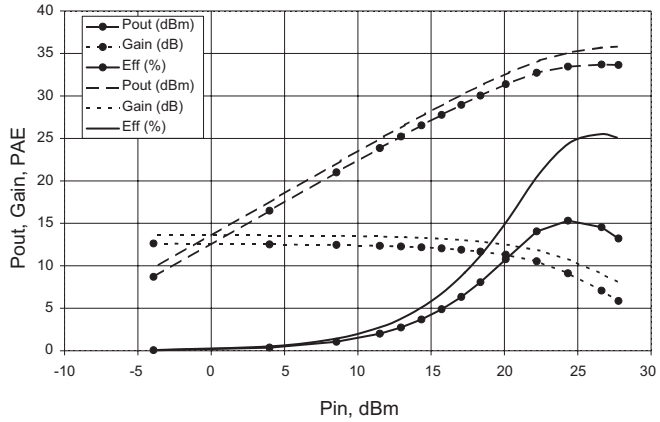

Fig. 5. Power performances of the SiC 1 mm device operating at 2 GHz, and biased in class A ($V_{\mathrm{DS}} = 40$ V) on a 50 Ω load (circle markers), and on the optimum load.

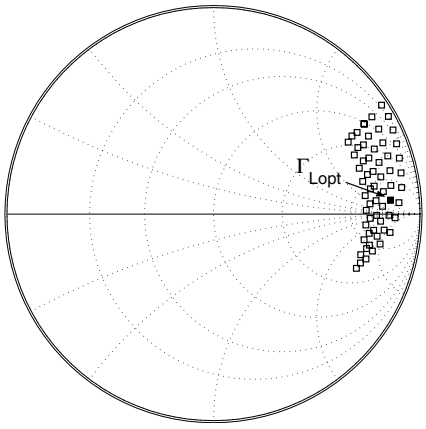

Fig. 6. Load-pull map of a $2 \times 25\,\mu$m device on sapphire technology, operating at 2 GHz, and biased in class B ($V_{\mathrm{DS}} = 30$ V). The marker shows the location of the optimum load.

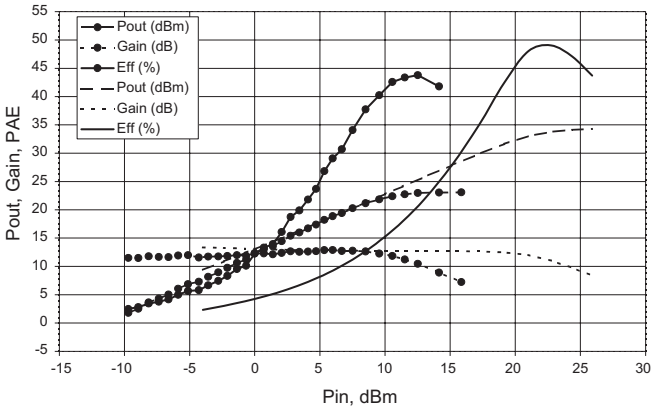

Fig. 7. Scaling properties of the sapphire devices. $2 \times 25\,\mu$m device (circle markers), and 1 mm device are compared at 2 GHz, biased in class B and on the optimum load.

and at 2 GHz: from load-pull maps, the optimum load is found to be $\Gamma_{\mathrm{L}} = (0.4, 17°)$. Fig. 4 shows the behaviour of output power, gain and PAE, as a function of the input power. The figure compares the performances on a 50 Ω load, and on the optimum load. It can be seen that in this large periphery device the optimum load is not far from the optimum termination. The output power reaches 35 dBm (3.2 W/mm), while efficiency is even lower than in the case of a $2 \times 100\,\mu$m device. Finally Fig. 5 shows that the power performances of the same device with $50\% I_{\mathrm{DSS}}$ and 40 V bias do not change significantly with respect to the 30 V bias case, but PAE is dramatically reduced. By comparing results in Fig. 3 and Fig. 4, we can finally comment on the scaling properties of the the two SiC devices with optimum loads. Before starting the discussion, it is important to point out that the two devices do not respect the scaling of the DC current; in fact I_{DSS} is 560 mA and 140 mA for the 1 mm and the $2 \times 100\,\mu$m devices, respectively. This imperfect scaling can be due either to the higher power dissipated in the large periphery device, which leads to a higher device temperature, or to layout differences. In class A, the ratio of the I_{DSS} in the two devices should lead to a an expected maximum output power difference of 6 dB; measured data show that the output power rises from 30.5 dBm in the small periphery device, to 35 dBm in the 1 mm device, with approximately 5 dB of improvement, *i.e.* slighly less than the expected 6 dB. It is therefore confirmed that the major problems in the device periphery scaling is related to the DC behaviour.

Turning to the devices fabricated on sapphire substrates, it must be noted that the sapphire thermal conductivity is much lower than the SiC conductivity [10], making therefore desirable to bias these devices in higher efficiency modes than in class A, to decrease power dissipation. Class B has been chosen as the best test condition. Fig. 6 shows the load-pull characterization at 2 GHz on the small periphery device $2 \times 25\,\mu$m (two fingers of $25\,\mu$m) in class B. The optimum load is $\Gamma_{\mathrm{L}} = (0.86, 3°)$. Observe that the whole map is made on an area of the Smith chart with very high reflection coefficients. For a 1 mm periphery device in class B the load-pull measurements show an optimum load $\Gamma_{\mathrm{L}} = (0.43, 23°)$. Fig. 7 shows the scaling behaviour of the two sapphire devices at 2 GHz and optimum loads. The output power at 1 dB compression point rises from 21.5 dBm for the $2 \times 25\,\mu$m device to 33 dBm for the 1 mm device, with 11.5 dB increase instead of 13 foreseen by the simple periphery scaling rule. At 5 dB compression point the 1 mm device exhibits an output power of 2.8 W/mm.

Channel pinch-off voltage required for class B device bias, is particularly critical for GaN HEMT. For this reason, a simple experimental procedure has been exploited, based on

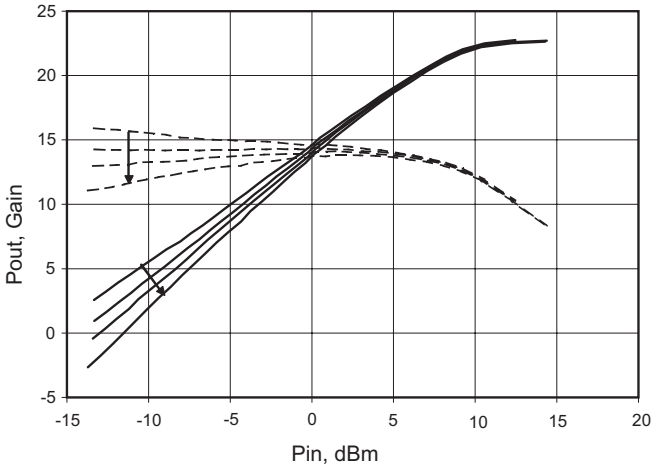

Fig. 8. Gain (dashed lines) and output power (solid lines) behaviour of a $2 \times 25\,\mu$m sapphire device at 2 GHz and various bias conditions from class AB to nearly class C. Arrows show the behaviour with decreasing gate voltages from $V_{GS} = -3.5$ V to $V_{GS} = -3.8$ V with step of 0.1 V. Flat gain, corresponding to class B condition, is obtained for $V_{GS} = -3.6$ V.

the typical behaviour shown in Fig. 8. This figure reports the ouput power and gain as a function of the input power, for a $2 \times 25\,\mu$m device with 4 different gate voltages applied chosen around a rough estimation of the pinch-off voltage, so as to bias the device from class AB to nearly class C. Class B can be identified as the bias condition for which a flat gain is obtained for low power condition, while in class AB or class C gain compression or expansion vs. input power is observed. Again in Fig. 8, observe that, when the power saturation is reached, the device ouput power is the same for all cases. Finally, note that the maximum output power is roughly the same for 1 mm devices from the two technologies, and this is because sapphire devices are fabricated with a more advanced technological process. The same performances improvements are therefore expected also in the most recent SiC-based devices, now under testing, fabricated with the same improved technology.

While the new SiC devices will be suitable for high power and highly linear applications, the sapphire devices already exhibit interesting properties. That indicates that, despite the poor thermal behaviour, they can be viable candidates for medium power applications, once operating in a high-efficiency class.

IV. Conclusions

An extensive power characterization of GaN-based HEMT devices from Selex has been presented. Devices fabricated both on SiC and sapphire substrates, with different layout have been considered. The characterization includes power sweeps and load-pull measurements at the fundamental frequency, from class A to class B. The active load-pull set-up already developed in Politecnico di Torino, has been ameliorated under many respects in order to meet the severe contraints, especially imposed by GaN HEMTs. Concerning the devices fabricated on SiC substrates, results show that $2 \times 100\,\mu$m devices biased in class A are capable of 5.7 W/mm in strong compression, and the PAE is as high as 35%. 1 mm devices from the same technology and with the same bias conditions, can deliver 3.2 W/mm, and the lowering of the output power has been traced back to the degradation of the DC current for the large periphery device with respect to the small one, probably due to heating effects. Measurements show that increasing the drain bias may result in negligible improvements of the output power if the DC dissipated power is too high. For next generation devices, one of the key issues will be the need of high efficiency operation (e.g. in class E or F). Characterization in these conditions will play a significant role. Sapphire based devices have been tested in class AB and class B conditions in order to lower the DC dissipated power. Despite the poor thermal behaviour, they exhibit 2.8 W/mm and can be viable candidates for medium power applications when in a high-efficiency class.

Acknowledgements

This work was partially supported by the Italian Ministry of University and Research through the PRIN 2003 project "GaN power HEMTs for wideband systems up to 30 GHz". Research reported here was performed in the context of the network TARGET–"Top Amplifier Research Groups in a European Team" and supported by the Information Society Technologies Program of the EU under contract IST-1-507893-NOE, www.target-net.org.

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