Organic chip packaging technology for high speed processor applications

Organic Chip Packaging Technology For High Speed Processor Applications

Bernd Garben, Andreas Huber, Dierk Kaller, Erich Klink
IBM Deutschland Entwicklung GmbH
Stefano Grivet-Talocia
Dipartimento di Elettronica, Politecnico di Torino

Abstract

The high dense interconnect (HDI) organic chip packaging technology has made rapid development advancements in the last few years. Due to the high dense wiring structures in the build up layers and newly also in the laminated core, high signal I/O applications and dense chip area array footprints can be supported. In the present paper the electrical characteristics of the HDI organic chip packaging technology are described with regard to signal and power integrity. In addition different applications for single-chip and multi-chip modules are discussed

Introduction

The evolution of the high dense interconnect (HDI) organic chip packaging technology has taken very fast development steps during the last eight years and a similar rapid advancement can be predicted also for the near future. While the first generation of the organic chip carrier technology was only capable to support wire bonded chips with very low signal I/O counts, the invention of build up layers with micro via-holes in 1992 attached to both sides of the laminated core, enabled this technology to facilitate also flip-chip applications with modest signal I/O counts. This technology is considered as the second generation (GEN 2). The standard card & board technology, used as chip carrier, is generally viewed as the first generation.

The third generation (GEN 3) of the organic chip carrier technology however has made a further significant jump ahead due the development of the fine line core technology. Table 1 shows the key factors of the technology roadmap spanning from the second to the third and finally to the predicted future generation. One key factor is the line width of the build up layers and core layers (w - in figure 1) and the second important factor is the via land size (V2 in figure 1). Table 1 shows the improvements in line width and the reduction of the core via land which is the main achievement factor of generation 3. The reduction of the core via land size is obtained due to the development of the fine line core technology. Figure 1 depicts the standard organic chip carrier technology of the second generation (GEN 2). On top and bottom of a laminated core, two fine line build up layers are processed. Figure 1 describes the cross section of a 2-2-2 structure. This means that 2 build up layers on top and 2 build up layers on bottom are applied on a laminated core consisting out of two layers.

The third generation (GEN 3) solves the disadvantage that the high wiring capabilities of the build up layers are not any more disturbed or even "disconnected" by the coarse core ground rules. The large core via land size (V) blocked the connectivity between the wiring in the top build up layers with the wiring in the bottom build up layers. In generation 3 (GEN 3) the fine line core technology has now achieved similar ground rules as the build up layers.

While generation 2 (GEN 2) was already used as single chip module for processor applications with modest signal I/O counts of several hundreds, the third generation (GEN 3) can support very high signal I/O counts with more than 1000 signals per chip. In addition also small multi-chip modules can be wired and some applications will be shown in this paper.

	GEN 2	GEN 3	Future
Line width BU/core [µm]	65/75	30/30	20/25
Via land BU/core [µm]	150/500	70/150	55/80

Table 1: Organic Chip carrier technology roadmap

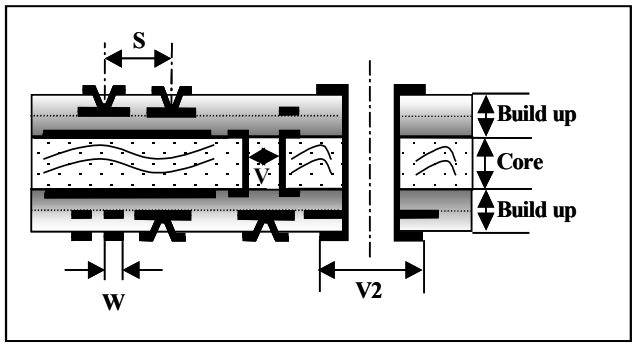

Figure 1: Organic chip carrier technology (2-2-2) Build up layers on laminated core

Electrical characteristics

Table 2 summarizes the trend of the key electrical parameters. The values of the dielectric constant reduce from 4.0 of today's build up layer and core materials to 3.0 in the near future. In addition the dielectric loss decreases by a factor of ten from 0.03 to the very low value of 0.003 for future core materials.

The impedance of the build up layers is below 50 Ohm for the second generation (GEN 2) and will increase to 50 Ohm. The impedance of the core layers is at 50 Ohm today and increases to values above 50 Ohm. It has to be emphasized that the characteristic impedance varies because of the decreasing spacing between lines.

	GEN 2	GEN 3	Future
ε – BU/core	4.0	3.5	3.0
tan δ – BU	0.03	0.02	0.01
tan δ – core	0.03	0.01	0.003
Z_0 BU/core [Ω]	40 / 50	50 / 50	50 / 55
NE Xtalk BU/core	1 / 6 %	5.5 / 8 %	6.5 / 9 %

Table 2: Summary of key electrical parameters

The coupling between adjacent lines increases continuously due to denser wiring. The saturated near end cross talk (NE X-Talk) values demonstrate this tendency. This behavior is similar to the on-chip wiring development, described in [2]. The maximum routing lengths is increasingly determined by cross talk effects.

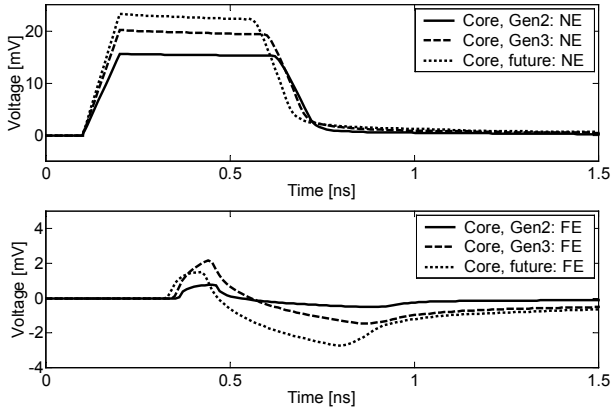

Figure 2a: Comparison of near end (NE) and far end (FE) coupled noise of a line pair with a parallel line length of 40 mm wired in the core layers.

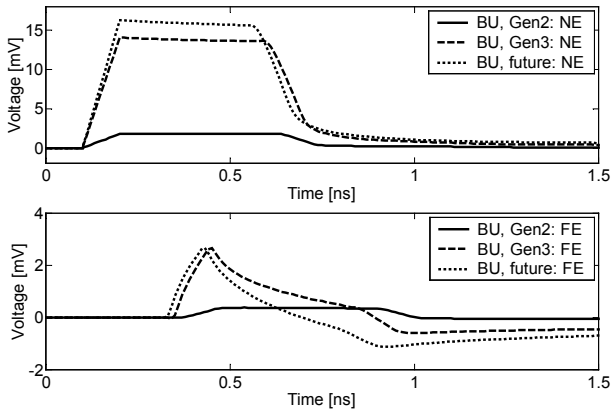

Figure 2b: Comparison of near end (NE) and far end (FE) coupled noise of a line pair with a parallel line length of 40 mm wired in the build up layers (BU).

Figure 2a and Figure 2b depict the cross talk analysis of a line pair with a parallel line length of 40 mm, a typical value valid for small multi-chip modules (for single-chip modules the dense parallel line length is significantly shorter). The voltage curves of near end (NE) and far end (FE) noise are shown for build up and core layers. The active line is connected to a 50 Ohm driver with a signal rise time of 100 ps and 500 mV swing. The results show that the near end (NE) and far end (FE) coupled noise values increase through the generations, because of the significant higher wiring density as shown in Table 2. Although the coupled noise values are not high, they have to be carefully taken into account during system design. This is achieved with a detailed system timing and coupled noise analysis including all coupling segments along the lines. To guarantee accuracy the transmission line models and the simulation algorithm must account for frequency dependent parameters.

Figure 3 describes the transmission eye for a 40 mm transmission line using a single rail (not differential) signal transmission scheme including coupling of one neighbor line. To achieve a proper signal transmission from the driver to the receiver, the criteria for the opening of the signal transmission eye is a minimum of the half bit time. This means for a bit time of 100 ps (10 GHz) an opening of 50 ps is needed. The vertical height for this eye is defined by the used receiver technology. It has to be noted that this criteria does not define the highest possible transmission frequency for the transmission channel, but is used as a simplified standard rule.

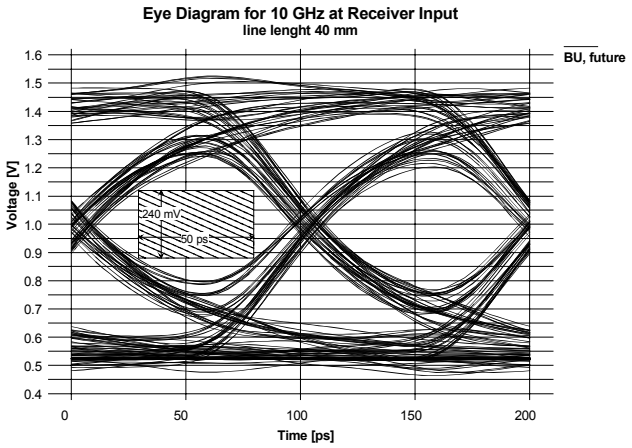

Figure 3: Eye simulation with opening criteria for secure signal transmission (min width = 50ps, min. amplitude = ±120 mV)

There exist additional transmission circuit methodologies and schemes, such as driver predistortion, channel equalization, coupled noise cancellation and others, which increase the bandwidth per channel further. However these methods are not described in this paper.

In Table 3 the timing and noise simulation results for the eye opening are listed for the technology generations with a cycle time of 100 ps. Due to increasing noise and

especially increasing attenuation the eye opening decreased going to smaller line dimensions.

Eye opening @ ±120 mV	BU GEN 2	BU GEN 3	BU Future
	59 ps	55 ps	50 ps

Table 3: Comparison of eye opening for a 40 mm long line wired in BU layers at 10 GHz.

Figure 4 and 5 describe the details of the mid frequency power noise analysis. Figure 4 shows the equivalent subcircuit model applied for the power noise analysis. The elements C1,R1 represent a portion of the on-chip decaps. The elements L2, C2, R2 represent a section of the on-module capacitors and L3,C3,R3 depict a portion of the on-card capacitors. The inductances L5,L6 are schematically inserted and describe the effective loop inductance of the V/GND planes and via-holes on the module and on the card, connecting to the on-module and on-card capacitors respectively. The resistances (r5,r6) and the capacitances (C5,C6) also belong to these planes. Actually the total power distribution network is modeled by a 3D field solver which supports EM wave propagation through the multi-layers. The current sources i(t) represent synchronously switching on-chip currents.

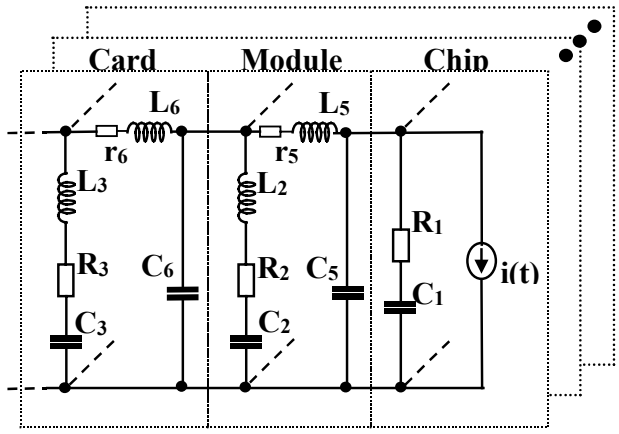

Figure 4: Equivalent subcircuit for mid frequency power noise analysis.

Figure 5 shows the results of the mid frequency power noise analysis comparing the technology of the first generation with the technology of the second generation. Due to the much less effective V/GND loop inductance which connects the on-module decaps to the chip, the power noise is significantly reduced by more than 40 % . The smaller effective loop inductance is achieved by the thin insulation build up layer, which separates the voltage and the GND planes. As the dielectric thickness of the build up layers continues to decrease from generation 2 to generation 3, the mid frequency power noise is further reduced.

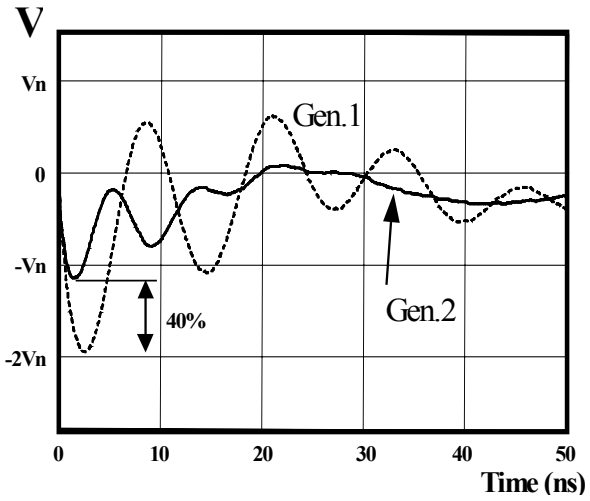

Figure 5: Mid frequency power noise analysis. Comparison of GEN 2 with GEN 1

Processor packaging applications

The second generation of the HDI organic chip packaging technology is used for medium dense chip I/O single chip module applications as e.g. I/O chip sets and processors. With the introduction of generation 3 the applications will be extended to high I/O single chip modules with very dense area array flip chip footprints. These chip footprints will have bump pitches below 200µm. Figure 6 shows a typical application. The single chip module technology can either consist out of a multi-layer fine line core with or without build up layers on top and bottom side of the core. In this case the off-module connections are provided with the solder ball connects.

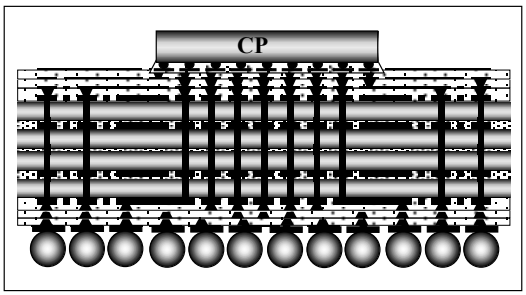

Figure 6: Single Chip Module application with fine line core technology and build up layers

Figure 7 describes an extension of the technology capabilities by using the module back side for on-module decaps. If these mid frequency decaps are assembled in a core pocket as shown in Figure 7, the effective V/GND loop inductance is further reduced by the short distance to the chip and by the high number of V/GND via-holes. This leads to a further reduction of the mid frequency power noise. (see Figure 5)

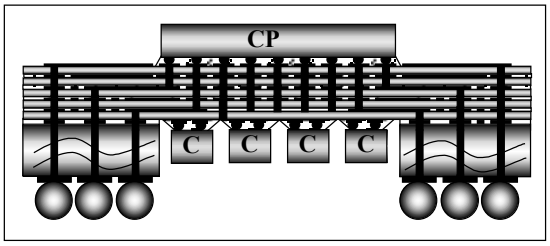

Figure 7: Double sided Single Chip Module application with fine line core technology and on module decaps on module back side embeded in core pocket.

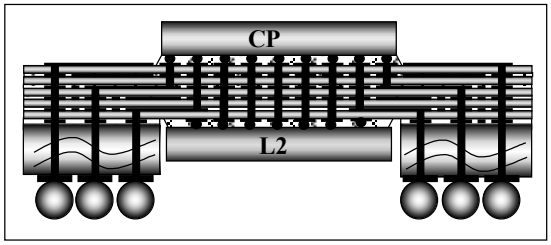

Figure 8: Double sided Multi-Chip Module application with fine line core technology. L2 cache chip embedded in core pocket on module back side.

The third generation of the HDI organic chip packaging technology can also support small multi-chip module applications due to the high wiring capabilities. The classical multi-chip module is realized by assembling two chips side by side close to each other on the top side of the module. A typical application can consist out of the processor chip and its private L2 cache chip.

Also more than two chips can be applied on the top surface of the multi-chip module, as long as they can be supported by the wireability of the layers and the thermal, the assembly and rework requirements.

Figure 8 shows a specific multi-chip module application by using a cavity in the core for the back side mounted L2 cache chip. Due to the dense vertical structure, the chip to chip signal and power connections are basically only stacked via-holes through the build up layers or fine line core layers. The extremely short signal path, supports a very high speed interface. This structure can basically support the processor cycle speed as CP-L2 interface performance. The high number of signals with the fast cycle time leads to a very high bandwidth.

However to support this structure the chip footprints of the processor and L2 chip have to be optimized towards each other. A high number of V/GND bumps and via-holes can also help to achieve a single sided cooling system.

Conclusions / Summary

The characteristics and benefits of the HDI organic chip packaging technology have been demonstrated. It has been shown that the third generation has superior characteristics with regards to wireability. Therefore large and dense chip footprints can be supported. This will lead to high signal I/O count single-chip and small multi-chip module applications.

The results of the electrical signal integrity analysis revealed cross talk values which are not very high, but they have to be controlled carefully during the system design. The mid frequency power noise analysis displayed significantly reduced values.

References

[1] Tummala, R. R., Microsystem Packaging, McGraw-Hill (New York, 2001), pp. 321. [packaging fundamentals …]

[2] Winkel T.; Kaller D. ; Huber A.: "Determination of Critical Line Length for On-Chip Interconnects for the Future Technologies as predicted in the SIA Roadmap", 4th IEEE Workshop on Signal Propagation on Interconnects, 2000