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Development of Demonstrator Kit for designing Practical EMC Compliant System / Kye Yak, See; Oswal, M.; Khan ngern, W.; Canavero, Flavio; Christopoulos, C.; Grabinski, H.. - STAMPA. - 1:(2005), pp. 179-187. (Intervento presentato al convegno 7th Electronic Packaging Technology Conference (EPTC 2005) tenutosi a Singapore (SINGAPORE) nel Dec. 7-9, 2005) [10.1109/EPTC.2005.1614391].

Availability:
This version is available at: 11583/1409451 since:

Publisher:
IEEE

Published
DOI:10.1109/EPTC.2005.1614391

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12 October 2024

Development of Demonstrator Kit for designing Practical EMC Compliant System

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Abstract

Electronic designers can timely design reliable and electromagnetic compatibility (EMC) compliant electronic systems if they focus on lowering emission levels from subsystems during design and development phases. In this paper practical design rules, which designers should adhere to produce an EMC compliant system, are explained and their effects are demonstrated with the help of a demonstrator kit.

1. Introduction

It is not uncommon for electronic designers to fix electromagnetic interference (EMI) issues in product after development phase. Fixing EMI issues late in the development phase is both time consuming and cost ineffective. Instead if designers during design phase focus on lowering emission level from subsystems then they could timely produce a reliable system that meets the international regulatory EMC specifications [1-3]. For example, an information technology equipment (ITE) whose radiated and conducted emissions level should not exceed CISPR-22 Class B limit [4].

In this paper, fundamental design rules, which designers should adhere to produce an EMC compliant system, are explained. Effects of following and not following these rules are demonstrated with help of an EMC design Demonstrator kit. The EMC design demonstrator kit consists of two versions of "mock-up" digital electronic product. With the backing of EMI measurement results, practical EMI suppression design techniques for a typical electronic product are explained and demonstrated.

2. Demonstrator Kit

The demonstrator kit consists of a poorly designed version and a well designed version of a "mock-up" electronic product. Like any typical electronic product, it has an AC inlet for AC power supply. The AC power is converted to low voltage DC power through a switched-mode power supply (SMPS). The DC power is then fed to a printed circuit board (PCB) that holds high-speed digital circuitry. The High-speed digital circuitry is interfaced with an external PCB, which contains resistive load, by a 1.5m shielded cable. Finally, a 30cm x 22cm x 12cm Steel casing encloses the PCB and the SMPS, as shown in Fig. 1.

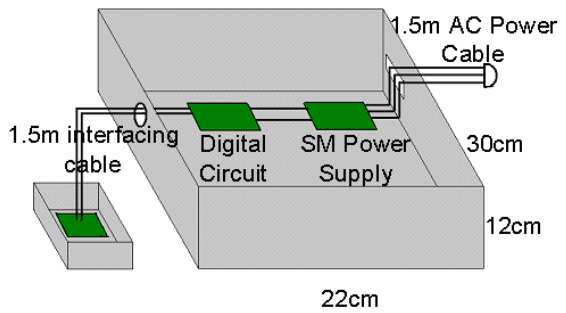


Figure 1: Complete Digital Electronic System

In order to explain design rules for designing PCB with low radiated emissions, two versions of PCB layout are designed for a simple digital circuit shown in Fig. 2. The digital circuit is designed to realistically represent a typical digital circuit, which consists of many IC gates running at different clock speeds.

Moreover, effect of interfacing cable on radiated emissions is studied in detail for implementing an effective interfacing solution which significantly lowers radiated emissions from interfacing cable. In addition, to explain guidelines for designing effective shielded enclosure, which sufficiently attenuates, radiated emissions from the enclosed digital circuit and switch mode power supply, two versions of Steel casing are designed and studied in detail. Finally, to develop design methodology for designing effective power line EMI filter, which reasonably attenuates conducted emission from the SMPS, two versions of power line EMI filter are designed and investigated in detail. The complete electronic system is carefully designed and packaged so that the contrast of EMI results between two version's PCB layout, interfacing techniques, shielding and power line EMI filter clearly explains the effectiveness of proper design guidelines to achieve low levels of radiated and conducted emissions.

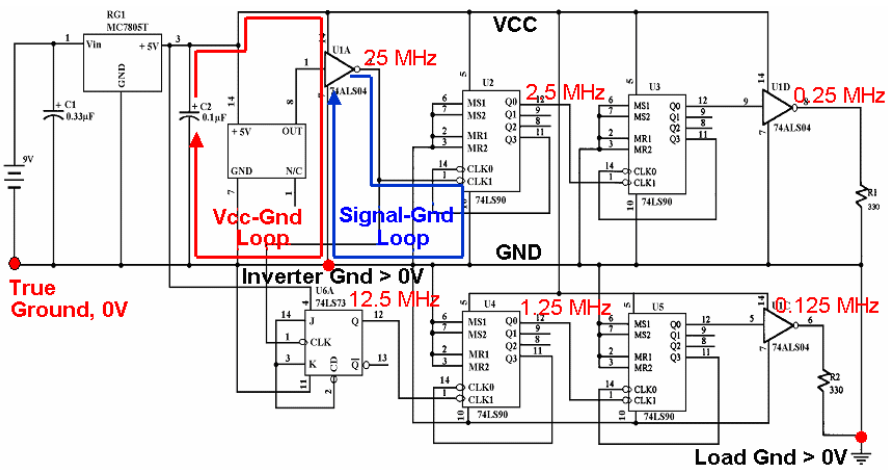


Figure 2: Simple Digital Circuit

3. Subsystem Comparison

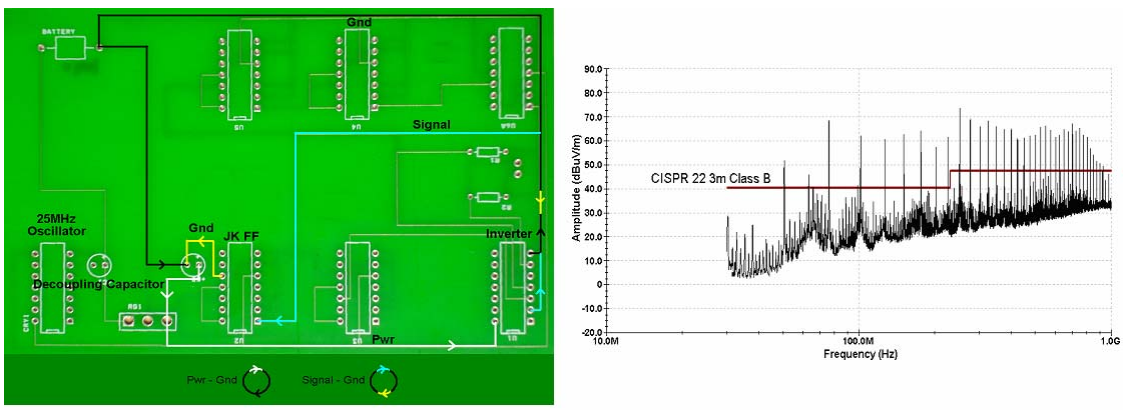
3.1 PCB Layout

In any electronic system PCB is the main source of emission and that's why it is critical to design a low radiating PCB [5-6]. In this section design rules to design a low radiating PCB are identified and their theoretical basis are explained by analyzing both poorly designed and well designed PCB layouts.

The digital circuit shown in Fig. 2 will be laid on single-layered double-sided PCB. Two versions of PCB layouts are implemented. The digital circuit is powered by 5V DC supply and the inverter (U1A) is switching at 25 MHz.Fig. 3a shows the poorly designed PCB layout. The PCB layout has power, ground and signal traces that are far apart. The IC gates and components are scattered across the PCB. A close look at the PCB layout reveals that it has large a Power-to-Ground loop between decoupling capacitor and inverter (U1A) and a large Signal-to-Ground loop between inverter (U1A) and JK

Flip Flop (U2). These large Power-to-ground and Signal-to-ground loops give rise to excessive level of radiated emissions, which is usually called the differential-mode radiation. Moreover, these large loops result in large inductance in the return current paths, which produce large ground bounce and cause the poorly designed PCB to emit common-mode radiation. In summary, large Power-to-ground and Signal-to-ground loops lead to high levels of differential-mode and common-mode radiation. The measured radiated emission emitted by the poorly designed PCB is shown in Fig. 3b, which clearly exceeded the CISPR 22 Class B limit.

To reduce radiated emission from the PCB, the IC gates and components are placed closer together to avoid large power/signal to ground loops. To further reduce the sizes of power/signal to ground loops, a ground plane is used. Fig. 4a shows the well-designed PCB layout. Unlike the case of poorly designed PCB layout, the well-designed PCB layout has a much shorter power trace from decoupling capacitor C2 to inverter (U1A) and the ground plane just below the power trace provides an immediate return path. Also, current on the short signal trace from inverter (U1A) to JK FF (U2) also returns on the ground plane and forms a small signal-ground loop. The small power/signal to ground loops radiate significantly less compared to the loops in poorly designed PCB layout. Small loop areas also reduce ground bounce hence common-mode radiation is also low. Radiated emission from the well-designed PCB layout (Fig. 4b) is comfortably below CISPR-22 Class B limit owing to strongly coupled and shorter power/signal and ground paths.



a b

Figure 3(a) Poorly Designed PCB Layout; (b) Radiated Emission from Poorly Designed PCB

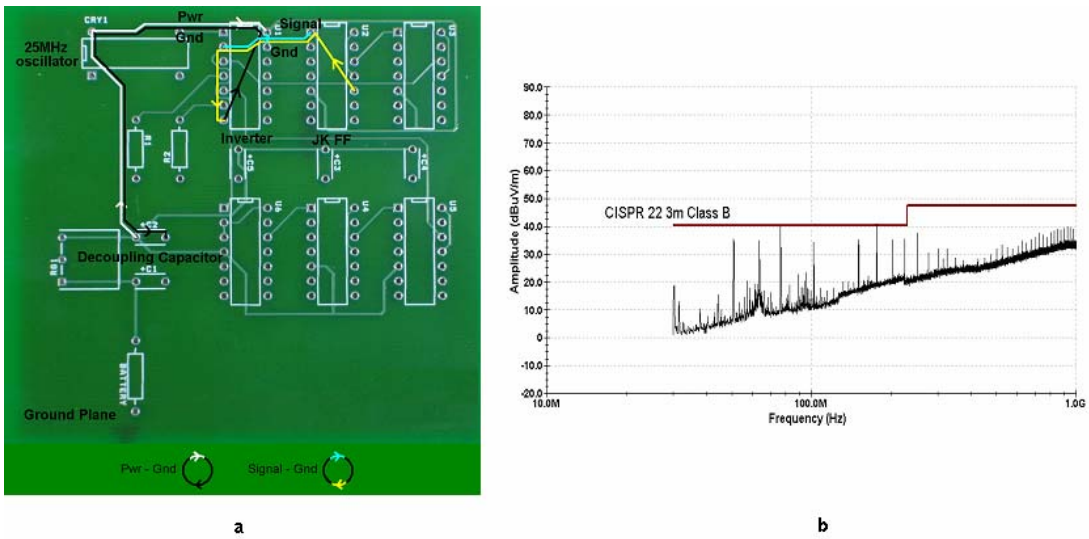


Figure 4(a) Well Designed PCB Layout; (b) Radiated Emission from Well Designed PCB

3.2 Interfacing Cable

Just like in case of PCB, interfacing cable radiate because of large Signal-to-Gnd loop (DM Radiation) and due to large voltage bounce across the interfacing cable (CM Radiation).

In order to study effect of interfacing cable on radiation level, 1 KΩ resistive loads were mounted on an external PCB and were interfaced to the test circuit by a 1.5m shielded interfacing cable. Two signal lines 0.25MHz and 0.125MHz and a ground line were interfaced between digital circuit and external PCB.

Fig. 5a shows radiation emission from poorly designed PCB without interfacing and with interfacing. Intituively, interfacing cable will radiate when high speed signal flows through signal lines and return on ground line. Theoretically, interfacing cable will radiate both DM and CM radiation. DM radiation is due to loose coupling between signal and ground lines. And CM radiation is due to CM current flowing through the signal and ground lines. Fig. 5b shows that average 60 dBuA CM current flows through the lines. This CM current is high enough for cable to emit high levels of radiation. CM current through the cable flows when the 1.5m long “wire-antenna” is powered by a high voltage bounce [7]. Fig. 5c shows that ground bounce voltage at the PS2 connector is max 202.35mV instead of ideal “0V”. This high ground bounce powers the cable and gives rise to CM current which in turn emits high level of radiation from the cable.

Previous analysis explains that in order to lower radiation level from the cable, grounding of the connector and blocking unwanted high frequency noise from flowing into the cable is critical.

In case of well-designed PCB, PS2 connector is placed close to battery so that it is properly grounded and ferrite core and bypass capacitors are used to block unwanted high frequency noise from flowing into the cable. Fig. 6 shows the implemented solution to lower radiation from interfacing cable. Bypass Capacitor of 20nF and 5nF are chosen so that unwanted high frequency noise is sufficiently bypassed to ground without affecting the operation of the circuit or distorting the signals. By means of measurement it was found that bypass capacitors were effective in bypassing noise to ground only over 30MHz to 100MHz frequency range. Hence to lower radiated emission above 100MHz ferrite core was fastened to the cable at a point close to the connector. Fastening ferrite core near the connector most effectively lowers emission from the rest of the cable by absorbing emission from the cable right at the point of origin of emission.

Fig. 7a shows that after implementing the solution radiation level lowers by average 15dB. Fig. 7b shows effect of the solution on the CM current which after the implementation drops to average 40 dBuA. And Fig. 7c shows that ground bounce experienced by connector has dropped to only 1mV becuause of placing the connector close to the battery.

Implemented solution shows that proper grounding of connector and blocking of unwanted frequency signal from flowing into the cable is effective in lowering radiation emission from the cable.

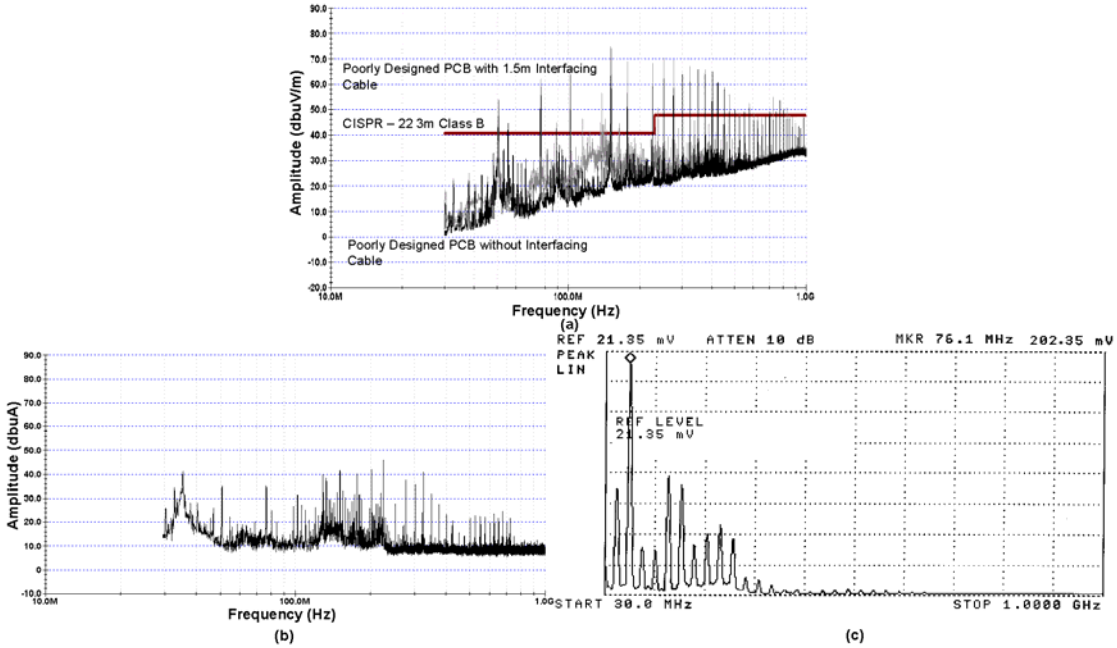


Figure 5(a) Radiation Emission from Poorly Desiged PCB with and without Interfacing Cable; (b) CM Current flowing through Interfacing Cable; (c) Ground Bounce at the Connector

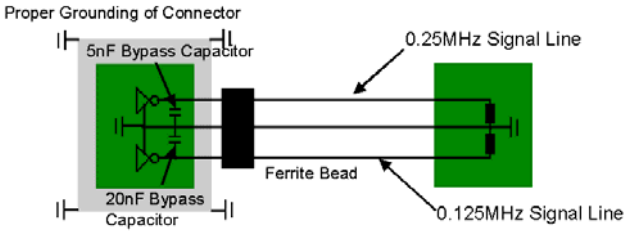


Figure 6: Implemented fix to reduce Radiated Emission from Interfacing Cable

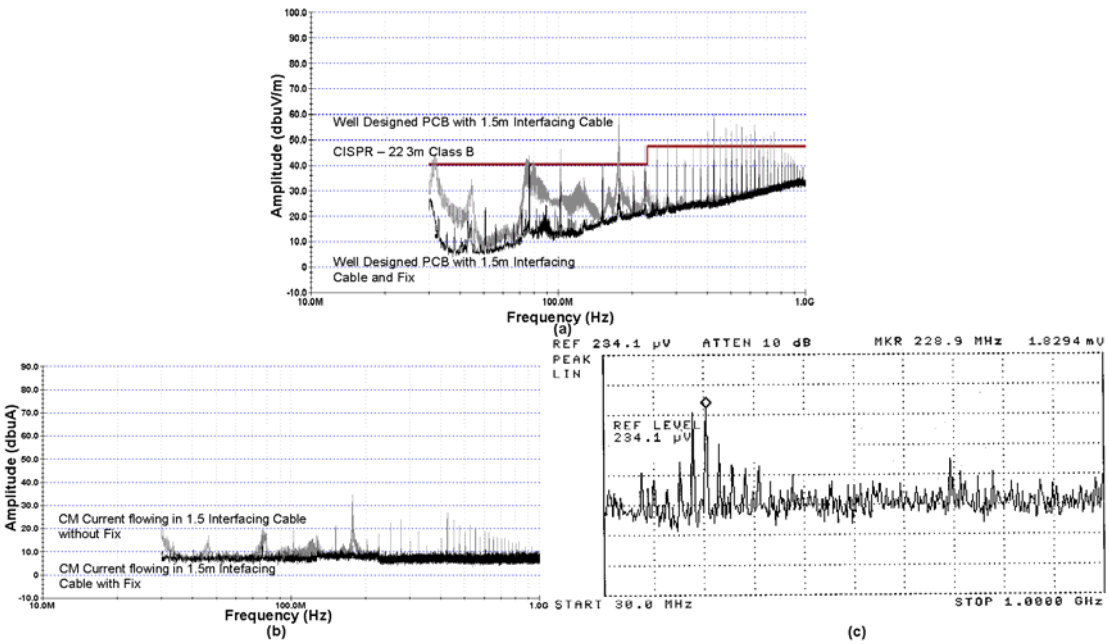


Figure 7(a) Radiation Emission from Well Desiged PCB with Interfacing Cable and with Fix; (b) CM Current through Interfacing Cable without and with Fix; (c) Ground Bounce at the Connector

3.3 Shielding

The metallic casing that encloses high-speed electronic system serves as a good EMI shield if properly designed [8]. A properly designed shielded enclosure should meet both thermal flow and EMI shielding requirements.

Fig. 8a shows the poorly designed shielded enclosure that only considered the ventilation needs. It has 3 long slots of length 25 cm and thickness 0.3 cm for effective ventilation. Fig. 5b shows the shielding effectiveness of the casing calculated using an EM simulation tool (Flomeric's FloEMC software). The shielding effectiveness (SE) is rather poor, especially at slot resonant (570 MHz) and cavity resonant (950 MHz and 1500 MHz) frequencies and the average SE over the frequency range is around 10 dB.

The cavity resonant frequencies can be estimated by:

$$fr_{cavityLMN} = \frac{c}{2}\sqrt{\left(\left(\frac{L}{length}\right)^2 + \left(\frac{M}{width}\right)^2 + \left(\frac{N}{height}\right)^2\right)}$$

where c is speed of light (3×10^8 m/s), L,M and N are positive integers to represent resonant modes (TEM/TE/TM modes) and only one of them can be 0 (e.g. f_{110}, f_{011}, f_{101}).

It is apparent that a big casing exhibits resonant behavior at lower frequency compared to a small casing, therefore first rule is to design just big enough casing to accommodate complete system.

Slot or aperture resonant frequency can be estimated by:

$$fr_{slot} = \frac{c}{2d}$$

where c is speed of light (3×10^8 m/s) and d is slot length or hole diameter in m.

It is obvious from the formula that a long slot or large aperture resonates at low frequency. Therefore they degrade SE although they provide effective ventilation.

To design a casing with high SE which also provides reasonable ventilation, first estimate lowest cavity resonant frequency of the shielding using the cavity resonant formula mentioned above. Normally, it is not possible to shift cavity resonant frequency to higher frequency because it mostly depends upon dimension of the shielding. Hence, designer can only choose dimension of openings so that they resonate at much higher frequency than lowest cavity resonant frequency. After choosing resonant frequency of the slot/aperture, calculate its dimension using the slot/aperture resonant frequency formula given above. And finally estimate SE at frequency range of interest to ensure that shielding is enough to attenuate high level of radiated emissions from electronic system.

Fig. 9a shows the well designed shielded enclosure. Unlike poorly designed shielded enclosure mentioned earlier, it has many small ventilating holes of 4.5 mm diameter. The calculated resonant frequency of the 4.5 mm hole is 33 GHz. Fig. 6b shows the SE of the well designed shielded enclosure. Even at cavity resonant frequencies SE is around 30 dB. SE is higher compared to poorly-designed shielded enclosure because of much smaller hole-size which resonates at much higher frequency than our frequency of interest (30 MHz to 1.8 GHz). Hence, to meet the ventilation needs and to ensure sufficient SE, enclosure with large number of smaller holes is a better option than small number of long slots.

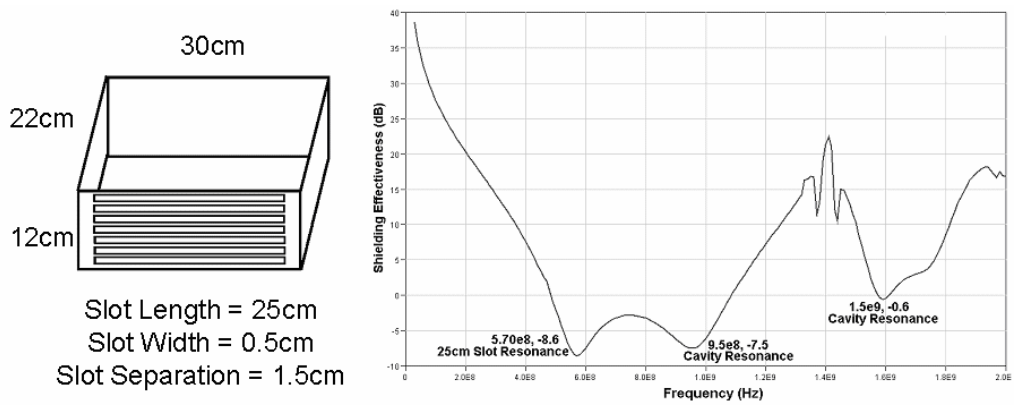


Figure 8(a) Poorly Designed Shielding; (b) Shielding Effectiveness of Poorly Designed Shielding

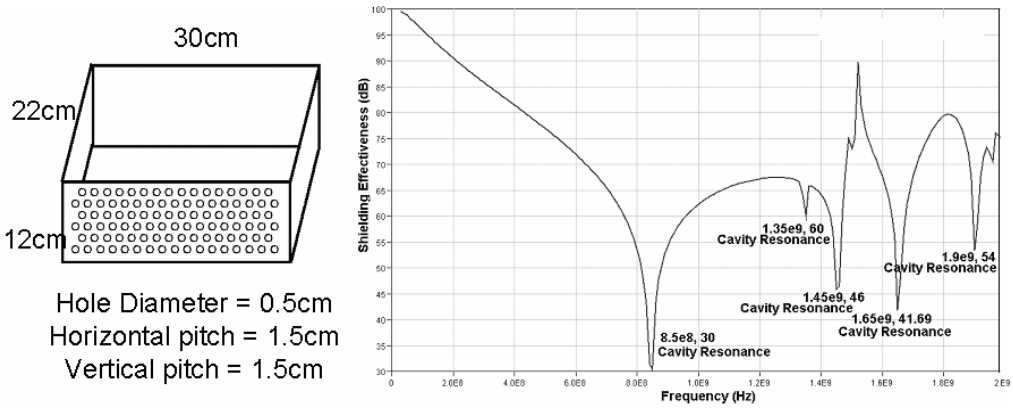


Figure 9(a) EM Compliant Shielding ; (b) Shielding Effectiveness of EM Compliant Shielding

3.3 Power Line EMI Filter

Power line EMI filter is used to attenuate conducted noise generated from SMPS. In this section procedure to design an effective power line EMI filter, which attenuates conducted noise on live and neutral power lines below CISPR-22 Class B limits, will be explained. A commercially available SMPS, model VTM 23WB is used for demonstration purpose.

To design an effective power EMI filter, it is essential to find out which mode of conducted noise should be targeted and at what frequency range. With line impedance stabilization network (LISN) and mode-discrimination network, the conducted emissions from the SMPS without power line EMI filter are measured. The measured results in Figs. 10a and 10b show that DM noise dominates in the frequency range 150 kHz to 10 MHz while CM noise is already lower than the limit. Hence, more attention should be paid to reduce the DM noise.

The frequency range of interest (150 kHz to 30 MHz) is split into three frequency bands, 150 kHz to 1 MHz, 1 MHz to 5 MHz and 5 MHz to 30 MHz. Appropriate CM choke, X2 Capacitor (between Live and Neutral) and Y2 capacitors (Live/Neutral to Earth) are properly chosen so that sufficient CM and DM filter attenuations can be achieved in the three given frequency bands. The leakage inductance (DM inductance) of the CM choke and X2 capacitor provide the necessary DM attenuation. The CM inductance of the CM choke and the Y2 capacitors provide the necessary CM attenuation, as shown in Fig. 11.

Table 1 tabulates the chosen CM choke, X2 and Y2 capacitors and their effective frequency ranges.

Frequency Band	Component	Effective Range
150 kHz to 1 MHz	X2 Capacitor, C1(0.33uF) + CM Choke, CM1 Y2Capacitor, C2/C3(0.0047uF) + CM Choke, CM1	Around 35.78 KHz Around 200 KHz
1 MHz to 5MHz	Common-Mode Choke, CM1 (Sumida UU16LF402) L_{CM}=4mH, L_{DM}=60uH	500KHz to 5MHz (DM operation)
5 MHz to 30 MHz	Y2 Capacitor, C2/C3 0.0047uF	> 5 MHz

Table 1: EMI filter Components

The power line EMI filter is incorporated in the SMPS and conducted emissions are measured. Figs. 12a and 12b prove the effectiveness of the designed EMI filter as it attenuates DM and CM conducted noise to reasonably low level with respect to CISPR-22 Class B limits.

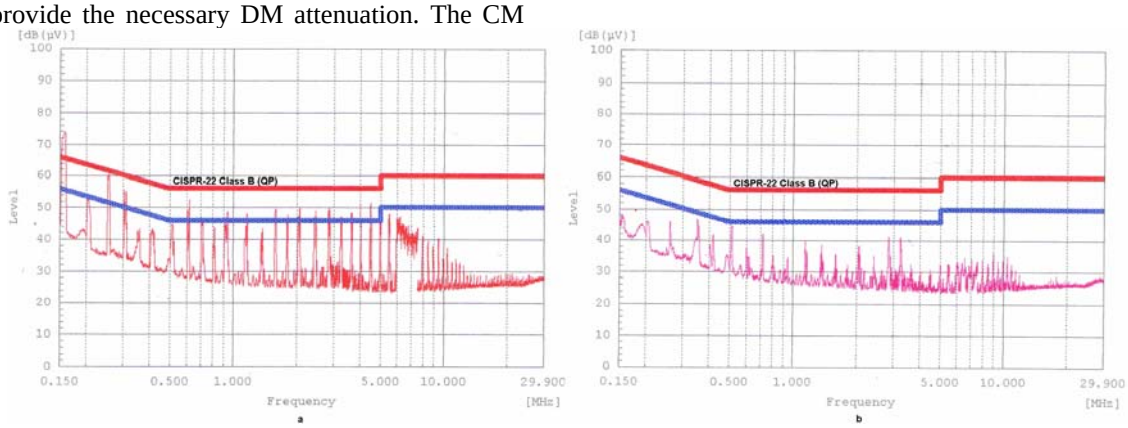


Figure10(a) Differential-Mode conducted noise from SMPS without EMI filter; (b) Common-Mode conducted noise from SMPS without EMI Filter

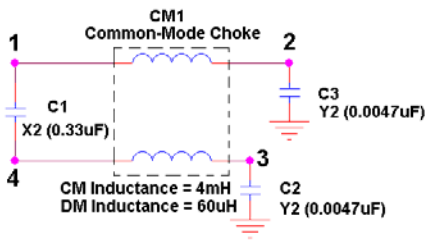


Figure 11: Power Line EMI Filter

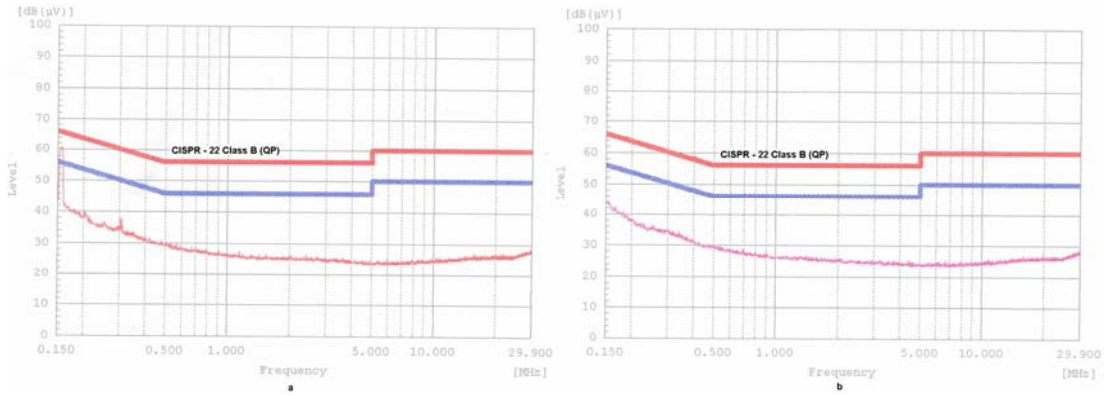


Figure 12(a) Differential-Mode conducted noise from SMPS with EMI filter; (b) Common-Mode conducted noise from SMPS with EMI Filter

4. Complete Electronic System

In this section all the subsystems are integrated to give a complete electronic system. The first electronic system is integrated and packaged from poorly designed subsystems. Another electronic system is made of well designed subsystems.

Fig. 13(a) shows the poorly designed electronic system. Although its poorly designed PCB, ,improper interfacing, poor shielding and SMPS with no EMI filter are enough to make the system fail the EN 55022 Class B EMI limits, there are other poor packaging practices, which make the EMI results even worst. Firstly, long DC supply cable from SMPS to digital circuit emits CM radiation because of large voltage bounce across the cable due to long cable's inductance and rapidly switching current flowing through it. Moreover, the long AC cable of the SMPS running over the oscillator picks up noise from the 25 MHz oscillator. It increases the conducted emission at the higher frequency band. Effects of long supply cables and mains cable over oscillator and 1.5m interfacing cable are apparent in radiated emission test results in Fig. 12 and conducted emission test results in Figs. 13.

Fig. 13(b) shows the well-designed electronic system with proper PCB layout, effective interfacing solution, good shielding design with CuBe gaskets and well-filtered SMPS. The SMPS is placed closed to AC power input and the PCB so that the DC supply wires and mains cable can be made very short. Radiated and conducted emissions are shown in Figs. 14, 15 and 16 respectively.

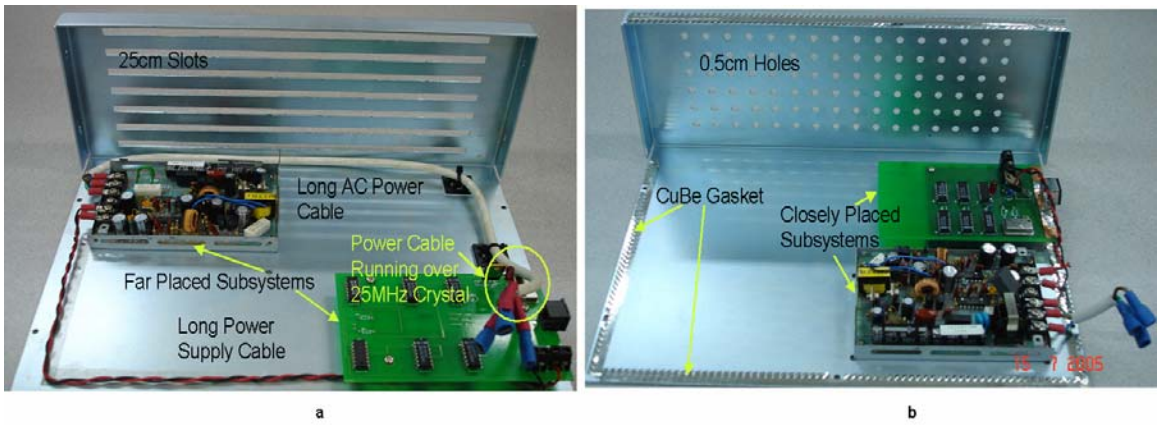


Figure 13(a) Poorly Designed System; (b) EMC Compliant System

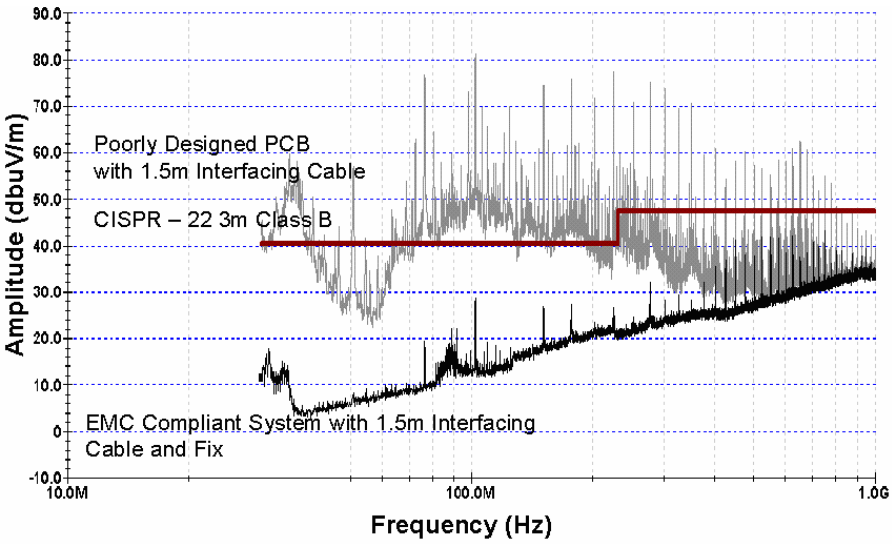


Figure 14: Comparison of Radiated Emission from Poorly Designed and EMC Compliant System

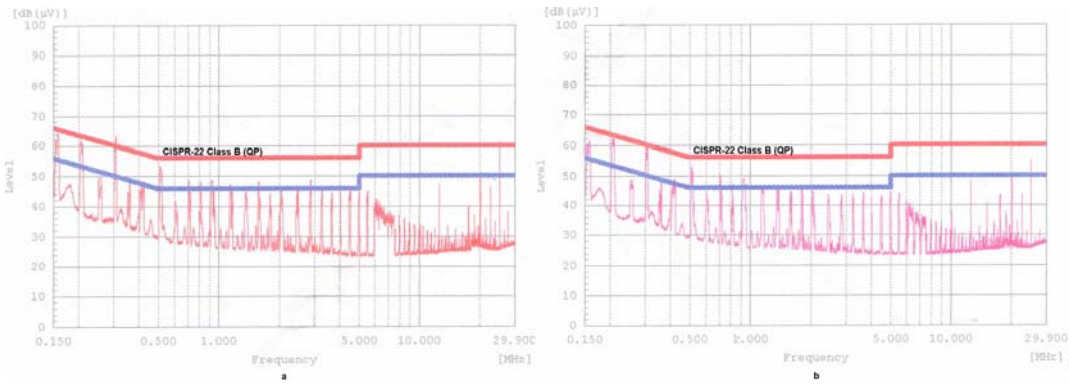


Figure 15(a) Conducted noise from Poorly Electronic system on Main's Neutral line
(b) Conducted noise from Poorly Electronic system on Main's Live line

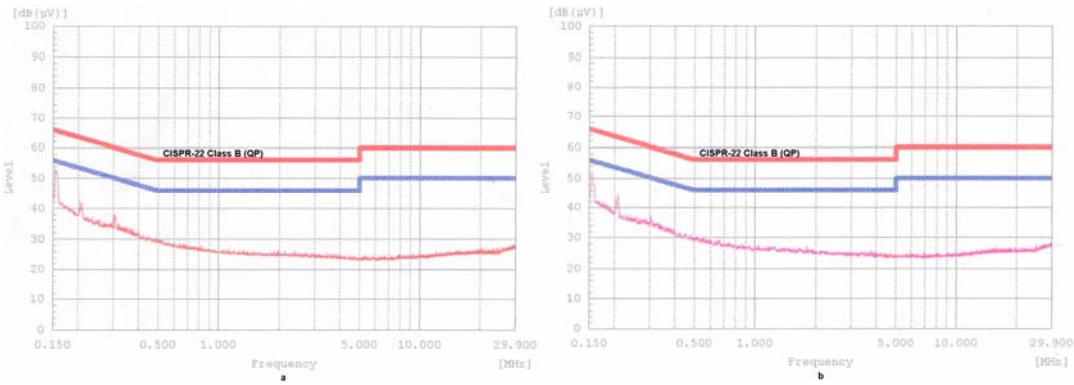


Figure 16(a) Conducted noise from Well-designed Electronic system on Main's Neutral line
(b) Conducted noise from Well-designed Electronic system on Main's Live line

Conclusion

With the EMC design demonstrator kit, practical EMC design guidelines to design PCB layout, Interface, Shielding and Power Line EMI filter were explained and demonstrated experimentally. These fundamental design rules are essential for System Designers to timely produce reliable and EMC compliant electronic systems.

Acknowledgement

The authors wish to acknowledge the funding support from the European Commission under the ASEAN-EU Universities Network Programme (AUNP). For more details on the project please visit www.aunp-emctraining.polito.it.

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