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Macromodeling strategy for digital devices and interconnects

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Abstract

This paper proposes a macromodeling approach for the simulation of digital interconnected systems. Such an approach is based on a set of macromodels describing IC ports, IC packages and multiconductor interconnect structures in standard circuit simulators, like SPICE. We illustrate the features of the macromodels and we demonstrate the proposed approach on a realistic simulation problem.

1 Introduction

The simulation of board-level interconnected systems is an important resource for the assessment of Signal Integrity (SI) and ElectroMagnetic Compatibility (EMC) issues in fast digital circuits. It requires efficient and accurate simulation tools, able to handle large structures and to allow for the higher order effects (as the nonlinear and dynamic behavior of interconnect terminations) caused by fast digital signals.

The main parts composing a board-level interconnected systems are pointed out by the block diagram of Fig. 1. The system is composed of a set of digital Integrated Circuit (ICs) output ports (*drivers* hereafter), possibly enclosed in a package, that drive a multiconductor interconnect structure loaded by the input ports of other ICs (*receivers* hereafter) and by their packages.

These systems can be effectively handled by standard circuit simulators, provided that each of their parts is represented by a suitable (linear or nonlinear) multiport element (*macromodel* hereafter). In this paper, we outline a complete set of macromodels for drivers, receivers, packages and interconnects, that allow the simulation of most real interconnected systems with reduced computational efforts and an high accuracy level.

2 Block macromodels

This section describes the proposed macromodels. The macromodels of drivers, receivers and packages are of behavioral type and are obtained by estimating suitable parametric models from the responses of the devices under modeling. The interconnect macromodels are instead built from the transmission line equations via rational approximations of the parameters. Every model is eventually cast as a set of first order ordinary differential equation (differential-difference equation for electrically-long interconnects) and implemented as an equivalent RC circuit with controlled sources.

Figure 1: Main parts of a generic board-level interconnected system. **D**: drivers; **PKG**: packages; **LINE**: interconnect; **R** receivers.

2.1 Drivers

In the parametric-behavioral approach, the modeling of drivers amounts to relate their port voltage and current by a suitable parametric equation. The equation (or model representation) must be nonstationary, in order to take into account the port logic state and state transitions. For this problem, we obtain the best results by the following discrete-time piece-wise representation:

$$i_{\rm out}(k) = w_1(k) f_1(k) + w_2(k) f_2(k) \qquad (1)$$

where $i_{\rm out}$ is the output port current expressed as a combination of two submodels f_1 and f_2 with weight coefficients w_1 and w_2. Submodels f_1 and f_2 describe the behavior of the driver when its output is in the High and the Low logic states, respectively, whereas w_1 and w_2 describe state switching. Submodels f_1 and f_2 are nonlinear dynamic parametric models based on the theory of Radial Basis Functions (RBF) [1]. They are linear combinations of Gaussian functions whose arguments are the past r samples of the port current $i_{\rm out}$ (r is the dynamic order of the model), and the present and past r samples of the port voltage $v_{\rm out}$. Each basis function is properly centered in the space of the voltage and current sequences and its amplitude decreases with the distance of the actual sequence from the function center.

The estimation of model (1) is carried out by a simple procedure [2] and is done by matching the output of the model to the output of actual drivers for suitable input signals [3, 4]. The whole modeling process has been developed and validated by applying it to several transistor-level models of commercial devices [2]. Besides its operation on actually measured waveforms has been demonstrated in [5].

2.2 Receivers

The development of receiver behavioral models is rather straightforward because, in contrast with output ports, their operation is hardly influenced by the IC internal states. For input port voltages in the range of power supply, receivers exhibit a mainly linear capacitive behavior, whereas outside such a range their behavior is dominated by the nonlinear protection circuits. This property and the physical structure of receivers suggest the following model representation

$$i_{\mathrm{in}}(k) = i_l(k) + i_{nl}(k) \tag{2}$$

where i_{in} is the current flowing into the input pin, and i_l and i_{nl} are a linear and a nonlinear submodel, respectively. As a linear submodel we use an AutoRegression with eXtra input (ARX) parametric model [6] defined by the linear combination of the present sample of the port voltage v_{in}, and the past r samples of v_{in} and i_{in} (again r is the order of the model). Submodel i_l is estimated by standard routines [4, 7] from suitable identification signals, that are obtained by driving the receiver with a multilevel voltage waveform spanning the range of the power supply. As a nonlinear submodel we use a two-piece RBF parametric model, that takes into account the contribution of the nonlinear protection circuits for v_{in} outside the power supply range. Such a choice yields receiver models operating at a good accuracy level. Details on the estimation of the outlined receiver models and on the assessment of their accuracy are in [2].

It is ought to remark that a simple receiver model composed of a shunt capacitor C_{eq} and a shunt nonlinear resistor belongs to the class defined by (2), as well. However such a basic model offers only a rough approximation of the device behavior, whereas the proposed model performs at a good accuracy level regardless of sources driving the receiver.

2.3 Package

Packages usually have a complex geometry with discontinuities and several adjacent conductors. This calls for either a full-wave characterization or a direct measurement. We turn the scattering characteristic obtained by full-wave simulations or measurements into lumped equivalents by estimating their poles. The sought poles are those contained within the modeling bandwidth and the estimation methods we use are either the Block Complex Frequency Hopping (BCFH) method [8, 9] or the Subspace-based State-Space System Identification (4SID) methods [10]. This approach identifies an approximate lumped multiport through a set of rational transfer functions characterized in terms of poles and residues through partial fraction expansion. Once the poles have been estimated, the residues are computed by least squares fitting the function samples. The models obtained with this approach have a solid physical foundation, because their poles are approximations of the actual poles of the modeled multiport element. This guarantees the stability of estimated models and helps the control of their passivity [11].

We tested the pole-estimation approach on both ideal multiport elements, composed of transmission lines and lumped parts, and on actual package structures, whose transient responses are computed by full-wave methods [12]. For both types of test structures, we obtain good models reproducing the scattering behavior of the original junctions over several GHz wide bandwidths. We also find that possible delays comparable to the rise/fall time of waveforms do not reduce significantly the performances of the exploited pole-estimation methods.

2.4 Interconnects

In order to take into account possible propagation effects experienced by wideband digital signals, we describe the interconnects as multiconductor transmission lines with frequency dependent per-unit-length parameters. Therefore, the main task is here to translate a possibly complex frequency-dependence for the line parameters into a simple lumped equivalent circuit.

Frequency-dependent line parameters $R(j\omega)$, $L(j\omega)$, $C(j\omega)$, $G(j\omega)$ evaluated or measured at some discrete and finite frequency points constitute the input data set for the model generation. This procedure can be devised for both scalar and multiconductor transmission lines. In this outline, for the sake of simplicity, we detail only the scalar case. The line equations in frequency

domain read

$$-\frac{d}{dz}V(z,j\omega) = [R(j\omega) + j\omega L(j\omega)]\, I(z,j\omega),$$

$$-\frac{d}{dz}I(z,j\omega) = [G(j\omega) + j\omega C(j\omega)]\, V(z,j\omega),$$

where the line is assumed of length $\mathcal{L}$. Many approaches can be found in literature for the extraction of a lumped model from the above equations (see, *e.g.*, [13] and references therein). The common background is the choice of a suitable frequency-domain function to be approximated with a simpler and known model (usually rational for ease of implementation). This approximation step has been performed with several different techniques (Padé, least squares, etc.). Regardless of the fitting method, the success of the approximation stage depends on the suitability of the model with respect to the specific target function to be approximated.

In order to guarantee the suitability of the model to the target function, we use a rational model with asymptotic constraints. The target functions to be approximated are the characteristic admittance $Y_c(s)$ and the delayless propagation operator $H(s)$, where s is the Laplace variable. A rational function approximation is therefore sought for as

$$\begin{aligned} Y_c(s) &= \sqrt{\tfrac{G(s)+sC(s)}{R(s)+sL(s)}} \simeq \textstyle\sum_k \frac{R_k^y}{s-p_k} + Y_\infty, \\ H(s) &= \exp\{sT + \\ &\qquad \mathcal{L}\sqrt{(G(s)+sC(s))(R(s)+sL(s))}\} \\ &\simeq \textstyle\sum_k \frac{R_k^p}{s-p_k} + H_\infty \end{aligned} \tag{3}$$

through a least-squares fit. The line delay T is extracted from the asymptotic values of the line parameters at $s = \infty$. The success of the least squares fit is insured by the explicit enforcement of their asymptotic values at low and high frequency, which are easily determined by the asymptotic values of the per-unit-length parameters. It should be noted that these asymptotic values are finite in any case. Therefore, convergence is insured, for a sufficiently high model order, over an extended bandwidth. This procedure insures also a correct identification of steady states (matching at $s = 0$) and causality of the line responses due to the specific form of the model.

3 Simulation example

As an example of the use of the presented macromodels, we study the interconnected system of Fig. 2, that is composed of a three-conductor lossy on-MCM interconnect (2 lands + reference plane) driven by two drivers and loaded by two receivers, that are CMOS devices used in IBM mainframe products.

Drivers and receivers macromodels are estimated from the responses of the detailed transistor-level (hereafter labeled as *reference*) models of the CMOS devices available in PowerSPICE. The drivers macromodel turns out to have dynamic order $r = 1$ and submodels f_1 and f_2 composed of eight and six basis functions, respectively (see section 2.1). The receiver macromodel has a dynamic order $r = 5$ and a nonlinear part defined by two RBF submodels composed of sixteen and nineteen Gaussian basis function (see section 2.2). The macromodels are implemented as PowerSPICE subcircuits and their responses are compared to those of the reference models in several simulations.

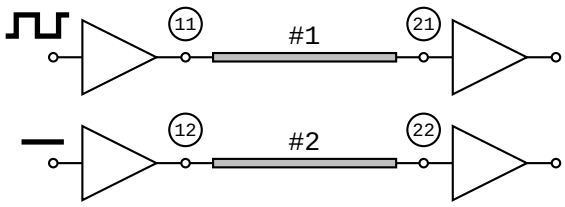

Figure 2: Interconnected system of the example of Sec. 3. Interconnect data: length 0.15 m, $l_{11} = l_{22} = 0.441\,\mu$H/m, $l_{12} = l_{21} = 14.4$ nH/m, $c_{11} = c_{22} = 144$ pF/m, $c_{12} = c_{21} = -1.38$ pF/m, dc resistance $24.4\,\Omega$/m, skin effect coefficient $11.7\,10^{-6}\,\Omega\,\mathrm{s}^{-1/2}$/m, dielectric loss factor $2.5\,10^{-3}$, $C_L = 1\,pF$.

As an example, Figure 3 shows the $v_{21}(t)$ and $v_{22}(t)$ voltage waveform of the network of Fig. 2 when the driver of land `#1` sends a pulse burst (bit pattern `"01101110101000000000"`) and the driver on land `#2` remains quiet in the Low logic state. The solid curves represent the reference response computed by the original transistor-level models of drivers and receivers, and the dotted curves represent the responses computed with the macromodels. The accuracy of response obtained with the macromodels is good also for the sensitive crosstalk waveform $v_{22}(t)$. In all experiments carried out, we found timing errors between our model and the reference always less than 20 ps (in most cases, the timing error is 5 ps), being $T_s = 10 \div 50$ ps the sampling time used in the estimation process. Such timing errors are obtained by computing the maximum delay between the reference and the model responses

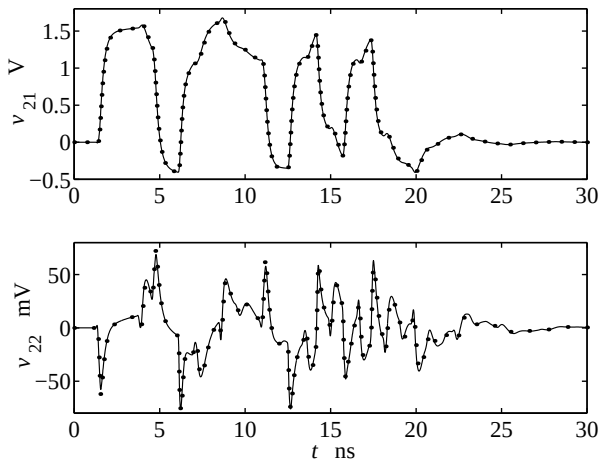

Figure 3: Far-end voltage waveforms $v_{21}(t)$ and $v_{22}(t)$ on the active and quiet line of the structure of Fig. 2. Solid lines: reference; dotted lines: macromodels.

measured at the crossing of a suitable voltage threshold.

Besides being accurate, the proposed macromodels can be generated at low cost and their numerical efficiency is fairly good. As an example, the CPU time required by the estimation of the macromodels of the above example is some ten seconds on a Pentium-II PC @ 350 MHz. Simulation times for the computation of the curves of Fig. 3 are compared in Tab. 1 (same CPU).

Models	**CPU time**
Reference	6 min
Macromodels	5 sec

Table 1: CPU time comparisons for the simulation of the network of Fig. 2.

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