On the Behavioral Modeling of Integrated Circuit Output Buffers

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I. S. Stievano, F. G. Canavero, I. A. Maio

Dip. Elettronica, Politecnico di Torino C. Duca degli Abruzzi 24, 10129 Torino, Italy
Ph. +39 011 5644184, Fax +39 011 5644099 (e-mail igor.stievano@polito.it)

Abstract: The properties of common behavioral macromodels for single ended CMOS integrated circuits output buffers are discussed with the aim of providing criteria for an effective use of possible modeling options.

1 Introduction

Behavioral macromodels of Integrated Circuits (ICs) input and output buffers are key elements for the simulation of Signal Integrity (SI) and electromagnetic compatibility effects in fast digital circuits. Buffer behavioral modeling is usually based on simplified equivalent circuits and the Input/output Buffer Information Specification (IBIS) [1]. Recently, other approaches to behavioral modeling have been proposed [2, 3, 4, 5], that supplement the IBIS resource. At this point, the number of variations that can be applied to the structure and implementation of behavioral models is large and guidelines on the use of possible options would be useful. The aim of this paper is to discuss the properties of common models, providing criteria that help in the choice of the best modeling approach for any specific simulation problem. For the sake of simplicity, the discussion focuses on models for single ended CMOS IC output buffers. However its results apply to other cases as well, and an example of a model for a Simultaneous Switching Noise (SSN) problem is also shown.

2 Output buffer models

This Section shortly reviews the modeling of CMOS output buffers. The ideal behavioral model of an output buffer would be the constitutive relation of its output port: $i = f(v, dv/dt, ..., v_i, dv_i/dt, ...)$, where i and v are the current and voltage of the output port, respectively, and v_i is any variable controlling the port logic state. However, such variables are not accessible and time-varying two-piece models are used instead

$$i(t) = w_1(t)i_1(v(t)) + w_2(t)i_2(v(t)) \tag{1}$$

where $i_n(t)$, $n = 1, 2$ are submodels describing the port behavior in the HIGH and LOW logic states, respectively, and $w_n(t)$, $n = 1, 2$ are weighting coefficients describing state transitions.

For the simplest version of (1), submodels i_n, $n = 1, 2$ are the static characteristics of the output port in the two logic states, and the model structure is justified by the equivalent circuit of the last stage of the buffer (*e.g.*, see the IBIS standard [1]). For the enhanced versions of (1), i_n, $n = 1, 2$ are dynamic models of the output port in fixed logic state. For all variants of (1), the weighting coefficients are best computed by the *two-waveform method* [6, 7], *i.e.*, by solving the linear equations for $w_1(t)$ and $w_2(t)$ that are obtained by replacing in (1) the current and voltage waveforms that are measured during a state transition for two different (lumped) port *reference loads*. Of course, model (1) holds only for problems with complete state transitions.

Many different dynamic models can be exploited as submodels of (1). The simplest one is obtained by adding a capacitive term to the static characteristic of the port (*e.g.*, see [1])

$$i_n(v(t)) = i_{sc,n}(v) + C_n \frac{dv}{dt} \tag{2}$$

where $i_{sc,n}(v)$ is the port static characteristic in the fixed HIGH ($n = 1$) or LOW ($n = 2$) logic state. Improved dynamic submodels can be obtained by using parametric nonlinear relations and system identification methods [3]. Parametric models are usually expressed as sums of nonlinear functions of the involved variables and their parameters are estimated by fitting the model responses to suitable transient responses of the input and output variables related by the model. Parametric models can be used in (2) to replace $C_n dv/dt$ as correction term to $i_{sc,n}(v)$, or as complete dynamic submodels, including both static and dynamic information.

Presently, parametric models based on Gaussian Radial Basis Functions (RBF)[1] and sigmoidal basis functions with ridge type argument [4] have been exploited. For output buffers, we obtain the best performance with the latter

[1] These functions allow a formal derivation of (1) independent of buffer equivalent circuit [3]

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functions, because their symmetry seems closer to the symmetry of the constitutive relations to be modeled, leading to simpler models.

3 Critical issues in output buffer modeling

According to the previous Section, model (1) can be used with many different submodels and several questions arise about which option could lead to the best performance in actual simulation problems. These questions are addressed in this Section.

Representation of static submodels When static submodels are used in (1), the only possible issue is the optimization of their representation. This issue is strictly related to modeled devices and model implementation. In fact, port characteristics are known by samples, and their optimum mathematical representation depends on their nonlinear behavior in the domain explored by voltage and current, and on the simulation engine. Lookup tables, polynomial and even linear interpolation can be exploited [5]. However, nowadays model (1) with static submodels is widely supported by commercial softwares based on IBIS and the possible optimization of submodel representation leads to marginal improvements.

Model dynamic behavior The most important question on model usage is why and when dynamic submodels should be used. The importance of dynamic behavior in fixed logic state depends on the device and on the bandwidth requested to the model. Modern drivers are designed to minimize dynamic effects for signals like those they generate. When this is the case, static submodels should be sufficient. However, when faster signals are expected or the device has a significant dynamic behavior, then dynamic submodels are needed.

In order to illustrate this idea, we compute the responses of the test circuit inside Fig. 1, where the driver is a fast low-voltage CMOS IBM driver kept in HIGH logic state and $e(t)$ is a disturbing step signal that simulates reflections from a real interconnect. Figure 1 shows the output port voltage waveform predicted by using a transistor-level model of the device (*reference*), a purely static model and a dynamic model (the one named *dynamic #1* in the next Subsection) for stepdown disturbing signals with falltime 50 ps and 200 ps. The latter value of falltime is close to the transition times of the signal generated by this device. For this device the error of the purely static model is significant and, as expected, the relative timing error grows as the falltime reduces.

A further important point, often overlooked, is the dynamic behavior during state transitions. The evaluation of the switching coefficients via the two-waveform method guarantees the correct response only when one of the reference load is driven. In normal operating conditions buffers drive interconnects and this condition is not met. When signals coming from the interconnect impinge on the output port during a state transition, significant errors may arise. The use of dynamic submodels mitigates this effect, even if it cannot eliminate it, as it is inherent in model (1). An example of this effect is illustrated by Fig. 2, where the responses of the test circuit of the previous example to a glitch received during a LOW to HIGH transition are shown. The error of both models is appreciable, yet the error of the static model is significantly larger.

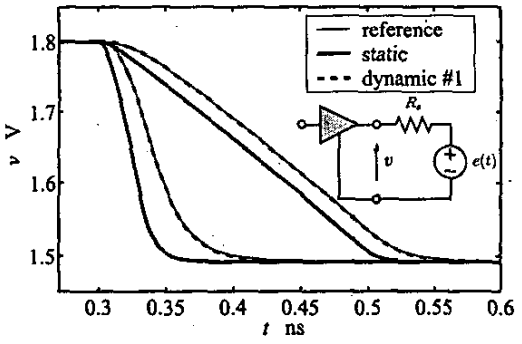

Figure 1: Voltage responses predicted by different device models for a high-performance driver in HIGH logic state disturbed by step signals (see Sec. 3).

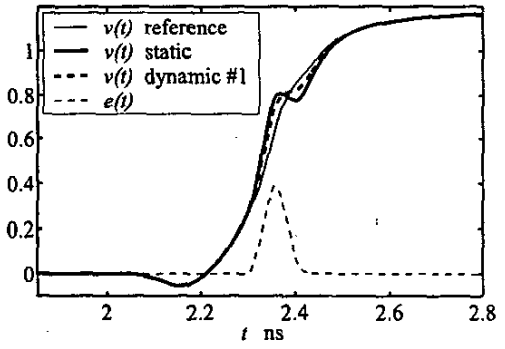

Figure 2: Voltage responses predicted by different device models for a high-performance driver disturbed by a glitch during a state transition (see Sec. 3).

Efficiency of parametric models The major concern in the use of parametric models as submodels of (1) is the efficiency penalty introduced by their complexity. However, for well devised parametric models, such a penalty is marginal. The complexity of a parametric model is described by the number of basis functions composing the model

(model size) and by the number of past time samples it must take into account (dynamic order). The dynamic submodels of common output buffers are composed of few basis functions (one to five) and have a low dynamic order (one or two). The CPU time for their evaluation, therefore, is close to the time required for static submodels.

In order to assess the accuracy and efficiency of different models, we build four models for the IBM device introduced in the previous Subsection and apply them to the simulation of a test circuit composed of the modeled device driving an open ended ideal transmission line with 50 Ω characteristic impedance and 0.2 ns delay. This simple test circuit describes a common problem of digital applications. The compared models are two static models and two dynamic models. The two static models are defined by linear submodels (model *static linear* in the following) and by lookup tables with 310 points (model *static nonlinear*), respectively. The dynamic models are defined by submodels with static characteristic plus parametric correction (model *dynamic #1*) and by parametric submodels including the static and dynamic information (model *dynamic #2*), respectively. All models are built form the responses of a transistor level model of the device. The parametric submodels of *dynamic #1* and *dynamic #2* are built with sigmoidal basis functions (parameter estimation details are in [4]) and turn out to have the sizes and dynamic orders listed in Tab. 4. For all models, the weighting coefficients are computed via the two-waveform method [6, 7] by using reference loads based on a 50 Ω resistor, equal to the transmission line characteristic impedance.

Figure 3 shows the output voltage waveforms predicted by different models when the driver sends a pulse on the transmission line. The reference response is computed by the original transistor level model. All computations are carried out both in PowerSPICE and PSPICE environments. For the modeled device, the characteristics of the output port in fixed logic states are nearly linear within the range of operating voltages and currents, and the response predicted by the *static linear* and *static nonlinear* models are hardly distinguishable. In Fig. 3 the prediction of the static models is collectively represented by the curve labelled static. Similarly, the responses of the two dynamic models are almost indistinguishable and only one curve is included in the Figure.

Since the reference loads for the evaluation of the switching coefficients use the line characteristic impedance, all model responses agree with the reference one in the first parts of the voltage swing of Fig. 3 (part of the waveforms before the first reflection) for both the up and the down transition. A timing error appears in the second part of the swings, where reflected waves impinge on the driver output port. In this part of the responses, the timing error of the static models is on the order of 20 ps and that of the dynamic models il less than 4 ps. It is ought to remark that the typical transition time of the modeled device is 200 ps and that the dynamic contribution to its behavior is moderate. The above timing errors are computed as maximum delays between reference and model responses measured at suitable voltage crossing (1.5 V for the up transition and 0.3 V for the down transition). The CPU time required for the solution of the test problem of this example by means of the different models and simulation environments are summarized in Tab. 4. It clearly appears that all models have comparable efficiency and a considerable efficiency gain with respect to the reference transistor level model. Besides, it is clear that for accurate SI predictions of applications involving high-performance devices dynamic models are preferable. As a final remark, it is worth noting that the numerical efficiency of dynamic models is independent of the transition time of the modeled devices. In fact, for a given output buffer, a variation of its transition time caused by a possible change of its input signal only requires the replacement of the weighting coefficients. No new estimation of submodels i_1 and i_2 is needed.

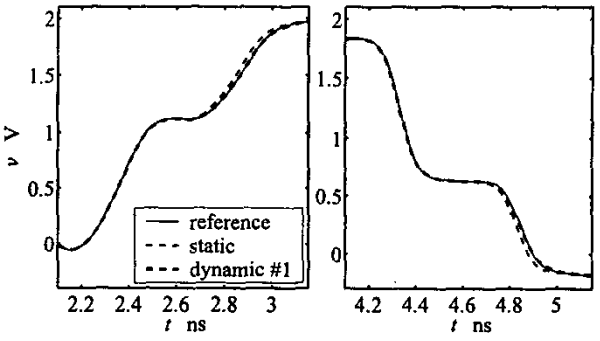

Figure 3: Output voltage waveforms for the example device sending an HIGH pulse on an open ended transmission line. Different models are used and only the first two signal edges are shown.

Model	CPU time	
	PowerSPICE	Pspice
reference	45.2 s	-
static lin	0.62 s	0.52 s
static nonlin	0.71 s	0.72 s
dynamic #1	0.72 s	1.65 s
dynamic #2	0.68 s	1.11 s

Model	submodel size		dynamic order	
	i_1	i_2	i_1	i_2
dynamic #1	1	2	2	2
dynamic #2	1	3	2	2

Table 4: CPU times and model details for the example of Fig. 3.

Multiport models A final concern on dynamic parametric models is their applicability to problems where more than two electric variables are involved, like in SSN problems, where the output and power supplier port of an output

buffer must be modeled at the same time. Actually, parametric models can be applied to multiport problems, because algorithms for parameter estimation can easily handle models with a few input variables.

As an example, we show the application of a two-port parametric model, developed in [8], to a SSN problem. The modeled device is again the IBM driver considered in previous examples. This example application is defined by 20 replicas of the modeled device driving 20 open ended transmission lines. The power supply port of every driver is connected to a common power supply network, that is modeled by the series connection of a resistor, an inductor and a $V_{dd} = 1.8$ V battery. Each driver is assumed to switch with a Gaussian random delay with respect to a reference switching time. The variance of the delay is 100 ps and the circuit response is simulated for ten different realizations of the distribution of switching delays.

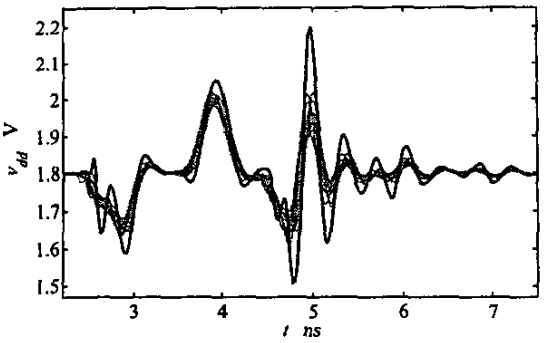

Figure 5: Voltage and current waveforms at the power supply port of 20 drivers switching almost simultenously (see Sec 3 for details).

Figure 5 collects the predicted voltage and current waveforms at the supply port, for the different switching delay realizations (gray lines) and for all drivers switching simultaneously (black line). The CPU time required for the simulation of this example (carried out by PowerSPICE) is about 50 s. In contrast, for this problem, the use of transistor level model would be very demanding for both memory requirements and CPU time.

4 Conclusions

In this paper we show that the choice of buffer macromodels depends on the simulation problem and on the properties of the modeled devices. For the simulation of fast signals, dynamic models are needed and can be effectively obtained by means of parametric models. The latter have marginal efficiency penalty and can be used for multiport problems as well.

Acknowledgements

This work was supported in part by IBM (*Faculty Award* 2002), by the Italian Ministry of University (MIUR) under a Program for the Development of Research of National Interest (PRIN grant #2002093437) and by CERCOM, Center for Multimedia Radio Communications of the Electronics Dept, Politecnico di Torino.

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