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Original
Parametric Macromodels of Digital I/O Ports / Stievano, IGOR SIMONE; Maio, Ivano Adolfo; Canavero, Flavio. - In: IEEE TRANSACTIONS ON ADVANCED PACKAGING. - ISSN 1521-3323. - STAMPA. - 25:2(2002), pp. 255-264. [10.1109/TADVP.2002.803260]

Availability:
This version is available at: 11583/1398460 since:

Publisher:
Piscataway, N.J. : IEEE

Published
DOI:10.1109/TADVP.2002.803260

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12 October 2024

Parametric Macromodels of Digital I/O Ports

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***Abstract*—This paper addresses the development of macromodels for input and output ports of a digital device. The proposed macromodels consist of parametric representations that can be obtained from port transient waveforms at the device ports via a well established procedure. The models are implementable as SPICE subcircuits and their accuracy and efficiency are verified by applying the approach to the characterization of transistor-level models of commercial devices.**

***Index Terms*—Circuit modeling, digital integrated circuits, electromagnetic compatibility, I/O ports, macromodeling, radial basis function models, signal integrity, system identification.**

I. Introduction

NOWADAYS the assessment of signal integrity (SI) and electromagnetic compatibility (EMC) effects in fast digital circuits during the design stage is becoming more and more important. At board and system levels, such an assessment is mainly carried out by simulating the evolution of signals propagating on the interconnection structures, i.e., on printed circuit board lands and cable wires. In these simulation problems, the numerical models representing the digital integrated circuits (ICs) driving and loading interconnects play a key role. The IC models must be both accurate and efficient enough to allow the prediction of sensitive effects, like radiation and crosstalk, and to handle the complexity of real problems at affordable computational costs. Besides, the IC models should work as macromodels of standard circuit simulation environments, in order to exploit their power and to be accessible to a large set of users.

The above requirements are well satisfied by behavioral models, that can be defined as sets of IC port constitutive relations obtained from external (possibly virtual) measurements. The most common approach to create behavioral models is via simplified equivalent circuits of IC ports, because equivalents allow physical insight and facilitate the implementation of models. An important example of the equivalent circuit approach to behavioral modeling is the widely adopted input/output buffer information specification (IBIS) [1], that has given rise to a large set of dedicated model libraries for the electronic design automation tools. The equivalent circuit approach, however, has also some inherent limitations. Mainly, the estimation of model parameters is best performed by virtual measurements carried on transistor-level models of the IC, and the effects taken into account by the model are decided *a priori*, when the equivalent circuit is selected.

Manuscript received January 14, 2002; revised March 29, 2002. This work was supported in part by IBM, Enterprise System Group, Poughkeepsie, NY, under a research grant.

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Digital Object Identifier 10.1109/TADVP.2002.803260

An alternative approach to behavioral modeling is the use of parametric models and input–output system identification methods [2]–[4] to approximate the IC port constitutive relations. The parametric approach to behavioral modeling has interesting advantages, that makes it a useful complement to the more traditional equivalent circuit approach. It automatically takes into account any physical effects significantly influencing voltages and currents of the IC ports and yields models that perform at a very good accuracy level with relatively high efficiency. Also the accuracy level of the models turns out to be weakly sensitive to the load they drive. Finally, if needed, the parametric approach allows the creation of behavioral models from actually measured input–output transient waveforms [4].

In this paper, we address the behavioral modeling of digital IC ports via parametric models. The use of parametric models to build behavioral models of ICs is illustrated from a general point of view and two specific parametric models for IC input and output ports are thoroughly described. The operation and performances of the proposed models are also shown by applying them to some typical digital devices, confirming the positive features of the parametric approach.

The rest of the paper is organized as follows. Section II defines the problem of creating behavioral models of digital ICs for SI and EMC simulations. Section III shortly reviews the main features of parametric models and Section IV describes in detail the modeling process, including the implementation of the model as a subcircuit for SPICE-like circuit simulators. The proposed models for IC output and input ports are presented in Sections V and VI, respectively, whereas a complete set of modeling examples is described in Section VII. Finally, Section VIII shortly discusses the performances of the proposed models.

II. Statement of the Problem

The objective of system level SI and EMC simulations is the prediction of signals on board and on cable interconnects for a specified logic activity of their drivers. In these simulations, the internal operation of ICs is neglected and the IC pins act as signal pattern generators or receivers loading the interconnect. The modeling of ICs for SI and EMC simulations, therefore, amounts to finding suitable relations between the voltage and the current of every port defined by IC pins, for a known logical activity of the ICs.

To address this problem, it is useful to divide IC ports into *input*, *output*, and *power supply ports*. In this paper, we focus on IC input and output ports. Output ports, for any kind of technology/architecture, are buffer circuits composed of cascaded inverter stages with growing driving capabilities. The structure of a generic output buffer is shown in Fig. 1, where $\overline{v}$ denotes the buffer input voltage (coinciding with the output of the functional part of the integrated digital circuit), $v_{\rm o}$ and $i_{\rm o}$ are the

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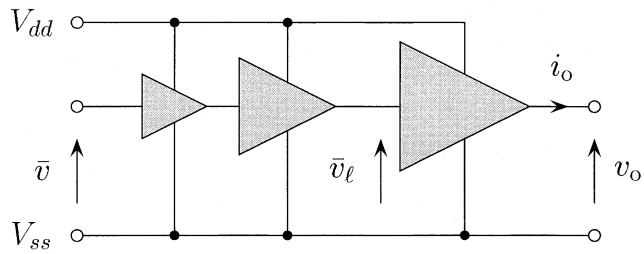

Fig. 1. Generic multistage output buffer and its relevant electric variables (defined in the text). Progressively increasing sizes of drivers represent their respective capability to drive the output current.

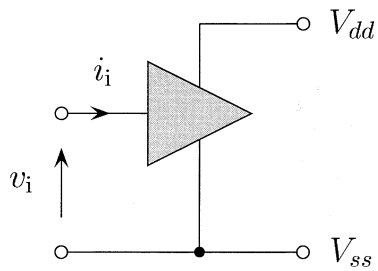

Fig. 2. Generic structure of an input port and its relevant electric variables (defined in the text).

voltage and current at the buffer output pin, respectively, and V_{dd} and V_{ss} are the power supply voltages (assumed constant in this paper).

For IC output ports, therefore, the sought model is a constitutive relation of the form

$$i_o = F_o(v_o, \overline{v}) \tag{1}$$

where F_o is a suitable nonlinear dynamic operator and $\overline{v}$ can be replaced by any variable controlling the logic state of the buffer, e.g., the input voltage of the last stage, $\overline{v}_\ell$.

Input ports can be described by the generic structure of Fig. 2, where i_i and v_i are the port current and voltage variables, respectively. Such circuits are hardly influenced by the logical activity of the IC that follows, and can be considered as simple one-port dynamic elements modeled by the relation

$$i_i = F_i(v_i) \tag{2}$$

where F_i is a nonlinear dynamic operator.

In this paper, we seek the constitutive relations (1) and (2) in the form of discrete-time parametric models. Next section shortly outlines the main properties of these models.

III. Parametric Models

Discrete-time parametric models are widely used in the area of automatic controls and system theory to model nonlinear dynamic systems from input/output data. Most multiple-input single-output nonlinear models of this family can be written as [5]

$$\begin{cases} y(k) = F(\mathbf{\Theta}, \mathbf{x}(k)) \\ \mathbf{x}(k) = [y(k-1), \ldots, y(k-r), \\ \qquad \mathbf{u}(k), \ldots, \mathbf{u}(k-r)]^T \end{cases} \tag{3}$$

where F is a nonlinear mapping from $\Re^{2r+1}$ to $\Re$ defining the *model representation*, $\mathbf{\Theta}$ is the vector of model parameters, $y(k)$ is the output sequence of the model, $\mathbf{u}(k)$ is the vector of input sequences and $\mathbf{x}(k)$ is the *regressor vector*, collecting the past r samples of the output and the present and past r samples of the input, r being the dynamic order of the model.

The class of nonlinear dynamic systems that can be represented by (3) within an acceptable error is very large, as outlined in [6]–[9]. In particular, every dynamic system defined by state-space equations involving only continuous nonlinear mappings can be approximated by the parametric model (3). Explicit indications on the form of model representation F are also given in [6] and [7].

From a formal point of view, the use of (3) to approximate the constitutive relations of multiport circuit elements is straightforward. As an example, the constitutive relation (1) of an output port can be cast in the form (3) by setting $y = i_o$ and $\mathbf{u} = [v_o, \overline{v}]^T$ (see Section V). In order to generate an actual model, however, two key steps must be carried out, i.e., the selection of a model representation F suitable for the system under consideration, and the estimation of its parameters $\mathbf{\Theta}$.

The selection of the model representation F is the crucial point of the modeling process, since good models arise only when the model representation is suitable for the system being modeled. The most natural way to define parameterized nonlinear mappings F is to use function expansions, possibly where every basis function is generated from a single mother function by translation and dilation, as in Fourier series. When different basis function expansions are considered, (3) accounts for several known nonlinear parametric modeling approaches, both from the system identification area and from other areas like neural networks, wavelets and fuzzy models (a complete and unified overview of the existing approaches can be found in [5]). As an example, (3) with F defined by an expansion of ridge-type sigmoid basis functions is equivalent to a *one-hidden-layer feedforward sigmoid neural network.* Two-hidden-layers networks can be obtained by using the values of the basis functions as a new regressor vector to be transformed by a second nonlinear function expansion, and so on. It is clear that the number of available options that could be applied to the modeling of a nonlinear circuit element via (3) is large. For the modeling of IC input and output ports, we mainly experimented with model representations defined by polynomial expansions and by gaussian radial basis functions (RBF) expansions. We obtained the best results with the latter and, in this paper, we exploit models defined by such a representation.

A Gaussian RBF representation can be written as [5]–[7]

$$\begin{cases} F(\mathbf{\Theta}, \mathbf{x}(k)) = \sum_{j=1}^{p} \alpha_j \Phi(|\mathbf{x}(k) - \mathbf{c}_j|, \beta_j) \\ \mathbf{\Theta} = [\alpha_1, \ldots, \mathbf{c}_1^T, \ldots, \beta_1, \ldots]^T \end{cases} \tag{4}$$

where Φ is the scalar mother function $\Phi(\xi, \beta) = \exp(-\xi^2/\beta^2)$ generating all the basis functions, $|\cdot|$ denotes the Euclidean norm and p is the total number of basis functions. Each basis function is defined by its position in the space of regressors (center $\mathbf{c}_j$) and by its spreading (scale parameter β_j). In order to visualize the geometrical meaning of this representation, it is

useful to consider a two-dimensional regressor space, where the jth term of (4) is a Gaussian surface centered in $\mathbf{c}_j$ with amplitude α_j and variance $\beta_j/\sqrt{2}$. The resulting F can be easily fitted to a complicated reference surface (i.e., the surface defining the modeled input output relation) over a finite domain. The RBF representations can be applied to a wide range of modeling problems, as they lead to general results on the existence on nonlinear parametric models [6], [7]. They are numerically efficient (the evaluation of an expansion term requires the evaluation of a norm in the multidimensional regressor space plus a scalar function) and the estimation of their parameters is easier than for other representations. Besides, the Gaussian RBF have local support, that further simplifies the parameter estimation and leads to asymptotically vanishing models. Finally, the Gaussian RBF representation allows model factorization that helps the interpretation of the model structure (see Section V). From a practical point of view, Gaussian RBF representations are well suited for IC ports, as they can produce a model meeting the accuracy and efficiency specification of real simulation problems, at a low modeling cost.

Once the model representation is chosen, the parameter estimation is obtained by means of standard methods, fitting the response of the model to the reference response of the system under consideration. The simplest fitting approach is to look for $\mathbf{\Theta}$ minimizing the mean square error between the model and the system responses. This means to find

$$\mathbf{\Theta}|\min\left\{\frac{1}{N}\sum_{k=1}^{N}[\overline{y}(k)-y(k)]^2\right\} \tag{5}$$

where $\overline{y}(k)$ is the sampled response of the system, $y(k)$ is the output sequence of the model and N is the number of available samples. The estimation algorithms used for the RBF models of this paper are suggested in [10], [11] and work well even for strongly nonlinear problems with several input variables.

IV. IC Modeling Process

The proposed IC port models are obtained by selecting a suitable model representation (usually a RBF or a piecewise RBF model, see below) and by carrying out the following steps.

Step i): Dynamic Order Estimation: This step amounts to estimating the dynamic order r of the modeled device, i.e., the number of past samples of the input and output sequences collected in the regressor vector $\mathbf{x}$. For both linear and nonlinear systems, the dynamic order is an inherent property that does not depend on the representation adopted to reproduce the system behavior. From a theoretical point of view, the dynamic order should be estimated *a priori*, from the transient responses of the system, before any modeling attempt is made. Results and algorithms for order estimation can be found in [12], [14]. In order to get indications on the range of possible r values for our modeled devices, we applied the order estimation methods of [14] to the transistor-level models of typical IC ports. The method works by estimating the order of linearizations of the modeled device around several randomly selected operating points. Based on the experience we gained in the modeling of IC ports, we can conclude that r values range in the interval $1 \div 4$. This means that, from a practical point of view, the dynamic order of IC ports can be directly found by repeating the complete modeling process for growing r values. The dynamic order will be the lowest r value leading to a *good quality model* [defined in step iii) below]. Of course, such a straightforward approach, calls for estimating several models, but, for RBF representations, this can be easily afforded.

Step ii): Generation of Transient Responses: This step amounts to driving the port to obtain transient voltage and current signals carrying information on its behavior. The excitation (input) and response (output) signals involved in this step are named *identification signals.* The driving waveforms (input identification signals) must be carefully designed in order to excite every possible dynamic behavior of the port [12]. For linear systems, this is easily accomplished by using input identification signals with a frequency content that spans the frequency interval containing the system poles; generally white noise or pseudorandom binary signals are used. For the nonlinear case, unfortunately, only qualitative guidelines are available for the design of the input identification signals. Such signals should contain large steps with rise times short enough to excite the fast dynamic behaviors of the system and flat levels allowing the system to approach steady state operations on several operating points. A superimposed small noise signal usually improves the ability of such signals to excite the system dynamics. The final results are multilevel signals with superimposed small noise. Of course the rise times of the steps and the durations of the flat parts must be tuned on the fastest and slowest time constants that can be observed in the system responses, and, as a further rule of thumb, the number of different levels should increase, as the nonlinearity of the static characteristic becomes stronger. Again, the design of the input identification signals is a matter of repeated estimation experiments, where the ability of different identification signals to yield good quality models is verified over a set of sample systems.

Step iii): Estimation and Validation of the Model: In this step, the model parameters $\mathbf{\Theta}$ are estimated and the quality of the obtained model is verified. The parameter estimation is carried out by applying a fitting procedure like the one outlined in the previous Section, to the identification signals. This is done by means of (5), where $\overline{y}(k) = \overline{y}(t = kT)$ is the sampled output identification signal, T is the sampling time, and $y(k)$ is the response of model (3) to the sampled input identification signal. The sampled identification signals must contain all the information of the original identification signals. Therefore the sampling time T must be smaller than the sampling time T_N defined by the Nyquist frequency of the identification signals. On the other hand, the sampling time should not be too small, in order to avoid oversampling and consequent numerical problems in the minimization of (5). As a rule of thumb, the ratio T_N/T should be on the order of $2 \div 6$.

The estimation procedure yields, along with the best values of the model parameters, the error of the model in reproducing the output identification signal. Such an error is the first indication of the model quality, because large errors at this stage imply the failure of the modeling process. Models accurately reproducing the output identification signal should be further validated by checking their response to an input signal different

from the input identification signal. In fact, models that reproduce well the identification signal may still fail to mimic the modeled system when the input signal is changed, e.g., overfitted models exhibit spurious dynamic behaviors not present in the original system and usually excited when the input signal is varied. As a conclusion, a model is considered *good* when it yields accurate predictions for both the input identification signal and suitable validation signals representing the class of allowed input signals [12].

Step iv): Circuit Implementation: The last step amounts to synthesizing the obtained parametric model as an equivalent circuit to be included in standard circuit simulation environments. Such a synthesis enables standard circuit simulators, like SPICE, to solve SI and EMC problems involving the real behavior of IC ports.

The synthesis is carried out by converting the estimated discrete-time model $i(k) = F(\mathbf{\Theta}, \mathbf{x}(k))$ into a continuous-time state space realization and by replacing the state equations with their circuit equivalents. Such a process is described below for the simple case

$$i(k) = F(\mathbf{\Theta}, [i(k-1), v(k), v(k-1)]^T) \tag{6}$$

i.e., a single input (v) and $r = 1$.

With the introduction of the auxiliary variables $x_1(k) = i(k-1)$ and $x_2(k) = v(k-1)$, (6) can be written as

$$\begin{cases} x_1(k) = F(\mathbf{\Theta}, \mathbf{x}(k-1)) \\ x_2(k) = v(k-1) \\ i(k) = F(\mathbf{\Theta}, \mathbf{x}(k)) \end{cases} \tag{7}$$

where $\mathbf{x} = [x_1, v, x_2]^T$. When first order finite differences are introduced, the following discrete-time state space representation arises

$$\begin{cases} x_1(k) - x_1(k-1) = F(\mathbf{\Theta}, \mathbf{x}(k-1)) - x_1(k-1) \\ x_2(k) - x_2(k-1) = v(k-1) - x_2(k-1) \\ i(k) = F(\mathbf{\Theta}, \mathbf{x}(k)). \end{cases} \tag{8}$$

Finally, the difference operator in (8) is approximated with a differential one (e.g., $(d/dt)z(t) \simeq (1/T)[z(kT) - z(kT - T)] = (1/T)[z(k) - z(k-1)]$). In such a way, the time variable t is restored and the following equivalent continuous-time state-space representation arises

$$\begin{cases} \dfrac{d}{dt}\begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} = \dfrac{1}{T}\begin{bmatrix} F(\mathbf{\Theta}, \mathbf{x}(t)) - x_1(t) \\ v(t) - x_2(t) \end{bmatrix} \\ i(t) = F(\mathbf{\Theta}, \mathbf{x}(t)). \end{cases} \tag{9}$$

The previous state-space equation can be effectively implemented in any circuit simulation environment by its equivalent circuit representation. To do this, the first two rows of (9) can be implemented by simple equivalent circuits with voltage controlled sources and the third by a current controlled source only. As an example, Fig. 3 shows the circuit synthesis of the second equation of (9). The circuit synthesis of the first equation is obtained by properly replacing the controlled source.

The complete equivalent circuit of (9) can be easily coded as a SPICE-like subcircuit, as shown in Fig. 4.

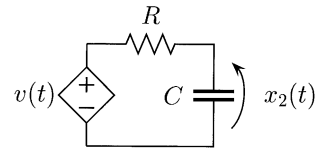

Fig. 3. RC equivalent circuit for $(d/dt)x_2(t) = (1/T)[v(t) - x_2(t)]$, ($T = RC$).

```
.subckt parmodel v ref
 + PARAMS:
 * sampling time T=Rx*C (Rx=1, C=T)
 + Rx = 1
 + T = ...
 * dx1/dt={F-x1}/T
   Cx1  x1 0  {T}
   R1   x1 z1 {Rx}
   Ex1  z1 0  value={V(F)}
 * dx2/dt={v-x2}/T
   Cx2  x2 0  {T}
   R2   x2 z2 {Rx}
   Ex2  z2 0  value={V(v,ref)}
 * output controlled current source i(t)=F
   Gy  v ref   value={V(F)}
 * model representation/structure
  EF F 0 value={...}
  RF F 0 {Rx}
 .ends
```

Fig. 4. SPICE implementation of the parametric model (6), via the representation (9).

V. Output Port Models

The aim of this Section is to derive a parametric model of the multistage output buffer, illustrated in Fig. 1. The constitutive relation of an output port (1) can be cast in the form of a parametric model (3) as

$$\begin{cases} i_o(k) = F(\mathbf{\Theta}, \overline{\mathbf{x}}(k)) \\ \overline{\mathbf{x}}(k) = [i_o(k-1), \ldots, i_o(k-r), v_o(k), \ldots, v_o(k-r), \\ \qquad v_\ell(k), \ldots, v_\ell(k-r)]^T. \end{cases} \tag{10}$$

In this equation, the driving voltage of the last inverter v_ℓ substitutes the buffer input voltage $\overline{v}$ for simplicity. In fact, in typical buffer structures, v_ℓ is almost completely controlled by $\overline{v}$. However, neither v_ℓ nor any other input variable driving the buffer are accessible in actual devices; therefore, simple state transitions or bit patterns need to be supplied in order to simulate the dynamic behavior of the modeled device. To solve this problem we focused on the Gaussian RBF model (4), where the spreading parameters β_j are assumed constant and equal to β, as suggested in [10], [11]. In such a way, (10) can be rewritten as

$$i_o(k) = \sum_j \alpha_j \exp\left(-|\overline{\mathbf{x}}(k) - \overline{\mathbf{c}}_j|^2/\beta^2\right). \tag{11}$$

Extensive estimation experiments carried out on virtual devices defined by transistor-level models of output buffers

showed that, in the subspace of regressors defined by v_ℓ samples, the centers $\overline{\mathbf{c}}_j$ are clustered around the supply voltages V_{dd} and V_{ss}. Therefore, if we force the centers where they naturally converge, i.e., $\overline{\mathbf{c}}_j^T = [\mathbf{c}_{1j}^T, V_{dd}, \ldots, V_{dd}]$ or $\overline{\mathbf{c}}_j^T = [\mathbf{c}_{2j}^T, V_{ss}, \ldots, V_{ss}]$, (11) splits into the sum of products

$$e^{-(|\hat{\mathbf{x}}(k)-V_{dd}\mathbf{I}|^2/\beta^2)}\left[\sum_j \alpha_{1j}\exp\left(-\frac{|\mathbf{x}(k)-\mathbf{c}_{1j}|^2}{\beta^2}\right)\right] + e^{-(|\hat{\mathbf{x}}(k)-V_{ss}\mathbf{I}|^2/\beta^2)}\left[\sum_j \alpha_{2j}\exp\left(-\frac{|\mathbf{x}(k)-\mathbf{c}_{2j}|^2}{\beta^2}\right)\right]$$

where

$$\begin{cases}\mathbf{x}(k) = [i_o(k-1), \ldots, i_o(k-r), v_o(k), \ldots, v_o(k-r)]^T \\ \hat{\mathbf{x}}(k) = [v_\ell(k), \ldots, v_\ell(k-r)]^T\end{cases}$$

and $\mathbf{I}$ is the identity element of $\Re^{r+1}$. This observation motivates the construction of the following approximate piecewise RBF (PW-RBF) model

$$\begin{aligned} & i_o(k) = w_1(k) f_1(\mathbf{\Theta}_1, \mathbf{x}_1(k)) + w_2(k) f_2(\mathbf{\Theta}_2, \mathbf{x}_2(k)) \\ & f_n(\mathbf{\Theta}_n, \mathbf{x}_n(k)) \\ & \quad = \sum_j \alpha_{nj}\exp(-|\mathbf{x}_n(k)-\mathbf{c}_{nj}|^2/\beta^2) = i_n(k) \\ & \mathbf{x}_n(k) = [i_n(k-1), \ldots, i_n(k-r), v_o(k), \ldots, v_o(k-r)]^T \\ & \quad n = 1, 2 \end{aligned} \tag{12}$$

where $f_1(\mathbf{\Theta}_1, \mathbf{x}_1(k))$ and $f_2(\mathbf{\Theta}_2, \mathbf{x}_2(k))$ are Gaussian RBF submodels taking into account both the static and the dynamic effects of the port behavior at fixed HIGH and LOW logic state, respectively, and $w_1(k)$ and $w_2(k)$ are time varying weight coefficients that account for the evolution of the port logic state and act as switches between submodels f_1 and f_2.

The above PW-RBF model arises systematically from the properties of cascaded inverter stages and of the Gaussian RBFs, as shown above, and inherits most of the strengths of RBF parametric models in approximating nonlinear dynamic systems. Besides, it can be easily estimated just from port voltage and current waveforms. Piecewise model structures are also typical of other approaches (e.g., IBIS), which however are based on simplified equivalent circuits justified by empirical considerations.

Once the model representation (12) is defined, the modeling procedure outlined in Section IV must be applied. The dynamic order of the modeled device is estimated in step i). We used the method in [14] to estimate the order r of detailed transistor-level models of typical output buffers, and always found r values in the range of $1 \div 2$. Hence, for practical purposes, the dynamic order of output ports can be estimated *a posteriori* by stepping the r value, as suggested in i) of Section IV.

The next steps of the modeling process are the generation of the identification signals [ii) of Section IV] and the estimation of the model parameters [iii) of Section IV]. The estimation of the model parameters requires two different sets of identification signals, one for the parameters of submodels f_1 and f_2 and one for the weight coefficients w_1 and w_2.

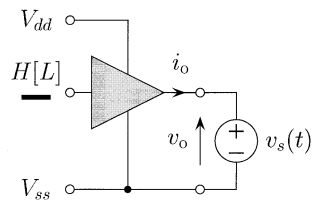

Fig. 5. Ideal setup for the generation of the identification signals for submodels f_1 [f_2]. A driving voltage waveform is applied to the port (submodel input variable v_s) and its corresponding current response (submodel output variable i_o) is recorded, while the buffer logic state is kept in the high [or low] level.

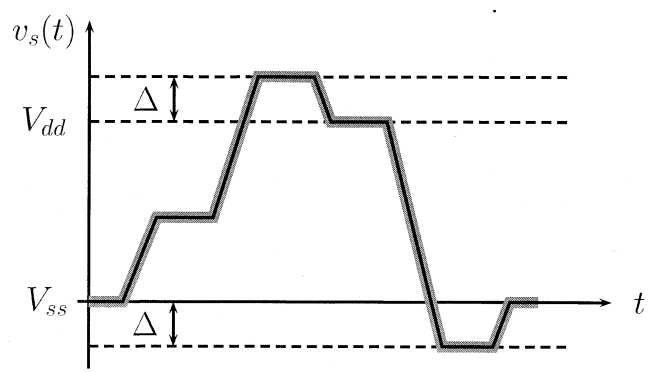

Fig. 6. Generic multilevel driving waveform $v_s(t)$ (see text for details). Thin black line: noiseless waveform; thick gray line: superimposed noisy signal.

The input variable of submodels f_1 and f_2 is the output voltage v_o, and the output variable is the output current i_o when the port is kept in a fixed logic state. The identification signals for submodels f_1 and f_2 are then obtained by applying a suitable voltage waveform to the output terminals and by recording the corresponding output current, while the buffer input is in a fixed logic state. Such an experiment is described by the ideal setup of Fig. 5. According to the guidelines outlined in ii) of Section IV, the driving waveforms (i.e., the input identification signals) are multilevel signals with superimposed small noise (see Fig. 6). These waveforms are composed of some $(4 \div 10)$ level transitions, spanning the range of operating voltages $[V_{ss} - \Delta, V_{dd} + \Delta]$, where Δ is the accepted overvoltage. Typical values of Δ are $(0.1 \div 0.2)V_{dd}$. The flat parts of the waveforms last for sufficient duration to allow the port to reach steady state operation and the edges have transition time t_t comparable to the switching times of the port $t_{\rm sw}$. Typical values of t_t are $(1 \div 5)t_{\rm sw}$. Extensive numerical experiments show that waveforms designed with the above guidelines lead to good modeling results for typical output buffers. Besides, these waveforms are simple enough to be easily generated by real waveform generators, in order to obtain the identification signals from actual transient measurements instead of computing them from the simulated responses of transistor-level models.

The estimation of parameters $\mathbf{\Theta}_1$ and $\mathbf{\Theta}_2$ is done by means of an application of algorithms [10], [11] to the sampled identification signals. According to iii) of Section IV, the sampling time T is set to $T = t_{\rm sw}/(10 \div 50)$. Such estimation algorithms are very efficient and enable users to estimate the RBF models in a few tens of seconds, on a Pentium PC. The key idea of the

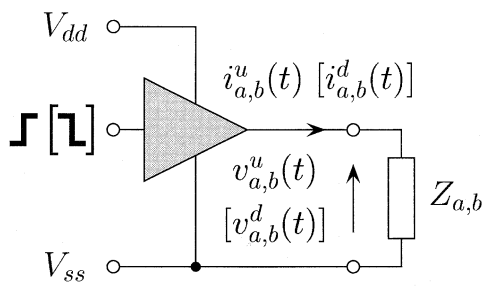

Fig. 7. Ideal setup for the generation of the identification signals for the weight coefficients w_1 and w_2. The port current and voltage waveforms are recorded while the port is loaded by two different loads and is driven to perform a up (or a down) state transition. Z_a represents a load resistor, and Z_b is the series connection of a resistor and a V_{dd} battery.

algorithms is that, for known positions (centers $\mathbf{c}_j$) and spreadings (scale parameters $\beta_j = \beta$) of the basis functions composing the model, the linear coefficients α_j are the solution of a standard least square problem. In order to estimate the centers, every point explored by the regressor vector $\mathbf{x}(k)$ is considered as a possible center $\mathbf{c}_j$ and the common scale parameter β is preset to a value ensuring a good overlapping of every possible basis function. Then, for models composed of $p = 1, 2, 3 \ldots$ basis functions, the following steps are repeated:

- a model with p functions is built by adding a new basis function to the model with $p-1$ functions; the center of the added basis function is the point $\mathbf{x}(k)$ giving rise to the largest decrease of the model fitting error;
- the statistical significance of the new model is assessed by computing suitable statistical indexes and the process is terminated when the most significant model is reached.

The above process is improved in [11] by considering also the exclusion of basis functions previously added to the model.

Once submodels f_1 and f_2 are estimated, the weight coefficients w_1 and w_2 are obtained from the second set of identification signals. Such identification signals are the voltage and current responses recorded during state transitions for two different load conditions. The ideal setup for the generation of such signals is shown in Fig. 7. For a single low-to-high (up) transition and for two different port loads (a) and (b), the sequences $(i^u_a(k), v^u_a(k))$ and $(i^u_b(k), v^u_b(k))$ are recorded. Their use in (12) leads to

$$\begin{cases} i^u_a(k) = w^u_1(k) f_1(\mathbf{\Theta}_1, \mathbf{x}_{1a}(k)) + w^u_2(k) f_2(\mathbf{\Theta}_2, \mathbf{x}_{2a}(k)) \\ i^u_b(k) = w^u_1(k) f_1(\mathbf{\Theta}_1, \mathbf{x}_{1b}(k)) + w^u_2(k) f_2(\mathbf{\Theta}_2, \mathbf{x}_{2b}(k)). \end{cases} \tag{13}$$

Then, the elementary weight sequences $w^u_1(k)$, $w^u_2(k)$ describing the transition can be obtained by simple linear inversion of (13), as follows:

$$\begin{bmatrix} w^u_1(k) \\ w^u_2(k) \end{bmatrix} = \begin{bmatrix} f_1(\mathbf{\Theta}_1, \mathbf{x}_{1a}(k)) & f_2(\mathbf{\Theta}_2, \mathbf{x}_{2a}(k)) \\ f_1(\mathbf{\Theta}_1, \mathbf{x}_{1b}(k)) & f_2(\mathbf{\Theta}_2, \mathbf{x}_{2b}(k)) \end{bmatrix}^{-1} \cdot \begin{bmatrix} i^u_a(k) \\ i^u_b(k) \end{bmatrix}. \tag{14}$$

The same procedure, repeated for a High-to-Low (down) transition, allows to compute two additional elementary sequences $w^d_1(k)$ and $w^d_2(k)$. Finally, a proper concatenation of $w^u_1(k)$, $w^d_1(k)$ and $w^u_2(k)$, $w^d_2(k)$ produces the final form of the weight coefficients for a given bit pattern. Of course, such a property holds only for state transitions spaced enough in time, so that every new transition starts after the previous one is completed. However, since the above validity condition is satisfied in properly working digital circuits, the obtained model is suitable for EMC simulations.

In principle, there are no restrictions on loads (a) and (b), which can be also real sources stimulating the output port. The best loads would be those allowing $\{i_a, v_a\}$ and $\{i_b, v_b\}$ to explore the widest possible region of the regressor space. Within the class of resistive circuits, it can be proven that the best choice is a resistor for load (a) and the series connection of a resistor and a V_{dd} battery for load (b).

Finally, in step iv) of the modeling process, model (12) is implemented as a SPICE-like subcircuit as described in the previous Section.

VI. Input Port Models

This Section is devoted to the development of a parametric model of the input port illustrated in Fig. 2. Common experience tells us that, for port voltage values in the range of the power supply voltage, input ports exhibit an approximately linear capacitive behavior, whereas outside such a range their behavior is dominated by the nonlinear protection circuits. This property and the physical structure of input ports suggest that the constitutive relation (2) is represented as

$$i_{\mathrm{i}}(k) = i_l(k) + i_{nl}(k) \tag{15}$$

where the port current i_{i} is split into two contributions, of which the first part, i_l, refers to the linear behavior of the port, and can be represented as a linear parametric model defined by an Auto-Regressive with eXtra input (ARX) scheme [12], as follows:

$$\begin{cases} i_l(k) = \mathbf{\Theta}_l^T \mathbf{x}_l(k) \\ \mathbf{x}_l(k) = [i_l(k-1), \ldots, i_l(k-r_l), \\ \qquad v_{\mathrm{i}}(k), \ldots, v_{\mathrm{i}}(k-r_l)]^T. \end{cases} \tag{16}$$

Equation (16) defines a linear combination of the components in the regressor vector $\mathbf{x}_l$, where $\mathbf{\Theta}_l$ is the vector of parameters collecting the unknown coefficients and r_l is the dynamic order of the submodel.

The second contribution in (15), i_{nl}, is a nonlinear model taking into account the port behavior in the voltage range where the effects of protection circuits cannot be neglected. We turn again to the RBF parametric representation of Section III, and adopt

$$i_{nl}(k) = g_u(k) + g_d(k) \tag{17}$$

where g_u and g_d are RBF models (4) for the up and the down protection circuits, respectively. The vectors of model parameters are $\mathbf{\Theta}_u$ and $\mathbf{\Theta}_d$, respectively; whereas the input variable is v_{i}.

It is ought to remark that the simplest realization of model (15) is composed of a shunt capacitor C_{eq} and a shunt nonlinear resistor defined by the i–v port static characteristic (hereafter, we will refer to this model as the i–v *model*). In fact, a capacitor and a nonlinear resistor are the simplest i_l and i_{nl} submodels

taking into account both the static and the dynamic behavior of input ports. However, such a basic model offers only a rough approximation of the port behavior, and it was proved to produce inaccurate results in simulation (see next Section), whereas the proposed model performs at a high accuracy level regardless of sources driving the receiver.

Once the model representation is chosen, the estimation of submodel parameters, i.e., $\mathbf{\Theta}_l$, $\mathbf{\Theta}_u$, $\mathbf{\Theta}_d$, is carried out once more by the procedure outlined in Section IV. The identification signals for the estimation of linear submodel (16) are obtained by driving the port with a voltage source producing a few steps within the range of the power supply, in a region where the port exhibits a nearly linear behavior. The unknown parameters $\mathbf{\Theta}_l$ are then computed by standard routines [11], [13]. Furthermore, the identification signals for the two RBF submodels in (17) are again obtained by driving the port with a voltage source producing noisy multilevel waveforms defined in the range $[V_{dd}/2, V_{dd} + \Delta^*]$, for submodel g_u, and $[V_{dd}/2, V_{ss} - \Delta^*]$, for submodel g_d, Δ^* is the accepted overvoltage. The unknown parameters $\mathbf{\Theta}_u$ and $\mathbf{\Theta}_d$ are then computed by the estimation routines [10], [11]. Finally, the estimated model is implemented as a SPICE-like subcircuit.

VII. Applications

In this Section, we show some examples highlighting the features and performances of the proposed models. The example models are estimated from the responses of detailed transistor-level models (assumed as *reference* hereafter) of the modeled devices and involve a commercial driver and some high speed IBM devices. All the estimated models are then implemented as SPICE-like subcircuits in order to compare their responses to the reference ones by using the same simulation environment.

Example 1: The first modeled device (MD1) is an output port of a high-speed CMOS driver (power supply: $V_{ss} = 0$ V, $V_{dd} = 1.8$ V) used in IBM mainframe products. The PW-RBF model estimated for MD1 has dynamic order $r = 1$ and its submodels f_1 and f_2 are composed of 12 and 10 basis functions, respectively.

Figs. 8 and 9 show examples of the identification signals used in the estimation process. Fig. 8 shows the identification signals for submodel f_1, and Fig. 9 shows the identification signals for the computation of the elementary weight sequences w_1^u and w_2^u according to (14). The sampling time used to discretize the identification signals is $T = 10$ ps. Finally, Fig. 10 shows the weight coefficients $w_1(k)$ and $w_2(k)$ forcing the PW-RBF model (12) to produce a Low-to-High transition followed by a high-to-low transition (bit pattern "`010`"). The previous sequences are obtained by concatenating the basic up and down sequences, i.e., by setting $w_1(k) = [w_1^u, w_1^d]$ and $w_2(k) = [w_2^u, w_2^d]$.

As a validation test, Fig. 11 compares the responses of MD1 when it applies a 4 ns pulse (bit pattern "`010`") to three ideal transmission lines, with different characteristic impedance and time delay values, terminated by a 1 pF capacitor. The accuracy of the PW-RBF model in reproducing the reference behavior of MD1 for generic dynamic loads can be clearly appreciated.

Example 2: The second modeled device (MD2) is the output port of a commercial low-voltage CMOS driver, namely the

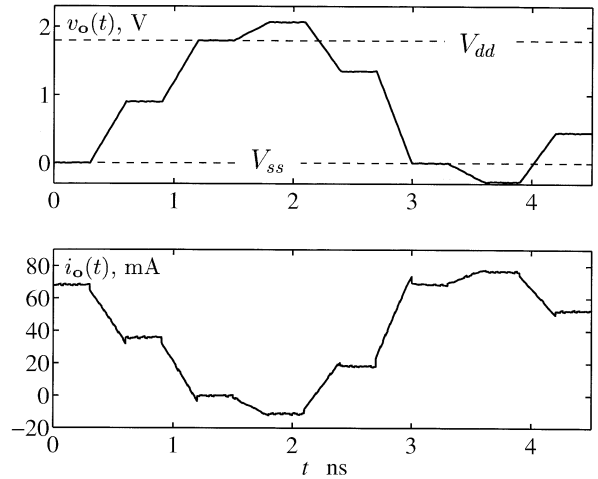

Fig. 8. Identification signals for the estimation of submodel f_1. The top panel shows the voltage driving waveform applied to the port as illustrated in the ideal setup of Fig. 5 and the bottom panel shows the port current response.

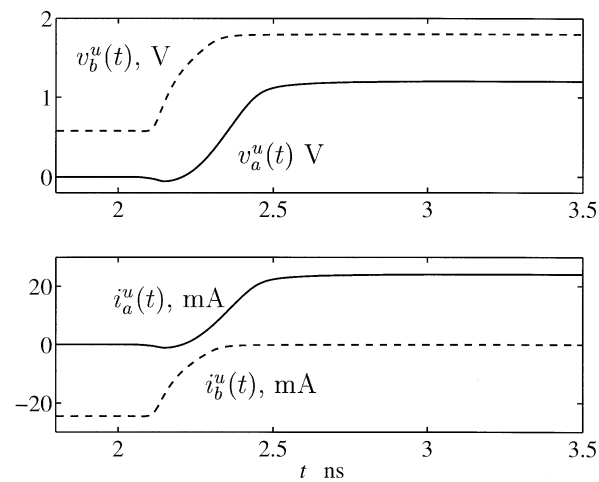

Fig. 9. Identification signals for w_1^u and w_2^u (up transition). The identification loads for the switching experiments of Fig. 7 are a 50-Ω resistor for load (a) and a 50-Ω resistor in series with a V_{dd} battery for load (b).

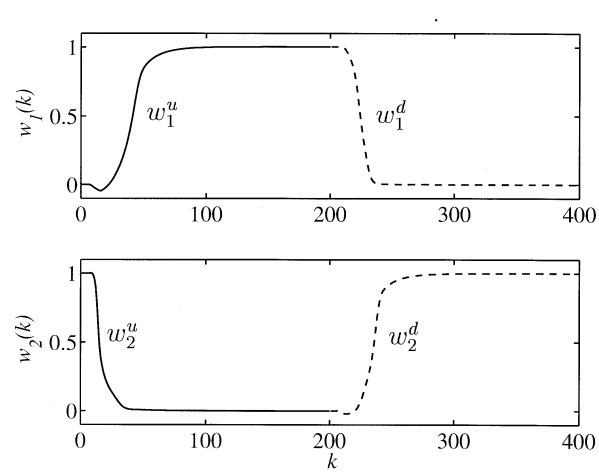

Fig. 10. Weight coefficients $w_1(k)$ and $w_2(k)$ forcing the PW-BF model to produce the bit pattern "`010`."

`74LVC244` ($V_{ss} = 0$ V, $V_{dd} = 3.3$ V). For this device, a transistor-level model (typical values of components) is available

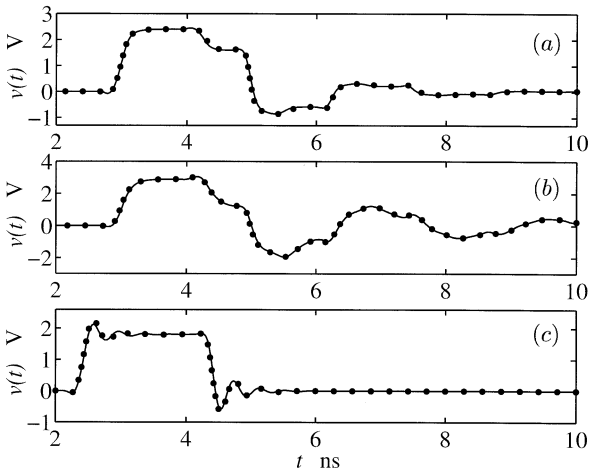

Fig. 11. Far-end voltage waveform $v(t)$ on three ideal transmission lines driven by the device named MD1. Solid lines: reference; dotted lines: PW-RBF model. Panel (a) refers to a line with $Z_c = 50\ \Omega$, $T_d = 0.6$ ns; (b) $Z_c = 100\ \Omega$, $T_d = 0.6$ ns; (c) $Z_c = 100\ \Omega$, $T_d = 40$ ps.

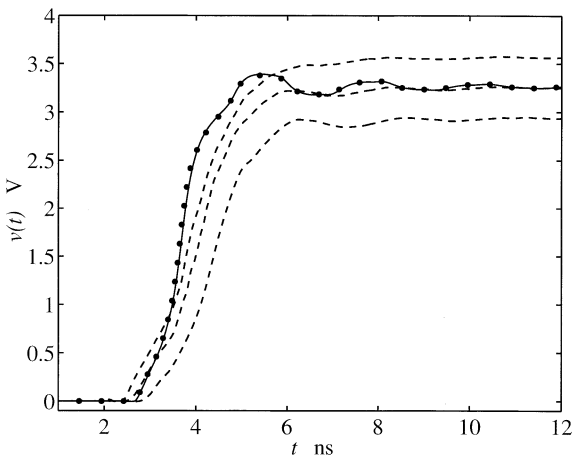

Fig. 12. Near end voltage waveform $v(t)$ on an ideal transmission line ($Z_0 = 100\ \Omega$, $T_d = 0.5$ ns) driven by the device named MD1 and loaded by a 1 pF capacitor. Solid line: reference; dotted line: PW-RBF model; dashed lines: fast, typical and slow IBIS models.

from the vendor, as well as an IBIS data set (version 2.1) including slow, typical and fast cases, that take into account the spreading of parameters due to the manufacturing process.

From the transistor-level model of MD2, we built a PW-RBF model (12), that turns out to have a dynamic order $r = 1$ and submodels f_1 and f_2 composed of 10 and 15 basis functions, respectively. The sampling time used in the estimation process is $T = 50$ ps. From the IBIS data set, we also built a typical, a slow and a fast IBIS model implemented as SPICE-like subcircuits.

In order to compare the accuracy of the PW-RBF model and of the IBIS models in predicting the actual behavior of MD2, we use a validation setup composed of an ideal transmission line ($Z_0 = 100\ \Omega$, $T_d = 0.5$ ns) driven by MD2 and loaded by a 1 pF capacitor. Fig. 12 shows the MD2 port voltage response predicted by the PW-RBF model and by the three IBIS models when the driver performs a low-to-high transition (bit pattern "`01`"). From this Figure, it is clear that the PW-RBF model turns out to be very accurate and could be safely used to replace the

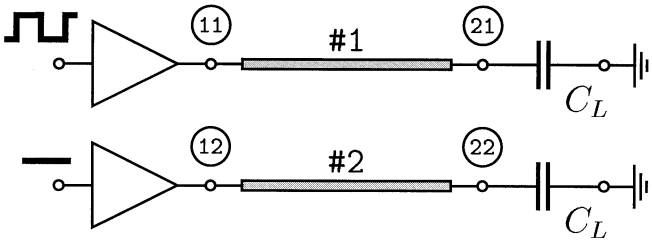

Fig. 13. Validation setup for Ex. 3. The coupled-line structure (length 0.1 m, $l_{11} = l_{22} = 0.441\ \mu$H/m, $l_{12} = l_{21} = 14.4$ nH/m, $c_{11} = c_{22} = 144$ pF/m, $c_{12} = c_{21} = -1.38$ pF/m, dc resistance 24.4 Ω/m, skin effect coefficient 11.7 10^{-6} $\Omega s^{-1/2}$/m, dielectric loss factor 2.5 10^{-3}) represents an MCM interconnect, and is driven by two MD3 devices (one active, one quiet), and loaded by capacitors with $C_L = 1$ pF.

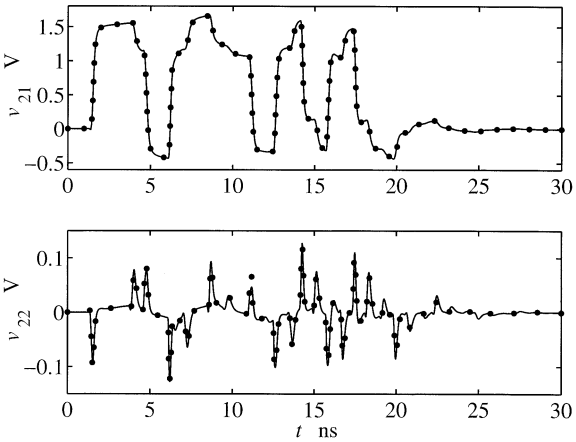

Fig. 14. Far-end voltage waveforms $v_{21}(t)$ and $v_{22}(t)$ on the active and the quiet line of the structure of Fig. 13. Solid lines: reference; dotted lines: PW-RBF model.

transistor-level model. However, IBIS models may lead to poor predictions, even if the parameter spreading is considered.

Example 3: The third modeled device (MD3) is another output port of an IBM CMOS driver ($V_{ss} = 0$ V, $V_{dd} = 1.5$ V). The PW-RBF model estimated for MD3 has dynamic order $r = 1$ and its submodels f_1 and f_2 are composed of nine and six basis functions, respectively. The sampling time used in the estimation process is $T = 10$ ps.

Fig. 13 shows the validation setup devised for this example. It is based on a three-conductor lossy on-MCM interconnect (2 lands + reference plane) driven by two MD3 devices and terminated by 1 pF capacitors. The device on land `#1` is active and sends a train pulse (bit pattern "`011 011 101 010 000`"), whereas the device on land `#2` remains quiet in the Low logic state (bit pattern "`000 000 000 000 000`").

Fig. 14 shows the far-end voltage waveforms $v_{21}(t)$ and $v_{22}(t)$ on both the active and the quiet land of the setup. This third comparison highlights that, in a realistic situation, also the far-end crosstalk signal, which is a sensitive quantity, can be carefully predicted by using PW-RBF models.

Example 4: The fourth modeled device (MD4) is the input port of a receiver ($V_{ss} = 0$ V, $V_{dd} = 1.8$ V) used in the same series of IBM products as those of the previous examples. For MD4, we estimate the two different models outlined

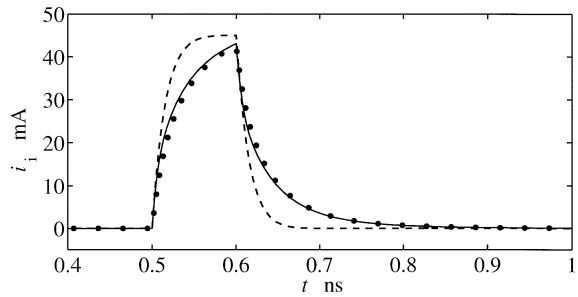

Fig. 15. Model responses for a receiver driven directly by an equivalent source (see text). Solid line: reference response; dotted line: parametric model; dashed line: i–v model.

in Section VI: the simple i–v model and the parametric model (15) defined by equations (16) and (17).

The estimated i–v model is composed of $C_{\rm eq} = 3$ pF and of the static i–v characteristic of the modeled device. The parametric model turns out to have a linear submodel i_l with dynamic order $r_l = 3$, and a nonlinear submodel i_{nl}^u with the following characteristics. The RBF submodel g_u of (17) has a dynamic order 3 and is made of 16 basis functions; while g_d has a dynamic order 2 and 19 basis functions. The sampling time used in the estimation process is $T = 10$ ps for submodel i_l, and $T = 20$ ps for submodels g_u and g_d.

The first validation is devised to stimulate the nearly linear behavior of the receiver: we drive MD4 by the series connection of a 5 Ω resistor and an ideal voltage source with a trapezoidal waveform (amplitude = 1 V, transition time = 100 ps). Fig. 15 shows the $i_{\rm i}(t)$ waveform computed with the reference model and the two estimated models for this validation. The gain of accuracy of the parametric model can be clearly appreciated.

As a second and more realistic validation test, we use a 10 cm long lossy transmission line loaded by MD4 and driven by the series connection of a 30 Ω resistor and an ideal voltage source with trapezoidal waveform. The pulse duration is 2 ns, the transition times are 100 ps long, and the amplitude of the pulse is set to 1.8 V, 2.2 V, and 2.8 V, in order to explore the nonlinear region of input voltages. Fig. 16 shows the $v_{\rm i}(t)$ waveform computed by the reference model and by the i–v and the parametric models. The accuracy of the proposed parametric model in both the linear and the nonlinear regions is clearly appreciable.

VIII. Performance Assessment

This section contains a summary of results, for various cases devised to test the performances of the proposed modeling technique.

The accuracy of our RBF models is quantified by a performance index representing the timing error, expressed as the maximum delay between the reference and the model responses measured at the crossing of a suitable voltage threshold (e.g., 50% of the signal swing). In all experiments conducted so far (about one hundred), we found timing errors between our model and the reference always less than 20 ps (in most cases, the timing error is 5 ps). It should be emphasized that, in the majority of cases, the resulting time errors reaches the minimum attainable threshold, since the sampling time used in the estimation processes is between 10 and 50 ps.

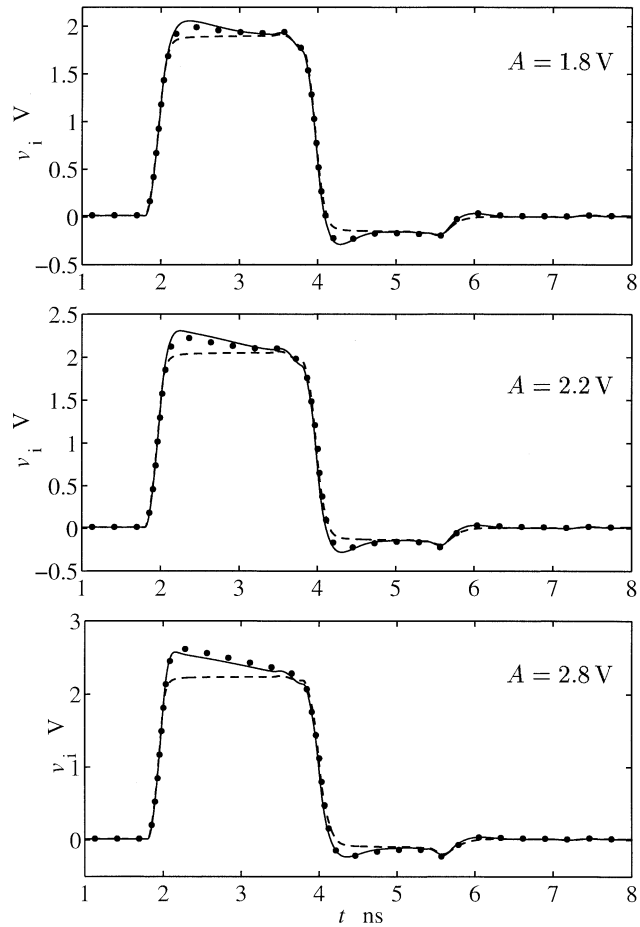

Fig. 16. Far-end voltage waveforms on a 10-cm-long lossy transmission line loaded by the device named MD4 and driven by the series connection of a 30 Ω resistor and an ideal voltage source producing a pulse whose amplitude is A. Solid lines: reference; dotted lines: parametric model; dashed lines: i–v model.

TABLE I
Results of a Simple PowerSPICE Simulation Test Involving the Example Driver MD1. Memory Used and Simulation Time for the Transient Simulation of the MD1 and of Its PW-RBF Model Performing a State Transition While They are Loaded by a 50 Ω Resistor

Model	Memory Used	CPU time
Transistor-level	40 Mb	80 sec
PW-RBF	7 Mb	4 sec

Additional indexes quantifying the cost of model production and its numerical efficiency are also considered. The CPU time required by the estimation of the models of the previous Section is some ten seconds on a Pentium-II PC @ 350 MHz. For the efficiency evaluation, we considered a simulation test consisting in the transient simulation of the example driver MD1 loaded by a 50 Ω resistor and performing logic state transitions. PowerSPICE was used as a simulation engine [15]. The memory used and the simulation time required by the reference transistor-level description of MD1 and by the PW-RBF model are compared in Table I, where we can appreciate the speed-up by a factor of 20 introduced by the proposed model. Based on a

wide set of simulations, we can claim that, as a rule of thumb, the estimated models for both input and output ports are always at least 20 times faster than transistor-level models.

IX. Conclusion

We address the development of digital I/O port macromodels for SI and EMC simulations by means of parametric models. Two specific parametric model representations are proposed and their use to obtain SPICE-like macromodels for generic devices is thoroughly illustrated. The numerical results obtained highlight the high accuracy level and the good numerical efficiency of the proposed modeling approach. The parametric models run faster than the corresponding source transistor-level models and almost maintain the accuracy of the source models for different test loads. Besides, the estimation process decides part of the structure of the model (i.e., the dynamic order and the component basis functions) from just a set of suitable transient waveforms. In contrast to behavioral models based on equivalent circuits, no specific measurements to estimate static characteristics or model circuit components are required, and the creation of parametric behavioral models from measured data is straightforward. The parametric approach to behavioral modeling, therefore, can be considered a useful complement to the conventional equivalent circuit approach, offering improved accuracy and load insensitivity as well as easier experimental characterizations. It can be exploited by any user with access to a circuit simulation environment and to device transient responses.

Acknowledgment

The authors would like to thank G. Katopis, IBM Enterprise System Group, Poughkeepsie, NY, for his kind support, belief in this approach, and encouraging the development of this research, D. Becker and Z. Chen, Enterprise System Group, IBM, Poughkeepsie, NY, for many stimulating discussions, and Z. Chen, for valuable assistance and help with the reference models.

References

[1] (1999, Sept.) I/O Buffer Information Specification (IBIS) Ver. 3.2. Tech. Rep. [Online]. Available: http://www.eigroup.org/ibis/ibis.htm.

[2] F. G. Canavero, I. A. Maio, and I. S. Stievano, "Black-box models of digital IC ports for EMC simulations," in *Proc. 14th IEEE Int. Symp. Electromagn. Compat.*, Zurich, Switzerland, Feb. 20–22, 2001, pp. 679–684.

[3] I. S. Stievano, Z. Chen, D. Becker, F. G. Canavero, G. Katopis, and I. A. Maio, "Behavioral modeling of digital IC input and output ports," in *Proc. 10th IEEE Topical Meeting Elect. Performance Electron. Packag. (EPEP)*, Cambridge, MA, Oct. 29–31, 2001.

[4] I. S. Stievano and I. A. Maio, "Behavioral models of digital IC ports from measured transient waveforms," in *Proc. 9th IEEE Topical Meeting Elect. Performance Electron. Packag. (EPEP)*, Scottsdale, AZ, Oct. 23–25, 2000, pp. 211–214.

[5] J. Sjöberg *et al.*, "Nonlinear black-box modeling in system identification: A unified overview," *Automatica*, vol. 31, no. 12, pp. 1691–1724, 1995.

[6] I. W. Sandberg, "Approximations for nonlinear functionals," *IEEE Trans. Circuits Syst. I*, vol. 39, pp. 65–67, Jan. 1992.

[7] ——, "Approximation theorems for discrete-time systems," *IEEE Trans. Circuits Syst.*, vol. 38, pp. 564–566, May 1991.

[8] A. Ponchet, J. L. Ponchet, and G. S. Moschytz, "On the input/output approximation of nonlinear systems," in *Proc. ISCAS'95 Conf.*, May 1995, pp. 1500–1503.

[9] S. Boyd and L. O. Chua, "Fading memory and the problem of approximating nonlinear operators with volterra series," *IEEE Trans. Circuits Syst.*, vol. 32, pp. 1150–1161, Nov. 1985.

[10] S. Chen, C. F. N. Cowan, and P. M. Grant, "Ortogonal least squares learning algorithm for radial basis function network," *IEEE Trans. Neural Networks*, vol. 2, pp. 302–309, Mar. 1991.

[11] K. Judd and A. Mees, "On selecting models for nonlinear time series," *Physica D*, vol. 82, pp. 426–444, 1995.

[12] L. Ljung, *System Identification: Theory for the User*. Englewood Cliffs, NJ: Prentice-Hall, 1987.

[13] ——, *System Identification Toolbox User's Guide*. New York: The MathWorks, Inc., Nov. 2000.

[14] M. Autin, M. Biey, and M. Hasler, "Order of discrete time nonlinear systems determined from input/output signals," in *Proc. ISCAS'92 Conf.*, May 1992, pp. 296–299.

[15] (2001, Aug.) PowerSPICE User's Guide, Version 1.5. [Online]. Available: http://w3.eda.ibm.com/ckttools/pwrspice.

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