Small-Signal Model of a Boost Converter Exploiting ZVS at the High-Side MOSFET

This is the author's version of the article that has been presented at IEEE MWSCAS2024
The editorial version of the paper is available at http://dx.doi.org/10.1109/MWSCAS60917.2024.10658716

Small-Signal Model of a Boost Converter Exploiting ZVS at the High-Side MOSFET

Francesco Gabriele*, Fabio Pareschi*,‡, Gianluca Setti¶,‡, Riccardo Rovatti†,‡, Giuseppe Calderoni§, Davide Lena§, and Maria Rosa Borghi §

* DET – Politecnico of Torino, corso Duca degli Abruzzi 24, 10129 Torino, Italy.
email:{francesco.gabriele, fabio.pareschi}@polito.it

¶ CEMSE, King Abdullah University of Science and Technology (KAUST), Saudi Arabia. email: gianluca.setti@kaust.edu.sa

† DEI – University of Bologna, viale Risorgimento 2, 40136 Bologna, Italy. email: riccardo.rovatti@unibo.it

‡ ARCES – University of Bologna, via Toffano 2/2, 40125 Bologna, Italy.

§ STMicroelectronics s.r.l. - Italy. email:{giuseppe.calderoni, davide.lena, maria-rosa.borghi}@st.com

***Abstract*—In this paper, a small-signal model for a synchronous Pulse-Width Modulated (PWM) Boost converter operating in Continuous Conduction Mode (CCM) embedding a Zero Voltage Switching (ZVS) network for the high side power MOSFET is proposed. The exposed analysis aims at extending the field of equivalent circuit models for DC/DC power converters, presenting a fully characterization of the dynamical alteration of the Boost converter traditional small-signal model when the ZVS network is introduced. The enhanced small-signal model results in a convenient tool exploitable since from the beginning of the compensation network design phase, as it permits to capture the main open-loop converter transfer function alteration, i.e., the control-to-output, line-to-output and output impedance transfer functions. The validity of the provided small-signal model is demonstrated through a set of SIMPLIS circuital simulations.**

I. Introduction

In the realm of power electronics, the quest for higher efficiency and enhanced reliability is one of the paramount concerns in the development of DC/DC power converters. Augmenting the power density and improving the system dynamic performances is indeed feasible by increasing the operating switching frequency. Nevertheless, this leads switching losses to emerge as a predominant factor in the computation of the overall converter power losses.

In this context the soft-switching approach, generally achieved by means of Zero Voltage Switching (ZVS) techniques, is useful to mitigate switching losses of PWM converters, besides minimizing the stress on semiconductor devices during switching transitions and reducing the generated high-frequency electromagnetic interference [1], [2]. ZVS is typically achieved in PWM converters through Quasi-Resonant, Zero-Voltage-Transition or Quasi-Square-Wave (QSW) architectures [3], [4]. Recent QSW converter architectures [5], [6] employ an additional control networks to turn the main device on with zero voltage across it, resulting in a greater improved efficiency. In this paper, we consider a standard architecture given by a Boost converter with a ZVS network for the High-Side (HS) power MOSFET, whose schematic is depicted in Fig. 1(a). A Zero Crossing Detection (ZCD) comparator is introduced to monitor the switching node SW and detect the optimum time instant to turn the HS on. This results in the efficiency improvement shown in the example of Fig. 2, where it is clearly inferrable how a Boost converter with an hard-switched HS MOSFET proves to be less efficient,especially at light-load working conditions.

Focusing on the key converter waveforms in Fig. 1(b), the ZVS network operation is significant during the dead-time interval T_d, which begin as soon as the Low Side (LS) MOSFET M^{LS} is turned-off. Throughout this time interval, the parasitic capacitance $\mathrm{C}_{\mathrm{MOS}}$ on the SW node is being charged by the peak current I_{pk} flowing into the filter inductance L. Note that, typically, the $\mathrm{C}_{\mathrm{MOS}}$ exhibits a strongly non-linear behaviour, making the theoretical evaluation of the system evolution in time during T_d non-trivial at all. However, it is indeed possible by means of measurements or transient simulations to identify the value of an equivalent linear capacitance that, replaced to the simplified schematic of Fig. 1(a), ensures a behaviour very similar to that of the real circuit. In the following, we implicitly assume this, and consider a linear $\mathrm{C}_{\mathrm{MOS}}$ capacitance.

Therefore, assuming I_{pk} is almost constant during T_d, the voltage node V_{SW} increases linearly. The ZCD circuit sets the switching time instant when the drain-to-source voltage of the HS MOSFET M^{HS} is close to zero. This technique further prevents the body diode $\mathrm{D}_{\mathrm{B}}^{\mathrm{HS}}$ from starting to conduct the inductor current, and it hence results in an optimum switching-on point for the M^{HS}. Indeed, turning prematurely the M^{HS} on during the V_{SW} is not favourable since it results to be hard-switched, while bringing the $\mathrm{D}_{\mathrm{B}}^{\mathrm{HS}}$ into conduction results in higher power dissipation due to the diode conduction and reverse recovery losses.

However, it is noteworthy that soft-switching techniques have a considerable effect on the power converter dynamics [7]–[11]. This necessitates an expansion of traditional small-signal models developed for PWM converters, which is pivotal in the controller design phase aimed at obtaining the desired system performances. Therefore, the objective of this paper is to extend the modeling approach proposed in [11] to the Boost in Fig. 1(a). As shown in our previous work, if the ZVS network is applied to the LS MOSFET in a synchronous

This is the author's version of the article that has been presented at IEEE MWSCAS2024
The editorial version of the paper is available at http://dx.doi.org/10.1109/MWSCAS60917.2024.10658716

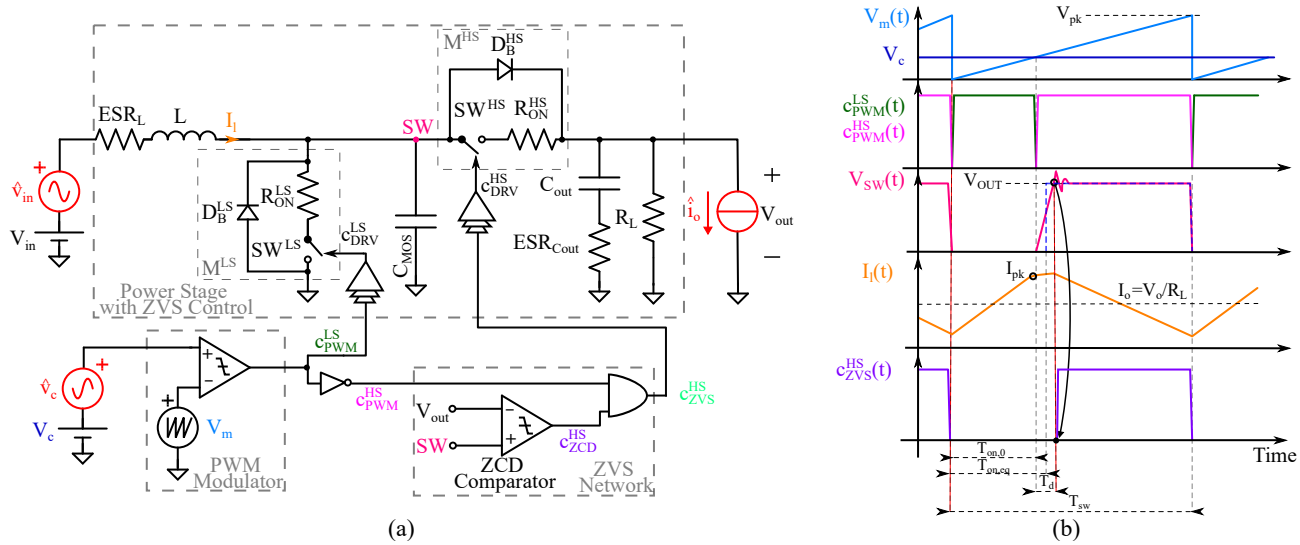

Fig. 1. (a) Schematic of a voltage-mode Boost converter with ZVS control on the HS. (b) A set of waveforms highlighting the action of the proposed ZVS control network on the HS power MOSFET of a synchronous Boost converter.

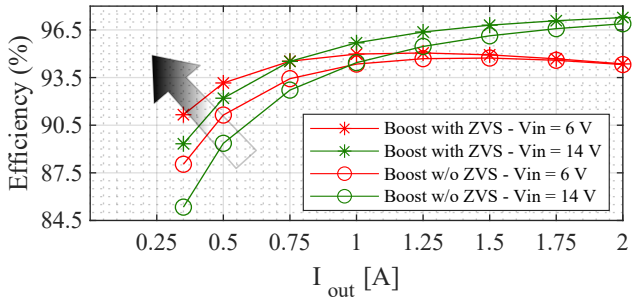

Fig. 2. Efficiency estimation of the Boost converter in Fig. 1(a) with the analysed ZVS network in CCM. The results are derived via the efficiency calculator tool available in SIMPLIS with the set of circuital component values reported in Table I.

Buck converter operating in CCM the overall system dynamics is impacted. The same phenomena can be specularly observed in a synchronous Boost converter when the same ZVS network acts on the HS MOSFET, and it is mathematically described in this work. Furthermore, an equivalent small-signal circuit model is presented. It allows to compute the main open-loop small-signal transfer functions, i.e., control-to-output, line-to-output and output impedance.

The paper is organized as follows. An in-depth analysis of the Boost converter in Fig. 1(a) is reported in Section II. The enhanced small-signal model is derived in Section III and it is validated through SIMPLIS simulations in Section IV. Finally, we draw the conclusion.

II. The Boost Converter and the ZVS Network on the HS MOSFET

The synchronous Boost converter embedding the proposed ZVS network shown in Fig. 1(a) comprises a power stage and a sawtooth-based PWM modulator.

The power stage includes an half-bridge, an inductance L and the output capacitor C_{out}, with the respective equivalent series resistances ESR_L an $ESR_{C_{out}}$. The input voltage V_{in} is placed at the converter input port while a resistive load R_L is connected at the convert output port. The half-bridge power MOSFETs $M^{HS,LS}$ are modelled as the parallel combination of a body diode $D_B^{LS,HS}$ and a conduction resistance $R_{on}^{HS,LS}$ with a switch $SW^{HS,LS}$ in series, and the overall parasitic capacitive effect on the switching node SW is represented by a capacitance C_{MOS} on the SW node. They are driven by the control signals c_{DRV}^{LS} and c_{DRV}^{HS}, respectively. The former is directly derived from a traditional sawtooth-based PWM modulator logic signal c_{PWM}^{LS}, while the latter results from the logic combination of the signals c_{PWM}^{HS} AND c_{ZCD}^{HS}. Similarly to what is reported in [11], and without loss of generality, we will assume from now on that the amplitude V_{pk} of the sawtooth waveform exploited from the PWM modulator is inversely proportional to the nominal input voltage value V_{IN} through a k_{FF} coefficient, i.e., $V_{pk} = k_{FF}/V_{IN}$. This permits to statically compensate the V_{IN} variation within a certain range. The ZCD comparator asserts the signal c_{ZCD}^{HS} at an appropriate time instant, implementing a break-before-make mechanism during T_d.

The converter output voltage is always regulated by the introduction of a controller, which is designed starting from a well-characterized system description in terms its inputs-outputs relationship. For a PWM DC/DC converter, this description is typically achieved through small-signal averaged models. These permits to capture the slow-scale dynamic of the system by replacing the switching network with a linear time-invariant model, which permits to make use of the well consolidated circuit analysis techniques. The traditional averaged small-signal model for a Boost converter operating in CCM is reported in Fig. 3(a), whose parameter expressions are

This is the author's version of the article that has been presented at IEEE MWSCAS2024
The editorial version of the paper is available at http://dx.doi.org/10.1109/MWSCAS60917.2024.10658716

grouped in Table III. From here on, the symbol $\hat{\cdot}$ denotes the small-signal perturbation, while the steady-state contribution is reported in capital letters. The switching network of the original circuit is replaced by an ideal transformer having a turn-ratio $M(D)$, where D is the converter steady-state duty-cycle, together with two controlled current and voltage sources, respectively $j(s)$, $e_s(s)$ and the equivalent averaged effect of the MOSFET conduction resistances R_{eq}. Moreover, an equivalent inductance L_e is defined. The system inputs are the duty cycle perturbation $\hat{d}_0$, the input voltage perturbation $\hat{v}_{\text{in}}$ and the load perturbation $\hat{i}_o$. The PWM modulator small-signal model relates the signal $\hat{d}_0$ with the control voltage perturbation $\hat{v}_c$. It is represented from the transfer function $H_{\text{PWM}}(s) = \hat{d}_0/\hat{v}_c = 1/V_{\text{pk}}$ [12]. Starting from the circuit schematic in Fig. 3(a) it is possible to straightforwardly derive the main open-loop transfer function by circuital inspection, as summarized in Table II.

The validation of a small-signal model in the frequency domain is carried out through SIMPLIS. Indeed, it is possible to find a Periodic Operating Point (by means of a POP analysis) of the switching system under analysis and make possible to perform an AC analysis. From the traditional small-signal model it is also possible to compute the main open-loop transfer functions, which are grouped in Table II. A direct comparison between the SIMPLIS simulation results and the transfer functions plotted in the frequency domain (i.e., imposing $s = j\omega$) is provided in Fig. 4. As inferable from the comparison, the proposed model does not allow to accurately capture the real circuit dynamics. Similarly to what has been reported in [11], the presence of a damping-effect can be observed in all the main transfer functions, confirming the inaccuracy of the traditional small-signal model and the need of an enhanced small-signal model.

III. The Enhanced Small-Signal Model

The enhanced small-signal model must contemplate the ZVS loop behaviour impact on the circuit dynamics, preserving the compactness of the traditional counterpart. This is achievable starting from the converter cyclostationary operating point depicted in Fig. 1(b), particularly focusing on its operation during the T_d. This additional state introduced by the presence of the ZVS control loop has the equivalent effect of altering the effective duty-ratio imposed on the converter. This can be intuitively explained just evaluating the pure DC component of the switching node converter waveform $V_{\text{SW}}(t)$: as long as the HS MOSFET is hard-switched, it is possible to evaluate the steady-state duty-ratio directly from the steady-state on-time value as $D = T_{\text{ON},0}/T_{\text{SW}}$. However, this is no longer true when the ZVS mechanism is introduced (i.e., $T_d \neq 0$) and from an intuitive standpoint, the greater the T_d is, the largest the impact it has on the converter dynamic.

As shown by the blue dashed-curve in Fig. 1(b), an equivalent ON-time can be defined reshaping the $V_{\text{SW}}(t)$. This leads to $T_{\text{on,eq}} = T_{\text{on},0} + T_d/2$ and it reflects on the duty cycle as:

$$d = \frac{T_{\text{on,eq}}}{T_{\text{SW}}} = \frac{T_{\text{on},0} + T_d/2}{T_{\text{SW}}}, \tag{1}$$

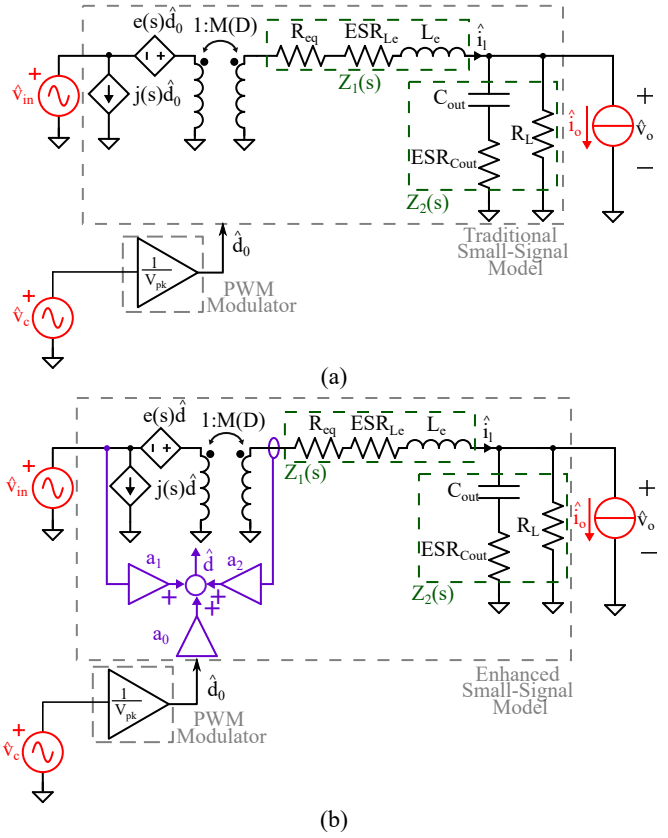

Fig. 3. Small-signal circuit models of a Boost converter power stage operating in CCM and the sawtooth-based PWM modulator. (a): without ZVS; and (b): with ZVS.

where $T_{\text{on},0}$ is the externally imposed on-time by the PWM modulator, while

$$T_d = \text{C}_{\text{MOS}} \frac{V_{\text{out}}}{I_{\text{pk}}}. \tag{2}$$

The peak-inductor current I_{pk} can be estimated through the small-ripple approximation [12] as

$$I_{\text{pk}} = I_l + \frac{V_{\text{in}}}{L} T_{\text{on},0}, \tag{3}$$

where I_l denotes the average inductor current. Substituting (3) and (2) in (1), the overall steady-state and small-signal duty-ratio expressions can be derived. This is done by replacing each quantity with a steady-state term plus a small-signal contribution, i.e.,

$$\begin{gathered} d = \hat{d} + D \qquad I_l = I_L + \hat{i}_l \qquad V_{\text{in}} = \hat{v}_{\text{in}} + V_{\text{IN}} \\ T_{\text{on},0} = T_{\text{ON},0} + \hat{t}_{\text{on},0}, \end{gathered} \tag{4}$$

and subsequently linearizing the obtained expression. As a final result, we get

$$\begin{aligned} \hat{d} &= a_0 \hat{d}_0 + a_1 \hat{v}_{\text{in}} + a_2 \hat{i}_l \\ D &= \frac{T_{\text{ON},0}}{T_{\text{SW}}} + \frac{\text{C}_{\text{MOS}} V_{\text{OUT}}}{I_{\text{PK}}} \frac{1}{2T_{\text{SW}}}, \end{aligned} \tag{5}$$

This is the author's version of the article that has been presented at IEEE MWSCAS2024
The editorial version of the paper is available at http://dx.doi.org/10.1109/MWSCAS60917.2024.10658716

TABLE I
BOOST CONVERTER COMPONENT VALUES - SIMPLIS SIMULATIONS

$R_L[\Omega]$	V_{OUT} [V]	$R_{on}^{HS}[m\Omega]$	$R_{on}^{LS}[m\Omega]$	L[µH]	C_{out}[µF]	$ESR_L[m\Omega]$	$ESR_{C_{out}}[m\Omega]$	f_{SW}[kHz]	C_{MOS}[nF]	$k_{FF}[V^2]$
37.5	15	15	15	3.3	22	30	10	750	4	30

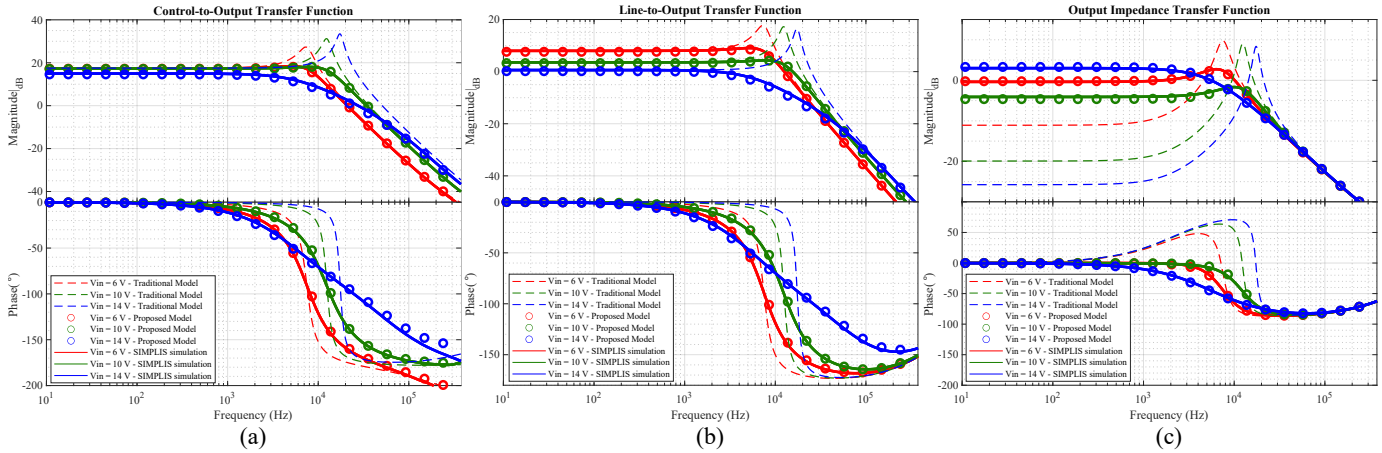

Fig. 4. Comparison between SIMPLIS simulation results and the traditional/enhanced small-signal models of the main transfer functions for different V_{in} values and the parameter values grouped in Table I. The proposed enhanced small-signal model has been validated up to $f_{SW}/2$ only for practical purposes. (a) Control-to-output transfer function $H_{vd}^{(ZVS)}(s)$. (b) Line-to-output transfer function $H_{vg}^{(ZVS)}(s)$. (c) Output Impedance $Z_{out}^{(ZVS)}(s)$.

TABLE II
TRADITIONAL SMALL-SIGNAL CIRCUIT MODEL MAIN OPEN-LOOP TRANSFER FUNCTIONS. $Z_1(s)$ AND $Z_2(s)$ ARE SHOWN IN FIG. 3(A)

$H_{PWM}(s)=\frac{\hat{v}_c}{\hat{d}_0}(s)[V^{-1}]$	$H_{vd}(s)=\frac{\hat{v}_o}{\hat{d}_0}(s)$ [V]	$H_{vg}(s)=\frac{\hat{v}_o}{\hat{v}_{in}}(s)$	$Z_{out}(s)=\frac{\hat{v}_o}{\hat{i}_o}(s)$ [Ω]
$\frac{1}{V_{pk}}=\frac{V_{IN}}{k_{FF}}$	$\frac{e_s(s)M(D)Z_2(s)}{Z_1(s)+Z_2(s)}$	$\frac{M(D)Z_2(s)}{Z_1(s)+Z_2(s)}$	$Z_1(s)\|\|Z_2(s)$

TABLE III
SMALL-SIGNAL CIRCUIT MODEL PARAMETER VALUES

L_e	ESR_{L_e}	R_{eq} [Ω]	$e_s(s)$ [V^{-1}]	$j(s)$ [A^{-1}]	$M(D)$
$\frac{L}{(1-D)^2}$	$\frac{ESR_L}{(1-D)^2}$	$\frac{R_{ON}^{HS}D+R_{ON}^{LS}(1-D)}{(1-D)^2}$	$V_{OUT}\left(1-\frac{sL}{R_L(1-D)^2}\right)$	$\frac{V_{OUT}}{R_L(1-D)^2}$	$\frac{1}{(1-D)}$

a_0	a_1 [V^{-1}]	a_2 [A^{-1}]
$1-\frac{C_{MOS}V_{OUT}V_{IN}}{4I_{PK}^2L}$	$-\frac{C_{MOS}V_{OUT}T_{ON,0}}{4I_{PK}^2LT_{SW}}$	$-\frac{1}{(1-D)^2}\frac{C_{MOS}V_{OUT}}{2T_{SW}I_{PK}^2}$

where the parameters expressions a_0, a_1 and a_2 are detailed in Table III.

The extended Boost converter small-signal circuit model is shown in Fig. 3(b). Similarly to what has been achieved in [11], the presence of the ZVS network generates: *i*) an $\hat{i}_L$ feedback-loop, due to the non-zero a_2 coefficient; *ii*) a $\hat{v}_{in}$ feed-forward path, due to the non-zero a_1 coefficient; *iii*) a gain-modulation of the control-to-duty signal path, due to the non-unitary a_0 coefficient. These additional terms can be easily appended to the traditional small-signal model without affecting its compactness and maneuverability.

IV. MODEL VALIDATION

The open-loop small-signal model is validated through a direct comparison with SIMPLIS simulation results. The exploited components values are summarized into Table I, and the previously exploited set of V_{IN} values is considered for the validation process.

A. Control-to-Output Transfer Function:

The control-to-output transfer function is derived by applying a perturbation $\hat{v}_c$ and measuring the output voltage response $\hat{v}_o$. This can be derived from Fig. 3(b) as

$$H_{vd}^{ZVS}(s)=\frac{\hat{v}_o}{\hat{d}_0}=\frac{a_0e_s(s)M(D)Z_2(s)}{Z_1(s)+Z_2(s)-a_2e_s(s)M(D)}. \quad (6)$$

The overall control-to-output transfer function is achieved as $H_{PWM}(s)H_{vd}^{ZVS}(s)$ and it is plotted in Fig. 4(a). The model captures the introduced damping-effect, which is due to the added current-feedback loop or, equivalently, to a lossless resistance at the converter output-port with value $-a_2e_s(s)M(D)$. Additionally, the $\hat{v}_c$ amplitude is also altered by the presence of the a_0 coefficient, which appears in series on the signal propagation path.

B. Line-to-Output:

The line-to-output transfer function is derived by applying a perturbation $\hat{v}_{in}$ and measuring the output voltage response $\hat{v}_o$. From the small-signal model in Fig. 3(b) it is hence possible to compute it as

$$H_{\mathrm{vg}}^{\mathrm{ZVS}}(s) = \frac{\hat{v}_o}{\hat{v}_{\mathrm{in}}} = \frac{(1 + a_1 e_s(s))M(D)Z_2(s)}{Z_1(s) + Z_2(s) - a_2 e_s(s)M(D)}. \quad (7)$$

Even then, the presence of a damping-effect due to the a_2 coefficient is evident. The a_1 coefficient further establishes an input voltage feed-forwarding term which alters the converter audiosusceptibility. The derived transfer function is plotted together with the SIMPLIS simulation results in Fig. 4(b).

C. Output Impedance:

The output-impedance transfer function is derived by applying a load perturbation $\hat{i}_o$ and measuring the output voltage response $\hat{v}_o$. From Fig. 3(b), it is possible to compute

$$Z_{\mathrm{out}}^{\mathrm{ZVS}}(s) = \frac{\hat{v}_o}{\hat{i}_o} = Z_1(s)||Z_2(s)||(-a_2 e_s(s)M(D)). \quad (8)$$

The open-loop output impedance is impacted by the introduction of a small signal resistance in the converter output port only. A comparison among the derived transfer function and the SIMPLIS simulation results is reported in Fig. 4(c).

V. Conclusion

An enhanced small-signal model for a synchronous Boost converter featuring ZVS at the HS MOSFET has been proposed. The model permits to accurately capture the dynamic impact due to the presence of the introduced ZVS network and it is suitable for controller design purposes. The validity of the model has been verified through SIMPLIS simulation results, which further confirmed the correctness of the modeling process.

References

[1] G. Hua and F. Lee, "Soft-switching techniques in PWM converters," *IEEE Transactions on Industrial Electronics*, vol. 42, no. 6, pp. 595–603, Dec. 1995. doi: 10.1109/41.475500

[2] H. Chung, S. Hui, and K. Tse, "Reduction of power converter EMI emission using soft-switching technique," *IEEE Transactions on Electromagnetic Compatibility*, vol. 40, no. 3, pp. 282–287, 1998. doi: 10.1109/15.709428

[3] S. Sharifi, M. Jabbari, and H. Farzanehfard, "A new family of single-switch ZVS resonant converters," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 6, pp. 4539–4548, 2017. doi: 10.1109/TIE.2017.2674632

[4] H. Bodur and A. Bakan, "A new ZVT-ZCT-PWM DC-DC converter," *IEEE Transactions on Power Electronics*, vol. 19, no. 3, pp. 676–684, 2004. doi: 10.1109/TPEL.2004.826490

[5] B. Majmunović, B. McDonald, S.-Y. Yu, and J. Strydom, "90°-Valley unified controller for zero-voltage-switching quasi-square-wave (ZVS-QSW) boost converter," *IEEE Transactions on Power Electronics*, pp. 1–10, 2024. doi: 10.1109/TPEL.2024.3378168

[6] J. Yu, L. Zhou, R. Shen, Z. Shi, and A. Niu, "Research on the optimal control timing of ZVS-QSW," *IEEE access : practical innovations, open solutions*, vol. 12, pp. 33 769–33 778, 2024. doi: 10.1109/ACCESS.2024.3368805

[7] J. Costa and M. Silva, "Small-signal models of quasi-resonant converters," in *ISIE '97 proceeding of the IEEE international symposium on industrial electronics*, vol. 2, 1997, pp. 258–262 vol.2. doi: 10.1109/ISIE.1997.648946

[8] J. Costa and M. Silva, "Small-signal models and dynamic performance of quasi-square-wave ZVS converters with voltage-mode and current-mode control," in *38th midwest symposium on circuits and systems. Proceedings*, vol. 2, 1995, pp. 1183–1188 vol.2. doi: 10.1109/MWSCAS.1995.510306

[9] A. Witulski, "Comparison of buck converter small signal dynamics for pulse-width modulated and quasi-resonant switches," in *Fifth annual proceedings on applied power electronics conference and exposition*, 1990, pp. 195–204. doi: 10.1109/APEC.1990.66412

[10] F.-S. Tsai, "Small-signal and transient analysis of a zero-voltage-switched, phase-controlled PWM converter using averaged switch model," *IEEE Transactions on Industry Applications*, vol. 29, no. 3, pp. 493–499, 1993. doi: 10.1109/28.222417

[11] F. Gabriele, F. Pareschi, G. Setti, R. Rovatti, D. Lena, and M. R. Borghi, "Small-signal circuit model for synchronous buck DC/DC converter featuring ZVS at low-side," in *2023 IEEE international symposium on circuits and systems (ISCAS)*, 2023, pp. 1–5. doi: 10.1109/ISCAS46773.2023.10182213

[12] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*, 2nd ed. Springer, 2001.