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Characterization Procedure for Effective Evaluation of III-V Compound Semiconductor Technology

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***Abstract*—In this paper, a characterization procedure for III-V compound semiconductor technology is proposed, with the aim of investigating the performance of state-of-the-art transistors for mm-wave applications. The whole procedure has been successfully applied to a 0.1-µm GaAs pHEMT process, which was characterized under DC, small- and large-signal operations, after a first stress experiment necessary to assess its robustness and stability.**

Keywords— GaAs, HEMT, S-parameter measurements, large-signal measurements, millimeter-wave frequency.

I. Introduction

Nowadays, high capacity and data rates are essential in many applications over the millimeter-wave spectrum as V (40 GHz – 75 GHz) and W (75 GHz – 110 GHz) frequency bands [1] - [4]. This scenario poses significant challenges to the research community that can approach the solution from different perspectives, at device or system level. One of the most important aspects of the game is the screening of the most suitable technology, which must exhibit reliable and outstanding performance for the selected application.

Since technologies such as GaN and GaAs have undergone significant advancements in recent years, aimed at optimizing their performance and reliability up to millimeter-waves, it is important to have a methodology capable of efficiently and effectively characterizing new process variants, extracting, within a reasonable amount of time, key information about the robustness of the active devices and their performance in terms of output power, efficiency, and maximum operating frequency. Equally important is the evaluation of the impact of the well-known dispersive effects on these characteristics, which is essential both for improving the technological process and for providing clear insights into the suitability of a technology for specific applications. Eventually, to meet the requirements of applications (e.g., space communications) it is important to characterize the device temperature-dependent behavior [5].

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In this paper, we propose a characterization procedure for millimeter-wave transistor technologies. The first step of the proposed procedure is the evaluation of technology robustness by means of 24-hour accelerated (i.e., at 80 °C) stress measurements under actual operating condition. This turns out to be a crucial step because, if the technology is not sufficiently stable, it is meaningless to proceed with further performance characterization or even with modeling. After that, the small-signal characterization has to be performed to extract, from the scattering parameters, key figure of merits such as f_T and maximum available gain. Eventually, large-signal low-frequency characterization is performed to evaluate, on one hand, the impact of low-frequency dispersion phenomena and, on the other hand, the performance in terms of output power, drain efficiency, dynamic breakdown voltage, etc. [6]. It is important to point out that, with the aim of reducing time and costs, high-frequency large-signal measurements are not carried out, relying on the low-frequency load-pull characterization to meaningfully assess, as demonstrated in [6], the technology performance. It is worth noticing that the proposed procedure has general validity and can be seamlessly extended also to Silicon technologies.

II. Measurement Setup

The proposed method has been applied to evaluate a state-of-the-art 0.1-µm GaAs (Gallium Arsenide) technology from United Monolithic Semiconductors (UMS). To apply the proposed methodology, fully remotely controlled DC, S-parameter and large-signal low-frequency (LSLF) measurement setups are used.

For DC and S-parameter measurements a conventional setup has been adopted. A high-resolution (4 µV; 20 fA) and accuracy (V: 0.05%, I: 0.2%) DC source (HP4155) provides the bias for the device-under-test (DUT). An Anritsu Vector Network Analyzer (VNA), with an operating frequency range from 10 MHz to 125 GHz, is used to acquire the S-parameters. Custom PC software controls the entire measurement process, setting a bias grid for gate and drain voltages and automatically

performing the DC I/V and S-parameter measurements in the whole grid within the defined safe operating area.

To perform the large-signal low-frequency characterization, the setup shown in Fig. 1 is adopted, which exploits the same DC source in combination with a 2-channel arbitrary function generator (Tektronix AFG 3252), to drive the DUT input port

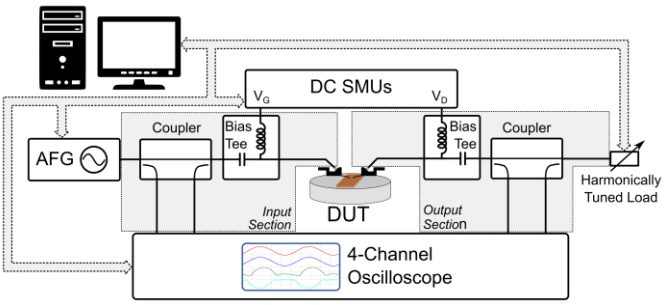

Fig. 1. Measurement setup adopted for DC and low-frequency load-pull measurements.

with incident sinusoidal (or distorted) voltage waveforms in the desired frequency range (2 MHz). Incident and reflected waves at the DUT ports are separated by two dual-directional couplers (frequency range: 10 kHz–400 MHz) and sent to a 12-bit 350-MHz 4-channel oscilloscope (Tektronix MSO54) for the acquisition. To set the output load, we use an electronically controllable tuner coupled with a frequency multiplexer, which controls the load impedance up to the third harmonic, enabling the synthesis of both conventional and high-efficiency classes of operation that require harmonic manipulation of the load. Higher harmonics see a short-circuit termination.

To calibrate the waveform data at the DUT reference plane, the signal paths (i.e., "input section" and "output section" in Fig. 1) and the RF probes have been preliminarily characterized by measuring their S-parameters. They can be easily adopted to shift the reference plane from the oscilloscope connectors to the RF probe tips. Any nonideality of the oscilloscope receivers has been considered negligible, which is a reasonable assumption considering the specification of the instrument at the operating frequency adopted for the following characterization (i.e., 2 MHz at fundamental).

Because of the low-frequency operation, the setup and its calibration remain very stable over time, thus allowing long measurement sessions without showing any sensible drifts.

III. Evaluation of Technology Robustness

Before starting the characterization of the selected technology, its robustness needs to be verified in terms of its performance stability during operation. To this aim, we performed a preliminary stress measurement on a fresh device sample. The adopted setup, reported in Fig. 1, implements a time-domain oscilloscope-based load-pull system operating in the megahertz range. This enables the direct characterization of the active part of the transistor, since the reactive effects are negligible for the investigated technology at these frequencies. Its operation above the cut-off frequency of trap and thermal effects allows collecting data consistent with the DUT microwave operation, providing access to variables hidden at high frequency, such as the instantaneous resistive gate current, which is commonly assumed as one of the most sensitive parameters to device degradation [7].

The selected DUT is a 6x40-µm pHEMT, mounted on a brass carrier. The stress condition has been set by applying a realistic class-AB load line (V_D = 3 V, I_D = 26 mA, and load = 37.7 Ω) at 2 MHz, which provides an output power of 17.16 dBm with a drain efficiency of 47.7 %. This condition has been kept applied to the transistor for a total of 24 hours at a carrier temperature of 80 °C, periodically monitoring the input and output waveforms and evaluating the device performance. Using the same setup, DC measurements have been carried out before and after the 24-h stress test to check for significant degradation effects, such as the shift of the threshold voltage and the breakdown walkout [6]. The results of this characterization are reported in Fig. 2. The data show excellent performance in terms of device stability, with minimal variations of the reported parameters. A slight change of the load line after the stress is reported in Fig. 2a, possibly related to a small shift of the threshold voltage, visible in Fig. 2d and estimated in 20 mV. This produces a minor reduction of the output power (about -0.1 dB after 24 h), and no significant variation of the efficiency. The very good stability of the technology can be clearly appreciated in Fig. 2e, where the sub-threshold gate current is reported: despite its sensitivity to device degradation, no appreciable change is observed. These results confirm the robustness of the investigated technology, hence ensuring that the following characterization campaign provides accurate and representative results.

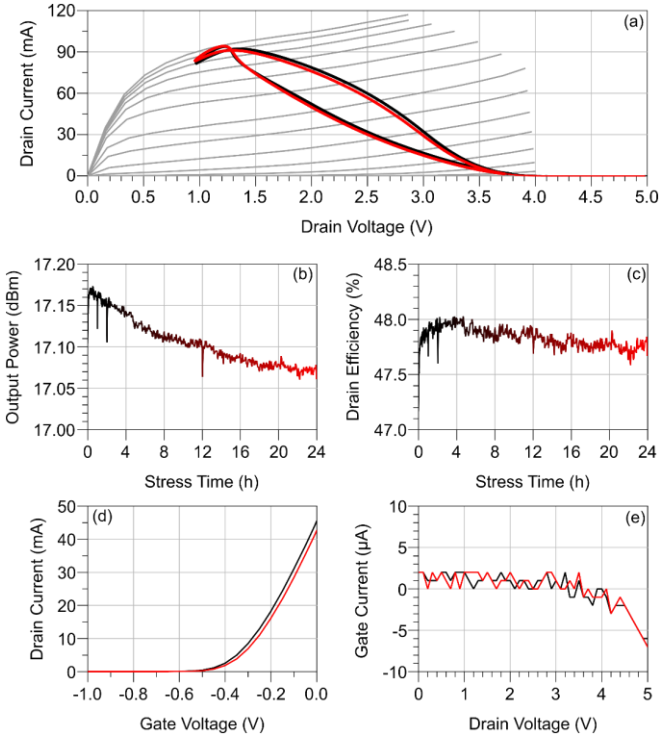

Fig. 2. Stress measurement results: (a) class-AB stress load line at 2 MHz and preliminary DC characteristics; (b) output power and (c) drain efficiency vs stress time; (d) I_D-V_G transcharacteristic at V_D = 3 V; (e) I_G-V_D

transcharacteristic at V_G = -1 V. In (a), (d) and (e), data acquired before (black lines) and after (red lines) the 24-h stress measurement are reported.

IV. Technology Performance Evaluation

After assessing the technology stability, the full characterization can be performed. DC characterization is performed on a 6x40-µm fresh sample of the same wafer. The DC I_D-V_D and I_D-V_G characteristics are shown in Fig. 3, measured at two different temperatures: 30 °C and 80 °C.

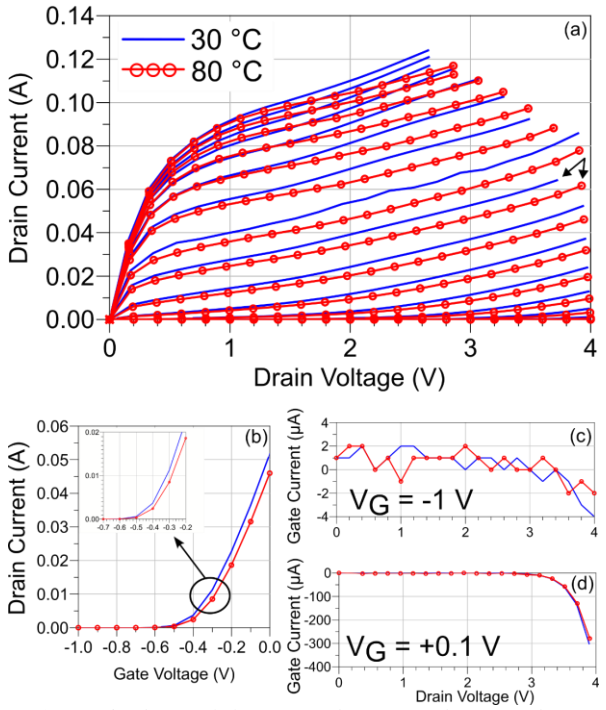

Fig. 3. (a) DC I/V characteristics measured at 30 °C and 80 °C on the 6x40 µm pHEMT. V_G from -1 V to 0.8 V with step 0.1 V, and V_D from 0 V to 4 V with step 0.2 V. Black arrows highlight the V_G = 0 V. (b) Focus on theresold voltage I_D Vs V_G at V_D = 3 V.

The trend of variation with temperature seems the usual one, since the drain current decreases by increasing the temperature. Variations on gate current are not significant, which is another indicator of the technology robustness, consistently with the results of the stress measurement. This behavior suggests a moderate impact of trapping effects on dynamic I-V characteristics. S-parameter measurements are reported in Fig. 4 and Fig. 5. The frequency range under investigation is 1-120 GHz, with a frequency step of 250 MHz.

The S-parameter measurements have been carried out, using TRL calibration, in the same bias grid of the DC I-V characteristics in Fig. 3. Fig. 4 shows the S-parameters at a constant drain bias of 3 V and for gate bias from -0.6 V to 0.6 V with step 0.1 V. Fig. 5 shows the short-circuit current gain (h_{21}) and the maximum available/stable gain (MAG/MSG) for the class-A bias corresponding to V_G = -0.1 V, V_D = 3 V, I_D = 30 mA. The f_T of the transistor, estimated from h_{21}, is about 83 GHz.

S-parameters have been also measured at 30 °C and 80 °C on the same 6x40-µm device, at a constant voltage of 3 V and for gate bias from -0.6 V to 0 V. Fig. 6 shows the results. As the plots show, the variation with temperature is as expected, with a slight reduction of the gain (i.e., S_{21}), an increase of the output impedance (see S_{22}), and a slight deterioration of S_{12}, whereas no important changes are visible on the S_{11}. In agreement with previous results, temperature effects on the device behavior are limited, confirming the high level of technology performance.

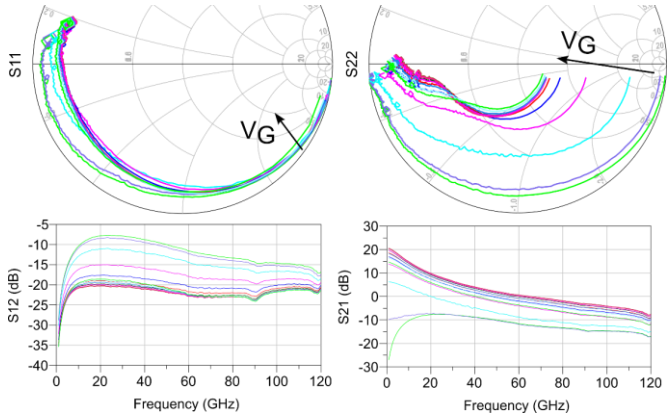

Fig. 4. Measured S-parameters for the 6x40-µm pHEMT from 1 GHz to 120 GHz, V_G = -0.6 V ÷ 0.6 V step 0.1 V, V_D = 3 V.

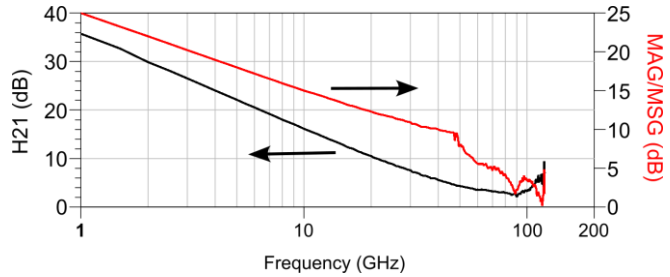

Fig. 5. Magnitude of h_{21} parameter and MAG/MSG for the 6x40-µm pHEMT from 1 GHz to 120 GHz at V_G = -0.1 V, V_D = 3 V, I_D = 30 mA. Dashed line is the linear extrapolation of h_{21} to 0 dB.

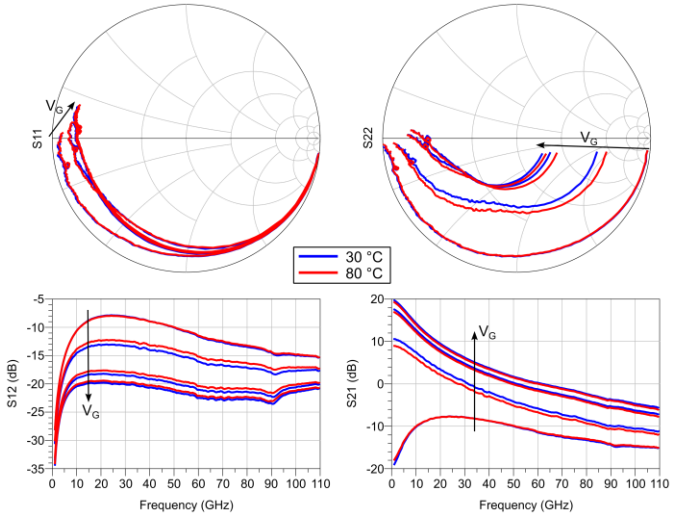

Fig. 6. Measured S-parameters for the 6x40-µm pHEMT from 1 GHz to 110 GHz at 30 °C and 80 °C, V_G = -0.6 V ÷ 0 V step 0.2 V, V_D = 3 V.

The last step of the proposed procedure involves the large-signal characterization at low frequency, using the setup in Fig. 1. It is worth noticing that characterizing the transistor at such a low frequency enables the accessing of the current generator so that the performance in terms of output power and drain efficiency can be accurately evaluated [6]. Fig. 7 shows the LSLF characterization of another fresh 6x40-µm device at the bias V_G = -0.25 V, V_D = 3 V, I_D = 11 mA for two temperatures, i.e., 30 °C and 80 °C. Different load conditions are synthesized for increasing input power levels. It can be seen that, as temperature increases, both output power and drain efficiency decrease, except for operations close to saturated output power. Indeed, the maximum output power reached at f_0 = 2 MHz at 30 °C is 16.8 dBm with a drain efficiency of 51.5 % and at 80 °C is 16.4 dBm with a drain efficiency of 50.5 %.

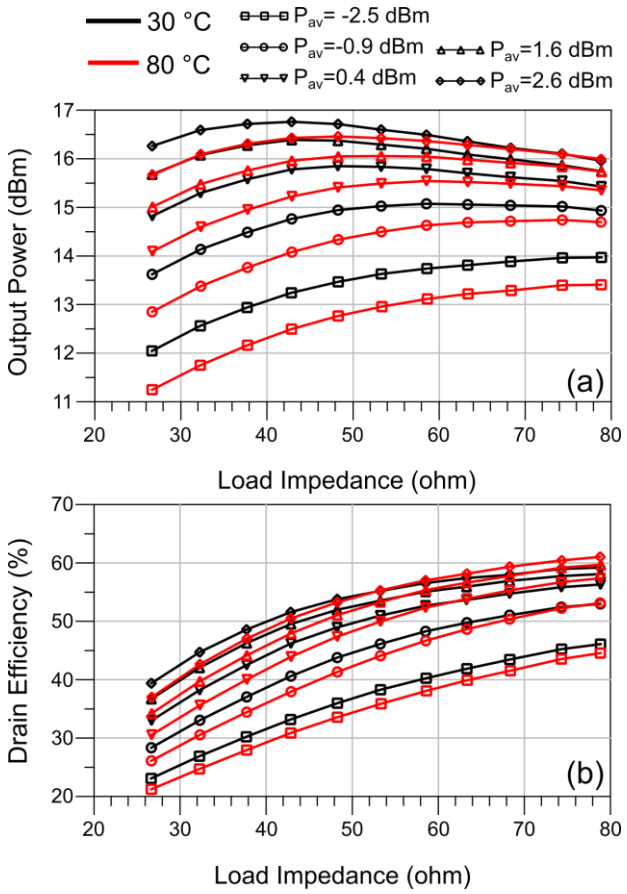

Fig. 7. (a) Output power and (b) drain efficiency measured on the 6x40-µm GaAs pHEMT at f_0 = 2 MHz for two temperatures: 30 °C (black) and 80 °C (red). Bias is V_G = -0.25 V, V_D = 3 V, I_D = 11 mA. The load impedance is swept from 25 Ω to 80 Ω and input power from -2.5 dBm to +2.6 dBm.

Fig. 8 and Fig. 9 show the load lines and the drain and gate time domain waveforms corresponding to the highest input-power level at 30 °C and 80 ° C, respectively (i.e., P_{av} = 2.6 dBm, corresponding to a gate voltage peak of 0.6 V). A slight knee walkout can be appreciated from Fig. 8a, where the DC I-V characteristic at V_G = 0.6 V has also been reported. At 80 °C the same slight knee walkout is visible in Fig. 9a where the DC I-V characteristic at 80 °C and V_G = 0.6 V has also been reported.

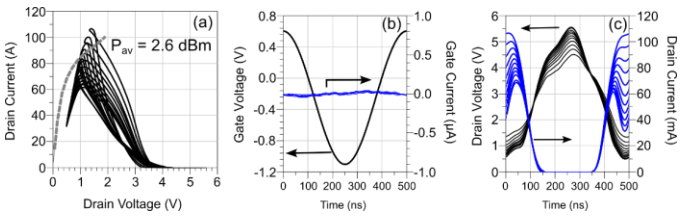

Fig. 8. (a)Load lines, (b) gate and (c) drain voltage and current waveforms measured on the 6x40-µm GaAs pHEMT at f_0 = 2 MHz, V_G = -0.25 V, V_D = 3 V, I_D = 11 mA for the constant input power 2.6 dBm, by sweeping the load impedance from 25 Ω to 80 Ω. Temperature is 30 °C.

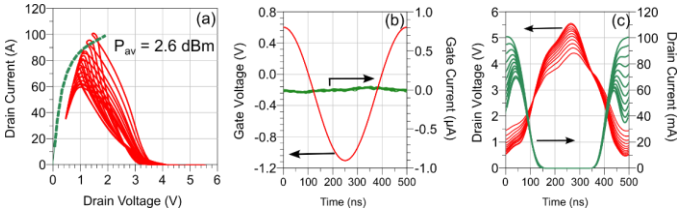

Fig. 9. (a)Load lines, (b) gate and (c) drain voltage and current waveforms measured on the 6x40-µm GaAs pHEMT at f_0 = 2 MHz, V_G = -0.25 V, V_D = 3 V, I_D = 11 mA for the constant input power 2.6 dBm, by sweeping the load impedance from 25 Ω to 80 Ω. Temperature is 80 °C.

V. Conlcusion

A characterization procedure for investigating the DC, small- and large-signal performance of III-V compound semiconductor technology for mm-wave applications has been proposed. The procedure has been applied to a representative sample of a 0.1-µm GaAs pHEMT technology demonstrating its robustness and state-of-the-art performance.

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