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Active Thermal Balancing Strategy for Direct Parallel Connection of SiC MOSFETs

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ABSTRACT silicon carbide (SiC) MOSFETs are increasingly favored in high-power density applications due to their superior thermal and electrical performance compared to Si-IGBTs. However, current ratings of individual SiC MOSFET dies are limited, requiring multiple devices in parallel to meet high-current demands, as is typical in traction applications. Parallel operation introduces current and thermal imbalances related to parameter mismatches and layout asymmetries, which degrade reliability and efficiency. This article presents the extensive investigation of a new active thermal balancing control strategy that dynamically adjusts device duty cycles using case temperature feedback. Experimental validation demonstrates significant enhancements in thermal equilibrium and robust performance of parallel-connected SiC MOSFETs under switching transients at the limit of the device safe operating area. Results confirm effective switching loss redistribution without impacting overall efficiency. Consequently, the strategy removes thermal imbalance as a limiting factor in parallel SiC MOSFET operation, mitigating localized thermal overstress, promoting uniform device utilization across the parallel set, and improving long-term reliability by preventing persistent temperature gradients caused by parameter dispersion and commutation-loop asymmetries.

INDEX TERMS Active temperature balance, parallel connection, silicon carbide (SiC) MOSFET, safe operating area (SOA).

I. INTRODUCTION

Wide bandgap semiconductors such as SiC MOSFETs are increasingly favored for power electronic converters due to their excellent thermal performance, superior tradeoff between high voltage rating and conduction properties, and fast switching speeds [1], [2]. Their reduced switching losses yield higher efficiency and power density than Si-IGBTs, while their voltage and thermal headroom extends these gains to regimes where silicon is constrained, driving an ongoing replacement of Si devices in high-power, high-frequency applications [3]. However, the adoption of SiC MOSFETs presents challenges, particularly the limited current capacity of a single die (around 200 A) caused by manufacturing constraints like defect density and wafer yield [4], [5], [6]. Therefore, multiple SiC MOSFETs are often connected in parallel, either as discrete devices or within multichip modules, to achieve higher current ratings [7], [8].

Parallel operation introduces current and thermal imbal-

ances that originate from both circuit asymmetries and device parameter variations. During the switching transients, unequal common-source and power-loop parasitic inductances unbalance the dynamic current sharing among the paralleled devices [9], [10], while dispersion in device parameters, such as threshold voltage and transconductance unbalances both the static and dynamic current, an effect amplified by the relatively immature SiC manufacturing process compared to Si-based devices [11]. The resulting current mismatch produces an uneven distribution of switching losses and, in turn, of device temperatures. Additionally, it also lowers the robustness of the parallel group under stress conditions, where deviations between devices may impose additional derating [12]. The excessive heating caused by these imbalances can therefore compromise the system reliability and lifetime. Several mitigation solutions have been proposed in the literature [13].

These include **passive balancing methods**, such as chip

screening for parameter matching (e.g., $R_{DS,ON}$, $V_{GS,th}$, g_{fs})

[14], [15], [16], and tuned external components like differential inductors or decoupling capacitors to suppress circulating currents [19], [20]. While effective, passive approaches lack real-time adaptability and are subject to parameter degradation over time [17], [18]. Moreover, they introduce additional parasitics into the commutation loop.

In contrast, **active balancing methods** regulate the switching events in real-time by adjusting gate voltage, gate current, or switching instants, typically via active gate drivers (AGDs) or digital [e.g., field-programmable gate array (FPGA)-based] feedback [21], [22], [23]. In [21], an analog AGD senses the switching disparity among the devices from the Kelvin-source voltage, proportional to di/dt , and injects or sinks gate current to anticipate or delay the appropriate device and equalize dynamic current at nanosecond-scale, but requires high-bandwidth (HBW) analog sensing and careful calibration. Multilevel AGDs extend the above by imposing multiple gate-voltage levels to improve both static and dynamic current sharing, at the expense of additional hardware and control overhead, raising implementation complexity [22]. FPGA-based timing-synchronization schemes detect parasitic-induced timing skew and align switching edges at high resolution, mitigating transient current overshoot [23].

Beyond current-based feedback, temperature-centric strategies regulate or equalize junction temperatures of individual dies, enhancing thermal balance but relying on temperature-sensitive electrical parameter (TSEP)-based estimation, whose on-line use at high di/dt is compromised by bandwidth and parasitic inductance sensitivity, with estimator accuracy affected by device aging unless recommissioned [24], [25], [26]. Complementarily, active temperature management via equivalent gate-resistance control shapes switching loss to attenuate low-frequency ΔT_j , with a tunable reliability-efficiency tradeoff, providing a hardware-efficient regulator when device-level temperature moderation, rather than per-die current balancing, is the primary objective [27]. Overall, these methods have proven effective in both static and dynamic current sharing or thermal balancing. However, they can introduce significant cost and complexity, especially in high switching frequency, where accurate timing and current sensing are crucial. A comparison of representative passive and active balancing approaches, including the proposed method, is summarized in Table I

The present paper builds on the simple thermal balancing method first proposed by the authors in [28] to develop an innovative active thermal balancing control strategy that dynamically adjusts duty cycles to equalize the case temperatures of parallel-connected SiC MOSFETs. The proposed control method equalizes temperatures, improves loss distribution, and enhances system reliability. The new contributions in comparison to the conference work are:

- 1) *Selective Compensation Methods*: Beyond the symmetrical compensation method introduced in [28], two novel selective duty-cycle compensation methods (turn-ON and turn-OFF) are introduced, identifying their

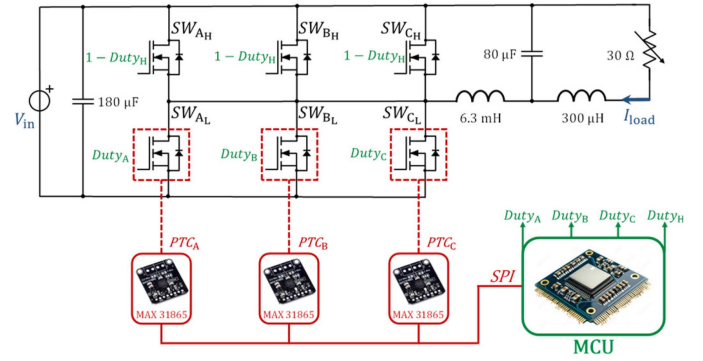


FIGURE 1. Functional schematic of the proposed setup.

physical balancing mechanism and comparing their effectiveness.

- 2) *Robustness and Safe Operating Area (SOA) Validation*: Dedicated double-pulse tests at the device maximum current rating are introduced to rigorously validate the strategy under intentionally induced transient current imbalances, and to confirm its robustness and SOA compliance.
- 3) *Switching-Loss Redistribution Analysis*: A quantitative analysis from the double-pulse test (DPT) results shows that the compensation redistributes switching losses among the switches while leaving total switching loss essentially unaffected.
- 4) *Systematic Regulator Calibration*: A systematic design procedure for the integral gain of the thermal-balance regulator is derived from the experimentally extracted switching loss versus duty-cycle sensitivities.
- 5) *Dedicated Dead-Time Management*: A refined dead-time strategy is implemented to ensure reliable operation despite the individual duty-cycle offsets, without introducing excessive control complexity.

The rest of the article is organized as follows: Section II introduces the proposed control strategy, Section III details the main experimental setup, Section IV presents comparative experimental results, Section V describes the system identification and calibration of the thermal balance regulator and verifies the robustness of the proposed technique. Finally, Section VI concludes with key advantages over existing techniques and future work.

II. PROPOSED CONTROL STRATEGY

A. SYSTEM OVERVIEW

The proposed system consists of a half-bridge converter with three parallel-connected SiC MOSFETs for both the low and high-side switches (see Fig. 1). A dedicated gate driver controls each low-side MOSFET, while the high-side devices share a common driver. A voltage generator supplies the converter, while the load consists of a variable resistor connected via an LCL filter. In the experiments, the load current is always positive (i.e., entering the switching node) so that only the low-side devices operate in hard-switching mode while the

TABLE 1. Comparison of Passive and Active Balancing Methods for Parallel-Connected SiC mosfets

Ref.	Method	Class	Balancing Target	Sensing	Complexity	Advantages	Limitations
Ke et al. [15]	Chip screening / classification	Passive	Dyn. current	None (offline device sorting)	Low-no added hardware	Reduces initial parameter-driven imbalance	No real-time adaptability, large sorting population
Zeng et al. [19]	Differential-mode choke	Passive	Dyn. current	None	Medium-passive magnetic component, requires magnetic design	Low cost; no control loop	Adds magnetics/parasitics; not adaptive
Qu et al. [20]	Optimized power-loop layout	Passive	Dyn. current	None	Medium-custom layout	Improves transient sharing and thermal uniformity	Fixed at design stage; layout-specific
Wang et al. [21]	Analog AGD	Active	Dyn. current	Per-device common-source inductance voltage	High-custom GD per device	Real-time dynamic current balancing	HBW analog sensing and calibration
Wei et al. [22]	Multilevel AGD	Active	Static + Dyn. current	Per-device current	Very high-multi-level GD IC per device	Balances both static + dynamic current	Large hardware and control overhead
Takagi et al. [23]	FPGA edge-timing synchronization	Active	Dyn. current	Per-device common-source inductance voltage edge	High-FPGA detectors per device	Precise edge alignment; robust to aging	Detection hardware and per-device tuning
Ewanchuk et al. [24]	GD with selective die activation	Active	T_j	Per-die T_j estimation (TSEP-based)	High-multi-die driver + estimator	Die temperature equalization; raises usable current	Sensitive to T_j estimation accuracy and aging
Prop.	Per-device duty-cycle offset	Active	T_{case}	Per-device T_{case} (LBW thermal sensor)	Medium-individual drivers + MCU	LBW sensing, no TSEP estimation; insensitive to aging and symmetric-layout	Per-device sensor and driver; needs calibration

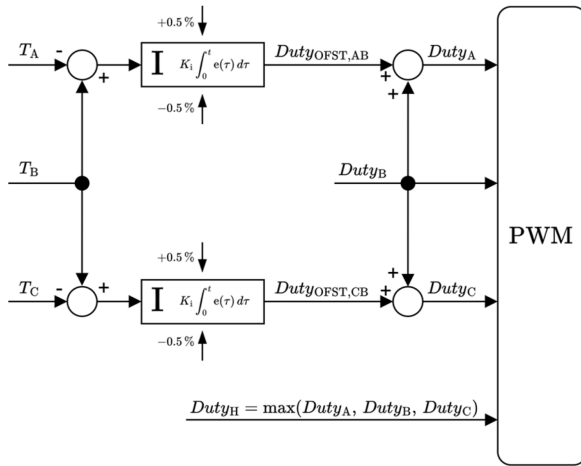


FIGURE 2. Functional schematic of proposed temperature balancing technique.

high-side devices operate in soft switching mode (i.e., not thermally critical). The **case temperatures** of each of the low-side MOSFETs are monitored via platinum resistance temperature detector (RTD) temperature sensors. The choice of the case temperature rather than estimating junction temperature is motivated by robustness: T_{case} can be directly measured with a low-bandwidth sensor, is insensitive to commutation parasitics and aging-induced drift that affect TSEP-based estimation, and accurately follows the slow thermal dynamics that the balancing loop must regulate.

B. THERMAL BALANCING CONTROL

Fig. 2 shows the functional schematic of the proposed control strategy. The low-side device B_L is arbitrarily selected as the thermal reference, while two purely integral regulators control the remaining devices, each minimizing the temperature difference $T_{B_L} - T_x$, $x = \{A_L, C_L\}$ with respect to the reference, by adjusting the corresponding duty-cycle offset. The resulting offsets redistribute switching losses from the hotter

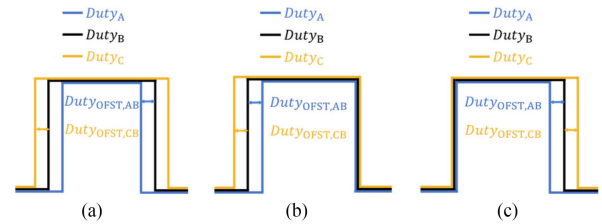


FIGURE 3. Representation of duty-cycle offsets from reference $Duty_B$. (a) Symmetrical turn-on compensation. (b) Selective turn-on compensation. (c) Selective turn-off compensation.

devices toward the cooler ones, progressively reducing the thermal imbalance within the group. This approach enables real-time compensation for thermal imbalances arising from device parameter variations or layout asymmetries. Since the regulators operate on differential temperatures, the choice of reference device does not affect the balancing outcome, it only determines the sign and magnitude of the individual offsets. Three compensation techniques are proposed as follows.

- 1) *Symmetrical Compensation*: Offsets are symmetrically introduced to the turn-ON and turn-OFF transitions [see Fig. 3(a)].
- 2) *Turn-ON Compensation*: Offsets are synchronized to the turn-ON transitions [see Fig. 3(b)].
- 3) *Turn-OFF Compensation*: Offsets are synchronized to the turn-OFF transitions [see Fig. 3(c)].

While the low-side switches are driven with individual duty-cycle commands, a single common duty cycle is applied to all high-side switches. The high-side duty cycle $Duty_H$, visible in Fig. 4, is selected as the maximum among the low-side duty cycles, thus ensuring no risk of short circuits. The duty-cycle offset is limited to ± 0.5 p.u%, corresponding to a maximum timing shift of ± 50 ns at $f_{sw} = 100$ kHz. As verified by the DPT analysis in Section V, this range is sufficient to induce full device transient current redistribution during switching, while ensuring that the proposed thermal balancing

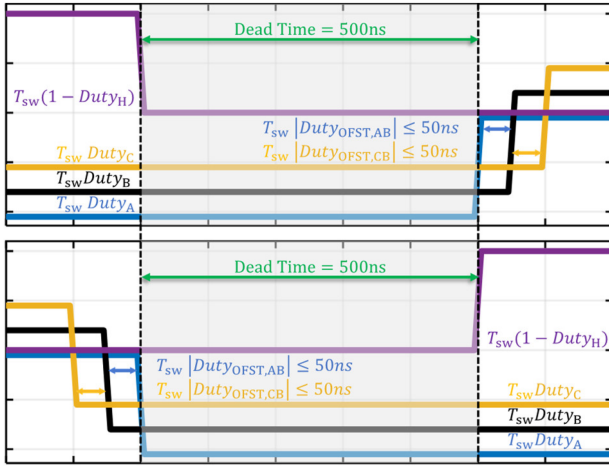


FIGURE 4. Turn-on and turn-off driving signals for the symmetrical compensation case. A dead time of 500 ns is dictated by the last device turn-OFF, so that the first turn-ON transition is always 500 ns from the last turn-OFF.

approach maintains device operation within datasheet-defined transient current and thermal limits.

The regulator's integral gain K_i is calibrated using the device thermoelectrical model, experimentally extracted. The full procedure for the design of K_i is presented in Section V-C.

The dead time was set as a fixed 500 ns interval between the last device to turn-OFF (accounting for all compensation offsets) and the first device to turn-ON, ensuring shoot-through immunity. For example, Fig. 4 shows the dead time introduced for the case of symmetrical compensation, where the dead time window is enforced after all turn-OFF transitions finish, before the first turn-ON transition occurs.

III. EXPERIMENTAL SETUP

The experimental setup represented in Fig. 5(a) comprises the Custom Power Board, the microcontroller unit (MCU) Board, the LCL filter, and the load resistance. The power board is a half-bridge converter made with three parallel-connected IMZ120R030M1H 30 mΩ CoolSiC 1200 V SiC trench MOSFETs by Infineon. The MCU embeds high-resolution timers (192 ps) for fine duty-cycle adjustments. Considering the switching frequency of 100 kHz and dead time of 500 ns, this corresponds to a 0.002% discretization of the duty cycles. The paralleled devices are visible in Fig. 5(b). The case temperature of each power device is monitored by a platinum-based RTD element (1 kΩ NB-PTCO-192). Each element is read by a dedicated MAX31865 RTD-to-digital converter, which communicates with the MCU over a multislave SPI interface. The temperature values are sampled by the control interrupt service routine at 20 kHz and are digitally low-pass filtered before being used by the thermal regulators. Among the devices, all sensors are placed at the same package location, specifically to the front case surface above the source-tab region, as indicated in the manufacturer's bonding diagram (see Fig. 6), and exhibit negligible long-term drift (below 0.03% after 1000 h at 300 °C). Sensor-to-sensor offset mismatch is

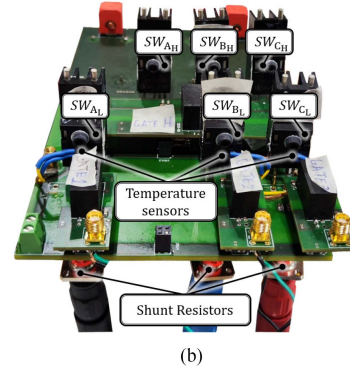
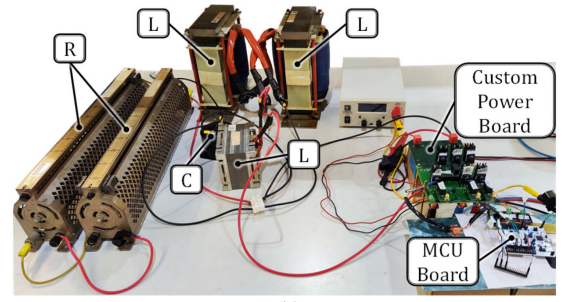


FIGURE 5. (a) Overview of the experimental setup. (b) Custom power board with parallel SiC MOSFETs and temperature monitoring.

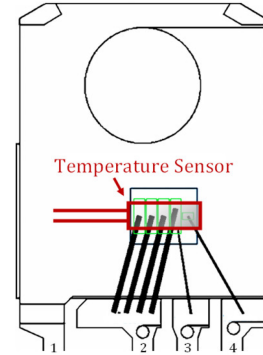


FIGURE 6. Internal bonding diagram of TO-247-4 package showing the placement of the platinum RTD temperature sensor mounted on the front case surface above the source tab (pin 2).

removed by a one-time offset initialization performed at thermal equilibrium before each test, so that the balancing loop acts only on relative case-temperature differences. Because the regulators are purely integral with a loop crossover well below the thermal pole, the measurement chain is insensitive to high-frequency noise and tolerant to small static errors. Each power device has an individual heatsink. A dedicated double-pulse-test setup was later used to focus on individual turn-ON losses at the limits of the SOA current of the devices, as presented in Section V.

IV. COMPARATIVE RESULTS AT CONSTANT CURRENT

Constant load current tests are performed to evaluate the performance of the proposed thermal balancing control. The tests were conducted for four scenarios

- 1) No compensation.

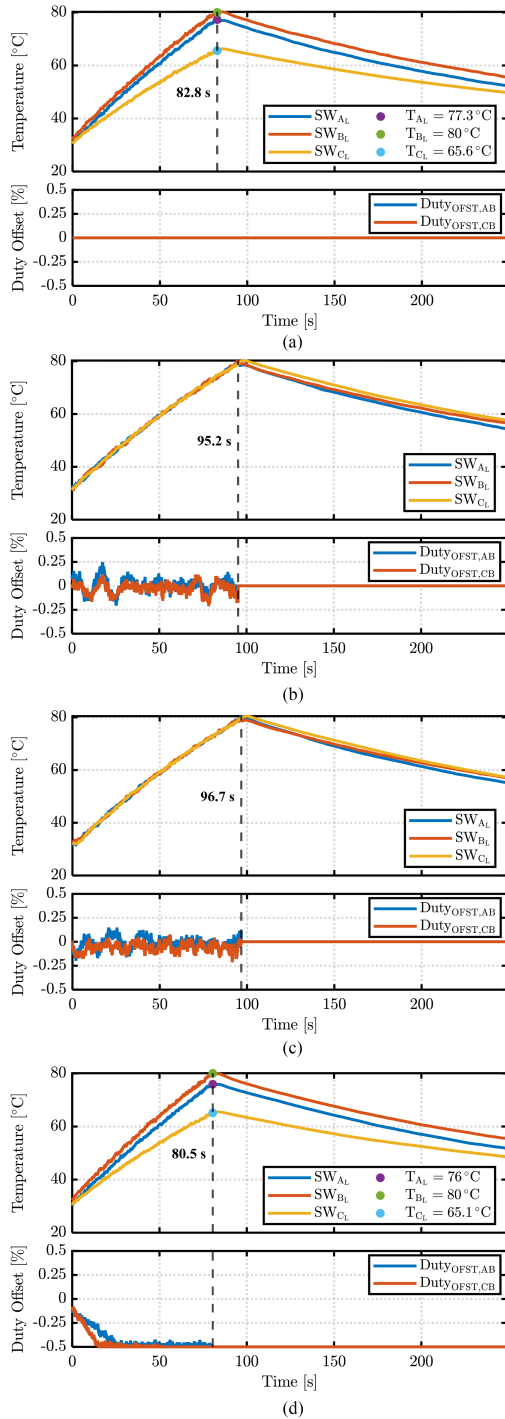


FIGURE 7. Temperatures and duty-cycle offsets of the low-side switches during the constant load current test. (a) Active temperature balance off. (b) Symmetrical duty-cycle compensation. (c) Selective turn-ON compensation. (d) Selective turn-OFF compensation.

- 2) Symmetrical compensation.
- 3) Turn-ON compensation.
- 4) Turn-OFF compensation.

Test conditions refer to: $R_{g,ON} = R_{g,OFF} = 39 \, \Omega$; $R_{load} = 30 \, \Omega$; $V_{in} = 500 \, V$; and $Duty_{ref} = Duty_B = 55\%$ resulting in a constant load current of 6 A with a load resistor of 30 Ω . The switching frequency is $f_{sw} = 100 \, kHz$,

while the frequency of the control's interrupt service routine is $f_{ISR} = 20 \, kHz$.

A. CONSTANT-CURRENT TEST

The results obtained from the constant load current test for the four cases are shown in Fig. 7. For each test, all devices start at room temperature conditions, and the test ends when the case temperature of one of the devices reaches 80 °C, to avoid damaging the system.

Fig. 7(a) refers to the case without thermal compensation: a thermal imbalance of 14.4 °C occurred between device B_L and device C_L , reaching the 80 °C limit after 82.8 s.

Fig. 7(b) refers to symmetrical compensation: thermal balance was achieved, thus enabling the extension of the time to reach 80 °C to 95.2 s. The bottom plot of Fig. 7(b) shows the correcting $Duty_{OFST,AB}$ and $Duty_{OFST,CB}$ signals imposed by the integral compensator to maintain the thermal balance. It can be observed that the steady-state compensation is very low, below 0.25% of the duty cycle.

Fig. 7(c) refers to turn-ON compensation. Case temperatures are again equalized, and the 80 °C limit is reached after 96.7 seconds. Similar to the previous case, the duty-cycle compensation does not exceed 0.2% of the duty cycle, resulting in a negligible impact on the load voltage.

Fig. 7(d) refers to turn-OFF compensation: in this case, the balancing effect proves to be ineffective, as a thermal imbalance of 14.9 °C occurred between device B_L and device C_L , and the 80 °C temperature limit is reached after 80.5 s. The duty-cycle compensation signals reported in the bottom plot reach the saturation limit set to -0.5% .

B. RESULTS ANALYSIS

The turn-ON and symmetrical compensation methods effectively equalized the temperatures of the devices. Conversely, turn-OFF compensation was not effective because, for the investigated SiC MOSFET, the turn-OFF losses are negligible in comparison to turn-ON losses, as indicated in the device datasheet [29]. Therefore, it is evident that in the symmetrical compensation technique, where the applied duty-cycle offset is split between the turn-ON and turn-OFF edges, only the turn-ON component of the command contributes appreciably to the redistribution of thermally-relevant switching losses. The turn-OFF component therefore contributes little to the balancing action, reducing the effective use of the commanded duty-cycle correction.

As a result, the symmetrical strategy requires a larger overall duty-cycle offset than the selective turn-ON strategy to achieve the same effective thermal equilibrium. This explains the slightly better performance of the selective turn-ON strategy, which applies the entire correction to the dominant loss-producing transition and therefore achieves a slightly larger extension of the time to the 80 °C limit than the symmetrical strategy (96.7 s versus 95.2 s). Thus, for the tested device, whose switching stress is dominated by turn-ON losses, selective turn-ON compensation is the preferred implementation. It should be noted, however, that this conclusion is linked to the loss distribution of the selected device;

for devices in which both turn-ON and turn-OFF transitions contribute significantly to the switching losses and thermal stress, the symmetrical compensation strategy may become preferable.

The results of the constant-current tests suggest further investigation of individual currents and switching losses, and how they redistribute under active temperature balancing, since at the selected switching frequency of 100 kHz, the switching losses constitute the predominant component of total device losses, in comparison to conduction losses.

C. INDIVIDUAL SWITCHING LOSS MEASUREMENT

The current of each low-side device was measured during turn-ON commutation, using three coaxial SDN-414-01 shunt resistors (10 mΩ, 400 MHz bandwidth, 1 ns rise time). The resistance of each shunt was individually characterized, and the measured value—within approximately 1% of the nominal 10 mΩ—was used as the corresponding per-channel scale factor when converting the measured voltage to current. The drain-source voltages were acquired with matched passive probes. Since the passive probes and coaxial shunts exhibit closely matched, low propagation delays, and the channel-to-channel skew of the oscilloscope is below 100 ps, no additional interchannel deskewing was applied. All waveforms were captured with a Rohde and Schwarz MXO 58 oscilloscope (8-channel, 100 MHz analog bandwidth, 12-bit vertical resolution), and the switching energies were obtained by integration of the instantaneous product of the measured V_{DS} and I_D over a fixed common time window, applied identically to all devices and all compensation cases. The recorded turn-ON transients exhibit 10%–90% durations in the range of 20–30 ns for both the V_{DS} fall and the I_D rise, several times longer than the 3.5 ns rise time of the 100 MHz analog bandwidth, limiting the finite-bandwidth error in the energy integral to below approximately 2%. The residual uncertainty is thus dominated by the shunt tolerance ($\approx 1\%$) and this finite-bandwidth term ($< 2\%$); as both are common to the three nominally identical channels and every compensation case, the relative redistribution of switching losses and the constancy of the total switching loss are preserved.

The turn-ON switching transients were captured with and without compensation to evaluate how the controller redistributes switching losses to compensate for thermal imbalance. It must be noted that the waveforms were acquired at specific instants during the constant-current test, during which the compensator-induced duty-cycle offsets can vary between positive and negative values [e.g., Fig. 7(b) (bottom plot) shows the continuous adjustment of the offset duty cycle].

D. TURN-ON LOSS DISTRIBUTION

Fig. 8 shows the oscilloscope waveforms during the turn-ON transient for each control technique.

- 1) *Without Compensation* [see Fig. 8(a)]: All three low-side devices operate with the same duty cycle, turning ON simultaneously. Case temperatures are not equalized, in line with the results of Fig. 7(a). The results

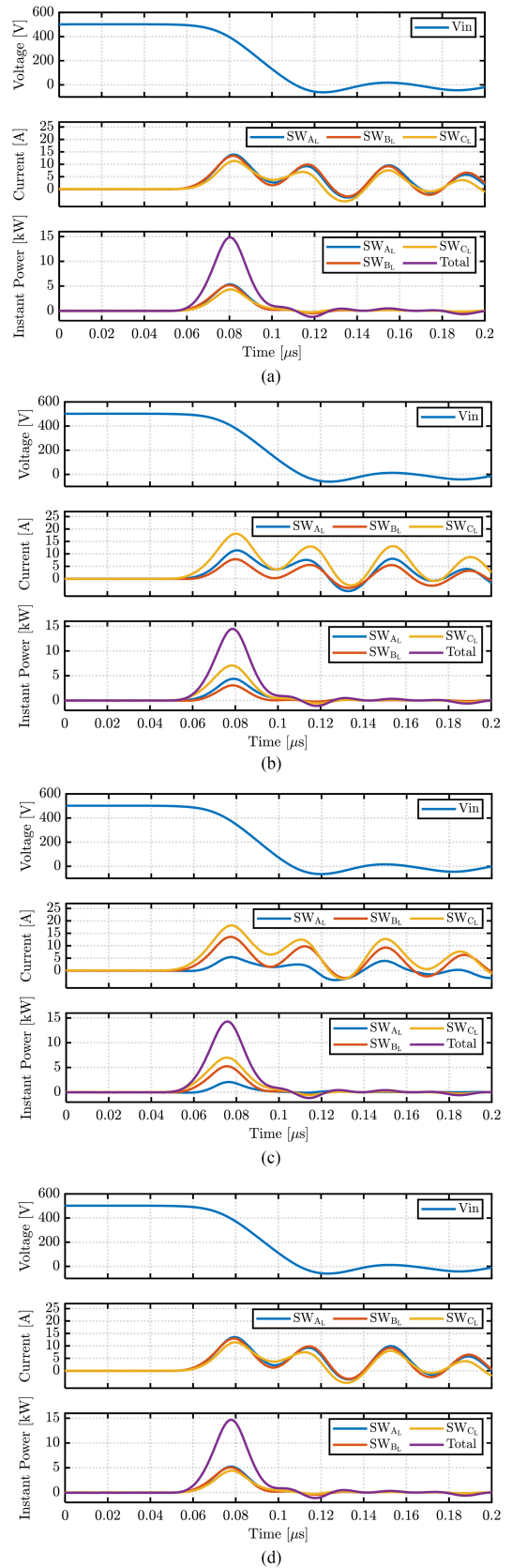


FIGURE 8. Current and instant power of the low-side devices during turn-ON. (a) No compensation. (b) Symmetrical compensation. (c) Selective turn-ON compensation. (d) Selective turn-OFF compensation.

show that switching losses are evenly distributed among the devices.

- 2) *Symmetrical Duty-Cycle Compensation* [see Fig. 8(b)]: The compensator identifies the temperature imbalance and anticipates the turn-ON of CL and AL relative to BL. This is in line with what was shown in Fig. 7(a) and (b), where without compensation, CL and to a lesser extent AL tended to operate at a lower temperature with respect to BL.
- 3) *Selective Turn-on Compensation* [see Fig. 8(c)]: The thermal compensator detects the temperature imbalance among the devices and anticipates the turn-ON command of CL, while delaying the turn-ON command of AL, relative to BL. As a result, turn-ON losses are mostly on CL and BL, while device's AL losses are significantly reduced. This effectively redistributes the turn-ON switching losses, minimizing the thermal imbalance.
- 4) *Selective Turn-off Compensation* [see Fig. 8(d)]: The turn-ON is simultaneous, with no redistribution of switching losses (i.e., this technique does not impact the turn-ON time). The waveforms are like the case without thermal compensation.

E. TURN-OFF LOSS DISTRIBUTION

As mentioned above, the SiC MOSFET datasheet [29] deems the turn-OFF switching losses marginal with respect to turn-ON and total switching losses. In addition, especially at low load currents, the dominant contribution to the turn-OFF switching energy E_{off} is the output capacitance charge energy E_{oss} , which is independent of the timing shifts introduced by the compensation. Therefore, while the compensation alters the switching instants, the E_{oss} remains unchanged, making the turn-OFF compensation technique ineffective in redistributing thermal loads under these conditions.

F. CURRENT BALANCING VERSUS THERMAL BALANCING

The results show that active thermal balancing improves converter utilization by enforcing uniform temperatures among paralleled devices, thereby alleviating localized thermal over-stress. It is important to note that thermal uniformity in parallel-connected SiC MOSFETs cannot be guaranteed by solely imposing identical switching current or equalized switching energy, as device-to-device variations in junction-to-case and case-to-ambient thermal resistances, together with differences in transient thermal impedance, can lead to unequal junction-temperature evolution, even under identical electrical operating conditions. Consequently, identical loss profiles may still result in different junction-temperature swings and average junction temperatures due to nonuniform thermal paths. The proposed approach addresses this limitation by intentionally introducing a controlled current imbalance during commutation, redistributing switching losses to compensate for thermal-path asymmetries. Thus, both the peak junction-temperature and the temperature swing of the most thermally stressed device are reduced, yielding more homogeneous thermal loading of the parallel group, enhancing

component utilization, system lifetime and long-term robustness [30].

V. SYSTEM IDENTIFICATION AND CALIBRATION OF THE THERMAL BALANCE REGULATOR

To further verify the applicability of the proposed active thermal balancing approach under extreme switching transient conditions, and to confirm that all devices consistently operate within their SOA when compensation is applied, dedicated DPTs were conducted using the same custom power board described in the previous sections. These tests focused on the turn-ON transition, which is the critical phase for thermal stress, as mentioned earlier. The experimental setup used an input voltage of 800 V combined with a 7.2 μH load inductor while the low and high-side switches consist of three parallel-connected MOSFETs. The load current was set to 135 A (45 A per switch).

A. CURRENT IMBALANCE VERSUS TURN-ON ANTICIPATION

To deliberately induce significant switching current imbalances, gate-timing offsets were introduced. Specifically, the turn-ON gate pulse of the low-side device C_L was anticipated by up to 50 ns, corresponding to the duty-cycle offset saturation limit of the proposed thermal balancing strategy (0.5%). A key observation is that typical operational offsets are below 25 ns ($< 0.25\%$) as visible for example in Fig. 7(c).

Fig. 9 shows comparative turn-ON waveforms for four scenarios.

- 1) Aligned gate commands [see Fig. 9(a)].
- 2) 5 ns anticipation of device C_L turn-ON pulse [see Fig. 9(b)].
- 3) 25 ns anticipation [see Fig. 9(c)].
- 4) 50 ns anticipation [see Fig. 9(d)].

Without compensation, transient current spikes reached a maximum of 94 A, with a maximum imbalance of 24 A. At 5 ns anticipation, spikes and imbalance improved to 90 A and 13 A, respectively. At 25 ns, spikes in device CL reached approximately 114 A with a 64 A imbalance. The worst case, 50 ns anticipation, caused a spike of 150 A and a 123 A imbalance.

According to the MOSFET datasheet, the device can withstand a maximum pulsed drain current of 150 A, confirming that these transient conditions remain within device limits. The literature verifies the robustness of Infineon's 1200 V SiC trench MOSFETs under repetitive pulses up to six times the nominal current without degradation [31], supporting the method's reliability under intentional imbalance. Consequently, these dedicated DPT tests validate that the proposed thermal balancing method maintains device operation well within datasheet-defined transient current and thermal limits, even under extreme imposed gate timing offsets.

B. EFFECT OF TURN-ON ANTICIPATION ON SWITCHING LOSSES

The switching losses of the parallel devices were experimentally evaluated for the different turn-ON compensation levels

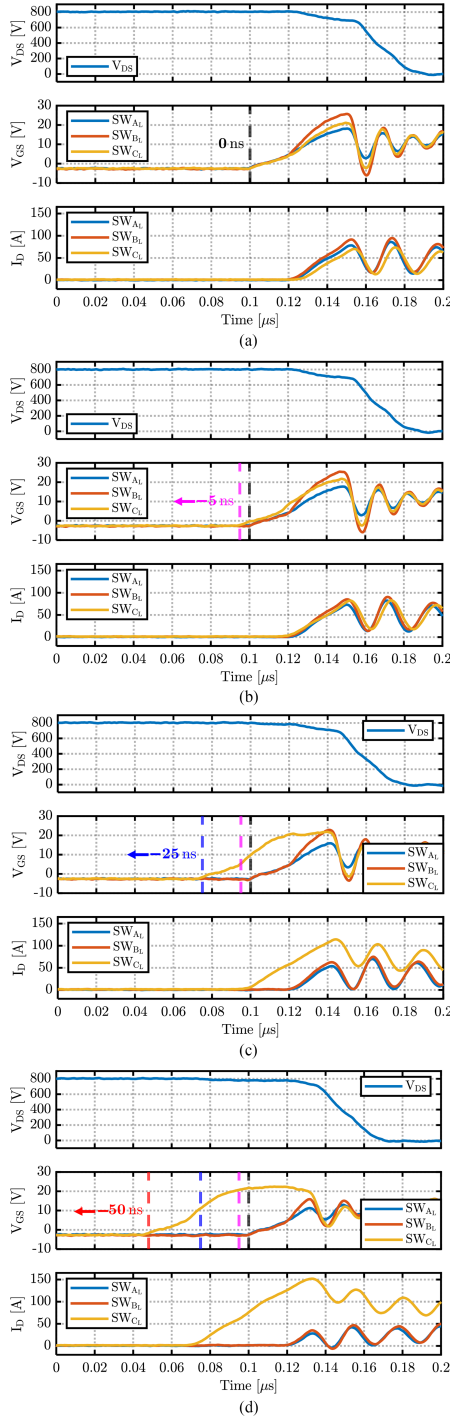


FIGURE 9. DPT turn-on waveforms comparison among the devices. (a) Aligned gate pulses. (b) C_L turn-on pulse anticipated by 5 ns. (c) C_L turn-on anticipated by 25 ns. (d) C_L turn-on anticipated by 50 ns.

of device C_L and for different load current levels, to investigate how their redistribution impacts the total switching loss, as shown in Fig. 10.

At high load current [see Fig. 10(a)] two main loss regions appear.

- 1) Area A (green): Below 22 ns anticipation (0.22% duty-cycle offset), typical of operation under thermal

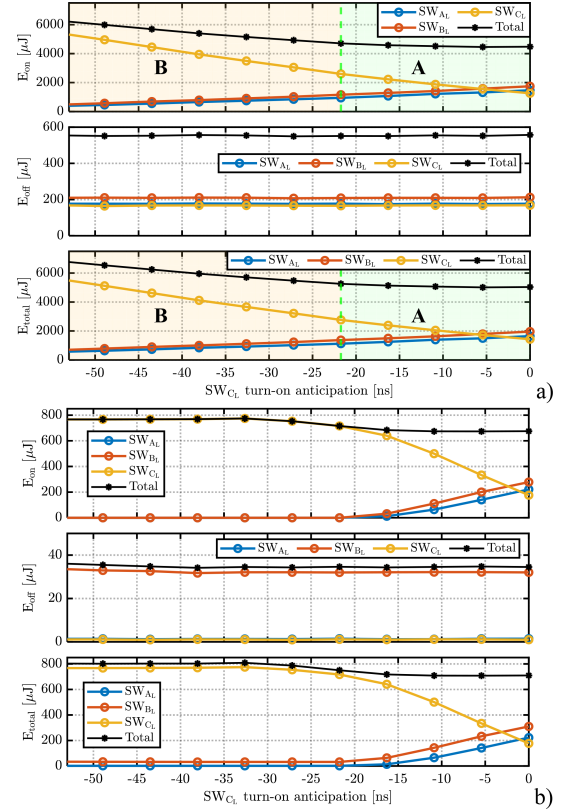


FIGURE 10. Switching losses redistribution for different levels of anticipation of the device C_L turn-ON transition. (a) Load current 135 A. (b) Load current 6 A.

balancing. Here, loss redistribution occurs with minimal impact on total switching losses, increased by at most 4.5%.

- 2) Area B (orange): From 22 ns to 50 ns anticipation (0.22% to 0.5%). In this region total losses increase substantially (up to 32%), as device C_L absorbs most of turn-ON current.
- 3) For a compensation above 50 ns, device C_L will conduct the entire turn-ON current, maximizing switching losses well beyond acceptable thresholds.

In the example of Fig. 7(c) it can be observed that for the selective turn-ON technique, the instantaneous duty-cycle offset never exceeded 0.2%, with an average duty-cycle compensation of 0.06% during the constant load current test. The analysis of Fig. 10(a) reveals that the loss increase corresponding to 20 ns (0.2%) is 4.3% while at 6 ns (0.06%) anticipation there is no total loss increase, suggesting that the proposed control method redistributes the losses among the devices while keeping the **total switching losses** substantially unaffected.

It should also be noted that for systems with a larger number of paralleled devices (e.g., 7–8 devices), the same principle applies, but the saturation limit must be scaled according to the total commutation current and the individual device SOA, so that no single device is allowed to absorb a disproportionate share of the commutation current. If the

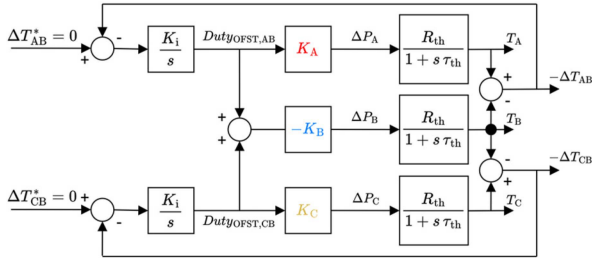


FIGURE 11. Thermal balancing block diagram for the three parallel devices.

required compensation exceeds the per-device saturation limit, the switching-energy redistribution can be distributed across multiple devices simultaneously. For instance, rather than anticipating the turn-ON of the coolest device alone, the two coolest devices can be advanced by the same offset, effectively sharing the additional commutation current between them and keeping the peak current of each device within acceptable bounds. This preserves the thermal-balancing effect while maintaining all devices within their electrical and thermal stress limits.

At low load current [see Fig. 10(b)], a substantial fraction of the turn-ON energy corresponds to the charging and discharging of the MOSFET output capacitance C_{oss} , which is a voltage-dependent parameter, while being only weakly affected by the load current. As a result, the turn-ON anticipation of device C_L shifts the commutation instant among the parallel devices, redistributing the absorption of the capacitive energy, while the total switching loss is only slightly affected, increased at most by less than 7% even at the saturation limit.

C. CALIBRATION OF THE THERMAL BALANCE REGULATOR

The thermal balance regulator must operate robustly over the entire load-current range, from the low current of Fig. 10(b) up to the highest load current of Fig. 10(a). To select a single integral regulator gain K_i that guarantees stability under all operating conditions, a control-oriented model is derived and calibrated using the DPT data of Fig. 10, using a first-order approximation of the device thermal dynamics.

The control-oriented model rests on three simplifying assumptions, supported by the results of the previous sections: (i) the regulated quantity is the directly measured device case temperature; (ii) the device thermal impedance is approximated by a single dominant pole, i.e., a first-order model with thermal resistance R_{th} and thermal time constant τ_{th} , adequate here because the low-bandwidth balancing loop interacts only with this dominant pole and not with the faster package dynamics; and (iii) mutual thermal coupling between devices is neglected, which is justified by the use of an individual heatsink for each device. Fig. 11 shows the thermal balancing control block diagram for the three parallel devices. The two regulators act on the duty-cycle offsets $Duty_{OFST,AB}$ and $Duty_{OFST,CB}$ to adjust the switching instants of devices

A_L and C_L , respectively, while the command of device B_L is unchanged.

Despite the unaltered command of B_L , its switching losses vary indirectly due to the commutation current redistribution. The controlled case temperature differences are defined as

$$\Delta T_{AB} = T_B - T_A \quad \Delta T_{CB} = T_B - T_C. \quad (1)$$

The blocks K_A , K_B , and K_C represent the relative sensitivities of each device switching loss with respect to duty-cycle offset. The incremental switching-loss variations entering the thermal plant can be expressed as

$$\begin{aligned} \Delta P_A &\approx K_A Duty_{OFST,AB} \\ \Delta P_B &\approx -K_B (Duty_{OFST,AB} + Duty_{OFST,CB}) \\ \Delta P_C &\approx K_C Duty_{OFST,CB}. \end{aligned} \quad (2)$$

The coefficients K_A , K_B , and K_C are defined as positive quantities by convention, meaning that the turn-ON anticipation of a device increases its switching losses, and vice-versa. The signs with which these sensitivities act in the control loop are handled by the summing junctions and by the block $-K_B$ in Fig. 11. In particular, the block $-K_B$ captures the fact that positive duty-offsets increase the losses of the controlled devices while decreasing the losses of the reference device B_L .

The data of Fig. 10 show that, in the typical operating region, the total switching loss remains approximately constant despite the redistribution among devices. Accordingly, when duty-cycle anticipation is applied to one device and the remaining duty cycles are kept fixed, the additional loss of the anticipated device is approximately balanced by the sum of the loss reductions of the remaining two devices. Also, loss sensitivities are linear in the range of interest 0–20 ns. Furthermore, the two uncontrolled devices can be reasonably assumed to share the resulting loss reduction equally.

Based on these observations, the sensitivities K_A , K_B , and K_C are obtained through linear fits of the measured losses P_A , P_B , and P_C as functions of $Duty_{OFST}$. For instance, in the **low-current** case of Fig. 10(b), a 10 ns turn-ON anticipation produces approximately 200 μ J increase of the anticipated device switching energy within the linear operating region; converting this timing offset to a per-unit duty-cycle shift $Duty_{OFST} = \Delta t/T_{SW}$ and considering $\Delta P = \Delta E_{SW}/T_{SW}$, this procedure yields the low-current loss sensitivities $K_{C,low} \approx 20$ kW/pu, $K_{A,low} \approx K_{B,low} \approx 10$ kW/pu. Applying the same method to the **high-current** condition [see Fig. 10(a)], this results in $K_{C,high} \approx 100$ kW/pu, $K_{A,high} \approx K_{B,high} \approx 50$ kW/pu.

Due to the linearity of the thermal dynamics and of the loss sensitivities in the operating region of interest, the multiloop system of Fig. 11 satisfies the superposition principle. As a result, each temperature-difference regulator can be calibrated independently by analyzing the corresponding single-input, single-output subsystem. In particular, the calibration of the ΔT_{AB} regulator is performed using the equivalent single-input, single-output representation shown in Fig. 12, which captures the closed-loop mapping between ΔT^*_{AB} and ΔT_{AB} .

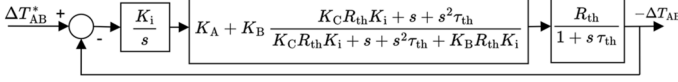


FIGURE 12. Equivalent single-input, single-output block diagram used for the calibration of the regulator, in which the block $G_{\text{loss}}(s)$ appears in the structure.

The ΔT_{CB} regulator follows the same design procedure due to the structural symmetry of the system.

The resulting closed-loop transfer function can therefore be derived from the equivalent block diagram of Fig. 12, where the interaction between loops is inherently accounted for.

The open-loop transfer function of the ΔT_{AB} loop is obtained by following the forward path of Fig. 12. The temperature-difference error $\Delta T_{AB}^* - \Delta T_{AB}$, whose set-point is set to zero to impose equal temperatures, is processed by the integral regulator K_i/s to produce the differential duty-cycle offset $\text{Duty}_{\text{OFST},AB}$. This offset is converted into the resulting switching-loss imbalance by the effective loss block $G_{\text{loss}}(s)$, which the thermal plant $G_{\text{th}}(s)$ then maps into the case-temperature difference ΔT_{AB} . Cascading these three blocks gives the open-loop transfer function:

$$L(s) = \frac{K_i}{s} G_{\text{loss}}(s) G_{\text{th}}(s). \quad (3)$$

The thermal plant $G_{\text{th}}(s)$ is the first-order model introduced in assumption (ii)

$$G_{\text{th}}(s) = \frac{R_{\text{th}}}{1 + s\tau_{\text{th}}} \quad (4)$$

and the loss block $G_{\text{loss}}(s)$ is

$$G_{\text{loss}}(s) = K_A + K_B \left(\frac{K_C R_{\text{th}} K_i + s + s^2 \tau_{\text{th}}}{\underbrace{\tau_{\text{th}} s^2 + s + (K_B + K_C) R_{\text{th}} K_i}_{F(s)}} \right). \quad (5)$$

The loss block $G_{\text{loss}}(s)$ of this equivalent representation is obtained by reducing the diagram of Fig. 11 for the ΔT_{AB} loop. The offset $\text{Duty}_{\text{OFST},AB}$ acts on the controlled device A_L directly through K_A , and on the reference device through the $-K_B$ branch. $\text{Duty}_{\text{OFST},AB}$ also excites the inner ΔT_{CB} loop, whose regulator generates $\text{Duty}_{\text{OFST},CB}$, acting once more on B_L through the same $-K_B$ branch. Solving the closed inner loop expresses $\text{Duty}_{\text{OFST},CB}$ as a function of $\text{Duty}_{\text{OFST},AB}$; substituting it turns the reference-device sensitivity into the term $K_B F(s)$, so that $G_{\text{loss}}(s) = K_A + K_B F(s)$ as in (5). In other words, the rational function $F(s)$ captures how the inner ΔT_{CB} loop modifies the effective loss-to-temperature channel seen by the ΔT_{AB} regulator. Through this inner-loop coupling, $F(s)$ introduces two additional poles and two zeros into $L(s)$, beyond the pole at the origin from the integrator and the thermal pole in $G_{\text{th}}(s)$. The additional poles are the roots of the denominator of $G_{\text{loss}}(s)$

$$\tau_{\text{th}} s^2 + s + (K_B + K_C) R_{\text{th}} K_i = 0. \quad (6)$$

The thermal parameters R_{th} and τ_{th} are extracted from the single-pulse transient thermal impedance of the device datasheet: the steady-state impedance level gives $R_{\text{th}} \approx 0.5$ K/W while the time at which the transient curve reaches 63% of this asymptotic value is approximately $t \approx 5$ ms, corresponding to one time constant of a first-order system. This yields $\tau_{\text{th}} \approx 5$ ms and $1/\tau_{\text{th}} \approx 200$ rad/s.

The additional poles from (6) evaluate to approximately 37 and 163 rad/s, i.e., one decade below and within the same decade as $1/\tau_{\text{th}}$, respectively. The additional zeros, which are the roots of the numerator of $G_{\text{loss}}(s)$, are located near the additional poles, forming a minimum-phase pole-zero pair. These dynamics originate in $G_{\text{loss}}(s)$ and therefore propagate directly into the open-loop transfer function $L(s)$.

Therefore, to prevent excitation of these higher-frequency dynamics, the integral gain is selected such that the unity-gain crossover frequency ω_c of $L(s)$ (i.e., the frequency at which $|L(j\omega_c)| = 1$ or equivalently 0 dB) satisfies $\omega_c \ll 1/\tau_{\text{th}} = \omega_{\text{th}}$, the thermal break frequency of the first-order thermal plant $G_{\text{th}}(s)$, and remains well below the additional poles identified in (6). Under this condition, the frequency range relevant for thermal balancing lies entirely in the low-frequency region where the dynamics introduced by $G_{\text{loss}}(s)$ are not excited. Consequently, $G_{\text{loss}}(s)$ can be approximated by its DC value. Evaluating (5) at $s = 0$ yields the DC gain of the loss block

$$G_{\text{loss}}(0) = K_A + K_B \frac{K_C}{K_C + K_B} \quad (7)$$

which is bounded between K_A and K_C . It is convenient to define the equivalent three-device loss sensitivity

$$K_{\text{eq}} = K_A + K_B \frac{K_C}{K_C + K_B}. \quad (8)$$

Substituting the measured sensitivities into (8), gives $K_{\text{eq,low}} \approx 16.7$ kW/pu and $K_{\text{eq,high}} \approx 83.3$ kW/pu.

Therefore, for the purpose of selecting K_i , for $\omega \leq \omega_c \ll \omega_{\text{th}}$ we can safely approximate:

$$G_{\text{loss}}(s) \approx K_{\text{eq}} \quad (9)$$

and the open-loop transfer function (3) simplifies to

$$L(s) \approx \frac{K_i K_{\text{eq}} R_{\text{th}}}{s(1 + s\tau_{\text{th}})}. \quad (10)$$

To ensure sufficient separation from the thermal dynamics, the loop crossover frequency is required to satisfy $\omega_c \leq 0.1\omega_{\text{th}} \approx 20$ rad/s, i.e., one decade below the thermal break frequency. For $\omega \ll 1/\tau_{\text{th}} = \omega_{\text{th}}$, the thermal pole in (10) has negligible magnitude effect, and the closed-loop bandwidth can be approximated by the open-loop cross-over frequency

$$\omega_c \approx K_i K_{\text{eq}} R_{\text{th}}. \quad (11)$$

Imposing $\omega_c \leq 0.1\omega_{\text{th}}$ leads to the condition

$$K_i \leq \frac{0.1\omega_{\text{th}}}{K_{\text{eq}} R_{\text{th}}} = \frac{0.1}{K_{\text{eq}} R_{\text{th}} \tau_{\text{th}}}. \quad (12)$$

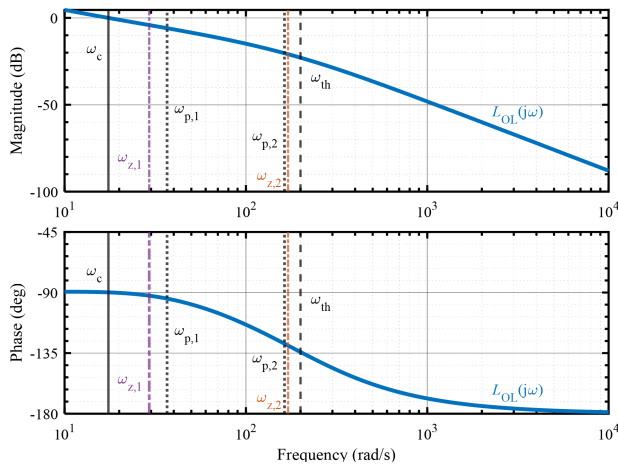


FIGURE 13. Bode diagram of the open-loop transfer function (3) in the high-current operating region for $K_i = 0.4 \times 10^{-3}$, illustrating the large phase margin of the thermal balance loop. The additional pole-zero pairs are: $\omega_{p,1} = 37$ rad/s; $\omega_{z,1} = 29$ rad/s; $\omega_{p,2} = 163$ rad/s; and $\omega_{z,2} = 170$ rad/s.

Substituting the K_{eq} limit values into (12) gives $K_{i,max,low} \approx 2.4 \times 10^{-3}$ and $K_{i,max,high} \approx 0.48 \times 10^{-3}$. As expected, the larger loss sensitivity at high current leads to lower admissible gain. To guarantee robust operation over the full current range, we select a common gain $K_i = 0.4 \times 10^{-3} < K_{i,max,high}$ and use this value at all load levels. With this choice, the estimated crossover frequency from (11) is $\omega_c \approx 17$ rad/s, safely below the thermal break frequency ($1/\tau_{th} \approx 200$ rad/s).

The stability margin provided by this calibration is best understood from the Bode diagram of the open-loop transfer function (3), plotted in Fig. 13 for the high-current case. The poles introduced by the inner ΔT_{CB} loop lie above the loop crossover frequency ω_c and are each paired with a nearby zero, so they do not interfere with the crossover. At the crossover frequency ω_c the overall loop phase is dominated by the -90° contribution of the integrator, combined with a modest thermal lag and a small phase lead from the loss block. As a result, a phase margin above 80° is obtained. This large phase margin implies an overdamped, nonoscillatory thermal response, in good agreement with the experimental results, where the device temperatures converge monotonically without overshoot for both positive and negative temperature imbalances.

A purely integral regulator was intentionally adopted rather than a PI structure. In doing so, the plant from $Duty_{OFFST}$ to ΔT (3) already has one pole at the origin, which is sufficient to guarantee zero steady-state temperature error, while the dominant limitation on the transient speed is the thermal time constant τ_{th} . Adding a proportional term is unnecessary, as confirmed by this analysis.

VI. CONCLUSION

This article presents an active thermal balancing strategy for paralleled SiC MOSFETs, based on direct case temperature measurement and individual duty-cycle adjustment, offering simplicity and robustness. Unlike existing active balancing

methods, it does not require HBW voltage/current measurements during switching. Moreover, unlike TSEP-based estimators, its performance is not affected by device-parameter drift caused by aging. The primary downside of this technique is the need for dedicated gate drivers and temperature sensors for each device. However, this added cost is offset by higher system reliability and improved component utilization. Furthermore, dedicated gate drivers reduce parasitic effects and provide greater flexibility on printed circuit board (PCB) layout design, reducing the emphasis for strictly symmetric device arrangement. Experimental results demonstrate that the proposed redistribution of switching losses successfully achieves thermal equilibrium: both the symmetrical and turn-ON compensation methods can effectively equalize device temperatures by redistributing the losses. In contrast, turn-OFF compensation is ineffective due to the negligible contribution of turn-OFF losses to overall thermal stress. Dedicated DPT tests at maximum current rating demonstrate robustness under extreme conditions and negligible impact on total switching loss. The proposed solution promises to enhance system lifetime and is particularly attractive in reliability-critical applications. Future improvements include integrating the method with smart gate drivers featuring built-in temperature sensing (e.g., Infineon 1EDI3030AS [32]) to further reduce cost and complexity. Future work will validate the method at multiple operating conditions including different switching frequencies and load-currents, while also extending the strategy to systems with more paralleled devices, high-side switches, and AC loads.

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