Doctoral Dissertation
Doctoral Program in Electrical, Electronics and Communications Engineering
(38^{th} cycle)

Efficient and Reliable Power Conversion Techniques for Distributed Photovoltaic Applications

Stefano Cerutti
******

Supervisors:
Prof. Francesco Musolino (academic supervisor)
Prof. Paolo Stefano Crovetti (academic supervisor)
Eng. Mario Giuseppe Pavone (company supervisor)
Dr. Francesco Gennaro (company supervisor)
Eng. Natale Aiello (company supervisor)

Doctoral Examination Committee:
Prof. Marco Liserre, Kiel University
Prof. Paolo Mattavelli, University of Padova
Prof. Federica Cappelluti, Politecnico di Torino

Politecnico di Torino
2026

Declaration

This publication is part of the project PNRR-NGEU which has received funding from the MUR – DM 352/2022.

I hereby declare that, the contents and organization of this dissertation constitute my own original work and does not compromise in any way the rights of third parties, including those relating to the security of personal data.

Stefano Cerutti
2026

* This dissertation is presented in partial fulfillment of the requirements for **Ph.D. degree** in the Graduate School of Politecnico di Torino (ScuDo).

Abstract

The global effort towards more sustainable energy production systems is fostering the widespread diffusion of both large-scale and small-scale distributed photovoltaic (PV) plants. To effectively support this transition, the technological advancement and cost reduction of PV modules must be accompanied by the development of more flexible, cheaper, more efficient, and more reliable Power Electronic Converters (PEC)

To address the demanding and often conflicting requirements imposed on PECs design, this work exploits multiple methodologies to explore innovative power converter solutions for module-level grid-tied and off-grid PV applications. Starting from a critical review of the state of the art, this thesis presents key research gaps and potential opportunities for improvement in the existing solutions, and proceeds with the analysis, design, and experimental validation of new converter topologies. This work collects the outcomes of three main research projects, unified by the common framework and guiding principles, such as the close adherence to realistic PV specifications.

The first project is devoted to the design of a high step-up DC-DC converter topology for parallel power optimizers (PPOs), addressing the demanding challenge to maintain high efficiency over a wide range of operating input voltages and power levels. The proposed topology combines in an innovative way the partial power processing approach and a multi-mode control scheme, ensuring optimal performances at a desired rated working point while preserving high efficiency out of the nominal conditions. Tests on a 700 W prototype demonstrated a 97.15 % California Energy Commission (CEC) efficiency and 97.8 % peak efficiency at the rated input voltage 39 V, and the correct operation and reduced efficiency drop across the wide

15 V–45 V input voltage range thanks to the multi-mode principle.

The second project introduces an innovative design methodology to optimize a PPO in terms of cost and weighted efficiency, while including an additional lifetime constraint under realistic mission profiles. Strong emphasis is devoted to the reliability modelling of power converters, which is often overlooked in PEC design, or based on oversimplified empirical models that neglect the physics of failure of components or the influence of mission profiles. A 500 W prototype was designed based on the optimal solution and characterized experimentally, revealing a 95.33 % CEC efficiency at the rated input voltage.

The last project investigates a quasi-resonant step-down power converter for off-grid PV-fed battery charging applications. The proposed non-isolated topology is derived from the half-bridge converter and enables the soft-switching of all its transistors thanks to a small additional inductor. The proposed converter mitigates some limitations of existing solutions related to achieving the soft-switching and high efficiency without increasing the electrical stresses and component count. A 100 W prototype is built and tested, showing a 94.5 % peak efficiency and a limited efficiency drop in the 20 %–100 % load range, thanks to the achievement of the soft-switching across most of the working points.

The exploration of innovative techniques in the design of new converter topologies allowed to achieve promising experimentally validated performance when compared to the state of the art. The innovative topologies and design methodologies investigated in this work will offer new insights to foster the research towards higher efficiency and more reliable power converters for distributed PV applications.

Contents

List of Figures

List of Tables

List of Acronyms

$\mu-$inv Microinverter.

A-IPOS Asymmetric Input-Parallel-Output-Series.

AC Alternate Current.

AD Accumulated Damage.

AP Area Product.

BAPV Building-Applied photovoltaic (system).

BCM Boundary Conduction Mode.

BIPV Building-Integrated photovoltaic (system).

BL Bridge-Linked (array configuration).

CC Current Circulating (phase).

CCM Continuous Conduction Mode.

CdTe Cadmium Telluride.

CEC California Energy Commission (efficiency).

CI Coupled Inductors.

CIGS Copper Indium Gallium Selenide.

CR Crossover Resonant (phase).

DC Direct Current.

DCX DC Transformer.

DDM Double Diode Model.

DPP Direct Power Path.

DUT Device Under Test.

DVM Discontinuous Voltage Mode.

EOL End of Lifetime.

ESS Energy Storage Systems.

EURO European (efficiency).

EV Electric Vehicles.

FET Field-Effect Transistor.

FM Frequency Modulation.

FMECA Failure Modes, Effects and Criticality Analysis.

FPGA Field Programmable Gate Array.

FPP Full-Power Processing.

FSM Finite State Machine.

GA Genetic Algorithm.

GCC Generation Control Circuit.

GMPP Global Maximum Power Point.

GUI Graphical User Interface.

HAL Hardware Abstraction Layer.

HC Honey Comb (array configuration).

HEMT High Electron Mobility Transistor.

HF High Frequency (mode).

HRTIM High-Resolution Timer.

HV High Voltage (mode).

IDE Integrated Design Environment.

IEA International Energy Agency.

InC Incremental Conductance.

IPOS Input-Parallel-Output-Series.

ISR Interrupt Service Routine.

KCL Kirchhoff Current Law.

LC Lifetime Consumption.

LCOE Levelized Cost of Energy.

LF Low Frequency (mode).

LUT Look-Up Table.

LV Low Voltage (mode).

LVDC Low-Voltage DC (system).

MIC Module-Integrated Converter.

MLCC Multi-Layer Ceramic Capacitor.

MLPC Module-Level Power Converter.

MM Multi-Mode.

MPP Maximum Power Point.

MPPT Maximum Power Point Tracking.

MS Multi-Stage.

MTBF Mean Time Between Failures.

MV Medium Voltage (mode).

MVDC Medium-Voltage DC (system).

NMOT Nominal Module Operating Temperature.

NOCT Nominal Operating Cell Temperature.

NREL National Renewable Energy Laboratory.

ODE Ordinary Differential Equation.

P&O Perturb & Observe.

PBT Pay-back Time.

PCB Printed Circuit Board.

PDF Probability Distribution Function.

PEC Power Electronic Converter.

PFC Power Factor Correction.

PPO Parallel Power Optimizer.

PPP Partial-Power Processing.

PSC Partial Shading Conditions.

PSM Phase-Shift Modulation.

PSO Particle Swarm Optimization.

PT Power Transfer (phase).

PV Photovoltaic.

PWM Pulse-Width Modulation.

RES Renewable Energy Sources.

RHP Right Half-Plane.

RMS Root-Mean-Square.

SC Switched Capacitors.

SDGs Sustainable Development Goals.

SDM Single Diode Model.

SEPIC Single-Ended Primary Inductor Converter.

SL Switched Inductors.

SMD Surface-Mount Device.

SPO Series Power Optimizer.

SRC Series Resonant Converter.

STC Standard Test Conditions.

TCT Total-Cross-Tied (array configuration).

TM Topology-morphing.

TMR Tunnel Magneto-Resistive (current sensor).

VDR Voltage Doubler Rectifier.

VFR Voltage Fifth-folder Rectifier.

VM Voltage Multipliers.

VQR Voltage Quadrupler Rectifier.

VRLA Valve-Regulated Lead-Acid (battery).

VSR Voltage Sixth-folder Rectifier.

VTR Voltage Tripler Rectifier.

WBG Wide Band-gap.

ZCD Zero-Current Detection.

ZCS Zero Current Switching.

ZVS Zero Voltage Switching.

Chapter 1

Introduction

1.1 Role of the photovoltaic source in the generation of electrical energy

The Agenda 2030 of the United Nations has identified a framework of 17 Sustainable Development Goals (SDGs) with 169 associated targets, to foster the integration of multiple dimensions of sustainability (People, Planet, Prosperity, Peace, Partnership) in the policy making process of the countries[1]. The 17 SDGs aim at translating the various aspects related to sustainability into recommended actions, ensuring that technological progress does not neglect social and economic development, and vice versa.

The SDGs include a specific goal related to the need of fostering the adoption and accessibility of clean energy technologies based on Renewable Energy Sources (RES), which should progressively replace the carbon-based technologies: *Goal 7: Ensure access to affordable, reliable, sustainable and modern energy for all*. The comprehensive nature of the formulation of this goal does not only encourage the technological improvement of the RES-based systems, but also insists on the accessibility of modern technologies to the least developed countries, in the attempt to reduce the gap with the most developed and wealthiest ones.

[1] https://sdgs.un.org/2030agenda (accessed Sept. 10, 2025)

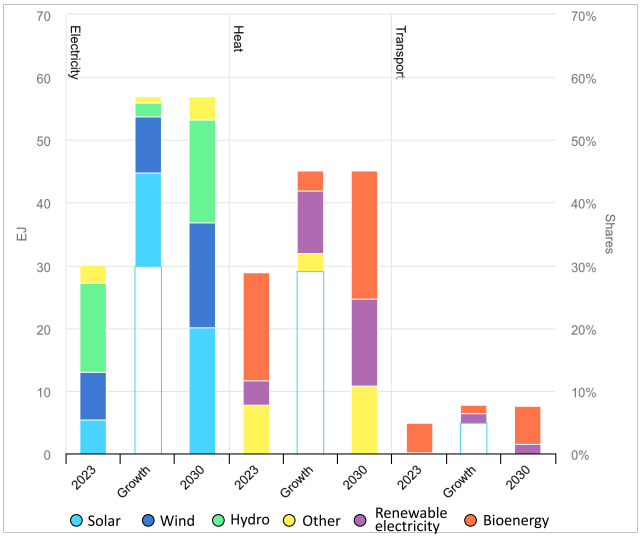


Fig. 1.1 Renewable energy demand growth by sector, main case, 2023-2030. Source: IEA (2024), Paris, Licence: CC BY 4.0.

In recent years, increasing attention to the energy-related development has pushed the global electricity access from 84 % in 2010 to 92 % in 2023[2], in spite of an increase in the global population from 6.45 billions of people (2010) to 8.09 billions (2023)[3].

As mentioned, a pivotal role for the implementation of SDG 7 is represented by the increasing spread of energy systems based on RES. Although the generation of electricity is often perceived as the main sector associated to a paradigm shift from fossil-based sources to RES, the adoption of RES is experiencing a boost also in the heat generation and transport sectors, as shown in Fig. 1.1. Projections for 2030 suggest that the share of renewable energy sources in the global electricity mix will almost double, raising from nearly 30 % to 56 %: the most relevant contribution is offered by the solar (photovoltaic) source [1]. In the heating sector, the growth of renewable energy demand is primarily driven by RES-fed electrical heating systems like heat pumps. In the transport sector, the share of RES is expected to remain below 10 % in 2030.

As this thesis addresses specifically PV-fed electrical systems, it is relevant to focus the analysis of the RES on the electricity generation sector. Fig. 1.2 shows the the evolution and forecast of the share of RES in the generation of electrical energy,

[2]https://sdgs.un.org/goals/goal7 (accessed Sept. 10, 2025)
[3]https://ourworldindata.org/population-growth (accessed Sept. 10, 2025).

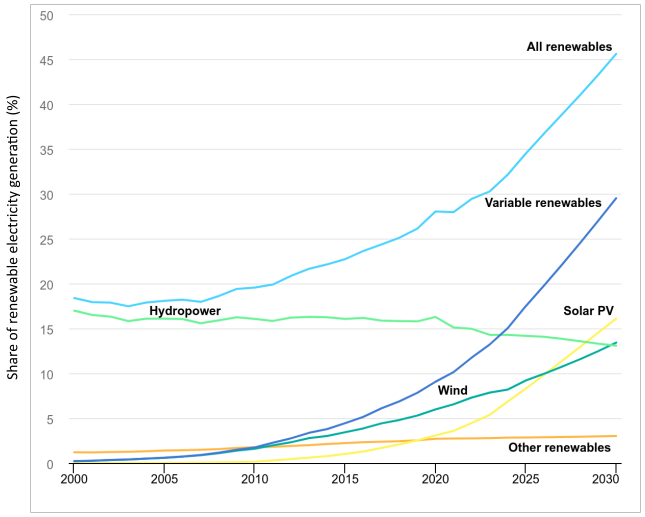


Fig. 1.2 Share of renewable electricity generation by technology in the 2000-2030 time window. Source: IEA (2024), Paris, Licence: CC BY 4.0.

at a world scale. Multiple relevant pieces of information can be derived from the data of the International Energy Agency (IEA):

- the total share of RES is expected to more than double in the 2000-2030 time window, accounting for approximately the 46 % of the total electricity generation in 2030 [2];
- compared to the past, the trend highlights a true paradigm shift from dispatchable RES, especially the hydro-electric power, to non-dispatchable / variable RES, namely, the PV and wind generators, which are expected to weight for almost two thirds of the total RES production in 2030;
- among the RES, the PV generation is experiencing the fastest growth, expecting to surpass the wind source in 2026 and the hydro-electric power in 2029, thus becoming the largest source of electricity generation worldwide.

The *SDG Report 2024* states that the installed capacity per capita from RES increased from 250 W in 2015 to 424 W in 2022, especially driven by developed and developing countries [3]. The new capacity installations are dominated by the PV plants: the cumulative installed capacity of PV generators has increased monotonically in the last years, especially driven by China (205 GW in 2019), Europe (147 GW in 2019) and USA (61 GW in 2019) [4].

A more detailed overview of the PV installed capacity by segment is illustrated in Fig. 1.3. At a global level, the cumulative installed capacity in the 2019-2024 period has more than doubled compared to the previous 2012-2018, even when considering the most conservative scenario. The data suggest that the commercial and industrial sectors dominate the new PV installations, followed by the residential sector and, more marginally, by the off-grid applications. Compared to other RES, one of the most inherent features of the PV source is its scalability and modularity, making it the most suitable source for small-scale distributed plants. The distributed PV, expected to account for approximately the 46 % of the total PV capacity in 2024, offers to public, commercial or private entities the opportunity to reduce the cost of energy, by exploiting the self-consumption of the PV energy.

Beside the generation, distribution and utilization of electrical energy from the PV source, increasing attention is devoted to the design of Energy Storage Systems (ESS) to improve the availability of the generated energy from PV plants [5]. ESS are crucial to mitigate the intrinsic variability of the PV generation, i.e., to store the surplus energy generated by the RES and not immediately utilized, and to supply the demanded load power when the RES generation is not sufficient. In addition, the adoption of ESS can foster the installation of PV systems in rural contexts or other scenarios where the accessibility to the electrical grid is not straightforward [6], as demanded by the SDGs of the United Nations 2030 Agenda [7]. Off-grid ESS are gaining attention in emerging green applications such as off-grid cooking systems [8], green hydrogen production plants [9] or charging stations for electrical light mobility [10]. The coupled integration of PV plants and ESS can represent a green alternative to traditional fossil-based off-grid generation systems.

The widespread diffusion of PV sources in the past years was largely driven by the increasing maturity of PV modules technology, which has led to a significant reduction of their price-per-watt. To give an exemplary idea of the evolution of PV panels cost over time, Fig. 1.4 shows the average yearly price-per-watt of commercial thin-film amorphous Silicon PV panels between 1975 and 2024, combining different sources of data from IRENA[4], Nemet[5] and Farmer and Landfond[6]. The graph shows that, despite minor localized increased prices in 1989, 2005 and 2022, the

[4]Available: https://www.irena.org/Publications/2025/Jun/Renewable-Power-Generation-Costs-in-2024 (accessed 28/10/25).

[5]Available: https://pcdb.santafe.edu/graph.php?curve=158 (accessed 28/10/25).

[6]Available: https://www.sciencedirect.com/science/article/pii/S0048733315001699 (accessed 28/10/25).

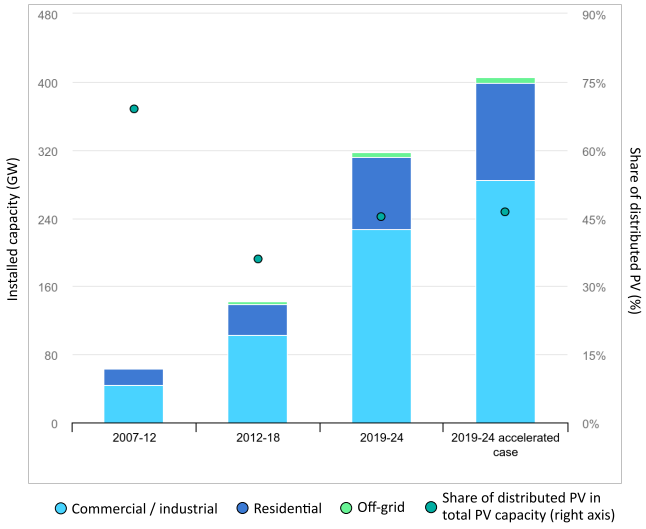


Fig. 1.3 Distributed PV capacity growth by segment, 2007-2024. Source: IEA (2019), Paris, Licence: CC BY 4.0.

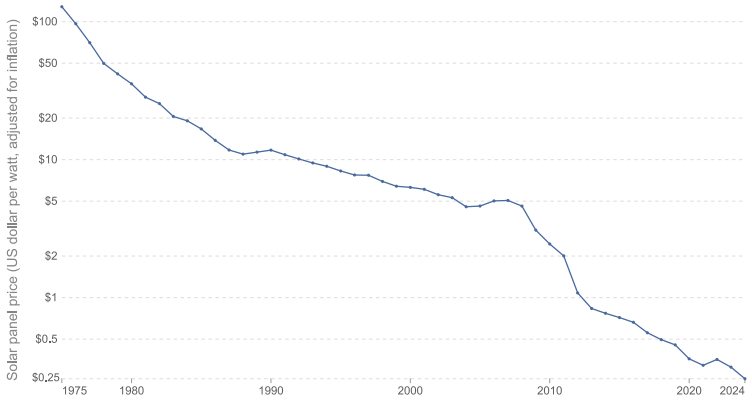


Fig. 1.4 Evolution of average yearly price-per-watt for thin film PV panels in the 1975-2024 period. Source: OurWorldinData.org/energy | CC BY.

average price has steadily decreased in the considered time window, passing from approximately 128 USD/watt to 0.26 USD/watt.

A more specific analysis of the evolution of the PV module prices in the residential sector is shown in Fig. 1.5 from data collected and analyzed by the NREL[7], which refer mainly to monocrystalline Silicon modules. In line with Fig. 1.4, the graph in 1.5 shows a steady decrease of the PV modules cost in the 2010-2023 period,

[7]Available: https://www.nrel.gov/solar/market-research-analysis/solar-installed-system-cost (accessed 28/10/25).

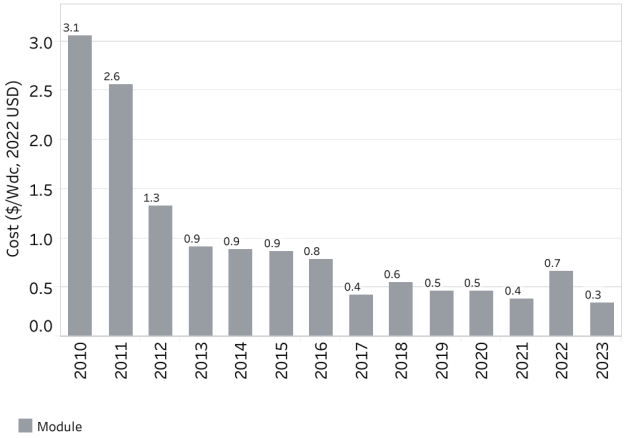


Fig. 1.5 Evolution of average yearly price-per-watt for PV panels in the residential section in the 2010-2023 period. Source: NREL, 2026

equivalent to an approximate 90 % reduction (from 3 USD/watt to 0.34 USD/watt).

1.2 Thesis objectives and outline

The increasing diffusion of both large-scale and small-scale PV plants, for both grid-tied and off-grid applications, can be sustained only when all the elements of the energy chain are individually optimized to ensure efficiency, reliability and cost effectiveness of the entire system. The environment-related variability of the PV generation and the inherent electrical characteristics of PV sources require auxiliary systems to harvest, collect and distribute the electrical energy when needed. In this context, Power Electronic Converters (PEC) are the key enablers of the PV technology, as they are designed to ensure an effective interface between the PV generators and the electrical grid or local loads. As the cost of PV panels reduces over time, pushed by the increasing maturity of the PV technologies and massive public investments in many countries, the timely focus on improving the design of PEC is crucial to keep fostering the widespread distribution of PV plants. The application-specific design of PEC translates into a set of often conflicting requirements that represent the main open challenges in this research field. First of all, PECs should be designed to enable the electrical interface between a variable PV source and a load: as such, specific voltage gain requirements and variable gain features are crucial, as well as the capability to work efficiently on a sufficiently wide set of operating conditions. The reduction of costs, partly enabled by the increasing maturity of the emerging technologies of power semiconductor devices, should also be addressed at a converter topology level; at the same time, however, the design choices to reduce costs should not compromise the reliability of PEC, namely, its capability to guarantee a continuous operation over a sufficiently long period of time. Finally, of the small size of PEC assists its easier mounting and integration to the rest of the subsystems of a PV plant.

This holistic and multi-criteria design approach constitutes an open and complex challenge in this research field, and still presents several opportunities for innovation, as attested by a vast and recent literature. This is especially true for Module-Level Power Converters (MLPC), in their two main configurations (micro-inverters and power optimizers), whose flexibility and inherent small-scale nature have gained significant interest in modern distributed generation systems such as Building-Integrated PV, Smart Grids and Renewable Energy Communities. At the same time, the simultaneous consideration of the conflicting design challenges becomes even more demanding for MLPC. In the last recent years, a variety of resonant, multi-level,

multi-mode and multi-stage converters have been proposed, trying to address multiple design targets in innovative ways. Staring from a critical review of the existing literature, to identify limitations and research gaps, this work investigated, for the first time, the combination of the Partial Power Processing (PPP) and multi-mode approaches in a new wide-range and high-efficiency converter topology.

This work also addressed from a design methodology perspective the non-trivial inclusion of reliability considerations into the design of PECs, which has often been approached in the existing literature through methods that either neglect the physics of failure mechanisms of the converter components or rely on oversimplified mission profiles. In response to these limitations, this work aims at proposing a new design methodology that incorporates a systematic reliability assessment with other conflicting objectives, such as cost and efficiency.

The content of this work is subdivided into three main projects, which can all be framed in the macro-field of high-efficiency PV-fed power converters. The rest of the thesis is structured as follows:

- Chapter 2 introduces the electrical characteristics of PV generators in order to justify the design challenges that they impose on PEC, and presents the different conversion architectures for both large-scale and small-scale PV plants;

- Chapter 3 presents a systematic and structured review of the previous literature addressing the main and most recent advances in the context of the work. A deep investigation of the previously proposed DC-DC converters for high step-up PV applications is followed by a survey of the most recent and widespread techniques for the reliability analysis of PEC, required to introduce a reliability-constrained optimization approach presented later. Finally, the most relevant previous solutions of PV-fed battery chargers are presented. The surveys aim at presenting the previously proposed solutions and to outline the conceptual flow adopted in this work toward the formulation of new technical contributions;

- Chapter 4 proposes a new solution of multi-mode partial-power processing DC-DC converter for high step-up and wide-range PV applications. The chapter includes all the main steps from the conceptualization of the topology, the analysis of the converter operation, the efficiency-oriented design and exper-

imental results, illustrating the main distinctive features and improvements compared to the state of the art;

- Chapter 5 introduces a new design optimization methodology that integrates the converter cost, efficiency and lifetime estimation for a cost- and reliability-aware design, often missing in the academic literature. The methodology is applied to the optimization of a partial-power processing PPO derived from the previously presented multi-mode converter;
- Chapter 6 introduces a new step-down DC-DC converter designed for off-grid low-voltage battery charging PV applications. As in Chapter 4, the complete steps, from the analysis of the topology to the discussion of the experimental results, are presented;
- Chapter 7 draws the conclusions of the thesis, highlighting the most relevant innovative findings of the research.

Chapter 2

Characteristics and Challenges of the PV generation

The purpose of this chapter is to present the framework that allows to justify, from the analysis of the electrical characteristics of PV generators, the main design challenges imposed to PEC, qualitatively introduced in the previous chapter. In addition, the various architectures of PV plants are introduced, highlighting advantages, limitations and design requirements of each one.

The conventional equivalent circuits used to model the electrical behaviour of PV sources are introduced in Section 2.1. Section 2.2 introduces the different architectures of PV plants, on the basis of the PEC stage, highlighting the advantages, drawbacks and typical scenarios in which they are employed. Finally, Section 2.3 summarizes the design requirements and challenges of PV-fed power converters, both from the performance, safety and regulations points of view.

2.1 Electrical characteristics of the PV sources

In order to identify the main design specifications of power converters for PV-fed applications, it is crucial to introduce the main electrical characteristics of the PV source. A deep investigation on the technology of PV panels is out of the scope of this work: here, only the essential physics-related aspects of the PV effect are introduced to justify the electrical behaviour of the source. The elementary unit of a

PV generator, independently on its scale, is the photovoltaic cell, which consists of a stack of semiconductor materials separated by one or multiple junctions. The shape, thickness and material of the photovoltaic cells are engineered to maximize the photoelectric effect, i.e., the generation of a couple of free charge carriers, electrons and holes, through the absorption of photons. In an irradiated PV cell, the built-in junction field enables the drift of free carriers through the semiconductor layers, and the connection of a load to the terminals determines the operating point and the extracted current from the cell. Usually, the PV cells are connected in series in a PV module (or panel) to increase the potential power harvesting of a single source. Larger scale PV plants combine multiple modules in series, to form the so-called strings, and strings can be parallelized in arrays [11].

Common equivalent circuit models to describe the electrical behaviour of PV sources (both cells and modules) are the Single Diode Models (SDM) or Double Diode Models (DDM), which were proved in many works to well-fit the non-linear behaviour of the PV characteristic [12–14]. It is relevant to observe that, in case of uniform irradiance, the electrical characteristic of a PV module, string or array simply represents a "scaled" version of the characteristic of the unit PV cell. As a consequence, models developed for PV cells can be adjusted to more complex PV sources. The equivalent circuits for the SDM and DDM are represented in Figs. 2.1a and 2.1b, respectively, and include:

- an irradiance-dependent current source $I_{\mathrm{ph}}(G)$, modelling the drift current flow due to the photovoltaic effect;
- one or two diodes in anti-parallel connection with respect to $I_{\mathrm{ph}}(G)$, which model the opposing diffusion current through the semiconductor junctions;
- an equivalent resistance R_{sh} in parallel, modelling the leakage losses;
- an equivalent resistance R_{s} in series, modelling the contact losses.

The main environmental variables that affect the equivalent circuit model parameters are the solar irradiance G (expressed as a power over a surface unit) and the cell (or panel) temperature T_{panel}.

The electrical characteristic of a PV source derives from the analysis of the equivalent circuit models in Figs. 2.1a and 2.1b. For a specific set of solar (uniform)

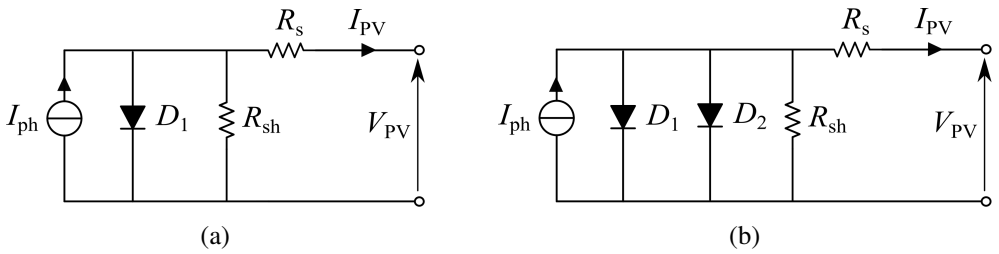


Fig. 2.1 Common equivalent circuits used for the modelling of the electrical characteristic of the PV sources. (a) Single Diode Model (SDM); (b) Double Diode Model (DDM).

irradiance and panel temperature, the qualitative behaviour or the current-voltage characteristic assumes the shape in Fig. 2.2a, using the sign convention of Figs. 2.1a and 2.1b. The product $V_{PV} \cdot I_{PV}$ represents the power that can be harvested when a certain voltage is imposed at the PV panel terminals. The characteristic shape of the curve allows to identify some parameters that are always reported in the PV panels datasheet as figures of merit:

- the short-circuit current I_{sc};
- the open-circuit voltage V_{oc};
- the Maximum Power Point (MPP), a unique working point defined as the couple of voltage V_{MPP} and current I_{MPP} for which the harvested power P_{MPP} is maximum.

The datasheet parameters refer to a set of Standard Test Conditions (STC), defined in [15] as follows: $G = 1000\,\mathrm{W/m^2}$ perpendicular to the surface, $T_{panel} = 25\,^{\circ}\mathrm{C}$, radiation spectrum in the $[280\,\mathrm{nm}; 4000\,\mathrm{nm}]$ range at air mass AM=1.5. The STC may not be representative of the ordinary outdoor operation of a PV panel: for this reason, alternative more realistic test conditions have been defined to characterize PV panels in the datasheet, such as the Nominal Operating Cell Temperature (NOCT) and Nominal Module Operating Temperature (NMOT) [16, 17].

A closer look at the I-V curve allows to observe that the current is more or less constant and equal to I_{sc} until the MPP. In the neighborhood of V_{MPP}, the increasing diffusion current through the junctions starts counterbalancing the photocurrent, until the open-circuit condition. Depending on the material, the rated MPP voltage can be located between $0.6V_{oc}$ and $0.85V_{oc}$. The technology of the panel influences the convexity of the characteristic, while the number and arrangement of the cells

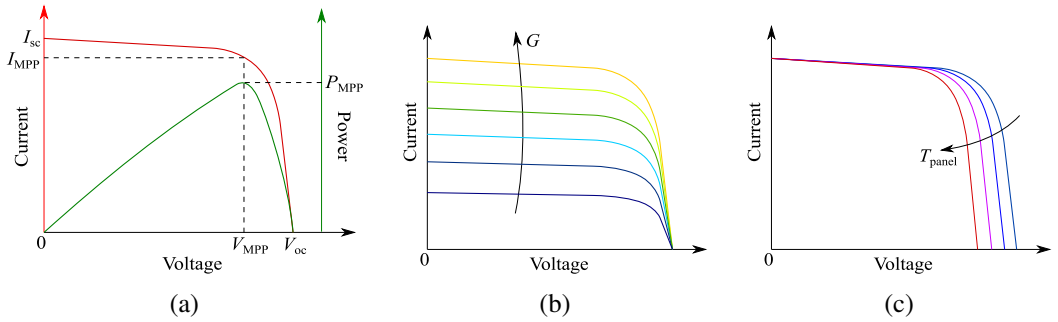


Fig. 2.2 Qualitative electrical characteristics of a PV source under uniform irradiance conditions. (a) Current-voltage (I-V) and power-voltage (P-V) characteristic of a PV source, highlighting the short-circuit current I_{sc}, the open-circuit voltage V_{oc}, the MPP current I_{MPP}, MPP voltage V_{MPP} and MPP power P_{MPP}; (b) Qualitative behaviour of the I-V characteristic at different irradiance G conditions; (c) Qualitative behaviour of the I-V characteristic at different panel temperatures T_{panel} conditions.

influence the specific values of the electrical parameters: nonetheless, the discussion can be applied in general to any PV generator.

Fig. 2.2b shows qualitatively the behaviour of the I-V characteristic at different solar irradiances. G affects mainly the intensity of the photocurrent I_{ph}, which represents the main contribution to the short-circuit current: this results in a mostly linear relationship between I_{sc} and G. On the other hand, the panel temperature affects mainly the diffusion mechanism and the scattering events in the semiconductor material: as shown in Fig. 2.2c, an increasing T_{panel} reduces the MPP and open-circuit voltages, while having an almost negligible contribution on I_{sc}. The PV panels datasheets usually report the linear temperature coefficients describing the percentage reduction of V_{oc} and P_{MPP} in presence of a temperature displacement compared to the nominal STC temperature.

The adoption of equivalent circuit models can not only fit the PV characteristic under uniform irradiance conditions, but can also be applied to predict the modification of the electrical characteristic during partial shading scenarios. One of the main technological constraints of PV panels is related to the connection in series of the solar cells, to increase the overall voltage at the module terminals: the series connection, however, constrains the total module current to the photocurrent of the least irradiated cell, severely limiting the available power that can be harvested. Without technological countermeasures, the shading of a single cell would compromise the energy harvesting of the entire module. For this reason, PV panels are

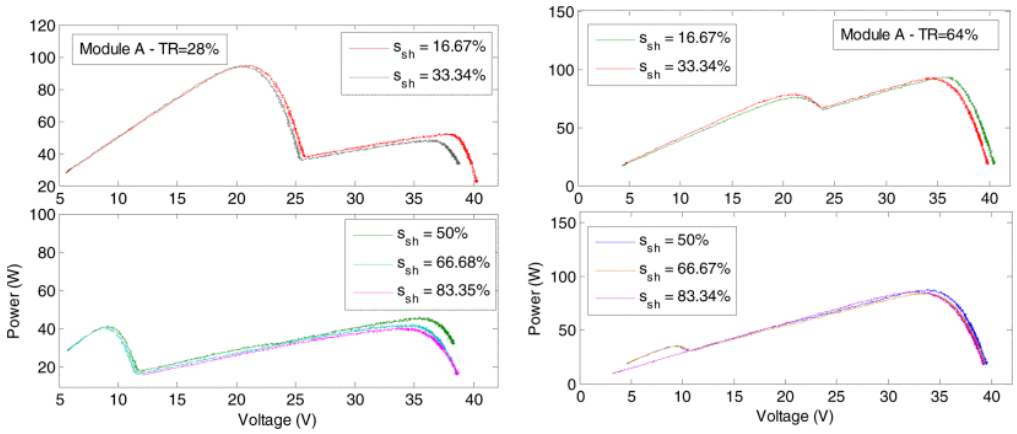


Fig. 2.3 Experimental P-V curves on a silicon monocrystalline PV panel under different partial shading scenarios. Source: [20]. s_{sh} represents the shaded fraction of the total area, while TR is the transmittance ratio of the material used to produce the shading: different TR corresponds to different irradiances of the shaded area. The experimental curves highlight how certain PSC induce a significant shift of the GMPP voltage

usually equipped with multiple bypass diodes, mounted in anti-parallel connection to a group of solar cells. The most important contribution of bypass diodes is to locally bypass a single cell or a group of cells subjected to shading: in this way, the lower photocurrent generated by the shaded fraction of the module is not imposed to the rest of the unshaded cells. The inclusion of bypass diodes has now become an established preventive measure to limit the power loss during partial shading conditions (PSC) [13].

One of the inherent effects of bypass diodes, however, is the significant modification of the electrical characteristic of a PV module under PSC, which depends on multiple aspects:

- the number of bypass diodes, associated to the number of series-connected solar cells that may be occasionally bypassed when shaded [12];
- the extension / fraction of the shaded area [13, 18, 19, 14, 20];
- the irradiance difference between the shaded and unshaded cells [12, 21, 19, 14, 20].

From a qualitative standpoint, bypass diodes are associated to the appearance of local power peaks in the P-V curve, which may occasionally shift the global MPP (GMPP) at voltages significantly lower than the rated MPP voltage. Fig. 2.3 shows

some experimental P-V curves picturing the effect of different PSC on the electrical characteristic of a monocrystalline silicon PV module with three bypass diodes [20]. s_{sh} represents the shaded fraction of the total area, while TR is the transmittance ratio of the material used to produce the shading. As it can be seen, a relevant reduction (-41 %) of the GMPP voltage is observed when the shading is localized (16.7 % and 33.3 %) and stronger ($TF = 28\,\%$, meaning that only 28 % of the test irradiance is transferred to the shaded cells). Almost twice the power (+94 %) can be harvested if the PV panel operates in the GMPP rather than in the local peak near the rated MPP voltage. Similar results were observed in other works:

- in [19], it was observed that a partial shading spread on all the sub-modules of a PV panel could shift the measured GMPP voltage to -45 % of the rated MPP voltage;
- in [14], different PSC were tested, and it was observed that the GMPP could range in the $[-39\,\%; +15\,\%]$ of the rated MPP voltage;
- an even stronger reduction (-60 %) of the GMPP voltage was characterized in [21].

A common observation in [20, 14, 21] was that the most radical modifications in terms of GMPP location are associated to localized and opaque shading scenarios, such as those induced by tree leaves or bird droppings covering a single solar cell or part of it. In light of these considerations, it is relevant to evaluate whether the power converters should be designed to harvest the PV energy over such a wide MPPT range. More detailed guidelines should be based on a statistical analysis of the fraction of time that a PV module spends in PSC that shifts the GMPP voltage far away from the uniform irradiance conditions. Unfortunately, this analysis would be inherently defective, since the IV characteristic under PSC depends on too many variables, both panel-related (arrangement and number of bypass diodes) and environment-related (frequency, size and transmittance of the shading obstacles).

In [22], an experimental characterization of the GMPP location was performed on a large-scale PV array during the passage of clouds. It was observed that the partial shading induced by the clouds movement led to temporary GMPP in the range $[-50\,\%; +16\,\%]$ of the rated MPP voltage. However, it was also measured that working in the lowest-voltage power peak would imply a limited $+2\,\%$ energy

harvesting compared to the operation in the neighborhood of the rated MPP voltage. This particular type of shading seems not to justify the wide-voltage design of inverters: however, as observed in the previously mentioned works, a wider MPPT range could lead to significant energy harvesting improvements in case of opaque and localized shading. This is especially true in residential PV applications, where chimneys or adjacent buildings could induce systematic shadings throughout the daytime.

2.2 Classification of PV systems according to the power conversion architecture

The inherent features of the PV source, however, such as its direct current (DC) nature and the strong variability of its electrical characteristic according to the environmental conditions, prevents the direct interface between the generator and the load: in other terms, the utilization of the PV energy is constrained by the need to convert it into a suitable alternative form. In this context, Power Electronic Converters (PEC), which represent the interface between the PV source and the electrical grid or local loads, play a critical role in the integration and utilization of the RES.

As anticipated, one of the intrinsic characteristics of PV plants is the modularity, which allows generators to be easily scaled up by connecting multiple cells, modules and strings. Regardless of the scale, PECs are needed to provide an effective interface with the grid or off-grid loads. Depending on the size of the PV array and of the functionality of the PEC, multiple PV architectures can be defined [23–25].

Centralized architectures

Centralized architectures employ a unique high power (normally $> 10\,\mathrm{kW}$) inverter to interface a PV array with the electrical grid. PV arrays are defined as the parallel connection of multiple strings, which are themselves constituted by series-connected PV modules. An example of centralized architecture is shown in Fig. 2.4a The PV arrays usually feed the inverter through a DC-link port between 500 V and 800 V. The voltage at the DC-link is normally converted into a three-phase AC voltage. The presence of a single PEC makes this solution the most common architecture for large-scale PV plants, thanks to its simple construction and cheaper implementation. On the other hand, from the reliability and availability points of view, a fault in the central inverter compromises the energy harvesting of the entire array.

One of the distinctive features of the centralized architecture is the low MPPT efficiency, the lowest among all PV architectures. This limitation is linked to the fact that the single PEC stage can only track a single MPP for the entire array [24]. Any mismatch between the electrical characteristics of the PV modules or string decreases the total available power that can be harvested. In addition, partial shading

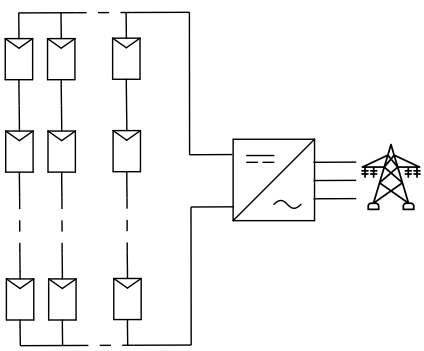
can drastically reduce the maximum power and create potential electrical hazards in specific panels or strings. This issue is partially compensated by the presence of blocking diodes in series to each string, which prevent them from acting as loads in these particular cases. Alternative array interconnections to the Series-Parallel have been explored to try limiting the impact of mismatches and non-uniform irradiance conditions, such as the Total-Cross-Tied (TCT), the Bridge-Linked (BL) and the Honey-Comb (HC), whose details can be found in [24, 26].

In [27], it was proved through a comparative analysis of large-scale PV plants that the MPPT losses due to the mismatch between the actual MPP voltage and the DC voltage imposed by the central inverter represents by far the first loss contribution on the total harvested power. Although an intermediate DC-DC stage can help to reduce the mismatch, it cannot overcome the non-uniform irradiance among strings or panels.

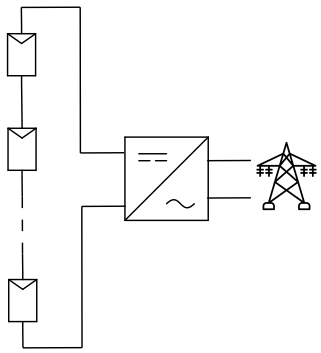
Some solutions have been proposed in the literature to limit the electrical characteristic mismatch between different strings, which may arise, for instance, by a single shaded PV module. The *voltage injection* approach is based on the injection of a bias voltage in the shaded / partially shaded string, to align its MPP voltage to the other strings [26]. The bias voltage is generated by an auxiliary DC-DC stage converting the array voltage. This approach can only offer a limited improvement in case of multiple shaded modules or strings. An alternative is to exploit an auxiliary DC-DC converter for each string, whose goal is to inject a sufficient offset voltage to forward-bias the bypass diodes of the shaded modules, in such a way that the energy harvesting from the irradiated remaining modules is preserved. This approach was proved to offer a significant energy harvesting improvement (from 23% to 95%) when strings are subjected to non-uniform irradiance scenarios [28].

String architectures

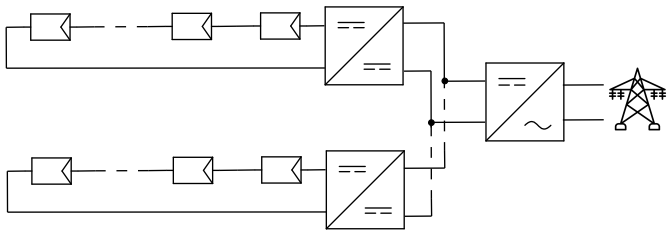
These architectures exploit an inverter for each string of PV modules, whose rated power is usually $< 10\,\text{kW}$, as shown in Fig. 2.4b. They represent wide-spread solutions for residential roof-top PV systems. In some cases, a dual conversion stage is adopted, where a DC-DC converter responsible for the MPPT is followed by the grid inverter. Compared to a single DC-AC stage, this approach allows to increase the MPPT efficiency, because the MPPT control is decoupled from the active and reactive power control of the inverter, which would impose a constant voltage at



(a) Centralized architecture.



(b) String architecture.



(c) Multi-string architecture.

Fig. 2.4 Medium and high power PV architectures based on arrays and strings.

the terminals of the string that may not correspond to the MPP voltage. In addition, since the DC-DC stage is designed to perform a voltage step-up, shorter strings can be used. A wide range of string inverter topologies have been proposed, mainly differing in the presence or absence of galvanic isolation, and in the single-phase or three-phase grid connection.

As in the case of centralized architectures, the series-connection of PV modules may cause mismatches and partial shading conditions that can dramatically reduce the yield of the PV system. The inclusion of PEC in the string can alleviate the issue by partially compensating the power mismatch between the PV modules: this solution is called *Generation Control Circuit* (GCC) [26, 29]. A first possibility of GCC is to design a multi-output PEC that forces each PV panel to work at the same constant voltage V_{string}/m, where V_{string} is the total string voltage and m is the number of PV modules in the string. Each converter output provides the difference between the string current and the current of the shaded PV module, but this system cannot extract the maximum power from each panel. An alternative more complex and more expensive solution, denoted by *multi-chopper* topology, is to equip each pair of PV panels with a Pulse-Width Modulated (PWM) DC-DC converter that implements

the MPPT for both the modules, enhancing the yield of the system in PSC [29]. A centralized and more complex controller is required to handle the individual MPPT. Multi-chopper solutions can be based on buck, buck-boost or flyback converters [30].

Multi-string architectures

An intermediate and flexible solution combining the advantages of the centralized and string architecture is the multi-string concept, in which every string is connected through a boost DC-DC converter to a common DC-link. A second inverting stage converts the DC-link voltage into a single-phase of three-phase AC voltage for the grid connection, as shown in Fig. 2.4c. The system can be scaled by adding more strings in parallel, but the rated power of the grid inverter is usually limited to $< 500\,\mathrm{kW}$ [23]. The advantage of the dual conversion stage is that the DC-DC converters are down-sized to the power of a single string and enable the string-level MPPT, which cannot be achieved with conventional centralized architectures. The same topologies of string inverters, isolated or transformerless, can be adapted for the multi-string DC-AC stage.

Recently, an increasing attention regarding large-scale PV plants has been devoted to Medium-Voltage DC (MVDC) distribution systems, interfacing the PV plant to a MVDC bus, usually in the $3\,\mathrm{kV} - 33\,\mathrm{kV}$ range. MVDC distribution systems offer the potential promising advantages of reduced cost and losses related to the cabling [31]. Multiple PEC architectures were compared in [32] integrating in a single performance indicator considerations on the losses in the cables, investment costs and cables and converters reliability. The simulative results showed that the number of LV-to-MV DC-DC converters is the main factor affecting the cost and reliability of the various solutions, especially for MW−range systems. On the other hand, an increased number of DC-DC stages allow to provide a more distributed MPPT, increasing the plant yield in PSC.

The attempt to compare centralized and multi-string PV architectures on the basis of their reliability is presented in [33]. As it will be detailed in Chapter 3, the reliability assessment of PECs is critical to analyze how influential is the power conversion stage in the whole conversion chain from the panel to the grid. In [33], a statistical and experimental analysis of the number and nature of the failures helped identifying the most crucial bottlenecks in a 2 MW centralized and in a 536 kW multi-

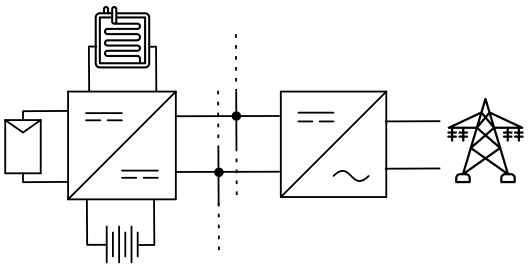


Fig. 2.5 Multi-port architecture interfacing a PV generator, a fuel cell and an ESS with a DC microgrid and the AC grid.

string plant. Using the Failure Modes, Effects and Criticality Analysis (FMECA) approach, the authors assigned a certain degree of severity, occurrence and detection to the different failure modes, and identified the most critical ones according to real-world data. The results showed that faults in the central inverter are characterized by a strong severity, meaning that a larger fraction of the PV power becomes unavailable in case of faults. On the other hand, the larger number of conversion stages in the multi-string architecture increases the occurrence of both faults in the inverters and in the DC cables.

Multi-port converters for different sources and loads

So far, the investigation was limited to converter architectures interfacing PV generators and AC grid only. Recent works in the literature have proposed DC-DC power converters designed to interface simultaneously multiple sources and/or loads, such as PV generators, fuel cells and Energy Storage Systems (ESS), to a local DC micro-grid. These solutions are gaining attention in the context of distributed generation and utilization of electrical energy from RES, to mitigate locally the intrinsic variability of PV generation. A representative block diagram of these solutions is shown in Fig. 2.5, but several different architecture configurations can be explored on the basis of the number and type of sources and loads.

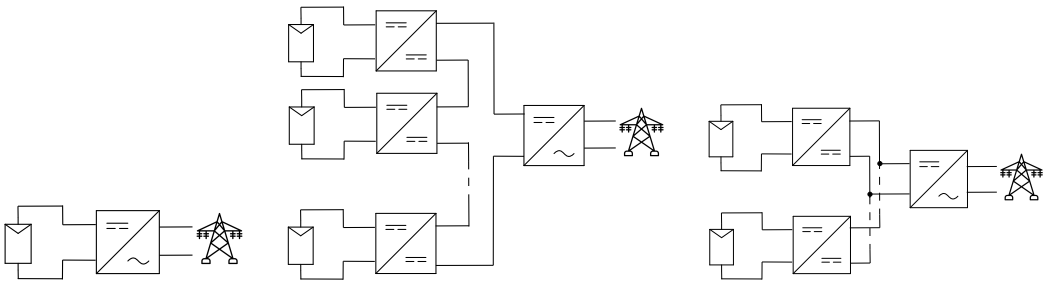
Most of the works of this research branch focus on the design of multi-port topologies, and innovative control approaches and system-level design considerations to optimize the interface among sources and loads of different nature, and characterized by different requirements. Conventional DC-DC converters are typically employed, such as triple active-bridges, push-pull or PWM converters derived from the synchronous boost. Examples can be found in the multi-port converters

presented in [34–36]. Other works exploit the Partial-Power Processing (PPP) approach to reduce the power ratings of the multi-port converter, allowing to improve the conversion efficiency and reliability of its components. Examples of multi-port PPP converters can be found in [37–40]. It is relevant to observe that the PV port is usually connected, in these cases, to a PV string or array.

AC module (microinverters) architectures

One of the fundamental and common limitations of the PV architectures investigated so far is the impossibility to harvest the maximum power from each PV panel when mismatches or non-uniform irradiance conditions occur. For large-scale PV plants, however, this drawback is significantly compensated by the lower initial investment costs of central inverters or multi-string inverters. When taking into account smaller PV plants for residential or commercial applications, instead, the maximization of the energy harvesting from all the PV panels can represent a desired condition to maximize the economic benefits related to the self-consumption of the RES-generated energy. In addition, especially when considering roof-top installations, partial shading scenarios can occur systematically, due to the presence of chimneys or adjacent buildings: in these conditions, the attractiveness of systems equipped with distributed MPPT increases even more. Systems in which every PV panel is equipped with an individual PEC are denoted by Module-Integrated Converters (MIC) or Module-Level Power Converters (MLPC).

A first popular concept of MLPC is represented by the micro-inverter (μ-inv), also called *AC-module*, in which every PV panel is individually connected to the low-voltage grid through a DC-AC stage, as in Fig. 2.6a [24, 23]. The PEC in this case must step-up the low voltage across the PV module (tens of volts) and invert it. In order to implement simultaneously the MPPT and AC power controls, both single-stage and dual-stage μ-inv have been proposed in the literature. Single-stage microinverters are characterized by a more challenging reactive power control [41], and require bulky electrolytic capacitors that limit the power density and reliability [24]. Dual-stage microinverters, on the other hand, consist of a high step-up DC-DC stage followed by an inverting stage, allowing for a more straightforward decoupling of the two controllers, at the expense of an increased component count. Many converter topologies were proposed and can be broadly classified on the basis of the presence or absence of galvanic isolation and the number of stages (one or two).



(a) Microinverter (μ-inv) architecture.

(b) Series Power Optimizers (SPO) architecture.

(c) Parallel Power Optimizers (PPO) architecture.

Fig. 2.6 Module-level PEC architectures.

The most intuitive advantage of micro-inverters is the modularity: since every PV panel is individually connected to the AC grid, the PV plant does not require a minimum number of panels, and panels of different power or voltage ratings can be combined without any mismatch issue. In addition, the parallel connection at the AC side ensures the individual maximum power extraction from each module, eliminating completely the yield reduction connected to PSC. In other terms, micro-inverters ensure the best MPPT efficiency. The combination of these elements makes this solution attractive for roof-top small-scale installations privileging the flexibility and the immunity to mismatches.

The power rating of micro-inverters is matched to that of PV panels in the hundreds of watts range. This allows discrete semiconductor devices and small or no heat sinks to be used. The power density is a critical design requirement for all the MLPC solutions, since the PEC are expected to be directly mounted on the back frame of the modules.

Compared to the previously-presented solutions, the maximum flexibility of micro-inverters carries the main drawback of an increased cost-per-watt, due to the larger number of PEC stages. The required high step-up gain is one of the main challenges to the cost, conversion efficiency and reliability of this solution: many creative solutions have been proposed in the literature to address this challenge, which will be presented in details in Chapter 3.

Power Optimizers

Beside micro-inverters, other MLPC have progressively become popular alternatives for their flexibility, high MPPT efficiency and modularity. They are denoted by *Power Optimizers* or *DC optimizers* and can actually be split into two categories [24, 42]:

- Series Power Optimizers (SPO), in which multiple MLPC are connected in series, like in Fig. 2.6b;
- Parallel Power Optimizers (PPO), in which the MLPC are connected in parallel to the same common DC bus, as in Fig. 2.6c.

Both solutions can be interfaced to the grid through an inverter, or be used in the context of DC microgrids to supply local DC loads.

SPOs exploit low voltage (near unity) gain PEC connected in a cascaded configuration. To keep the voltage gain low, a minimum number of PV panels is required in each string. The relaxed gain requirements and low voltage stresses allow the adoption of simple, efficient and non-isolated topologies such as the buck-boost converter, where all the semiconductor devices are rated for low voltages, comparable with the V_{OC} of the PV panels.

In principle, this kind of architecture should ensure the distributed MPPT. In case of uniform irradiance in the panels, all the SPOs generate equal voltages, while PSC induce non-uniform voltages that may result in temporary overvoltages. As known from the literature [43, 44], in extreme partial shading scenarios a centralized supervising control may be required to avoid overvoltages across some of the SPOs. In these cases, the safe operation of all the SPOs is guaranteed at the expense of losing the distributed MPPT.

Beside the presented control-based solutions, string current diverters have been proposed as an alternative to limit the impact of mismatches and partial shading in SPOs. They consist of half-bridge converters connecting the outputs of two consecutive SPOs, and including an inductor as storage element. In case of non-uniform irradiance, the conversion stage exploits the inductor to divert the string current and compensate the mismatch between the SPO outputs. In case of uniform irradiance, instead, the string current diverters are kept off and do not dissipate any power. This solution was proved to enhance by 15 % the MPPT efficiency of a partially shaded

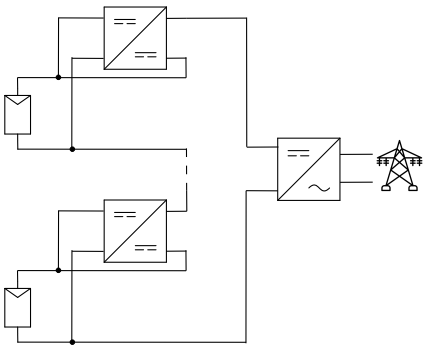


Fig. 2.7 Partial Power Optimizer architecture.

string compared to the single use of SPOs [45].

More similarly to micro-inverters, PPOs allow to completely decouple the power harvesting among multiple PV modules, because each panel is individually connected in parallel to the same DC-bus through the MLPC. As a consequence, they exhibit an excellent tolerance to mismatches and PSC. Differently from SPOs, they require a high step-up voltage gain, resulting in potentially decreased efficiency and reliability, and in more expensive active and passive components.

The previously presented power optimizers are designed to process the full PV power. Partial-Power Optimizers, based on the architecture illustrated in Fig. 2.7, have also been developed to improve the efficiency of SPO [42]. The output of the PEC is summed to the voltage of the PV panel, resulting in a reduction of the required voltage gain and in the transfer of some power with nearly 100 % efficiency. The topology of the PEC must be isolated or, in alternative, the input and output ports must be floating with respect to each other. The benefits of the PPP are maximized when the largest fraction of the power is directed through the most efficient path: this condition corresponds to the minimization of the voltage gain of the PEC. For this reason, this solution is better suited for the SPO concept, as illustrated in Fig. 2.7.

Sub-module power conversion

Exploiting the modular construction of PV panels, constituted by strings of cells connected in series or in parallel and equipped with bypass diodes, some works [24, 25, 46] have proposed to replicate the power optimization at sub-module level,

to maximize the power harvesting in case of PSC. In addition, the sub-module MPPT allows the elimination of the bypass diodes [24].

The potential energy yield was attested in a 4 kW PV plant to be up to $+18\,\%$ if the MPPT is performed at a sub-module level, and up to $+30\,\%$ with cell-level MPPT [46], under heavy partial shading scenarios. The advantage is almost null, instead, when the PV plant is subjected to uniform irradiance. The main limitation of these solutions is the high cost due to the difficult implementation and high number of PEC stages.

2.3 Requirements and challenges of PV-fed power converters

The increasing maturity of PV panels technology, associated to reduced costs and improved efficiency compared to the past, is shifting the attention to the design of the PEC. In addition, recent safety standards imposed by electric companies and governments have progressively be embedded in the design process. Independently from the specific PV architecture, it is possible to identify some requirements that apply to the PEC design [41, 23, 47].

Some of them can be generically classified as performance requirements. These include the conversion efficiency, defined as the ratio of the output and input electrical power. A high conversion efficiency implies reduced losses in the PEC, which in turns are associated to an improved reliability of the components and more relaxed thermal constraints. Considering the energy conversion chain from the solar energy to the electrical energy outgoing the PEC, the overall conversion efficiency η_{TOT} can be broadly computed as:

$$\eta_{\mathrm{TOT}} = \eta_{\mathrm{PV}} \cdot \eta_{\mathrm{MPPT}} \cdot \eta_{\mathrm{conv}}\,, \tag{2.1}$$

where η_{PV} is the conversion efficiency of the PV module, uniquely related to its technology and construction, η_{MPPT} is the MPPT efficiency, related partly to the configuration of the array / string, and party to the effectiveness of the control in harvesting the maximum power, whereas η_{conv} is the PEC efficiency.

The research on the PV technologies has pushed η_{PV} up to 25 % for the monocrystalline silicon, 22 % for the polycrystalline silicon, in laboratory environment [48, 49]. Efficiencies lower than 20 % can be reached with thin-fim technologies, such as amorphous silicon, Cadmium Telluride (CdTe) and Copper Indium Gallium Selenide (CIGS) [49]. Innovative cells based on hetero-junctions were proved to exceed the 25 % conversion efficiency [50, 51].

Regarding the MPPT efficiency, simple algorithms such as the Perturb & Observe (P&O) or the Incremental Conductance (InC) applied to the individual PV panels can already exceed the 98 % efficiency. The mismathces and non-uniform irradiance scenarios, as mentioned, are the main limiting factor to the MPPT efficiency.

The converter efficiency is largely affected by the selection of the topology of PEC and the technology of the devices. The peak efficiencies depend on the PEC architecture: large-scale PV inverters, for instance, are expected to be more efficient than micro-inverters, due to the required high step-up gain required and the limited scalability of some loss contributions, such as the quiescent and control losses. Due to the inherent power variability of a PV plant, the peak efficiency may not be the most representative figure of merit for a PV-fed power converter: at low irradiance operations, the PEC should still ensure a high part-load efficiency. This is the reason why more representative figures of merit have been defined, such as the European (EURO) efficiency or the California Energy Commission (CEC) efficiency, based on a weighted average of the converter efficiency at different power levels, aimed to reproduce the average performance of the PEC during an ordinary day[1].

Also the weighted efficiencies however, have the drawback of picturing the PEC performance in a limited operating range, at a single voltage. PSC, as described, may shift the MPP voltage far away from the rated value: as a consequence, a high-efficiency operation is desirable on the entire target MPPT range of the converter.

Power density is another performance requirement particularly for small-scale residential and commercial applications, while less relevant for large-scale plants. In case of MIC, the power converter must physically fit in the back-frame of the PV panel.

[1] https://www.pvsyst.com/help-pvsyst7/inverter_euroeff.htm (accessed Sept. 09, 2025)

One of the most common parameters of PV systems, especially when comparing multiple energy sources, is the Levelized Cost of Energy (LCOE), defined as the ratio of the sum of installation, maintenance and operational costs and the total harvested energy, defined over a target period [47, 52]. By combining in a comprehensive way both economic and yield-related considerations, this parameter represents a valid figure of merit to compare the cost-performance effectiveness of multiple solutions. An alternative economic indicator is the Pay-Back Time (PBT), defined as the number of years required to cover the initial investment of a PV system.

The reliability of the PEC is another critical design requirement, connected to the availability of the PV energy and to the overall costs of the PV system. Low-reliability PEC, indeed, are more likely to fail multiple times during the lifetime of a PV plant, implying increased replacement costs and a lower yield of the plant itself. Different PV architectures correspond, intuitively, to different levels of converter-level and system-level reliability. High-power central inverters or high-gain PEC (PPO), in general, feature a reduced converter-level reliability compared to string inverters SPO. Parallel architectures like PPO and micro-inverters, on the other hand, ensure an improved system-level reliability, because a failure in a converter does not compromise the productivity of the entire plant.

A detailed introduction to the design for reliability approaches is presented in Chapter 3.2. Ideally, and especially for MLPC, the lifetime of the PEC should match the lifetime of the PV panel at which it's connected, usually 25 years. However, for Building-Integrated PV (BIPV) applications, characterized by a more difficult accessibility to the plant, increased lifetimes are desirable.

Standardized additional requirements imposed on the design of PEC are the following:

- the maximum leakage current induced by the high-frequency harmonics of the modulation between the PV cells and the grounded panel frame. Some standards, such as DIN VDE 0126-1-1:2013-08 [53], define precise thresholds of leakage currents and corresponding maximum disconnection times. Both topological and control solutions have been investigated to limit this issue;

- some national codes, such as in Spain, require the galvanic isolation between the PV plant and the LV electrical grid [23];
- grid-tied PV systems are required to ensure a high (close to one) power factor and to generate an AC voltage synchronized with the grid [25];
- the anti-islanding is mandatory for grid-tied PV systems and consists in the fast disconnection of the PV converter in case of grid tripping, to prevent hazards to the locally supplied loads or to workers working at the PV-side. IEC 62116:2014 standardizes the test procedures for anti-islanding measures [54], whereas IEC 61727:2004 specifies the maximum disconnection times [55]. The anti-islanding methods, according to the level and involvement of the grid inverter in the detection of the abnormality, can be categorized into passive, active or communication-based [56].

Additional safety standards regulate the standardized test procedures of the protection systems in PV plants [57], the mandatory protection devices at the DC and AC sides of an inverter in distributed PV systems [58], the maximum tolerated open-circuit voltage or short-circuit current of disconnected low-voltage PV plants during technical maintenance or firefighting [59].

Selection criteria for a suitable PV architecture

On the basis of the presented considerations on the features of each PV architecture and the requirements imposed on the PEC design, it is possible to extract a list of general qualitative guidelines for the selection of a specific solution:

- the **application** is the first and most relevant criterion. It can actually be split into several application-related criteria, such as the plant capacity, the location of the installation (roof-top, building integration, open field, etc.), the exposure (probability of PSC), space constraints (especially in case of roof-top installations), the lifetime constraints (especially for BIPV systems). For large-scale plants, the minimization of costs may represent the guiding principle, which would lead to the selection of centralized or multi-string architectures; for smaller PV plants, instead, the maximization of the energy yield, enabled by module-level converters, may be preferred to reduce the pay-back time;

- the **module technology** can also represent a relevant influential criterion. The power rating and voltage rating of the single PV modules, for instance, constrain the power rating of grid inverters and the minimum length of strings. The module technology also influences the initial investment costs;
- the **electrical infrastructure** may also influence the choice of architecture. The presence of a LVDC infrastructure, for instance, makes the DC optimizers option more appealing, since it reduces the number of conversion stages;
- additional constraints, such as the galvanic isolation or the space constraints for the cabling, force the selection of PV architectures in which these requirements are met.

In general, the selection is based on multiple conflicting objectives, the foremost being the cost-performance trade-off. Tab. 2.1 summarizes the main advantages and drawbacks of the different architectures: the comparison takes into account in a qualitative way cost, MPPT and conversion efficiency, immunity to mismatches, ease of connection to the local electrical infrastructure.

Recently, an increasing attention is devoted to BIPV systems, which are installed directly in the construction phase of a building and, thus, are characterized by inherent features and requirements [60]. Flexibility and modularity are dominant design requirements in these cases, since the available installation area may be constrained by the geometry itself of the building. As mentioned, even stricter reliability constraints are imposed, given the difficult accessibility for replacing parts. Despite more expensive than Building-Applied PV (BAPV) systems, the hybrid combination of BIPV and BAPV was proved to exhibit an optimal trade-off between initial investment and energy yield [61].

Multiple attempts to qualitatively and quantitatively compare different PV architectures in residential BIPV context were proposed in the literature [60, 62]. A 100 kW BIPV plant was considered in [60], analyzing and comparing four different architectures: string inverters, micro-inverters (considering a LVAC infrastructure), SPOs and PPOs (LVDC infrastructure). The qualitative results showed that, among all the solutions, the PPOs maximized the MPPT efficiency, system reliability, modularity and flexibility. In [62], a more comprehensive analysis considers the techno-economic impact of the PV module technology (monocystalline silicon and

Table 2.1 Qualitative comparison of advantages and drawbacks of the different PV architectures.

Architecture	Advantages	Drawbacks
Centralized	Unique PEC stage Lowest cost for large-scale plants Easiest connection	Largest severity of failures Lowest MPPT efficiency Sensitive to mismatches among panels and strings Blocking diodes required to prevent hazards
String	Cost-effective solution for kW-scale plants No or low voltage gain step-up required	Sensitive to mismatches among panels Minimum number of panels required per string
Multi-string	String-level MPPT (not array-level)	More expensive than centralized architectures for large-scale plants Larger occurrence of failures
Microinverter	Best immunity to mismatches and PSC Highest MPPT efficiency Direct interface between panel and LV grid Maximum plant flexibility	Largest cost-per-watt Lowest conversion efficiency High step-up gain required
Series Power Optimizer	Low DC-DC voltage gain required Efficient and cheap PEC Distributed MPPT	Minimum number of panels required per string Need for supervisory algorithm to prevent overvoltages No MPPT in specific PSC
Parallel Power Optimizer	Best immunity to mismatches and PSC Highest MPPT efficiency Direct interface between panel and LVDC infrastrustrure Maximum flexibility	High step-up gain required Higher cost than SPOs Lower converter reliability than SPOs
Sub-module converter	Highest MPPT under any PSC Elimination of bypass diodes	Expensive and difficult integration No advantage for uniform irradiance conditions

CdTe) and PEC architecture (string inverter, PPO and micro-inverter) in two 100 kW BIPV case studies (one of the building characterized by a consistent partial shading). The analysis relies on efficiency and economic data of commercial PEC. The simulation results highlight multiple interesting considerations:

- the larger MPP voltage of the CdTe technology forces the adoption of shorter and more strings, making the string inverter solution more expensive than the PPO;
- for the same reason, the PPO solution resulted in the lowest pay-back time in the thin-film case, while comparable results were obtained between the PPO and string inverters for the silicon case;
- the PPO exhibited the highest annual energy yield in all the building and module technology cases.

Chapter 3

State of the Art

The purpose of this chapter is to introduce the state of the art with which this work will be compared. The previous chapter introduced the general context of the potential architectures and requirements of power converters designed for photovoltaic applications. The main requirements, namely, the high efficiency and the capability to operate over a wide range of operating points, were justified by the modelling and analysis of the impact of the environmental conditions on the electrical characteristic of PV generators.

The PPO concept was singled out as a flexible solution which still accepts multiple opportunities of innovation, from the adoption of Wide Band-gap (WBG) technologies, to innovative topological solutions, to the integration of multiple design approaches and constraints. Section 3.1 in this chapter proposes a classification of the most recent power converters designed for MLPC, with a specific focus on high-gain and wide-range PPO. Starting from introducing different step-up techniques, this section aims at identifying the most promising converter topologies from a performance standpoint, and at extracting qualitative considerations on the advantages and drawbacks of the different solutions.

Section 3.2 proposes a review of techniques for the reliability assessment of power converters. This will constitute a necessary introduction to the description of the design optimization methodology proposed in Chapter 5.

Finally, section 3.3 presents a review of PV-fed battery chargers for off-grid applications, aiming at identifying the state of the art in this context. This will serve as the basis for the development of a new converter topology, proposed in Chapter 6.

3.1 State of the art of high-efficiency parallel power optimizers

In the previous chapter, the description of the electrical characteristics of PV sources and their dependence on the environmental conditions have justified qualitatively the general performance requirements of PEC for this application. More quantitatively, the set of design specifications for a PEC should be based on the rated power and a reasonable voltage range of the PV source. In some cases in the literature, specific PV panels (in terms of technology and number of series-connected cells) are considered as references to tune the design of PEC: in these cases, for instance, the converters are optimized to achieve the highest performance in the neighborhood of the rated MPP voltage of the PV panel. In other cases, the objective of the design is made so as to ensure a flexible selection of the PV source, as in ultra-wide-range converters [63].

More specifically, when dealing with PPO or microinverters, the need for high step-up DC-DC converters in unavoidable, as the relatively low voltage of commercial PV panels (tens of volts) must be converted into suitably high voltage levels for the grid connection. To summarize, the desirable requirements of DC-DC converters for PPOs include the capability to work efficiently on a suitable power range and input voltage range, compliant with the MPP and with the influence of temperature, irradiance, and PSC. In all these working points, the converter must ensure the correct voltage step-up ratio. Power density and reliability, fundamental requirements for the commercialization of PV-fed converters, seem to be less frequently considered compared to performance metrics in the academic literature.

In the last decades, several papers have proposed a vast number of high step-up DC-DC converters aiming at addressing these simultaneous requirements. A clear classification of the exploited step-up techniques is not only relevant to provide a coherent organization of the existing literature, but also to outline common limitations and research gaps that can justify further advancements. In this section, an attempt is made to present the state-of-the-art converter topologies while highlighting the conceptual flow leading to the proposed solution. More in general, this section aims at presenting how the typical PEC specifications and requirements of DC-DC converters for PV applications were addressed in the past, and what opportunities of innovation were exploited to derive the proposed solution.

Due to the large number of exploited techniques, which are sometimes combined in innovative ways, it is not trivial to identify a unique taxonomy [64–66]. Nevertheless, significant overlaps can be highlighted between different reviews of high-gain power converters. In the systematic and comprehensive review presented in [64], some general characteristics are identified to offer a preliminary classification of PEC: the presence of galvanic isolation, the unidirectionality or bidirectionality of the power flow, their current-fed or voltage-fed nature, the implementation of hard switching or soft switching techniques, and the presence or absence of Right-Half Plane (RHP) zeros in their control-to-output transfer functions.

Some of them are particularly relevant for PV-fed applications: for instance, the inherently low input current ripple of current-fed topologies is beneficial to reduce the filtering requirements at the PV panel port and to minimize the power oscillations around the MPP induced by the switching operation; isolated topologies allow to comply with the galvanic isolation requirement imposed in some countries and, in addition, to inherently minimize the common-mode leakage currents between the PV panel and the ground [67].

The taxonomy proposed in the article is based on the main voltage boosting technique exploited in the power converter: switched capacitors (also denoted as charge-pump circuits), voltage multipliers, switched inductors, magnetic coupling (coupled inductors and high frequency transformers), multi-stage and multi-level converters. In general, PEC based on switched capacitors, voltage multipliers and switched inductors all rely on passive components acting as temporary energy storage elements: the alternate switching of active or passive devices in these converters enables the energy transfer between two different converter ports. Converters based on the magnetic coupling exploit this concept to transfer energy between multiple coils wound on the same magnetic core. In these cases, the turns ratios provide an additional degree of freedom to achieve a desired step-up gain. Finally, multi-stage/-level converters are based on the connection of multiple elementary stages in different ways. This group can be further sub-classified into cascaded, interleaved and multi-level topologies.

Concerning the PV and the fuel cells applications (often grouped together, given the similarities in terms of required gain and wide range), converters based on the magnetic coupling and multiple levels/stages are considered the most appropriate thanks to the flexibility of their design, the possibility to implement the soft-switching,

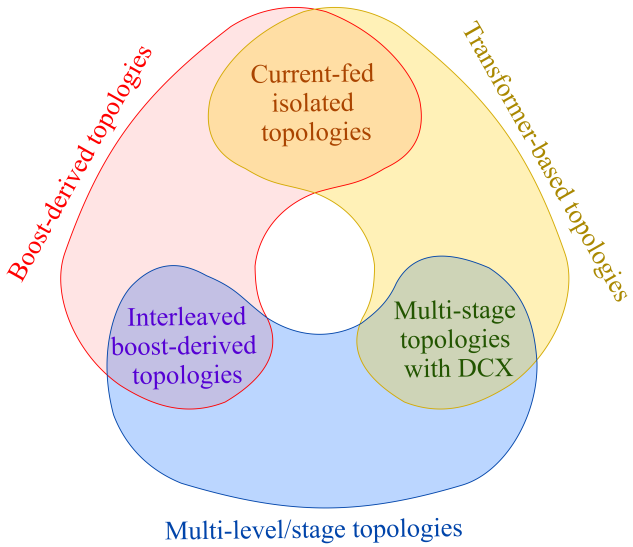


Fig. 3.1 Proposed classification of voltage-boosting techniques based on the analysis of high step-up converters for PV applications.

and the reduced voltage stresses of some components (especially in the multi-level concept). On the other hand, the presence of a transformer and/or multiple stages reduces the power density, which in some cases can be compensated by operating at higher frequencies.

Slightly different taxonomies, despite based on the same classification principle, are proposed in [65] and [66]. It is relevant to observe that, in both these papers, non-isolated and common grounded topologies are identified as the most appropriate solutions for renewable energy applications.

In this thesis, a slightly different taxonomy of high step-up DC-DC converters for PV applications is proposed and is shown in Fig. 3.1. The classification is still based on the employed voltage boosting techniques, as in [64], but is limited only to the techniques actually explored in the literature for the PV application: for instance, given the power ranges of typical PV modules (hundreds of watts) and the need to provide a variable voltage gain, converters based on fixed-gain charge-pump are not suitable for this application. Three macro-groups of DC-DC converters were identified and will be further detailed: boost-derived topologies, transformer-based topologies, and multi-level/-stage topologies.

A second relevant difference concerns the fact that converters are usually associated to a unique class in [64–66], to simplify the discussion. In many cases, as it will

be clarified, a rigid classification does not allow to effectively describe a converter operation: many DC-DC converter topologies are, indeed, obtained by integrating multiple step-up techniques and it is hard to identify a dominant one. For this reason, as shown in Fig. 3.1, specific sub-groups are highlighted at the intersections of the three macro-groups. The rest of this section describes in details the main features, advantages, disadvantages of each class, on the basis of the most recent topologies proposed in the literature. Firstly, the different macro-groups and sub-groups are presented, with specific focus on examples from the literature, and then some general qualitative and semi-quantitative comparisons are provided.

As a methodological note, this review is mainly based on peer-reviewed journal papers, especially *IEEE Transactions of Power Electronics*, *IEEE Journal of Emerging and Selected Topics in Power Electronics*, and *IEEE Transactions on Industrial Electronics*: the reason is that these journals typically accept for publication works characterized by a high degree of novelty that is supported by extensive experimental validation.

3.1.1 Boost-derived topologies

Given the inherent step-up requirement of PV applications, the conventional boost converter represents a natural starting point for the development of high-gain step-up DC–DC converters. Its reduced component count, low cost, current-source behavior, and shared ground between input and output ports make it an attractive solution from the power density, filtering, and leakage-current mitigation perspectives. The boost voltage gain in the Continuous Conduction Mode (CCM) follows the well-known (3.1). However, when operating at high duty cycles, the non-idealities of the converter components severely limit the maximum achievable gain, whereas the increasing voltage and current stresses on passive and active components limit the efficiency [64].

$$G_{\text{boost}} = \frac{1}{1-D}, \tag{3.1}$$

To overcome these limitations, extensive research has focused on boost-derived topologies aiming at preserving the advantages of the conventional boost while enhancing the voltage gain and reducing electrical stresses. These converters, which can be illustrated by the general architecture in Fig. 3.2, combine an input inductor–switch stage with one or more passive voltage-boosting networks. Typical

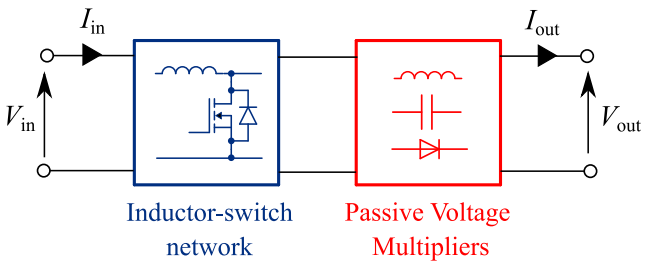


Fig. 3.2 General architecture of single-stage boost-derived converter topologies.

solutions integrate coupled inductors (CI), built-in transformers, switched-capacitors (SC) or voltage-multiplier (VM) networks, impedance-source networks, or their combinations [68–76]. The common objective is to achieve high gain at reduced duty cycles while limiting the voltage stresses across the semiconductor devices. Even higher voltage gains can be realized by employing quadratic or cubic boost topologies [77, 78].

Most of the above-mentioned converters rely on PWM control, with the duty cycle as the main control variable and additional gain factors linked to the turns ratios of CI or the number of VM stages. A major drawback is the hard-switching operation, which affects negatively the power density and EMI performance. To address this issue, resonant or quasi-resonant solutions have been proposed to enable partial or full soft-switching of the semiconductor devices [79–83].

Given the similar features and drawbacks, there are few converter topologies that are derived from the Single Ended Primary Inductor Converter (SEPIC) and buck converters [84–86] that are still included in this class.

Overall, boost-derived topologies offer reduced input current ripple and potentially lower semiconductor voltage stresses, at the expense of a high number of passive components (diodes and capacitors), which can jeopardize the power density, reliability, and cost of the converter. Interleaved implementations further mitigate current ripple and are discussed as a dedicated sub-category.

3.1.2 Transformer-based topologies

Transformer-based converters constitute a major class of high step-up solutions due to their inherent galvanic isolation and the high voltage gain enabled by the transformer, which, in principle, allows to reduce the number of passive components

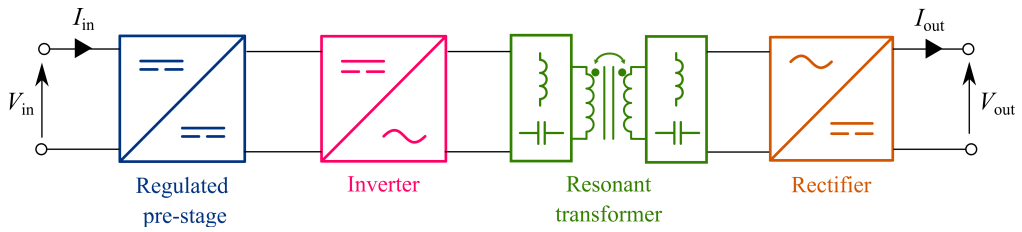


Fig. 3.3 General block scheme of resonant power converters for step-up PV applications.

required for the step-up. Beside the transformer turns ratio, which provides a fixed gain contribution, different modulation techniques were investigated to modify the voltage gain through the duty cycle, phase shift, switching frequency of the inverter transistors, or the duty cycle of the rectifier switches [87].

Most solutions belonging to this class can be described by the generic inverter–transformer–rectifier architecture shown in Fig. 3.3, consisting of a resonant isolated DC-DC topology (especially LLC and secondary-side Series Resonant Converters, SRC) with a front-end regulated stage that in some cases is absent. LLC and SRC converters represent the most common solutions due to their high efficiency, reduced switching losses, and improved EMI compared to hard-switched PWM topologies. However, their optimal performance is typically confined to a narrow operating range around the resonance frequency, wheres the efficiency can significantly degrade when the converter is forced to operate over a wide gain range, or at light loads, due to the losses in the transformer core and driving losses that do scale proportionally with the load [64]. Several approaches have been proposed in the literature to extend the gain range, such as the design of multi-resonant tanks [88], the multi-mode operation [89, 90], and topology-morphing rectifiers [91–95, 92]. While these solutions improve the flatness of the efficiency profile over a wide gain range, and reduce the extension of the frequency range to achieve a wide gain, they generally increase the circuit complexity and component count, especially in the rectifier stage. These solutions were analyzed with care, given the promising advantages in terms of wide-range operation. In particular, the capability of topology-morphing rectifiers to realize an additional gain step-up by simply controlling the conduction state of few transistors was considered an interesting technique to overcome the limitations of boost-derived converters at high gains operation and, at the same time, to reduce the efficiency drop of resonant converters operating far from the rated conditions.

Beside LLC and SRC-derived topologies, active-clamp flyback and push-pull converters [96, 97] represent other examples of transformer-based topologies. The transformer plays a crucial element in these converters to provide the galvanic isolation, define the voltage gain and enable the soft-switching through its magnetic parameters, but contributes significantly to the total losses and volume of the converter.

Different alternatives to enhance the wide-range operation consist in converters that include the front-end stage, as in Fig. 3.3: these converters can be classified more appropriately in the intersection of transformer-based topologies with the boost-derived or the multi-stage topologies.

3.1.3 Multi-level/stage topologies

The third macro-group identified in Fig. 3.1 consist of multi-stage and multi-level converters, which achieve high step-up ratios by combining multiple conversion stages or replicating capacitor-switch networks. Actually, most of the converters in this class are multi-stage, as multi-level converters are typically employed in higher voltage applications (800 V applications or above) to reduce the voltage stresses across the passive and active components, resulting in cost reduction and efficiency and reliability improvement. In multi-stage topologies, the overall voltage gain is obtained as the product or sum of the gains of the individual stages, according to their connections: with a proper selection of the two stages, they could represent an interesting solution to reduce the voltage and/or current stresses of the converter components, or limiting the efficiency drops of the individual stages when they are forced to operate at high gain.

Typical configurations for step-up applications include the cascaded architecture, (Fig. 3.4a), in which every stage processes the full power, and Partial-Power-Processing Input-Parallel-Output-Series (PPP-IPOS) architectures (Fig. 3.4b), in which each stage processes only a fraction of the total power. In IPOS architectures, a topological constraint requires that one the two stages must be isolated or, at least, the two stages should not share the same ground at the output port [98].

From a qualitative standpoint, cascaded architectures effectively reduce the gain requirement of each stage, whereas PPP-IPOS configurations inherently relax the current and voltage stresses of all the components, potentially offering higher

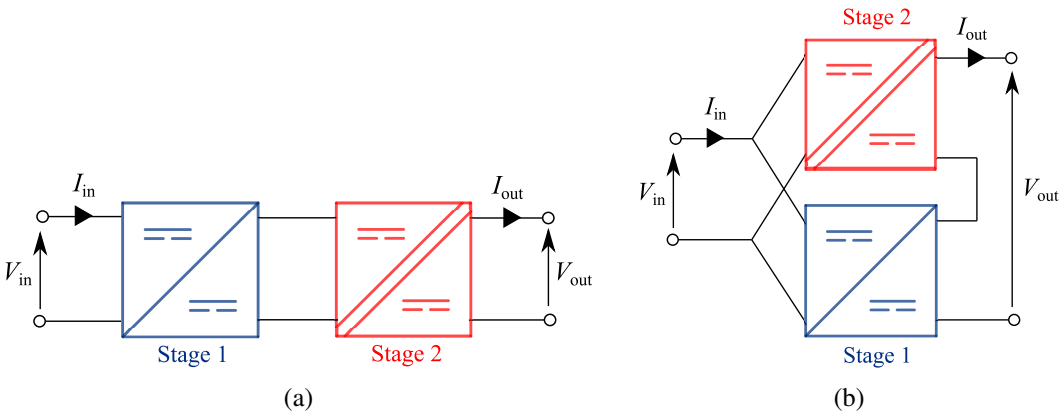


Fig. 3.4 Generic block diagrams of two different types of multi-stage converter architectures: (a) Cascaded; (b) Partial-Power-Processing Input-Parallel-Output-Series (PPP-IPOS).

efficiency. These benefits come at the cost of increased component count and more complex control strategies. The combination of different conversion stages gives rise to a large variety of multi-stage topologies: representative examples designed for PV applications were proposed in [99–101].

The boundary between multi-stage converters and other classes is not always sharp. For instance, multi-stage interleaved converters based on the repetition of boost-derived topologies should be included at the intersection between these two classes. On the other hand, multiple converters in the literature are based on LLC or SRC operating as DC transformers (DCX), designed to provide the largest fraction of the voltage gain, while additional auxiliary low gain and low power stages allow the fine modulation of the gain. These converters are in this thesis included in the intersection between multi-stage and transformer-based topologies, as shown in Fig. 3.1.

Before moving to the analysis of the converters based on the intersection of multiple classes, it is helpful to draw an overview of the main features, advantages and drawbacks of the three macro-classes of high step-up converters presented so far, which are listed in Tab. 3.1. The comparison is purely qualitative and inherently generic, but it can help to highlight common aspects that will be emphasized further in this section.

Table 3.1 Qualitative comparison of different step-up converter classes according to multiple features.

Feature	Boost-derived topologies	Transformer-based topologies	Multi-stage topologies
Galvanic isolation	No	Yes	Depending on stages
Input current ripple	Low	Higher	Depending on stages
Number of passive components	High	Lower	High
Soft-switching	Requires extra components	Assisted by magnetic design of the transformer	Depending on stages
Gain range	Limited by stresses	Wide with multi-mode operation	Wide

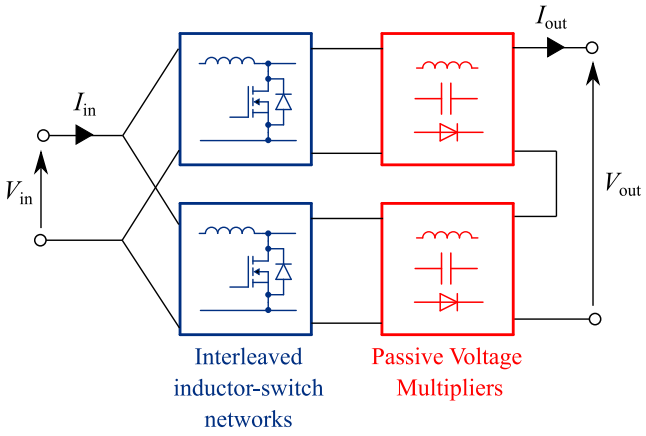


Fig. 3.5 General architecture of interleaved boost-derived converter topologies.

3.1.4 Interleaved boost-derived topologies

According to the proposed taxonomy shown in Fig. 3.1, interleaved boost-derived converters can be regarded as the intersection between boost-derived and multi-stage topologies. By properly phase-shifting the active devices of multiple boost-derived stages in IPOS configuration, as in Fig. 3.5, these converters can achieve at the same time an increased voltage gain and a significant reduction of input current ripple. The gain capability can be further enhanced by employing CI and VM [102–107], built-in transformers [108] or multi-level flying-capacitors networks [109]. As in single-stage boost-derived case, most converters in this class operate in CCM, leading to

hard-switching losses and increased EMI. In few examples, quasi-resonant solutions based on additional circuitry have been proposed to enable the soft switching of the converter transistors [110].

Few alternatives from the architecture of Fig. 3.5 were proposed in the modular multi-stage SC converter in [111], and in the hybrid boost-zeta converter in [112].

Globally, the modular architecture and a suitable control scheme of these architectures allow to provide a high voltage gain, reduce the electrical stresses of all the components and reduce or minimize the input current ripple, at the expense of high passive component count, limited frequency operation, and lack of galvanic isolation. An additional limitation is associated with the use of identical stages in interleaved converters, which generally results in a monotonic efficiency profile in the target voltage range. In PV applications, where optimal performance is desirable at a designated rated input voltage that may lie within the central portion of the operating range, such interleaved architectures may not be well suited. As a consequence, this work identified asymmetric IPOS converters as more promising solutions, due to their enhanced design flexibility in achieving optimal performance at arbitrary intermediate operating voltages.

3.1.5 Current-fed isolated topologies

Current-fed isolated converters are based on the introduction of a boost-like front-end stage to an isolated transformer-based topology, and can thus be included in the intersection between these two classes of converters. This approach provides an additional degree of freedom to enhance the voltage gain while reducing the input current ripple at the same time, compared to the voltage-fed counterparts. Many converters of this class are derived from hard-switched [113], quasi-resonant [114] or resonant [115, 116, 63] current-fed half-bridge topologies. Alternative current-fed solutions proposed in the literature are derived from the push-pull [117, 118], the full-bridge DC-DC converter [119–121], the SRC [122] and from the LLC [123].

Globally, this class of converters share with transformer-based topologies the galvanic isolation and, in most of the cases, the soft-switching of the active devices. The boost-like front-end stage helps reducing the input current ripple and enhancing the voltage gain capability, at the expense of the increased volume and losses introduced by the additional magnetic components.

Table 3.2 Summary table of different variations of the general block diagram in Fig. 3.3 for the state of the art resonant step-up converters for PV power optimizers.

Block	Examples
Pre-stage	Synchronous boost [124], reconfigurable PWM stage [125] quasi-Z source / Z source stage [90], current source (L) [115, 122], no pre-stage [88, 87, 97, 89, 93, 92, 94]
Inverter	Full-bridge [88, 87, 124, 122, 89–91, 93, 92, 125, 94], Half-bridge [115], Push-pull [97]
Resonant transformer	LLC [124, 92, 125, 94], LC [87, 115, 122, 97, 89–91, 93], LLCC [88]
Rectifier	VDR [88, 115, 124, 89, 90, 125], VQR [87], Topology-morphing rectifier [91, 93, 92, 94], Synchronous rectifier [122, 97]

3.1.6 Multi-stage topologies based on DCX

A final class of converters in the proposed taxonomy exploits resonant DC–DC converters operating as DC transformers (DCX), providing high efficiency at resonance but fixed voltage gain, and an additional stage, responsible for the gain modulation. Typically, the DCX stage is designed to process the largest fraction of input power and/or to realize the largest part of the overall voltage gain, so as to reduce the electrical stresses of the additional auxiliary stage. As in multi-stage topologies, multiple configurations can be realized: cascaded architectures as in Fig. 3.3 were proposed in [124, 125], while converters based on the PPP-IPOS concept were proposed in [126–129]. In both [128] and [127], the experimental characterization of IPOS and cascaded converters designed for the same specifications proved the superior efficiency of the PPP concept.

In general, these converters combine the high efficiency operation of DCX with the improved wide gain capability enabled by the additional stage, at the expense of increased component count and design complexity.

Tab. 3.2 summarizes different examples in the literature of transformer-based and multi-stage transformer-based topologies that can be described by the general block diagram of Fig. 3.3.

3.1.7 Comparison of state-of-the-art topologies

So far, a large number of step-up converters was analyzed to derive common features, advantages and drawbacks. In this section, an attempt is made to compare some of the main performance parameters extracted by the reviewed papers, in order to provide a more quantitative analysis of the different classes of converters. More precisely, the following parameters were considered for the comparison: the rated power, the CEC efficiency η_{CEC}, defined in (3.2), and the gain range ΔG, computed as in (3.3):

$$\begin{aligned}\eta_{\text{CEC}} = {} & 0.04 \cdot \eta_{10\%} + 0.05 \cdot \eta_{20\%} + 0.12 \cdot \eta_{30\%} + 0.21 \cdot \eta_{50\%} \\ & + 0.53 \cdot \eta_{75\%} + 0.05 \cdot \eta_{100\%}\end{aligned} \tag{3.2}$$

$$\Delta G = \frac{V_{\text{out}}}{V_{\text{in,min}}} - \frac{V_{\text{out}}}{V_{\text{in,max}}}\,. \tag{3.3}$$

While the CEC efficiency represents a well-established figure of merit to quantify the average performance of a PV-fed converter (either a microinverter or a power optimizer) during its ordinary operation, the gain range is a simplified parameter to describe its effectiveness in operating outside the rated voltage. The information on the CEC efficiency is not always available in the analyzed papers: in some cases, this value was computed from the reported experimental efficiency graphs at the rated voltage, applying (3.2). From a methodological standpoint, the voltage gain range of a converter in the literature was computed on the basis of the experimentally validated working points, and not simply by considering the theoretical target range specified in the design. In some cases, indeed, only experimental tests at a single, rated voltage were provided: for these converters, $\Delta G = 0$. This choice does not mean that these converters are unable to operate outside the rated voltage condition, but that there is no reported experimental evidence to establish that they operate in the correct way and with satisfactory performance outside that condition.

First of all, Fig. 3.6a shows the scatter plots of the CEC efficiencies and year of publication of the reviewed converters. The literature review only considered papers that were published in the most recent years, between 2010 and 2025. As it can be seen, the highest CEC efficiencies were obtained by boost-derived and transformer-

based topologies. The highest attested efficiency of multi-stage topologies was around 96 %.

Fig. 3.6b shows a scatter plot of the rated power and gain range of the reviewed converters. The simultaneous analysis of these two features allows to evaluate the capability of a converter to operate on a wide range of operating powers and voltages, both relevant requirements of PV applications. The scatter plot highlights that the highest rated powers were achieved by boost-derived and multi-stage topologies, while the best performances in terms of wide gain range were obtained by transformer-based and current-fed transformer-based topologies.

Finally, Fig. 3.6c shows the scatter plot of CEC efficiency and gain range of the reviewed converters. Boost-derived, transformer-based and current-fed transformer-based topologies do exhibit the best CEC efficiencies; in particular, multi-mode transformer-based converters offer the best balance between CEC efficiency and wide gain range.

The presented analysis of the existing literature allows to extract a clear overview of the common advantages and drawbacks of different voltage boosting techniques. The high-performances of multi-mode transformer-based topologies at and outside the rated operation make them the potentially most promising solutions to further enhance the wide-range operation of a power converter for PV applications. The design flexibility and high-voltage gain offered by multi-stage converters, without incurring in a large number of passive devices, could be exploited to properly design a converter so as to achieve its best performances at a desired rated condition. Finally, the reduction of the electrical stresses in PPP-IPOS converters could be exploited to select more efficient semiconductor devices.

Building upon these considerations, this work proposes the development of a novel converter topology characterized by wide voltage gain and high efficiency. As it will be detailed, the proposed converter combines for the first time the wide-gain feature of multi-mode topology-morphed converters with the design flexibility and reduced stresses of the PPP-IPOS architecture. Specific design choices operated on the two stages of the converter will be introduced to overcome the limitations of existing solutions in the literature, further enhancing the innovation of the proposed solution: as an example, the low-gain synchronous boost used as auxiliary stage will be operated in the Boundary Conduction Mode (BCM), overcoming the efficiency and EMI limitations of the CCM operation.

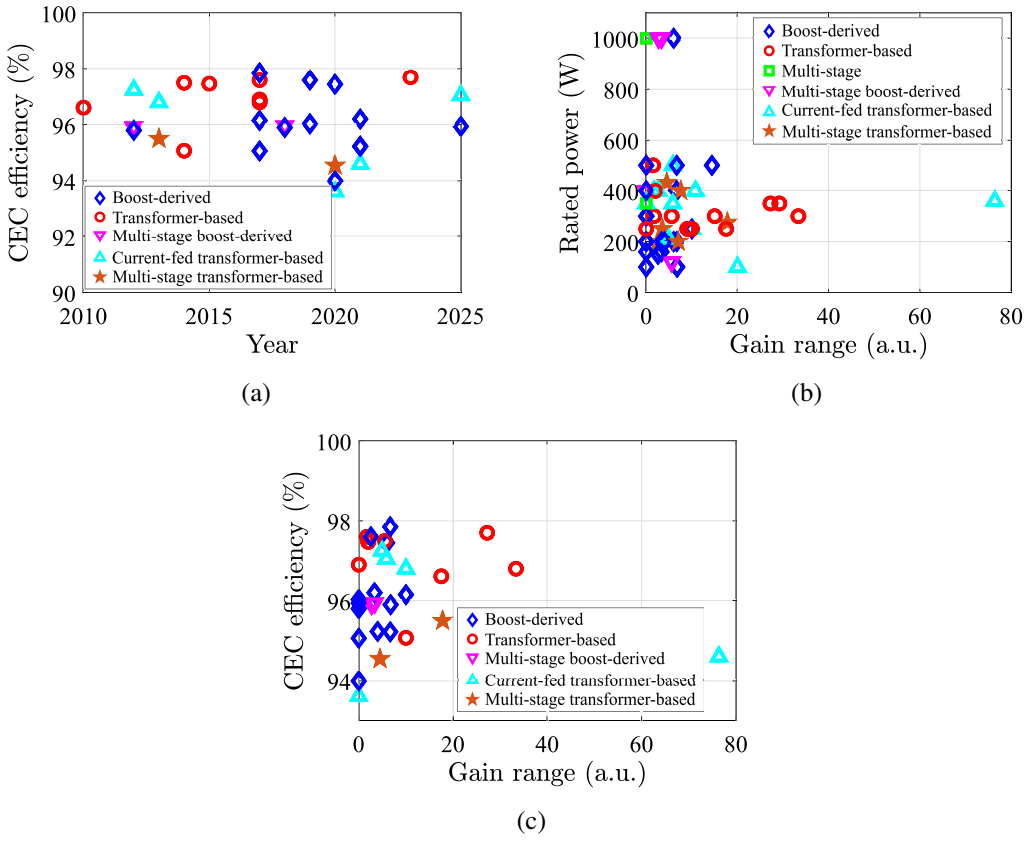


Fig. 3.6 Scatter plots of the reviewed papers: (a) CEC efficiency and year of publication of the analyzed papers; (b) Rated power and gain range; (c) CEC efficiency and gain range.

3.2 Reliability assessment of power converters

The review of the academic literature presented so far showed a predominant focus on optimizing the converters performances on a given range of operating conditions. Application-oriented metrics such as cost and reliability are very often neglected or addressed only superficially and qualitatively. Due to these limitations, Chapter 5 presents a systematic design optimization of the IPOS converter topology proposed in Chapter 4, which not only includes the maximization of the conversion efficiency as the goal of the design, but integrates cost- and reliability-aware considerations. The objective of this second design of the proposed converter aims at analyzing critical design aspects often disregarded in the scientific academic literature, which are instead crucial from the commercial point of view. The rest of this section is devoted to an introduction on the reliability modelling of PEC, with particular attention to the procedures used to estimate its lifetime based on a given mission profile.

As a general definition, reliability is the capability of a system / component to perform its intended function under specified conditions and in a designated period of time [130]. The performance of the system should be ensured within acceptable limits over the target time interval. This definition can be applied to multiple systems involving interacting elements and subsystems. For a systematic reliability analysis, it is important to clearly state what are the degradation or malfunctioning conditions at which the system can be considered to have failed. When the system fails, it is necessary to replace at least some of its parts, which will result in the temporary unavailability of the functions and replacement costs. When dealing with PV systems, the fault of one of its components can cause the unavailability of part or all the power harvested from the modules. The power converters responsible for the grid-interface were proved in multiple works to be the main source of failures in PV systems: in [131], the analysis of faults in 350 different sites of PV plants operated by SunEdison over a two-year period revealed that 43 % of the faults were connected to the grid inverters, while only 2 % were related to PV modules; in [132], the analysis of 180 large-scale PV plants in the 2015-2016 period identified 89 % failures in the grid inverter.

As said, the reliability of a system depends on the combination of the reliability of its components. Usually, the process of reliability analysis of a component is based on the derivation of its failure rate $\lambda(t)$, whose behaviour describes the probability

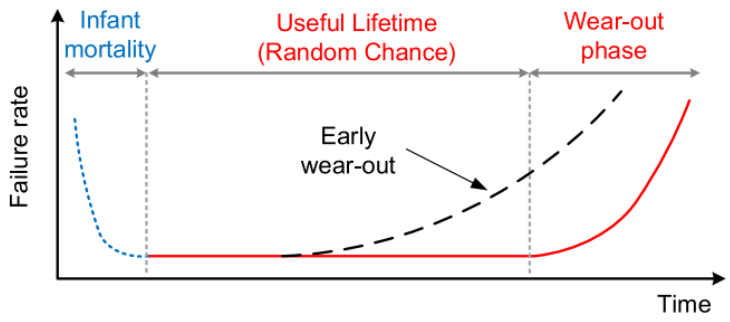


Fig. 3.7 Typical qualitative bathtub curve of the failure rate λ. Source: [130].

of a component to fail at a certain moment in its lifetime. A typical qualitative behaviour of a component $\lambda(t)$ is shown in Fig. 3.7. Given the peculiar shape, this qualitative behaviour is usually denoted a "bathtub" curve.

The curve shows an initial steep decreasing trend which is linked to the debugging and manufacturing processes, before the component/product starts its operation [130, 133]. The constant part of $\lambda(t)$ is linked to single-event catastrophic and random failures which may happen by change during the operation of the component, without taking into account its degradation. Typical failure modes associated to a constant λ, for example, are sudden short-circuits or dielectric breakdown in electrolytic capacitors, and high voltage breakdown, secondary breakdown or latch-up in semiconductor devices [134, 135]. The constant failure rate of components is difficult to predict and is based on historical data of failures of components operating at the same operating conditions [134]. A comprehensive database of failure rates for electronic components is provided by the Military Handbook, usually known as MIL-HDBK-217F (and its later updates) [136]. This latter handbook provides generalized guidelines to adjust the estimation of the failure rate of a component based on its operating conditions: according to this approach, the failure rate can be expressed as [137, 138]:

$$\lambda = \lambda_b \cdot \prod_i \pi_i \,, \tag{3.4}$$

where λ_b is the base failure rate specified in the MIL-HDBK-217F, whereas π_i are correction factors taking into account the specific stresses to which the component is exposed (average temperature stress, power dissipation, voltage, environmental conditions, vibrations, etc.) [138]. Given the random nature of the failures modelled by constant λ, the reliability of a component can be alternatively expressed in terms

of the Mean Time Between Failures (MTBF), defined as:

$$MTBF = \frac{1}{\lambda}. \tag{3.5}$$

Once the individual constant failure rates are computed for any component of a system, the total failure rate λ_{sys} of the system can be obtained by [138]:

$$\lambda_{\text{sys}} = \sum_i \lambda_i N_i, \tag{3.6}$$

where N_i is the number of components of the same type and exposed to the same stresses.

An important remark is that the failure rates predicted or estimated using this approach are based on empirical data that do not consider at all the physics of the failure mechanism: as such, the predicted reliability may not be accurate enough [134]. The FIDES approach was introduced in 2004 with the specific goal of integrating the physics of failures associated to thermal, electrical and mechanical stresses [139]. The approach proposes to compute the constant failure of a component as:

$$\lambda = \Pi_{\text{qm}} \Pi_{\text{pr}} \lambda_{\text{ph}} \Pi_{\text{pg}}, \tag{3.7}$$

where Π_{qm} is linked to the level of quality ensured during the manufacturing phase, Π_{pr} is linked to the various processes entailed in the components's lifecycle, λ_{ph} describes the intrinsic physics-related failure rate due to stresses on various nature, and Π_{pg} is a process-grade factor indicating an assessment of effectiveness of the adopted design methodology.

Independently of how λ is computed, the corresponding reliability function $R(t)$ of a component or system in which only random failures are considered is an exponential function:

$$R(t) = e^{-\lambda t}. \tag{3.8}$$

Other relevant and easily derived functions in this particular cases are the probability distribution function (PDF) $f(t)$ and unreliability function $U(t)$. As expressed in (3.9), $f(t)$ is an exponential PDF whose rate factor is the failure rate λ. The integration over time of $f(t)$ gives the cumulative likelihood that the component or system fails before time t: this function is thus denoted as unreliability function,

Device	Failure type	Failure rate	Failure mode	Failure mechanisms
Semiconductors	Catastrophic failures	Constant	Open circuit	Device failure in gate driver, Driver board short-, open-circuit
				Bond wire lift-off, Bond wire rupture after IGBT short-circuit
			Short circuit	High voltage breakdown
				Dynamic latch-up
				Second breakdown
				Impact ionization
				High temperature due to power dissipation
	Wear-out failures	Non-constant	Parameter drift	Chip solder joint cracking
				Baseplate solder joints cracking
				Wire bonds lift-off/cracking
*Al-Caps	Catastrophic failures	Constant	Open circuit	Self-healing dielectric breakdown
				Disconnection of terminals
			Short circuit	Dielectric breakdown of oxide layer
	Wear-out failures	Non-constant	Parameter drift	Electrolyte vaporization
				Electrochemical reaction
**MPPF-Caps	Catastrophic failures	Constant	Open circuit	Self-healing dielectric breakdown
				Connection instability by heat contraction of dielectric film
				Reduction in electrode area caused by oxidation of evaporated metal due to moisture absorption
			Short circuit	Dielectric film breakdown
				Self-healing due to overcurrent
				Moisture absorption by film
	Wear-out failures	Non-constant	Parameter drift	Dielectric loss
***MLC-Caps	Catastrophic failures	Constant	Short circuit	Dielectric breakdown
				Cracking; damage to capacitor body
	Wear-out failures	Non-constant	Parameter drift	Oxide vacancy migration; dielectric puncture; insulation degradation; micro-crack within ceramic

*Al-Caps: Aluminum-electrolytic Capacitors
**MPPF-Caps: Metalized Polypropylenes Film Capacitors
***MLC-Caps: Multi Layer Ceramic Capacitors

Fig. 3.8 Summary of common catastrophic and wear-out failure modes in semiconductor devices and capacitors. Source: [134].

as expressed in (3.10). Conversely, $R(t)$ can be described as the likelihood that the component of system survives until time t.

$$f(t) = \lambda e^{-\lambda t} \tag{3.9}$$

$$U(t) = \int_{-\infty}^{t} f(t')dt' = 1 - R(t)\,. \tag{3.10}$$

Coming back to the bathtub curve illustrated in Fig. 3.7, the rising part of the curve is related to the failure mechanism associated to the wear-out of the components induced by repeated electrical and thermal stresses, and its modelling can only be based on the analysis of the physics of the degradation mechanisms induced by the stresses. Some of them include, for example, the solder degradation and bond lift-off in semiconductor devices, and the electrolyte vaporization in electrolytic capacitors, which determine gradual parameters shifts leading eventually to unsatisfactory performance. Fig. 3.8 summarizes common catastrophic and wear-out failure modes in semiconductor devices and capacitors, which are, as explained, associated to the constant and rising sections of the failure rate curve, respectively [134].

A typical and established reliability analysis of a power converter which considers the wear-out failure modes of its components is described in [140, 141, 130] and is here illustrated through its main steps. In general, it consists in a bottom-up approach in which the stresses induced on the converter components are translated into individual PDF, which are then combined in a unique reliability function of the system.

Lifetime modelling of converter components

The converter reliability is limited by its most critical components, i.e., the components which are most likely to fail during the converter operation. Usually, the electrolytic capacitors and the semiconductor devices represent the main contributors to the converter failures, therefore the literature particularly focuses on these two classes of components [142]. Once having identified the critical components, a lifetime model based on experimental data should be derived. This is performed by exposing a certain number of components to repeated electrical or thermal cycles and monitoring a limited number of quantities that can be directly associated to a degradation mechanism. For instance, two of the main wear-out failure mechanism in IGBT power modules are the bond-wire lift-off, whose degradation can be linked to an increase of the collector-emitter voltage V_{ce}, and the degradation of the die soldering, which can be associated to an increase in the junction-case thermal resistance [140]. A threshold value of the observed quantity must be established to define when the component is said to fail for a specific type of degradation, e.g. a certain relative increase of V_{ce} compared to the initial value. At this point, analytical models based on empirical parameters are used to fit the experimental data. In the case of electrolytic capacitors, for instance, the lifetime L_o of a capacitor is usually expressed as a function of the operating voltage V_o and temperature T_o through two empirical parameters n_1 and n_2 [134]:

$$L_o = L_n \cdot 2^{\frac{T_n - T_o}{n_1}} \left(\frac{V_o}{V_n} \right)^{-n_2}, \tag{3.11}$$

where T_n, V_n and L_n are the nominal temperature, voltage and lifetime usually expressed in the capacitors datasheet.

In the case of power modules or discrete power semiconductor devices, the lifetime models are usually expressed in terms of the number of cycles to failure

$N_{\mathrm{f},i}$. $N_{\mathrm{f},i}$ describes after how many thermal cycles of a certain type, i.e. with given junction average temperature $\overline{T}_{\mathrm{j},i}$ and temperature ripple amplitude $\Delta T_{\mathrm{j},i}$, the device is considered failed. The reason for this dependence is that the different thermal expansion coefficients in different layers of a semiconductor component (pad to heat-sink, bond-wire to die, etc.) result in stress-strain deformations potentially leading to cracks and lift-offs [141]. The lifetime model includes the Coffin-Manson and Arrhenius terms of (3.12), with additional terms eventually taking into account operating voltages, current density per bond wire, and duration of thermal cycles [141, 143]:

$$N_{\mathrm{f},i} = A \cdot \Delta T_{\mathrm{j},i}^{B} \cdot e^{\frac{E_{\mathrm{a}}}{k_{\mathrm{B}}\left(\overline{T}_{\mathrm{j},i}+273\right)}}, \tag{3.12}$$

where A, B and E_{a} are empirical parameters. Similar models with different empirical parameters were derived for power modules [143–145] and discrete semiconductor devices [146–148]. The derivation of lifetime models consists in a long process and requires specific expensive instrumentation to impose the thermal cycles and measure the degradation effect on the devices under test (DUT): in many cases, therefore, the designers of power converters rely on the most suitable models available in the literature without repeating the characterization. This approach was also exploited, as it will be clarified, in this work.

Mission-profile based computation of accumulated damage

In general, the above-mentioned models provide an estimation of the lifetime of the DUT under a specified repeated thermal stress. In most of the applications, however, the computation of a single $N_{\mathrm{f},i}$ is not representative of the degradation induced by the variable working points of the mission profile. When dealing with complex mission profiles, the first step is to compute from every working point the corresponding electrical and thermal stresses on the DUTs: in PV applications, this approach consists in deriving, for each working point of the PV plant, the corresponding electrical stresses in every component of the converter and, through proper electro-thermal models, derive the associated junction temperature (for semiconductor devices). Every time-series of working points, thus, can be translated in a time-series of junction temperatures. These should be decomposed in elementary thermal cycles, relying on counting algorithms such as the rainflow counting [140, 141]. Each type of thermal stress, identified by i and repeated N_i times, generates an accumulated damage AD_i

equal to:

$$AD_i = \frac{N_i}{N_{\mathrm{f},i}}\,. \tag{3.13}$$

Under the Miner's assumption that all the damage contributions accumulate linearly, the total accumulated damage for the entire mission profile follows:

$$AD = \sum_i AD_i = \sum_i \frac{N_i}{N_{\mathrm{f},i}}\,. \tag{3.14}$$

When $AD = 1$, the device is considered failed. A similar approach can be followed for electrolytic capacitors.

Derivation of converter reliability

Reliability is an inherently statistical concept: a single, deterministic value of AD computed by (3.14) is not representative of the lifetime of a component and, even less, of the lifetime of a system in which the components is inserted. To take into account the unavoidable tolerances of the lifetime model and the physical parameters variations of the devices, a statistical approach based on Monte-Carlo simulations is often adopted [141, 133]. This approach consists in repeating the AD computation many times, assuming that the values of the model parameters and/or the working points of the mission profile are not fixed, but can vary according to pre-defined PDFs. If AD is the accumulated damage of a DUT after one mission profile, it follows that $1/AD$ represents the number of mission profiles that the DUT can sustain before failing. In the particular case in which the mission profile refers to one year, the term $1/AD$ coincides with the lifetime of the DUT expressed in years.

The repeated simulations give rise to a distribution of lifetimes $1/AD$ which can be fitted by a proper PDF (usually, a Weibull or Gamma distribution): by definition, the continuous function represents the unreliability $U_k(t)$ of the component k. In case of multiple components in a power converter, each one characterized by its specific $R_k(t)$ and $U_k(t)$, the unreliability of the converter can be computed as:

$$U_{conv} = 1 - \prod_k R_k = 1 - \prod_k (1 - U_k)\,. \tag{3.15}$$

In case of non-redundant components, the product of reliability functions underlines the fact that a single, unreliable component affects significantly the reliability of the complete converter. The lifetime of a power converter is usually expressed

as the time B_x at which a certain fraction x of converters has failed, according to the unreliability function $U_{\text{conv}}(t)$. For instance, B_1 denotes the time (in years) after which the 1 % of the converters has failed. In mathematical terms:

$$U_{\text{conv}}(B_x) = x \longrightarrow B_x = U_{\text{conv}}^{-1}(x). \tag{3.16}$$

The target lifetime of a power converter depends on the specific or desirable requirements of a specific application. In 2018, a survey on more than 80 companies revealed that the majority of the manufacturers in the PV and electric vehicles (EV) sectors target a lifetime of 10 to 20 years, while companies producing wind systems target 20-30 years [142].

3.3 State of the art of PV-fed battery chargers

The last part of this thesis introduces a new power converter designed for off-grid PV-fed low-voltage battery charging. In off-grid PV-fed scenarios, where the electrical grid is not available, PECs are usually designed as interfaces between the environment-dependent generator, namely the PV source, and the ESS: such a system ensures continuity of power delivery to the local loads, even during low-irradiance conditions. Consequently, battery chargers designed for this application not only need to consider the reliability of the charging procedure, to preserve the lifetime of the ESS, but should also take into account that the PV generation may vary significantly throughout the day. Thus, the same considerations performed for grid-tied PV systems, such as the need to track the MPP on a wide range of operating voltages and powers, can be applied in this case. Additional power converters, when needed by the application, can further convert the electrical energy from the ESS to other DC or AC loads. A generic power conversion chain of an off-grid PV-fed charging station is illustrated in Fig. 3.9.

Fig. 3.9 Typical power conversion chain of an off-grid PV-storage system supplying local DC or AC loads.

In this section, a preliminary review of the existing literature is presented to illustrate the most recent advances in the PV-fed battery charging application. It is important to observe that the review mainly focuses on small-scale, low-voltage PV-to-ESS, intended to assist the supply of local off-grid loads. The literature on solar-fed low-voltage battery chargers can broadly be split into three research branches.

Multi-input and/or multi-output Battery Chargers

Some works consider the power converter as a black box, and focuses on the design of innovative battery charge controllers to interface multiple ports or to optimally split the power flows from / to the battery to the local loads. Systems with different

source-load combinations were proposed, such as dual-input grid and PV module [149], 3-outputs hybrid controller [150], a reconfigurable 2 input PV-modules [151]. Ad-hoc controllers are designed in all the systems for an automatic and effective management of the power flows among the various sources and loads.

Innovative Embedded MPPT and Charge Controllers

In this research branch, innovative charge controllers specifically designed for the PV input are reported. In [152], the controller automatically switches between the bulk charging mode, where the maximum available power is delivered from the PV module to the battery, and the float charging mode, where a constant voltage is applied to the battery. In [153], where the controller maintains a low and fixed conversion ratio using the PWM, to maximize the conversion efficiency at the expense of working outside the MPP. In both cases, conventional buck converters are used, since the focus is not the optimization of the power conversion stage.

Innovative Power Converter Topologies for PV-to-ESS Applications

This last research branch includes innovative power converter topologies to be used as PV-fed battery chargers: as such, more attention is given on the hardware design rather than on the control algorithm. The main research question related to these works is to design power converters characterized by high efficiency on a reasonable input voltage range and power range, compliant with the PV source and battery load.

The charger in [154] is based on a PWM Single Ended Primary Inductor Converter (SEPIC), featuring buck-boost capability that allows to extend the available voltage range, but no indication on the conversion efficiency is provided. A SEPIC is also used in [155], where a hybrid dual-input PV-wind system is proposed as battery charger. The absence of soft switching limits the maximum switching frequency to 40 kHz and 50 kHz, respectively.

In [156], a buck-derived quasi-resonant converter is proposed, in which the resonance with an auxiliary capacitor allows to achieve the ZVS of the main MOSFET. A dual buck-derived case is proposed in [157], where a resonant inductor in series with the main switch allows to achieve its ZCS turn-OFF. Both topologies feature the soft commutation of the main transistors and a low component count, however

the resonant voltage pulses force to select higher voltage-rating devices, partially deteriorating the conduction losses. The measured peak conversion efficiency are below 89% and 85%, respectively.

Higher measured efficiencies and improved power density, thanks to the soft switching of the semiconductor devices, can be obtained with resonant topologies, such as the parallel-load resonant converter in [158] and the series-parallel resonant converter in [159]. Both solutions feature the desirable feature of a strongly non-linear static characteristic, allowing to achieve a wide variation of operating powers in a restricted frequency range. However, resonant converter are typically optimized to work at a constant frequency (slightly above the resonance frequency), requiring an additional conversion stage [158] or exhibiting deteriorated efficiencies at other working points [159]. The soft-switching benefits of a resonant converter are coupled with the voltage step-down capability of switched-capacitor networks in [160]. The generalized multi-stage topology achieves a high and flat conversion efficiency (between 93.3% and 95.3% in the wide $10\,\mathrm{W} - 100\,\mathrm{W}$ range) thanks to the ZCS of the switches, at the expenses of a large number of components and of a fixed voltage conversion ratio.

Considering the above-mentioned works, it is possible to identify three main approaches for the PV-to-ESS power conversion, associated to specific advantages and limitations: PWM hard-switched converters, quasi-resonant converters, resonant converters. Tab. 3.3 summarizes the main features of each category.

Compared to the PV-to-grid application, the literature review of PV-fed battery chargers revealed a limited attention, underlined by the low number of papers, especially in the most recent years. Given the relevance and the practical implications of PV-fed off-grid charging applications, this work investigates a new power converter topology trying to combine the benefits of the three presented converter categories, contributing to preserve the focus on this research branch. Chapter 6 describes the conceptualization and operating principle of the proposed topology, supported by experimental results on a PCB prototype.

Table 3.3 Qualitative comparison of the state-of-the-art PV-fed battery chargers.

Converters cluster	Main advantages	Main limitations
Hard-switched PWM	Low component count Simple control on wide range	Limited switching frequency (lower power density) Hard-switching (low efficiency) Bulky passive components
Quasi-resonant PWM	Soft switching Simple control on wide range	Required auxiliary components for soft switching Increased voltage stresses and / or current stresses
Resonant converters	Soft switching Improved power density	Optimized for a limited range of operating points Limited / fixed voltage gain Increased component count Non-linear and load-dependent static characteristic

3.4 Conclusions

A structured review of high step-up DC-DC converters was presented in the first part of this chapter, in the form of a classification based on the main voltage step-up technique employed in PV-fed MLPCs. The objective of the review was to extract qualitative considerations regarding the different techniques, identifying in a critical way advantages and drawbacks, and suggesting potential opportunities of improvement in the context of grid-tied MLPCs. Chapter 4 will begin from this analysis to conceptualize a new wide-range power converter topology aiming at addressing some of the limitations identified in the state of the art. A more quantitative simulation-based comparison will be presented at the beginning of the chapter to justify the adoption of the topology proposed in this thesis: as it will be detailed, the new converter topology is based on the integration of the multi-mode approach to an IPOS architecture.

A second part of this chapter introduced the common methodologies employed to assess the reliability of a power converter, as this topic is often neglected in the design phase of PECs. The objective of this part was to provide the necessary background to the reader to better understand the design optimization methodology proposed in Chapter 5.

The final part of this chapter was devoted to present a review of the state of the art of step-down power converters for off-grid PV-fed battery charging applications. Based on the critical analysis of the state of the art, Chapter 6 will introduce a new converter topology derived from a non-isolated half-bridge DC-DC converter, which employs a relatively small inductance to achieve the soft-switching of the converter transistors.

Chapter 4

Proposed Multi-Mode Partial Power Processing Optimizer

This chapter introduces the derivation, mathematical analysis, design and experimental characterization of a new high step-up power converter, capable of operating efficiently over a wide range of input voltages and powers, thanks to its multi-mode operating principle, thus addressing the challenges of PEC for PV applications.

Section 4.1 describes the conceptual flow to derive the new proposed topology, starting from simulation-based quantitative comparisons of different topologies. A thorough mathematical description of the converter operation in its three modes is provided in Section 4.2. The design of the converter, based on the specifications of a real PV module and guided by the analysis of the electrical stresses of every component, is presented in Section 4.3. The derivation of the static voltage gain and the description of the control architecture are detailed in Section 4.4. Section 4.5 presents the schematic and layout design of a 700 W prototype, the implementation of the firmware in a STM32 microcontroller, and the experimental results obtained on the prototype, including the main representative voltage and current waveforms in its operating modes, the efficiency profile on the designed power and input voltage range, and the comparison of the results with other exemplary converters of the state of the art. Finally, the conclusions and suggestions of future work are presented in Section 4.6.

4.1 Specifications and topology definition

4.1.1 Preliminary analysis on two-stage partial-power processing architectures

The review of the existing literature of PV-fed high step-up converters presented in Chapter 3 allowed to highlight the high performance and the wide-range capability of resonant converters, such as LLC or SRC, integrated in multi-mode and/or multi-stage topologies, as attested by many academic papers. In this section, the conceptual flow toward the definition of the proposed topology is strengthened even more by presenting the simulation results obtained on multiple two-stage architectures, to motivate the final selection of an asymmetric IPOS converter equipped with a topology-morphing rectifier. From a methodological standpoint, the approach followed in this section includes the following steps: each converter architecture is first introduced in terms of its system-level features and potential limitations, and a preliminary design is developed based on realistic PV module specifications. Subsequently, simulation results for the considered topologies are presented and discussed to justify the final topology selection.

The target specifications for this preliminary analysis are reported in Tab. 4.1, compliant with a 380 W monocrystalline Silicon commercial PV module, LG380N1C-E6[1]. The target voltage range is consistent with the widest operating ranges highlighted in the literature review and complies with the effect of severe PSC on the location of the MPP voltage, as discussed in Chapter 2.

Table 4.1 Target specifications for the comparison of two-stage architectures, based on the specifications of the PV module.

Design specification	Value
Rated input voltage $V_{\text{in,rated}}$	35.1 V
Minimum input voltage $V_{\text{in,min}}$	15 V
Maximum input voltage $V_{\text{in,max}}$	45 V
Rated power P_{rated}	380 W
Output voltage V_{out}	400 V

[1]Datasheet available at: https://solarwiseww.com.au/wp-content/uploads/2021/06/PDFLG-NeON-H-380-385W-N1C-E6-Datasheet.pdf.

As previously mentioned, a popular solution to mitigate the efficiency degradation of resonant converters operating outside resonance is to equip them with an additional auxiliary stage responsible for the gain modulation: in this way, the LLC or SRC can be optimized to work as DCX, at resonance, with the highest possible efficiency, while providing the dominant share of the required voltage gain. The most natural and intuitive way to do that is to exploit a full-power processing (FPP) cascaded architecture, shown in Fig. 4.1a, in which a front-end non-isolated stage provides the voltage gain $G_1 = \frac{V_1}{V_{in}}$, while a following resonant and isolated stage provides the voltage gain $G_2 = \frac{V_{out}}{V_1}$. A 2-level conventional boost converter is selected as the front-end stage due to its simple topology, low component count and reduced input current ripple, while a LLC converter working as DCX is chosen for G_2. The resulting topology was proposed for the PPO in [124]. In a cascaded architecture, both the conversion stages process the full power harvested from the PV panel, and the total conversion gain is obtained as the product of the individual gains:

$$G_{TOT} = \frac{V_{out}}{V_{in}} = \frac{V_{out}}{V_1}\frac{V_1}{V_{in}} = G_2 G_1 \,. \tag{4.1}$$

If G_2 is designed to be fixed, the required gain G_1 to track the MPP voltage on a desired MPPT range is obtained as:

$$G_1 = \frac{G_{TOT}}{G_2} \,. \tag{4.2}$$

One of the main benefits of this architecture is the overall galvanic isolation if at least one of the two stages is isolated; moreover, there is no restriction on the topology selection for the two stages, differently from PPP architectures. On the other hand, one of the most common and widespread limitations of cascaded architectures is the fact that, since both stages process the entire input power, the less efficient stage represents a bottleneck for the complete converter efficiency. Indeed, the overall converter efficiency η_{TOT} is calculated as the product of the efficiencies of the two stages η_1 and η_2, and is therefore lower than both η_1 and η_2:

$$\eta_{TOT} = \frac{V_{out}I_{out}}{V_{in}I_{in}} = \frac{\eta_2 V_1 I_1}{V_{in}I_{in}} = \frac{\eta_2\eta_1 V_{in}I_{in}}{V_{in}I_{in}} = \eta_1\eta_2 \,. \tag{4.3}$$

To overcome the inherent limitations of efficiency of the FPP approach, and at the same time to reduce the voltage gain requirements of the two stages, a potential

improvement consists in shifting towards a PPP topology. A first alternative architecture, denoted from now on as PPP-I, is obtained from the FPP version by creating a direct power path (DPP) between the input port and output port, characterized by an ideal 100 % efficiency [98], as shown in Fig. 4.1b. In this case, the galvanic isolation of at least one of the two stages is crucial to avoid short-circuits at the input port. The total gain expression for this architecture is easily obtained:

$$G_{\mathrm{TOT}} = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{V_3 + V_{\mathrm{in}}}{V_{\mathrm{in}}} = \frac{G_1 G_2 V_{\mathrm{in}} + V_{\mathrm{in}}}{V_{\mathrm{in}}} = 1 + G_1 G_2 \,, \tag{4.4}$$

from which the required gain G_1 follows:

$$G_1 = \frac{G_{\mathrm{TOT}} - 1}{G_2} \,. \tag{4.5}$$

Compared to the FPP case, for the same fixed G_2, the boost gain is slightly reduced. Assuming the two stages work with efficiency η_1 and η_2, respectively, the theoretical complete efficiency can be computed with a system-level analysis, as done for the FPP architecture:

$$V_3 I_{\mathrm{out}} = \eta_2 V_2 I_2 = \eta_1 \eta_2 I_1 V_{\mathrm{in}} \longrightarrow I_1 = \frac{G_1 G_2}{\eta_1 \eta_2} I_{\mathrm{out}} \tag{4.6}$$

from which:

$$\eta_{\mathrm{TOT}} = \frac{V_{\mathrm{out}} I_{\mathrm{out}}}{V_{\mathrm{in}} I_{\mathrm{in}}} = G_{\mathrm{TOT}} \frac{I_{\mathrm{out}}}{I_1 + I_{\mathrm{out}}} = \frac{1 + G_1 G_2}{1 + \frac{G_1 G_2}{\eta_1 \eta_2}} = \eta_1 \eta_2 \frac{1 + G_1 G_2}{\eta_1 \eta_2 + G_1 G_2} \,. \tag{4.7}$$

Since $\eta_1 \eta_2 < 1$, $\eta_{\mathrm{TOT}} > \eta_1 \eta_2$: the PPP-I overall efficiency, thanks to the DPP, is intrinsically larger than the FPP one. Another distinctive advantage is the reduction of all the current stresses in the two stages, as the total input current is split at the input port. An amount of power equal to $V_{\mathrm{in}} I_{\mathrm{out}}$ is transferred through the DPP, while the cascaded topology consisting of the boost and LLC converters processes the following share of input power:

$$\frac{\text{Power processed}}{\text{Total power}} = \frac{V_3 I_{\mathrm{out}}}{(V_3 + V_{\mathrm{in}}) I_{\mathrm{out}}} = \frac{G_1 G_2}{1 + G_1 G_2} \,. \tag{4.8}$$

As expressed in (4.8), the benefits of the reduced fraction of processed power are boosted at low total gain conditions, but are weakened at low input voltages, when $G_1 G_2$ is maximized.

At high step-up applications such as PPOs, the latter condition prevents the full exploitation of the potential benefits offered by the PPP. To overcome this limitation, an alternative hybrid PPP topology can be defined, in which a full-power front-end stage is followed by a second PPP IPOS stage, with a DPP established between the DC-link port and the output port, as proposed in [101]. The resulting topology, denoted from now on as PPP-II, is shown in Fig. 4.1c. Differently from PPP-I, in this modified version the DPP is applied only at the second stage and not at the entire converter. The front-end boost stage is designed to regulate V_1 to a constant voltage, that is further boosted by the second PPP stage. As intuitive, this hybrid architecture will exhibit intermediate characteristics between the FPP and PPP-I topologies. The expression of the total gain is:

$$G_{\mathrm{TOT}} = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{V_3 + V_1}{V_{\mathrm{in}}} = (1+G_2)\frac{V_1}{V_{\mathrm{in}}} = G_1(1+G_2)\,, \tag{4.9}$$

from which the variable boost gain follows:

$$G_1 = \frac{G_{\mathrm{TOT}}}{1+G_2}\,. \tag{4.10}$$

To derive the theoretical total efficiency, an intermediate step is required:

$$V_3 I_{\mathrm{out}} = \eta_2 V_1 I_2 \longrightarrow I_2 = \frac{1}{\eta_2}\frac{V_3}{V_1} I_{\mathrm{out}} = \frac{G_2}{\eta_2} I_{\mathrm{out}}\,, \tag{4.11}$$

from which:

$$I_1 = I_2 + I_{\mathrm{out}} = \left(1 + \frac{G_2}{\eta_2}\right) I_{\mathrm{out}}\,. \tag{4.12}$$

The total converter efficiency becomes:

$$\eta_{\mathrm{TOT}} = \frac{V_{\mathrm{out}} I_{\mathrm{out}}}{V_{\mathrm{in}} I_{\mathrm{in}}} = \frac{V_{\mathrm{out}} I_{\mathrm{out}}}{V_1 I_1}\frac{V_1 I_1}{V_{\mathrm{in}} I_{\mathrm{in}}} = (1+G_2)\,\frac{1}{1+\frac{G_2}{\eta_2}} \cdot \eta_1 = \eta_1 \eta_2 \frac{1+G_2}{\eta_2 + G_2}\,. \tag{4.13}$$

Since $\eta_2 < 1$, $\eta_{TOT} > \eta_1\eta_2$, resulting in an improved theoretical efficiency compared to the FPP converter thanks to the DPP. Differently from the boost, the DCX-LLC processed a fraction of the total power that depends on the selection of the fixed gain G_2:

$$\frac{\text{Power processed (LLC)}}{\text{Total power}} = \frac{V_3 I_{out}}{(V_1+V_3)I_{out}} = \frac{G_2 V_1}{(1+G_2)V_2} = \frac{G_2}{1+G_2}. \tag{4.14}$$

While a low G_2 enhances the benefits of the DPP, on the other hand it increases the gain requirements of the boost: an optimal trade-off should take into account the electrical stresses of both the boost and LLC.

The main fundamental limitation of PPP-II, shared with the FPP topology, is the fact that the boost converter needs to be designed to process the rated PV power, representing a potential efficiency bottleneck. To overcome this limitation, while maintaining the reduced electrical stresses of the PPP, an asymmetric IPOS architecture is considered at last. The resulting topology is shown in Fig. 4.1d and will be simply denoted as IPOS. Compared to PPP-I and PPP-II, no DPP is implemented here. The resonant converter is designed to process the largest fraction of input power, whereas the boost is supposed to modulate the gain with minimal processed power. An LLC or another galvanically isolated topology is required by construction for the IPOS architecture [161]. The total gain of the converter is:

$$G_{TOT} = \frac{V_{out}}{V_{in}} = \frac{G_1 V_{in} + G_2 V_{in}}{V_{in}} = G_1 + G_2, \tag{4.15}$$

from which the required boost gain follows:

$$G_1 = G_{TOT} - G_2. \tag{4.16}$$

It is evident that, being the converter gain obtained as a sum, and not as a product, of the stages gains, increased G_1 and G_2 will be necessary for the same high step-up requirements. Moreover, for a fixed G_2, there is a linear relationship between G_{TOT} and G_1, meaning that a wide target gain range reflects in equally wide boost gain requirements. At first sight, these two considerations together would suggest that the overall performance of this architecture would be strongly undermined: however,

it is important to highlight that none of the two conversion stages processes the entire input power, resulting in reduced electrical stresses on all the components and an improved theoretical efficiency. From the definitions of the individual stage efficiencies in (4.17) and (4.18), the overall converter efficiency can be expressed as in (4.19).

$$\eta_1 = \frac{V_3 I_{\text{out}}}{V_{\text{in}} I_1} \longrightarrow I_1 = \frac{G_1}{\eta_1} I_{\text{out}} \tag{4.17}$$

$$\eta_2 = \frac{V_4 I_{\text{out}}}{V_{\text{in}} I_2} \longrightarrow I_2 = \frac{G_2}{\eta_2} I_{\text{out}} \tag{4.18}$$

$$\eta_{\text{TOT}} = \frac{V_{\text{out}} I_{\text{out}}}{V_{\text{in}} I_{\text{in}}} = (G_1 + G_2) \frac{I_{\text{out}}}{I_1 + I_2} = \frac{G_1 + G_2}{\frac{G_1}{\eta_1} + \frac{G_2}{\eta_2}} = \eta_1 \eta_2 \frac{G_1 + G_2}{\eta_2 G_1 + \eta_1 G_2} \,. \tag{4.19}$$

Once again, being $\eta_1 < 1$ and $\eta_2 < 1$, the overall efficiency is enhanced compared to the FPP architecture, assuming the same η_1 and η_2. The fraction of power processed by the i-th stage, where $i \in [\text{boost}, \text{LLC}]$, is directly related to the stage gain G_i:

$$\frac{\text{Power processed}_i}{\text{Total power}} = \frac{G_i V_{\text{in}} I_{\text{out}}}{V_{\text{out}} I_{\text{out}}} = \frac{G_i}{G_{\text{TOT}}} \,. \tag{4.20}$$

Following the system-level analysis presented so far, four different converters were preliminarily designed on the basis of the specifications in Tab. 4.1, and employing a conventional boost and a LLC converter to realize the gains G_1 and G_2, respectively. Their schematics are shown in Fig. 4.2a and Fig. 4.2b, respectively. More in details, the LLC includes a resonant LC tank at the primary side of the transformer, and a VDR, to halve the required turns ratio n of the transformer. As it is operated as a DCX, its gain is constant and depending only on n:

$$G_2 = 2n \,. \tag{4.21}$$

The general guiding principle for all the converters, as anticipated, was to minimize the boost gain on the target voltage range, which translates into a design equation for n:

$$G_1(V_{\text{in}} = V_{\text{in,max}}, G_2 = 2n) = 1 \,. \tag{4.22}$$

According to the specific architecture (FPP, PPP-I, PPP-II, IPOS), different values of n may be obtained and should be rounded to attainable numbers of turns.

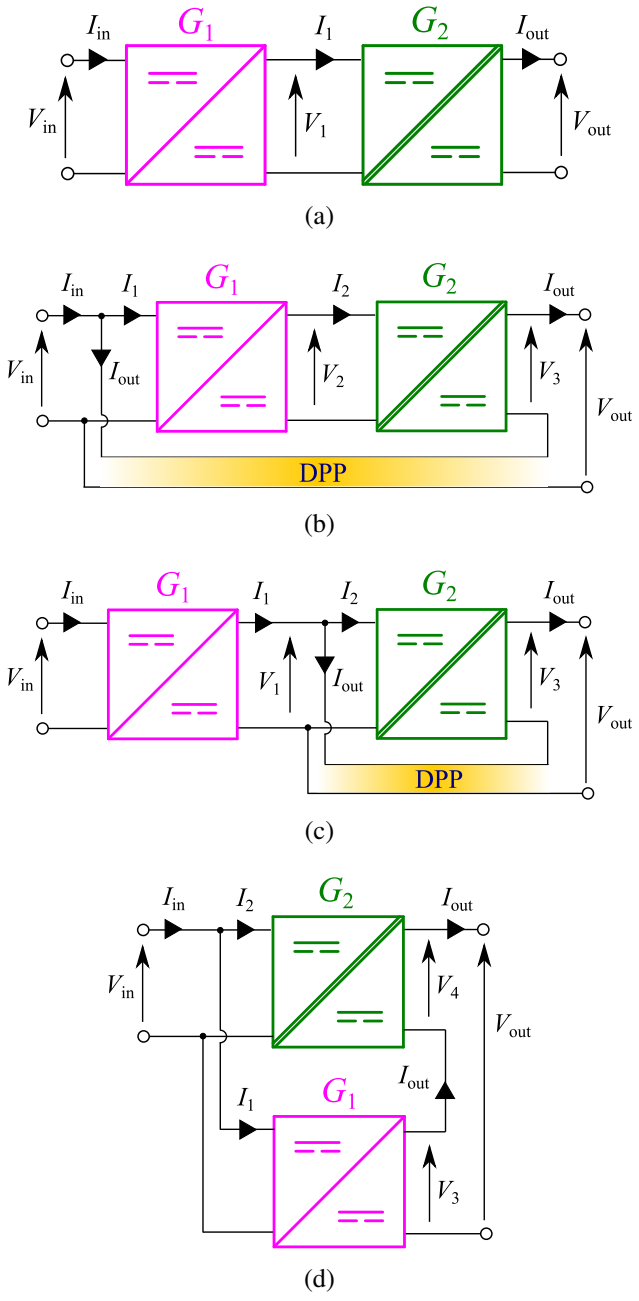


Fig. 4.1 Schematics of the 2-stage architectures considered in this analysis. (a) Cascaded full-power processing (FPP) architecture; (b) Conventional partial-power processing architecture (PPP-I), with direct power path (DPP) between input and output port; (c) Modified partial-power processing architecture (PPP-II), with DPP between intermediate port and output port; (d) Input-Parallel-Output-Series architecture (IPOS).

From (4.22), $n = 2$ was selected for the FPP, PPP-I and PPP-II converters, whereas the IPOS was designed with $n = 4$, given the higher required voltage gain of the

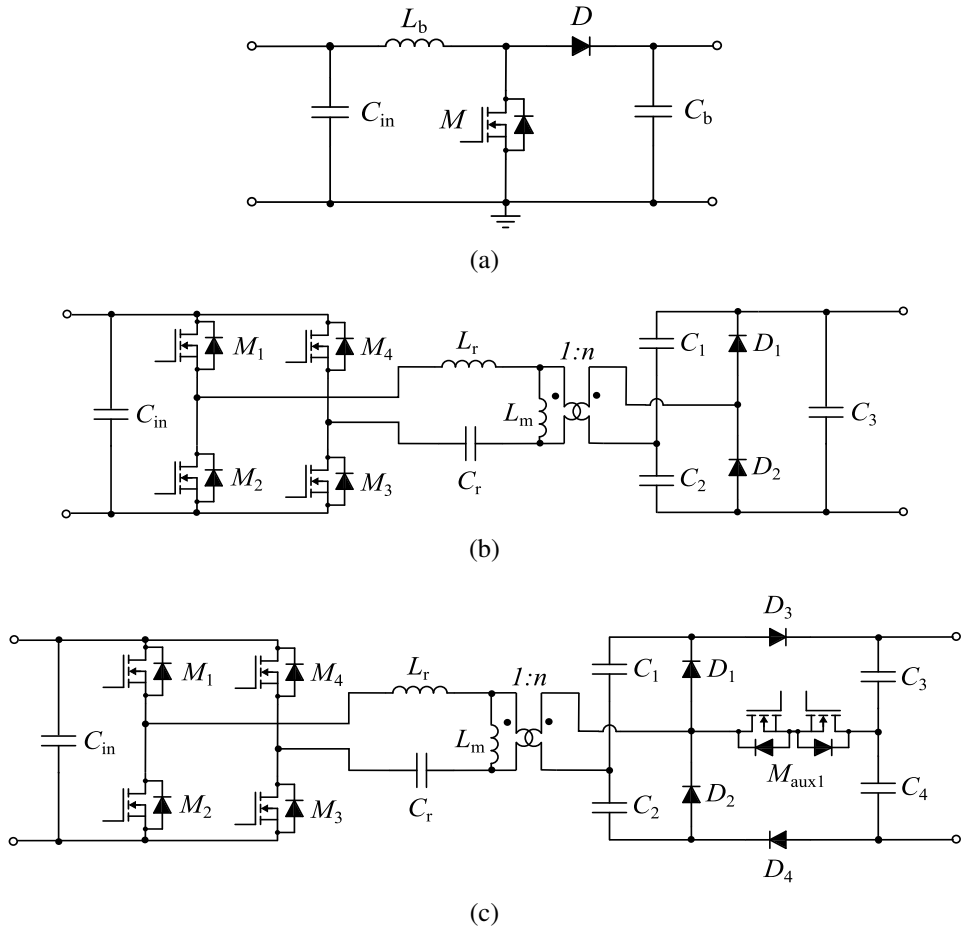


Fig. 4.2 Schematics of the topologies used for the comparison of the two-stage architectures. (a) Conventional boost; (b) LLC with VDR; (c) LLC with topology-morphing rectifier (VDR–VQR).

LLC. For the IPOS architecture, according to (4.16), assuming $G_2 = 8$, the required boost gain at the minimum input voltage would be:

$$G_1(V_{in} = 15\,\mathrm{V}) \approx 18.7\,. \tag{4.23}$$

A conventional boost converter would hardly be capable of realizing such a high gain, which would result in extremely high duty cycles. In addition, according to (4.20), at the voltage $V_{in} = 15\,\mathrm{V}$ the power processed by the boost would be 70 % of the total input power, undermining the potential for efficiency improvements resulting from the unbalanced power splitting.

Table 4.2 Comparison of the different analyzed two-stage architectures according to some relevant system-level specifications and design parameters.

Specification / parameter	FPP	PPP-I	PPP-II	IPOS
Transformer turns ratio n	Low (2)	Low (2)	Low (2)	High (4)
LLC gain G_2	Low (4)	Low (4)	Low (4)	High (8/16)
Boost gain G_1 range	Limited (2.2–6.7)	Limited (2.0–6.4)	Limited (1.8–5.3)	Wide (1.0–11.1)
Total gain expression	$G_1 \cdot G_2$	$1 + G_1 \cdot G_2$	$G_1 \cdot (1 + G_2)$	$G_1 + G_2$
Max voltage stress on boost devices	Medium (100 V)	Medium (90 V)	Medium (80 V)	High (210 V)
Max voltage stress on LLC full-bridge devices	Medium (100 V)	Medium (90 V)	Medium (80 V)	Low (45 V)
Fraction of power processed by boost / LLC at $V_{in} = 35.7$ V	100 % / 100 %	91 % / 91 %	100 % / 80 %	28.6 % / 71.4 %
Fraction of power processed by boost / LLC at $V_{in} = 15$ V	100 % / 100 %	96.2 % / 96.2 %	100 % / 80 %	40 % / 60 %

To overcome this limitation, only for the IPOS converter, the LLC was equipped with a topology-morphing rectifier, with the possibility to either implement a duplication or a quadruplication of the voltage at the secondary side of the transformer. This modified LLC is illustrated in Fig. 4.2c. Extensive details on the design and operation of the rectifier will be provided further in this work: for the purpose of this preliminary analysis, it is sufficient to consider that the LLC can realize two discrete gain values, namely $2n$ and $4n$, to reduce the boost gain requirements on the entire input voltage range.

Tab. 4.2 summarizes the main system-level design parameters and gain requirement, the main voltage stresses for the selection of the power semiconductor devices, and the fractions of processed power by each stage. It is evident that the IPOS architecture will present significantly reduced current stresses in the boost, thanks to the low fraction of processed power, at the expense of more challenging gain requirements.

The four converters were simulated in PSIM environment. To take into account the losses in the semiconductor devices, Spice models for the power MOSFETs and power diodes were selected for each architecture from the STMicroelectronics catalog based on their maximum voltage stresses. The boost converters were designed to operate in Continuous-Conduction Mode (CCM) at fixed 50 kHz frequency, whereas the resonant tanks of the LLC were designed to set the resonant frequency at 100 kHz. The losses for the capacitors and magnetic components were modelled with constant series resistances. It is evident that, for a systematic comparison, every topology

should be optimized in terms of components selection and critical design parameters: however, this optimization is out of the scope of this preliminary analysis, whose goal was to validate the qualitative considerations of this section and underline the promising potential of the asymmetric IPOS architecture.

The simulations of the four alternative solutions were performed in three representative working points:

- rated input voltage and power, $V_{in} = 35.1\,V$, $P_{out} = 380\,W$, to evaluate the performance of the converters in the most frequent working voltage and full power;
- rated input voltage and 20 % power, $V_{in} = 35.1\,V$, $P_{out} = 76\,W$, to evaluate the performance of the converters at lighter loads, i.e., at reduced solar irradiances;
- minimum input voltage and corresponding PV power, $V_{in} = 15\,V$, $P_{out} = 168\,W$, to evaluate the performance of the converters at the boundary of the MPPT range, where the PV panel may work in presence of PSC.

Tab. 4.3 summarizes the efficiency results for each stage and the total converter efficiency, at the rated working point. If only the individual stages efficiencies are taken into account, the PPP-II architecture outperforms, thanks to the reduced boost gain and the reduced fraction of power processed by the LLC. In the IPOS architecture, both the stages exhibit lower efficiencies, due to the higher boost gain and LLC turns ratio. However, since both stages, and especially the boost converter, process a lower fraction of the input power, the total dissipation is overall attenuated: as a result, the IPOS solution results in the best converter efficiency.

Table 4.3 Comparison of simulated efficiencies and gains for the different analyzed two-stage architectures for the rated operating point: $V_{in} = 35.1\,V$, $P_{out} = 380\,W$.

Efficiency / gain	FPP	PPP-I	PPP-II	IPOS
η_1 (%)	96.0	96.4	97.0	94.0
G_1 (a.u.)	2.85	2.60	2.28	3.40
η_2 (%)	97.7	97.5	97.8	96.8
G_2 (a.u.)	4	4	4	8
η_{TOT} (%)	92.6	93.5	94.0	96.2

The results at low power operation are reported in Tab. 4.4. In this condition, the PPP-II performs as the best solution, both at the individual stage level and whole converter level.

Table 4.4 Comparison of simulated efficiencies and gains for the different analyzed two-stage architectures for the low-power operating point: $V_{in} = 35.1\,V$, $P_{out} = 76\,W$.

Efficiency / gain	FPP	PPP-I	PPP-II	IPOS
η_1 (%)	98.3	98.3	98.4	95.8
G_1 (a.u.)	2.85	2.60	2.28	3.40
η_2 (%)	96.5	97.0	97.1	90.7
G_2 (a.u.)	4	4	4	8
η_{TOT} (%)	94.7	95.6	96.0	93.1

At the minimum input voltage operation, the simulation results show, once again, the improved efficiency of the IPOS architecture, as reported in Tab. 4.5. As in the rated working point, the individual efficiencies are lower than in the PPP-II solution, due to the increased step-up gains, but the partial-power approach enhances the global converter efficiency. Notice that the IPOS architecture is the only converter whose global efficiency is located between the efficiency values of its individual stages, instead of being lower than either of them.

Table 4.5 Comparison of simulated efficiencies and gains for the different analyzed two-stage architectures for the low-voltage operating point: $V_{in} = 15\,V$, $P_{out} = 168\,W$.

Efficiency / gain	FPP	PPP-I	PPP-II	IPOS
η_1 (%)	90.2	90.0	92.7	89.2
G_1 (a.u.)	6.66	6.42	5.33	10.7
η_2 (%)	97.9	97.9	97.9	96.0
G_2 (a.u.)	4	4	4	16
η_{TOT} (%)	87.1	87.2	89.5	92.4

This preliminary analysis, which represented the basis for the investigation of the new converter topology proposed in this work, highlighted the strong influence of different topological connections of two stages on the performance of two-stage architectures. The IPOS solution turned out to be the most-promising topology to be further investigated, thanks to the beneficial asymmetric power splitting and the decoupling of the individual efficiencies on the overall performance. The next section presents the derivation of the complete converter topology, optimized for the final target specifications.

4.1.2 Optimization of the IPOS topology

The concept of asymmetric IPOS topology, resulting as a promising solution for wide-range PPO applications, was considered as the starting point for the development of a new converter topology integrating the PPP and the multi-mode approaches. The integration of the two approaches aims to ensure a high efficiency at the rated working point while mitigating the efficiency degradation over a wide gain range.

The design of the converter presented in this chapter, thus, mainly addresses the optimization of the conversion efficiency on a wide voltage range. Additional cost- and reliability-aware design criteria will be introduced in a further optimization of the proposed converter, presented in Chapter 5.

The schematic of the proposed converter topology is shown in Fig. 4.3, consisting of a synchronous boost converter and an SRC with topology-morphing rectifier, connected in the IPOS configuration. The main relevant differences compared to the preliminary topology, composed of a conventional 2-level boost and a LLC with primary resonance, are the following:

- the diode D of the boost converter was replaced by MOSFET M_{HS}, to improve the efficiency;
- in the topology-morphing rectifier, diodes D_3 and D_4 were as well replaced by MOSFETs M_{aux2} and M_{aux3}, respectively, for the same purpose;
- the resonant converter includes the resonant tank at the secondary side of the transformer: in this way, capacitors C_{r1} and C_{r2} (with $C_{\mathrm{r1}} = C_{\mathrm{r2}} = C_{\mathrm{r}}$) can be used simultaneously for both the resonant tank and the VDR, a popular solution to enhance the power density [90, 89]. Moreover, the current stresses at the secondary side of the transformer are significantly reduced compared to the primary side. Differently, from the conventional LLC topology with primary-side resonant tank, the SRC is not capable of realizing a voltage gain higher than the transformer turns ratio.

From the control point of view, the CCM operation of the boost will be replaced with the Boundary Conduction Mode (BCM), to achieve the ZVS of both transistors, and a specific additional operating mode will be introduced to track the MPP at the highest input voltages of the target MPPT range, which would be unfeasible

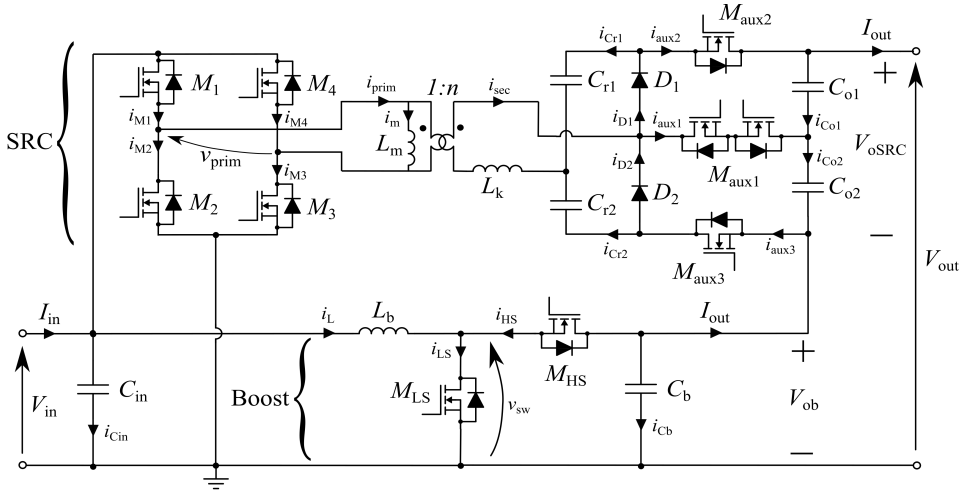


Fig. 4.3 Schematic of the proposed multimode IPOS converter.

otherwise. A deeper investigation on the voltage and current stresses will be presented to guide the components selection for this converter.

4.2 Multi-mode operation

In an IPOS converter, as explained, both conversion stages operate simultaneously to realize the required voltage gain. Since, in the proposed solution, different converters are considered for the two stages, there is no synchronization between them, and the operation of the two converters can be analyzed separately.

In this section, the converter operation will be detailed, highlighting the main features of the multi-mode approach that allows to cover a wide voltage range defined by the specifications. The analysis will be then applied to the design of a specific prototype once the PV panel specifications are detailed.

Since the two topologies, namely the SRC and synchronous boost, are widespread and well-known converters, their operation will be briefly recalled, while more attention will be devoted to the contribution of the topology-morphing rectifier.

4.2.1 Medium voltage mode (MV)

From the preliminary conceptual considerations, the main design principles behind the proposed solution are the following:

- the resonant operation of the SRC, to ensure that this stage always operates in its highest efficiency condition, with a fixed voltage gain, denoted by G_2;
- the minimization of the boost gain, to limit, as much as possible, the contribution of its losses on the overall architecture.

From the architecture point of view, the exploited concept is to assist an efficient and high power *main* stage represented, in this case, by the SRC, with a lower power and variable gain *auxiliary* stage, consisting of the boost. Similar considerations were exploited in [162, 126, 128, 127] in which, however, the input voltage range is limited by the auxiliary stage design.

At resonant operation, the SRC gain is fixed and depend uniquely on the transformer turns ratio. The SRC is designed to process the largest fraction of the total input power, to ensure that the majority of the PV energy is directed along this highest-efficiency path. This is especially desirable in the neighborhood of the most frequent working voltages of the PV panel. As will be clarified, it is possible to

derive a design equation for the transformer ratio to minimize the boost gain (and, thus, its processed power) in correspondence of a desired rated voltage. In this way, the voltage and power specifications of the auxiliary stage, responsible for the implementation of the MPPT, can be relaxed.

In the neighborhood of the rated input voltage, the SRC rectifier is designed to work as a VDR. As a consequence, the total SRC gain becomes $G_1 = 2n$, where n is the transformer turns ratio, and the boost gain must meet (4.16). From (4.16), it is possible to imply that there exists an input voltage, denoted by V_{th}^{+}, for which the required boost gain becomes unitary. A second implication is that the boost gain G_2 rises hyperbolically as the input voltage decreases.

At low voltages, to limit the extreme gain requirements of the boost, the rectifier morphs from VDR to VQR to provide an additional duplication of the SRC gain. The boundary voltage at which the topology-morphing of the rectifier is triggered will be from now on denoted as V_{th}^{-}. The topology morphing unlocks a new operating mode at low voltages, which will be described in Sec. 4.2.2. For voltages higher than V_{th}^{+}, on the other hand, where the required boost gain would be < 1 another operating mode must be identified in order to continue regulating the gain, as detailed in Section 4.2.3. For these reasons, the operating mode exploited in the input voltage range that includes V_{rated} is named *Medium Voltage* (MV) mode.

The resonant operation of SRC with secondary-side resonant tank was extensively described in many previous works, like [89] or [90]. To realize a constant gain independently from the load condition, the converter transistors must operate at the resonance frequency of the secondary tank:

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{(C_{\text{r1}} + C_{\text{r2}})L_{\text{k}}}} = \frac{1}{2\pi\sqrt{2C_{\text{r}}L_{\text{k}}}}, \tag{4.24}$$

where L_{k} is the leakage inductance of the transformer, which is exploited in the resonant tank without the need of external additional inductors.

The steady-state analysis of the converter waveforms is carried out under the following assumptions:

- the SRC transistors are ideal, except for their output parasitic capacitances, which are involved in the switching process;
- the diodes of the SRC rectifier are ideal;
- the filter capacitors of the rectifier, namely C_{o1-o2}, are assumed to be sufficiently large to maintain a stable voltages across them;
- the input filter capacitor is also assumed to be sufficiently large to maintain a stable input voltage.

The operation is based on two alternate phases associated to the conduction periods of $M_1 - M_3$, corresponding to the positive half of the sinusoidal current i_{sec}, and of $M_2 - M_4$, corresponding to the negative half of the sinusoidal current i_{sec}. All transistors conduct for slightly less than half a resonant period, and a small deadtime is introduced to avoid the cross-conduction of two transistors in the same bridge leg. The presence of a finite magnetizing inductance L_m of the transformer introduces a triangular circulating current at the primary side of the transformer, superimposed to the sinusoidal current shaped by the resonant tank. Since, ideally, the primary voltage v_{prim} is a pure AC square wave with amplitude V_{in}, the positive and negative slopes of the magnetizing current become $\pm\frac{V_{in}}{L_m}$. If the magnetizing inductance is properly designed, the peak positive and negative values of the magnetizing current allow to achieve the ZVS turn on of M_{1-4}, ensuring the correct discharge of the transistor output parasitic capacitances during the deadtimes.

To ensure that the rectifier of the SRC works as a VDR, the bipolar and bidirectional auxiliary MOSFET M_{aux1} must be kept off, while two two MOSFETs M_{aux2} and M_{aux3} must be on. As shown in Fig. 4.4a, the equivalent circuit of the rectifier collapses to the conventional VDR topology exploited, for instance, in [90]. The rectifier generates an output voltage V_{oSRC} obtained by doubling the peak value of the square-wave secondary voltage of the transformer. The output filter capacitors C_{o1} and C_{o2} are designed to be much larger than the resonant capacitors C_{r1} and C_{r2}. As such, they are not involved in the resonance and can be modelled as constant voltage generators during a resonant period. Figs. 4.4b and 4.4c show in a simplified way what devices conduct during each phase of the SRC operation. From the modelling point of view, it is equivalent to assume that the rectifier input is connected to a sinusoidal current generator. During the positive half of the sinusoid, diode D_1 is forward biased, while D_2 is off. During the negative half, the situation is opposite.

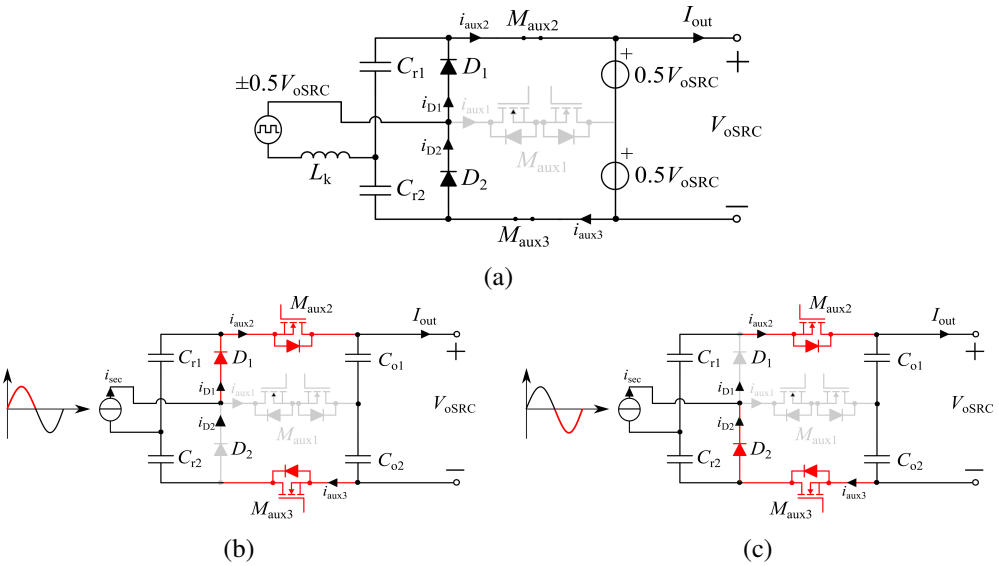


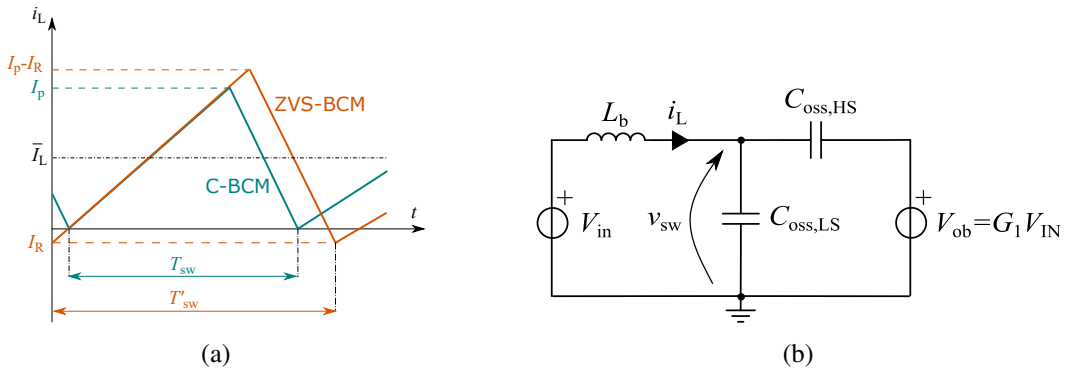
Fig. 4.4 Equivalent models of the VDR in the MV mode of the converter. (a) Equivalent circuit model of the VDR, highlighting the conduction state of the auxiliary MOSFETs; (b) Conducting devices during the positive half of the resonant current; (c) Conducting devices during the negative half of the resonant current.

It is important to observe that both M_{aux2} and M_{aux3} conduct a rectified sinusoidal current during the complete resonant period.

Differently from the preliminary analysis presented in Section 4.1, the synchronous boost converter is operated in a variable frequency BCM which, despite the larger ripple on the inductor current i_{L}, allows to reduce the current stresses and to achieve the soft switching of both transistors compared to the CCM. As well-known, the voltage gain of a boost in BCM can be modified by means of the duty cycle:

$$G_1 = \frac{1}{1-D}. \tag{4.25}$$

In a conventional BCM operation (C-BCM), also denoted as Transition Mode, the high-side MOSFET M_{HS} is controlled to be turned off when the triangular inductor current i_{L} falls to 0, as shown in Fig. 4.5a. The correct timing is ensured by a Zero Current Detector (ZCD) circuit. This condition allows to achieve the ZCS of M_{HS}, but may be ineffective to discharge the parasitic capacitance of M_{LS} during the deadtime [163, 164]. As a result, the remaining energy stored in its C_{oss} is dissipated during the turn on switching, causing additional losses in the MOSFET and increased EMI. To limit these issues, it is possible to extend the conduction time



(a) (b)

Fig. 4.5 Modelling of the BCM boost to achieve the ZVS turn ON of the low-side MOSFET. (a) Qualitative waveforms of the boost inductor current in the C-BCM and the modified ZVS-BCM. (b) Equivalent circuit of the boost during the dead time between M_{HS} turn OFF and M_{LS} turn ON.

of M_{HS} until the inductor current reaches a negative value $I_R \leq 0$, sufficient to assist the ZVS turn ON of M_{LS}: in this way, its switching losses are minimized. To stress the soft-switching benefits of this approach, this alternative BCM is here denoted as ZVS-BCM. The comparison of the inductor current waveforms in the C-BCM and ZVS-BCM is shown in Fig. 4.5a. Notice that this approach is only feasible with synchronous boost converters, since the high-side diode of a conventional boost would not be able to conduct a negative current. For the same average current $\bar{I}_L$ and input-output voltages, the ZVS-BCM determines an increased period T'_{sw} and increased RMS currents, but minimal turn on losses of M_{LS}.

Fig. 4.5b shows the equivalent circuit of the boost during the deadtime between the turn off of M_{HS} and the turn on of M_{LS}. This equivalent circuit is functional to derive analytically the minimum required I_R to achieve the ZVS condition. The following assumptions and initial conditions are made:

- the input and output voltages are constant during the deadtime. At steady state, $V_{ob} = G_1 V_{in}$;
- the off MOSFETs can be modelled temporarily by their parasitic capacitances $C_{oss,LS}$ and $C_{oss,HS}$, with $C_{oss,LS} = C_{oss,HS} = C_{oss,b}$. The strong non-linearity of C_{oss} can be disregarded if the charge-equivalent capacitances are considered;
- the initial inductor current is $i_L(0) = I_R$, which is the target unknown of the system;

- the initial switching node voltage is $v_{\mathrm{sw}}(0) = G_1 V_{\mathrm{in}}$.

During the deadtime $t_{\mathrm{dead,b}}$, the system can be modelled by a linear system of two Ordinary Differential Equations (ODE):

$$\begin{cases} v_{\mathrm{sw}} + L_{\mathrm{b}} \frac{di_{\mathrm{L}}}{dt} = V_{\mathrm{in}} \\ i_{\mathrm{L}} = 2C_{\mathrm{oss,b}} \frac{dv_{\mathrm{sw}}}{dt} \end{cases} \tag{4.26}$$

The system can be solved with the initial conditions mentioned above. Imposing that i_{L} falls to zero before the end of $t_{\mathrm{dead,b}}$ allows to determine the minimum I_{R} to completely discharge $C_{\mathrm{oss,LS}}$:

$$I_{\mathrm{R}} < -\frac{V_{\mathrm{in}}}{Z_0} \cdot \frac{1 + (G_1 - 1)\cos\left(\omega_0 t_{\mathrm{dead,b}}\right)}{\sin\left(\omega_0 t_{\mathrm{dead,b}}\right)}, \tag{4.27}$$

where $Z_0 = \sqrt{L_{\mathrm{b}}/2C_{\mathrm{oss,b}}}$ and $\omega_0 = 1/2\pi\sqrt{2C_{\mathrm{oss,b}}L_{\mathrm{b}}}$. As mentioned in [164], $I_{\mathrm{R}} = 0\,\mathrm{A}$ should already be sufficient to ensure the ZVS when the boost gain is higher than 2. In practical cases, however, since the turn-off of a device is not instantaneous, a minimum negative current may in any case be required for a complete ZVS. Since both G_1 and $C_{\mathrm{oss,b}}$ depend on the working input voltage V_{in}, the minimum I_{R} is a function of V_{in} for a specific selection of MOSFETs. Clearly, among all the possible negative I_{R}, the minimum value obtained by (4.27) is recommended to minimize the conduction losses.

The main relevant voltage and current waveforms for both the SRC and boost converters in the MV mode are illustrated in Fig. 4.6. The SRC waveforms are dominated by the resonant operation of the tank, allowing to achieve the ZCS of the rectifier diodes. A proper design of the magnetizing inductance of the transformer enables the ZVS turn-on of the input transistors as well. The sinusoidal voltage ripple generated by the resonance is superimposed on a $\frac{V_{\mathrm{oSRC}}}{2}$ offset for both resonant capacitors. The boost waveforms are shaped by the PWM control signals and highlights the quasi-resonant behaviour during the deadtime between the high-side and low-side conduction periods. The duration of the timing interval dt_{ext}, corresponding to the negative extension of the current i_{L}, will be detailed in Section 4.4. The SRC and boost waveforms, as explained, are not synchronous.

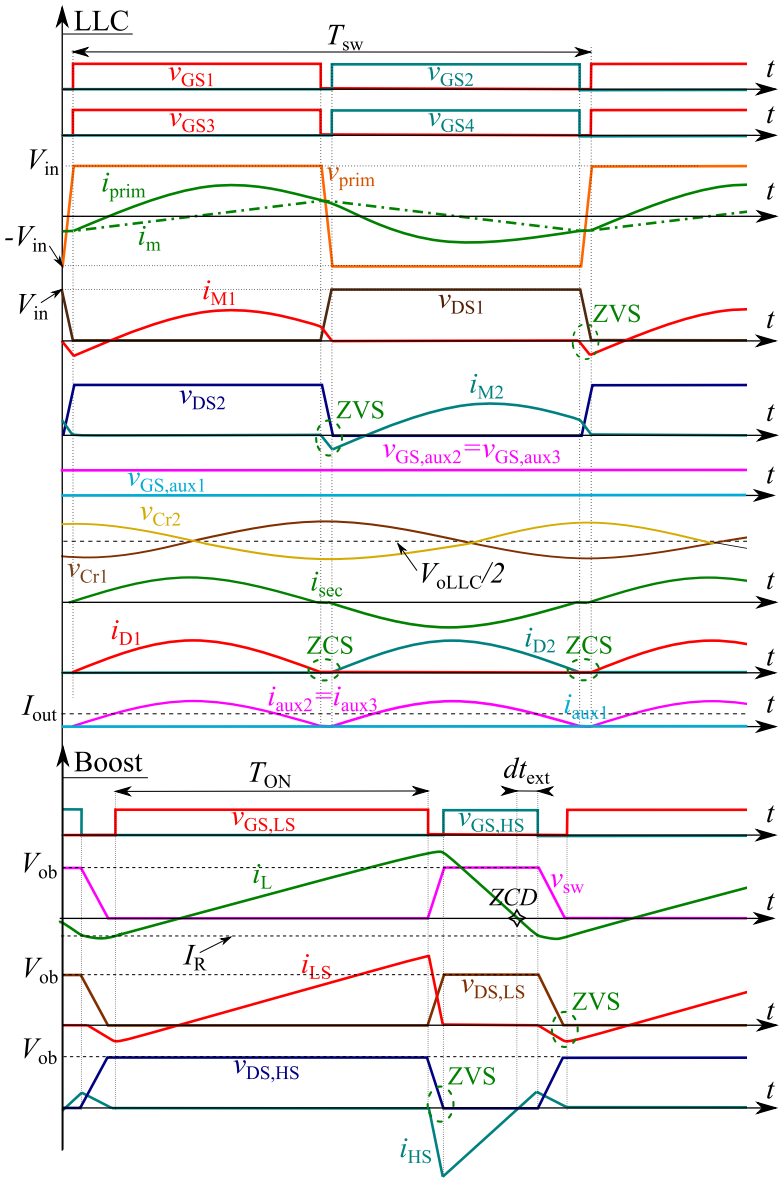


Fig. 4.6 Main current and voltage waveforms of the converter in the MV mode.

4.2.2 Low voltage mode (LV)

Morphing the SRC rectifier into a VQR, at the voltage V_{th}^{-}, introduces an additional duplication of the SRC gain, which significantly limits the boost gain requirements at low input voltage operation. In a boost controlled in BCM, indeed, all current and voltage stresses of its components increase with the voltage gain [163], as it will be pointed out in Section 4.3. Moreover, in absence of a technique to reduce the boost

gain, the larger peak currents and lower BCM frequency would more likely induce saturation in the boost inductor, and would tighten the filtering requirements of the DC filter capacitors.

In the LV mode, the SRC still operates as a DCX with fixed gain, $G_2 = 4n$, with the only difference of the quadruplication of the gain achieved by the rectifier. No significant difference compared to the MV mode can be highlighted in the operation of the full-bridge. Differently from the MV mode, the sinusoidal voltage ripple of the resonant capacitors is superimposed to a $\frac{V_{\text{oSRC}}}{4}$ offset. The derivation of the current and voltage stresses will be presented in Section 4.3.

The equivalent circuit of the SRC VQR is shown in Fig. 4.7a, which highlight the conduction states of the auxiliary MOSFETs: M_{aux1} is kept on, while M_{aux2} and M_{aux3} are kept off. Their body diodes are exploited to provide a conduction path for the pulsed resonant currents i_{aux2} and i_{aux3}. This configuration allows to realize a voltage gain factor equal to 4 between the output voltage V_{oSRC} and the amplitude of the square voltage at the secondary side of the transformer. As in the MV case, the output filter capacitors are assumed to behave as constant voltage generators during a resonant period. Figs. 4.7b and 4.7c show what devices of the rectifier conduct the current in each half of the resonant period. During the positive half of the sinusoidal i_{sec}, as shown in Fig. 4.7b, the conducting devices are the diode D_1, the auxiliary MOSFET M_{aux1} and the body diode of the auxiliary MOSFET M_{aux3}, which is in the interdiction state. During the negative half, as shown in Fig. 4.7c, the conducting devices are diode D_2, the auxiliary MOSFET M_{aux1} and the body diode of the auxiliary MOSFET M_{aux2}, which is kept off. More details on the operation of a VQR can be found in [165]. In a conventional VQR, diodes are normally adopted to replace M_{aux2} and M_{aux3}: however, this choice would cause significantly increased conduction losses when the rectifier is used as a VDR.

As far as the boost converter is concerned, there is no relevant difference in the operation within a switching period. The required boost gain is determined by (4.28), which is achieved by the ZVS-BCM operation, as in the MV case:

$$G_2 = G_{\text{TOT}} - 4n\,. \tag{4.28}$$

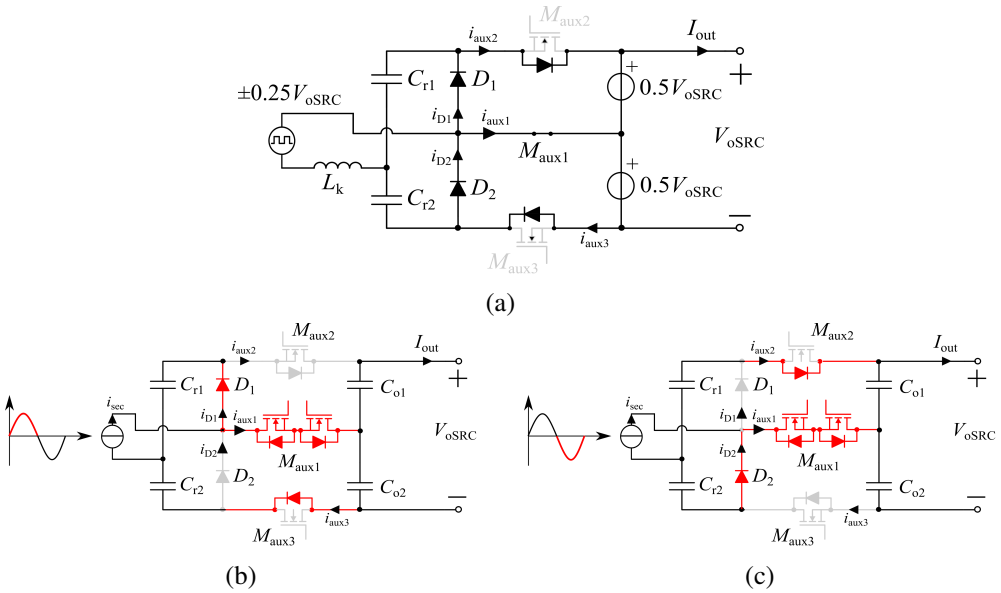


Fig. 4.7 Equivalent models of the VQR in the LV mode of the converter. (a) Equivalent circuit model of the VQR, highlighting the conduction state of the auxiliary MOSFETs; (b) Conducting devices during the positive half of the resonant current; (c) Conducting devices during the negative half of the resonant current.

The main relevant converter waveforms for both the SRC and boost are illustrated in Fig. 4.8. The ZVS of the full-bridge MOSFETs and the ZCS of the rectifier diodes are preserved. The quasi-resonant behaviour of the boost inductor current during the deadtime between the turn off of M_{HS} and the turn on of M_{LS} is highlighted.

4.2.3 High voltage mode (HV)

As described, V_{th}^{+} represents the voltage level in the MV mode at which the boost gain falls to 1. At low panel temperatures or partial shading conditions, however, the MPP voltage may be shifted above this level: in these cases, since the SRC provides a fixed gain, the gain regulation would be lost. For this reason, a third operating mode is introduced to extend the converter operation for $V_{\mathrm{in}} > V_{\mathrm{th}}^{+}$. V_{th}^{+} can be then considered the boundary between the MV and the HV modes. The inherent step-up characteristic of the boost converter prevents this stage from achieving $G_1 < 1$, thus the gain regulation should be performed by the SRC.

Well-known control approaches to regulate the gain of a SRC converter are the frequency modulation (FM) and phase-shift modulation (PSM), which uniquely

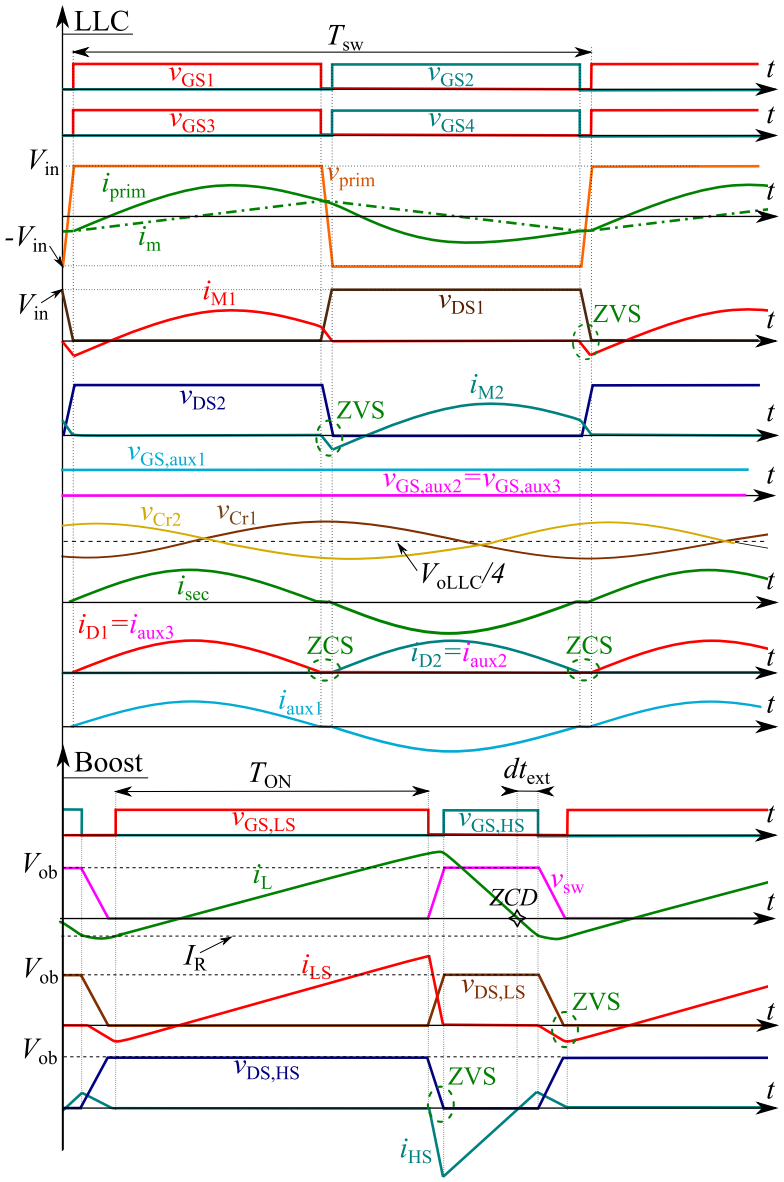


Fig. 4.8 Main current and voltage waveforms of the converter in the LV mode.

involve the control sequence of the converter devices and do not require additional auxiliary components [166]. The FM consists in operating the full-bridge transistors above the resonance frequency, in the so-called inductive mode [167]. Independently from the location of the resonant tank, at the primary or secondary side of the transformer, this approach results in a reduced voltage gain compared to the one obtained at the resonance frequency. The FM features the benefit of preserving the ZVS of the full-bridge transistors, while the ZCS of the secondary side diodes is lost.

On the other hand, the PSM consists in maintaining the transistors operation at the resonance frequency, but introducing a phase shift Φ between the conduction periods of the devices in the two legs of the full-bridge [168]. The overall effect is to obtain a reduced voltage gain compared to the case in which $\Phi = 0°$. The introduction of a phase shift implies a non-uniformity of the current stresses between the leading and lagging legs of the full-bridge, but the soft switching of the devices can still be preserved in most the operating range [168]. Clearly, both control strategies introduce higher order harmonics on the currents that increase the conduction losses and deteriorate the converter efficiency compared to the rated operation at the resonance frequency. In addition, the gain profile and electrical waveforms strongly depend on the resonant tank parameters and on the load condition. Between the two solutions, the PSM approach is selected in this case to limit the high-frequency losses in the transformer core and windings that may arise when the converter must work outside the rated MPP voltage.

The detailed derivation of the voltage and current waveforms for the PSM was extensively described in [90, 168, 89], and will not be replicated here. Fig. 4.9 shows the qualitative waveforms of the proposed converter. The phase shift Φ between the gate signals of the two legs increases the RMS currents in the SRC, thus larger conduction losses are expected in this operating mode compared to the MV mode, for the same transferred power.

In the HV mode, the synchronous boost can be simply turned off: the continuous output current I_{out} is conducted through the inductor L_{b} and the body diode of the high-side transistor, minimizing the boost losses. The proposed IPOS converter collapses into the conventional step-up PPP architecture, in which a fraction of the input power is transferred to the output port with theoretical 100 % efficiency [98]. The nearly ideal conversion efficiency of the boost in this case is expected to partially compensate for the efficiency drop in the SRC.

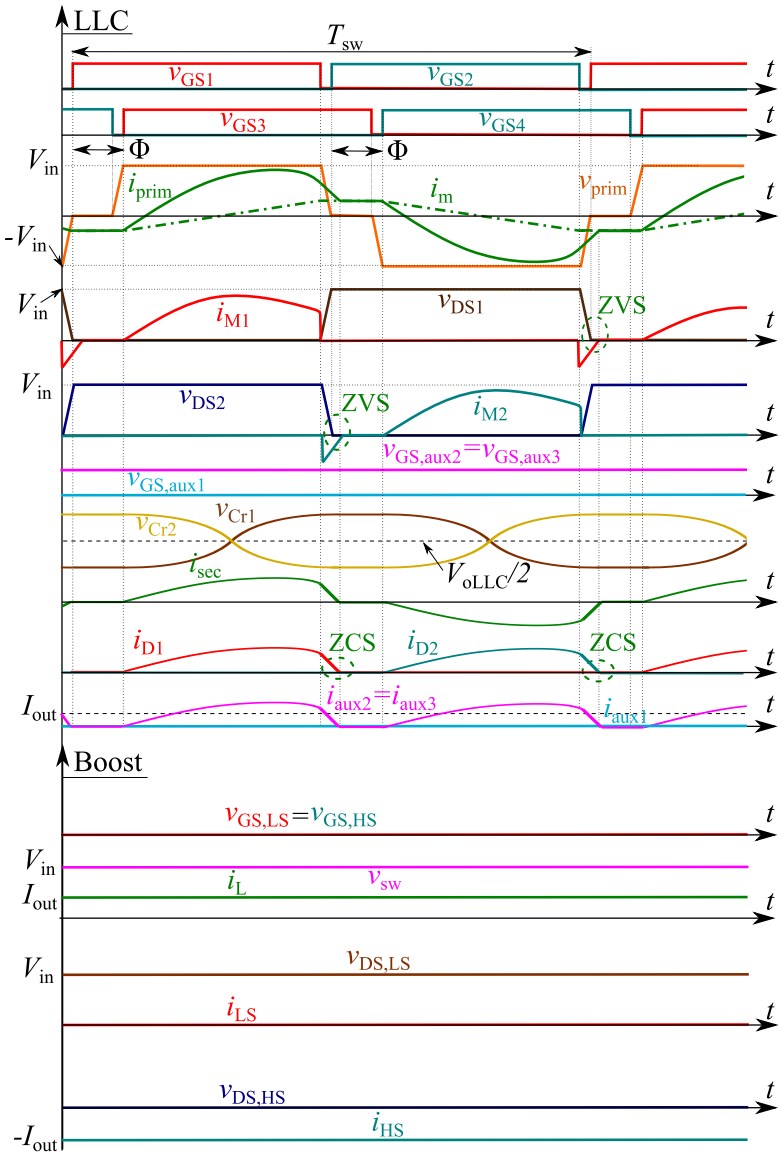


Fig. 4.9 Main current and voltage waveforms of the converter in the HV mode.

Table 4.6 Main specifications of the proposed converter.

Specification	Value
Rated input voltage V_{rated}	36.5 V
Rated power P_{rated}	700 W
Input voltage range $V_{\text{in,min}} - V_{\text{in,max}}$	15 V–45 V
Output voltage V_{out}	350 V

4.3 Converter design

In this section, the main electrical stresses and design equations for the converter components are introduced, to help a designer select suitable off-the-shelf components. The section is organized as follows: the SRC stage design, the boost stage design, and the schematic and layout design are described in Sections 4.3.1, 4.3.2 and 4.5.1, respectively.

The definitive specifications of this converter refer to the heterojunction bifacial PV module 3SUN-B60 3SHBGHAA-680W[2]. The main specifications of the converter are summarized in Tab. 4.6. Compared to the preliminary specifications considered in Section 4.1, the new target PV panel exhibits 700 W rated power. Moreover, the output voltage is reduced to 350 V, becoming the standard for residential DC microgrids [169].

At a system level, the main design parameter that strongly affects the electrical stresses on all the converter components is the turns ratio of the transformer, n, properly normalized to feasible numbers of turns. As anticipated, the turns ratio should be designed to minimize the boost gain G_1 in correspondence (or in the neighborhood, at least) of the target input voltage V_{rated}, located in the MV mode:

$$G_1(V_{\text{rated}}) = \frac{V_{\text{out}}}{V_{\text{rated}}} - 2n \stackrel{!}{=} 1 \Longrightarrow n = \frac{1}{2}\left(\frac{V_{\text{out}}}{V_{\text{MPP}}} - 1\right). \tag{4.29}$$

Using $V_{\text{rated}} = 36.5\,\text{V}$ and $V_{\text{out}} = 350\,\text{V}$, $n \approx 4.29 \longrightarrow n = 4$.

Once n is adjusted to comply to feasible numbers of turns, the input voltage V_{th}^{+} at which the boost gain is unitary (at the boundary between the MV and HV mode)

[2]Datasheet available at: https://www.enfsolar.com/pv/panel-datasheet/crystalline/61873.

becomes:

$$V_{\text{th}}^{+} = \frac{V_{\text{out}}}{2n+1}\,. \tag{4.30}$$

In the LV mode, when the SRC rectifier works as a quadrupler, it is possible to define another voltage at which the boost gain is reset to 1. This voltage can be assumed as the boundary between the LV and MV modes V_{th}^{-} and can be computed as:

$$V_{\text{th}}^{-} = \frac{V_{\text{out}}}{4n+1}\,. \tag{4.31}$$

In correspondence of both the voltages V_{th}^{+} and V_{th}^{-}, local efficiency peaks are expected, since the boost gain and processed power are minimized.

More in general, n determines the fraction of power processed and the required gain imposed on each converter stage, SRC or boost. Once n is set from (4.29), the voltage gains and electrical stresses can be determined for any input voltage and power level. Together with the input capacitor C_{in}, the turns ratio is the only design parameter involving simultaneously the two converter stages. As a result, the rest of the design can be carried out independently for the SRC and boost. Using (4.29)

Some common assumptions and definitions are recurrent in the following discussion and are clarified now:

- the worst-case electrical stresses of the components are derived at steady state operation: a conservative design should always consider an overhead to take into account transient overcurrents and overvoltages;
- the filter capacitors C_{in}, C_{b}, C_{o1} and C_{o2} are assumed to supply all the AC parts of the input and output currents, which can thus be treated as constant;
- the voltage ratings of the passive and active devices are based on the worst-case peak voltages across them, at steady state;
- the current stresses of the components, helpful for the estimation of the conduction losses, are expressed in terms of average and RMS currents on a switching period T_{sw}, following the conventional definitions of (4.32) and (4.33), respectively:

$$\bar{I} = \frac{1}{T_{\text{sw}}} \int_{0}^{T_{\text{sw}}} i(t)dt \tag{4.32}$$

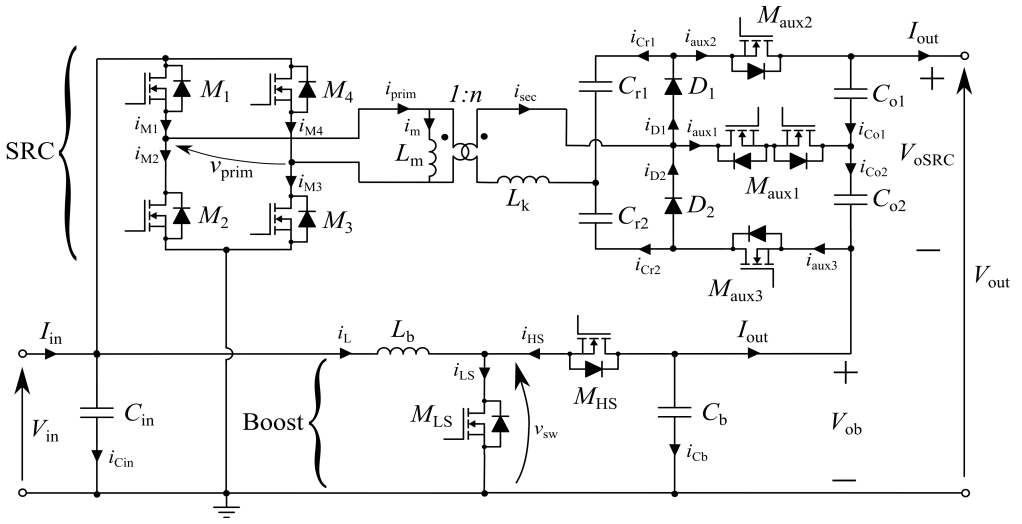


Fig. 4.10 Schematic of the proposed multimode IPOS converter.

$$I_{RMS} = \sqrt{\frac{1}{T_{sw}} \int_0^{T_{sw}} i^2(t)dt} \tag{4.33}$$

- the definitions of average and RMS currents are applied to the analytical current waveforms extracted from the analysis of the converter operation.

To assist the following discussion, the schematic of the converter topology is reported again in Fig. 4.10.

4.3.1 SRC design

The voltage and current waveforms of SRC converters operated at resonance is not a new topic and was previously discussed in many works, such as [90, 89, 124, 170]. Here, only the most relevant waveforms are recalled, with the specific goal of offering an intuitive comparison between the LV and MV modes. The possibility to express the current stresses of the components analytically in both the operating modes makes it easy to highlight eventual benefits or disadvantages. The operation in the HV mode, which is based on the PSM, does not offer the possibility to derive analytical expressions. In this case, a detailed overview of the electrical stresses should be based on preliminary simulations. On the other hand, since the converter is designed in such a way to set the MPP rated voltage in the MV mode, the worst-case current stresses are expected to be found in this mode.

The rectifier electrical stresses can be expressed in terms of the constant output current I_{out} and output voltage V_{oSRC}. The current stresses of the full-bridge MOSFETs will be derived in a later moment, by reflecting the resonant current at the primary side of the transformer. For the sake of compactness, two intervals of time are defined to identify the two halves of a switching period: T_1 identifies the conduction periods of M_1 and M_3, where $i_{\text{sec}} > 0$, while T_2 identifies the conduction periods of M_2 and M_4, where $i_{\text{sec}} < 0$.

When the rectifier works as a VDR, M_{aux1} is off and the currents i_{aux2} and i_{aux2} assume a rectified sinusoidal shape whose average value is I_{out}:

$$i_{\text{aux2}}(t) = i_{\text{aux3}}(t) = \frac{\pi}{2} I_{\text{out}} |\sin \omega_{\text{res}} t|. \tag{4.34}$$

From the assumptions of ideal output capacitors, their current stresses are pure AC currents derived from $i_{\text{aux2}} - I_{\text{out}}$. From the current balance equations applied at the other nodes of the rectifier, the currents through the resonant capacitors and diodes can be expressed analytically as in (4.35), respectively:

$$i_{D1}(t) = i_{D2}\left(t - \frac{T_{\text{sw}}}{2}\right) = \begin{cases} \pi I_{\text{out}} \sin \omega_{\text{res}} t, \ t \in T_1 \\ 0, \ t \in T_2 \end{cases} \tag{4.35}$$

$$i_{\text{Cr1}}(t) = i_{\text{Cr2}}(t) = \frac{\pi}{2} I_{\text{out}} \sin \omega_{\text{res}} t. \tag{4.36}$$

Since the resonant current through the secondary winding of the transformer splits equally through the resonant capacitors:

$$i_{\text{sec}}(t) = 2 i_{\text{Cr1}}(t) = \pi I_{\text{out}} \sin \omega_{\text{res}} t. \tag{4.37}$$

When the rectifier works as a VQR, i_{sec} is split between the rectifier diodes and the auxiliary MOSFET M_{aux1}, therefore modifying the current balances in all the rectifier nodes. In particular, the currents through the body diodes of M_{aux2} and M_{aux3} lose their rectified sinusoidal shape and become half-wave sinusoids. The application of the Kirchhoff current laws at the nodes of the rectifier leads to the

following modified expressions:

$$i_{\mathrm{D1}}(t) = i_{\mathrm{aux3}}(t) = \begin{cases} \pi I_{\mathrm{out}} \sin \omega_{\mathrm{res}} t, \ t \in T_1 \\ 0, \ t \in T_2 \end{cases} \tag{4.38}$$

$$i_{\mathrm{D2}}(t) = i_{\mathrm{aux2}}(t) = \begin{cases} 0, \ t \in T_1 \\ \pi I_{\mathrm{out}} \sin \omega_{\mathrm{res}} t, \ t \in T_2 \end{cases} \tag{4.39}$$

$$i_{\mathrm{sec}}(t) = 2\pi I_{\mathrm{out}} \sin \omega_{\mathrm{res}} t \tag{4.40}$$

$$i_{\mathrm{Cr1}}(t) = i_{\mathrm{Cr2}}(t) = \frac{1}{2} i_{\mathrm{sec}}(t) = \pi I_{\mathrm{out}} \sin \omega_{\mathrm{res}} t \tag{4.41}$$

$$i_{\mathrm{aux1}}(t) = i_{\mathrm{sec}}(t) + i_{\mathrm{D2}}(t) - i_{\mathrm{D1}}(t) = \pi I_{\mathrm{out}} \sin \omega_{\mathrm{res}} t \,. \tag{4.42}$$

Independently from the topology of the rectifier, the current stresses at the primary side of the transformer are obtained reflecting i_{sec}. In addition, the presence of a finite magnetizing inductance introduces a triangular current i_{m} with null average value and peak-to-peak ripple equal to $\frac{V_{\mathrm{in}}}{2L_{\mathrm{m}} f_{\mathrm{res}}}$, independently from the load condition:

$$i_{\mathrm{prim}}(t) = n i_{\mathrm{sec}}(t) + i_{\mathrm{m}}(t) \,. \tag{4.43}$$

The value of L_{m} of the resonant transformer is usually designed with care for two simultaneous purposes [170]:

- to provide a sufficient energy storage to assist the ZVS turn on of the full-bridge devices during the deadtime;
- to shape, together with the leakage inductance, the gain profile in frequency-modulated LLC converters: the inductance ratio, more in details, determines the step-up capability of LLC converters when operating below resonance.

In this work, the location of the resonant tank at the secondary side and the exploitation of the converter at the resonance frequency restrict the design criteria to the ZVS condition requirement alone. As a result, the value of L_{m} is designed to the

maximum value that ensures the ZVS condition [170, 163]:

$$L_{\mathrm{m}} < \frac{t_{\mathrm{dead}}}{8 C_{\mathrm{oss}} f_{\mathrm{sw}}}, \tag{4.44}$$

where t_{dead} is the deadtime of the full-bridge legs, while C_{oss} is the energy-equivalent output capacitance of MOSFETs M_{1-4}. The selection of the maximum value allows to minimize the circulating current that increases the conduction losses in the full-bridge transistors. However, a more conservative lower value should be considered to account for the potential underestimation of the parasitic capacitances. In any case, especially at heavy loads, the contribution of the magnetizing current could be assumed to be negligible compared to the resonant current induced by the electromagnetic coupling between the two windings. This assumption allows to simplify $i_{\mathrm{prim}}(t) \approx n i_{\mathrm{sec}}(t)$ and to derive analytical expressions for the current stresses in the full-bridge MOSFETs:

$$i_{\mathrm{M1}}(t) = i_{\mathrm{M3}}(t) = \begin{cases} n i_{\mathrm{sec}}(t), \ t \in T_1 \\ 0, \ t \in T_2 \end{cases} \tag{4.45}$$

$$i_{\mathrm{M2}}(t) = i_{\mathrm{M4}}(t) = \begin{cases} 0, \ t \in T_1 \\ -n i_{\mathrm{sec}}(t), \ t \in T_2 \end{cases} \tag{4.46}$$

The peak voltage of the full-bridge transistors is V_{in}. Since they are expected to turn on at zero voltage, it is crucial to select transistors with low ON-resistance $R_{\mathrm{DS,ON}}$ to ensure a high efficiency over the wide power range of the proposed converter. Figs. 4.4a and 4.7a can help identify the voltage stresses on the rectifier semiconductor devices.

A particular attention should be devoted to the design of the resonant tank components, namely $C_{\mathrm{r1}} = C_{\mathrm{r1}} = C_{\mathrm{r}}$, and L_{k}. Their values are linked to each other through the resonance frequency, which is this work is set as a degree of freedom: a typical resonance frequency f_{res}=100 kHz for step-up MOSFETs-based SRC converters [89, 90] was selected, later adjusted to 90 kHz to comply with the actual leakage inductance of the transformer prototype. Among the infinite combinations of C_{r} and L_{k}, it is necessary to identify an additional design equation to single out a single couple of values.

Table 4.7 Comparison of the steady-state voltage and current stresses of the SRC components in the MV and LV mode.

Converter component	Peak voltage stress		RMS current stress		Average current stress	
	LV	MV	LV	MV	LV	MV
Full-bridge MOSFETs M_{1-4}	V_{in}	V_{in}	$n\pi I_{\text{out}}$	$\frac{n\pi}{\sqrt{2}}I_{\text{out}}$	$n\pi I_{\text{out}}$	$\frac{n\pi}{\sqrt{2}}I_{\text{out}}$
Transformer primary winding	V_{in}	V_{in}	$\frac{2n\pi}{\sqrt{2}}I_{\text{out}}$	$\frac{n\pi}{\sqrt{2}}I_{\text{out}}$	0	0
Transformer secondary winding	$\frac{V_{\text{oSRC}}}{4}+\frac{I_{\text{out}}}{f_{\text{res}}C_{\text{r}}}$	$\frac{V_{\text{oSRC}}}{2}+\frac{I_{\text{out}}}{2f_{\text{res}}C_{\text{r}}}$	$\frac{2\pi}{\sqrt{2}}I_{\text{out}}$	$\frac{\pi}{\sqrt{2}}I_{\text{out}}$	0	0
Rectifier diodes D_{1-2}	$\frac{V_{\text{oSRC}}}{2}$	V_{oSRC}	I_{out}	I_{out}	I_{out}	I_{out}
Auxiliary MOSFET M_{aux1}	0	$\frac{V_{\text{oSRC}}}{2}$	$\frac{\pi}{\sqrt{2}}I_{\text{out}}$	0	0	0
Auxiliary MOSFETs $M_{\text{aux2-3}}$	$\frac{V_{\text{oSRC}}}{2}$	0	$\frac{\pi}{2}I_{\text{out}}$	$\frac{\pi}{2\sqrt{2}}I_{\text{out}}$	I_{out}	I_{out}
Resonant capacitors $C_{\text{r1-r2}}$	$\frac{V_{\text{oSRC}}}{4}+\frac{I_{\text{out}}}{f_{\text{res}}C_{\text{r}}}$	$\frac{V_{\text{oSRC}}}{2}+\frac{I_{\text{out}}}{2f_{\text{res}}C_{\text{r}}}$	$\frac{\pi}{\sqrt{2}}I_{\text{out}}$	$\frac{\pi}{2\sqrt{2}}I_{\text{out}}$	0	0
Output capacitors $C_{\text{o1-o2}}$	$\frac{V_{\text{oSRC}}}{2}$	$\frac{V_{\text{oSRC}}}{2}$	$I_{\text{out}}\sqrt{\frac{\pi^2}{4}-1}$	$I_{\text{out}}\sqrt{\frac{\pi^2}{8}-1}$	0	0

In this case, a minimum capacitance value can be derived by imposing that the maximum sinusoidal peak-to-peak voltage ripple across the resonant capacitors does not exceed V_{oSRC}:

$$\Delta V_{C\text{r}} = \frac{1}{C_{\text{r}}}\int_0^{\frac{T_{\text{res}}}{2}} i_{\text{Cr1}}(t)dt = \frac{1}{2C_{\text{r}}}\int_0^{\frac{T_{\text{res}}}{2}} i_{\text{sec}}(t)dt = \frac{\pi I_{\text{out}}}{2\pi f_{\text{res}}C_{\text{r}}} = \frac{I_{\text{out}}}{2f_{\text{res}}C_{\text{r}}} < V_{\text{oSRC}}\,, \tag{4.47}$$

resulting in the following design equation:

$$C_{\text{r}} > \frac{1}{2f_{\text{res}}}\left(\frac{I_{\text{out}}}{V_{\text{oSRC}}}\right)_{\text{max}}. \tag{4.48}$$

It is relevant to observe that, despite the different RMS values, the average current of the auxiliary MOSFETs M_{aux2} and M_{aux3} are equal in the two modes.

Custom transformer design

Very often, the specific inductances (both magnetizing and leakage) and the power ratings required for a target resonant converter require a custom design of the transformer. The design process starts from the rated power and frequency specifications,

Table 4.8 Design specifications of the custom SRC transformer.

Design specification	Value
Rated frequency	100 kHz
Rated power	580 W
Configuration	1 primary coil, 1 secondary coil
Turns ratio $n = \frac{N_2}{N_1}$	4
Peak primary voltage	45 V
Maximum primary current (RMS / peak)	17.8 A / 25 A
Peak secondary voltage	300 V
Maximum secondary current (RMS / peak)	4.4 A / 6.3 A
Leakage inductance seen at the secondary coil	25 µH–35 µH
Magnetizing inductance seen at the primary coil	50 µH–60 µH
Target primary winding AC resistance	<15 mΩ
Target secondary winding AC resistance	<250 mΩ
Isolation type	Basic

the target magnetizing and leakage inductances, the desired turns ratio, the required type of isolation, and potential additional constraints (such as the presence of auxiliary windings). The optimization of the magnetic component involves both the geometry and material of the core, and the arrangements and wire type of the windings.

For this converter, the design specifications of the custom transformer are reported in Tab. 4.8. The peak electrical stresses are based on the worst cases highlighted in Tab. 4.7. The reported maximum AC resistances at the primary and secondary windings refer to a maximum 5 W loss tolerated for each winding, to ensure a satisfactory efficiency of the transformer. However, the AC losses in the windings of a magnetic component are not straightforward to model and characterize. The analytical or approximated models available in the literature prove that the AC resistances are strongly dependent on the operating frequency, type and diameter of the wire (Litz or solid, round or square) and arrangement of the windings [171–174]. In general, a Litz wire diameter comparable or lower than the skin depth helps reducing the losses due to the skin effect, while an optimized arrangement of the primary and secondary coils can significantly reduce the proximity effect losses.

Table 4.9 Main measured parameters of the transformer prototype.

Parameter	Measured value
Magnetizing inductance seen at the primary coil	57.5 µH
Leakage inductance seen at the secondary coil	29.3 µH
Primary winding DC resistance	1.6 mΩ
Secondary winding DC resistance	31.2 mΩ

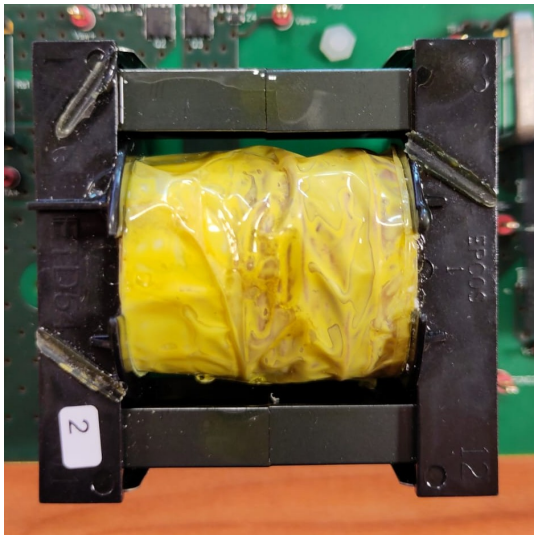


Fig. 4.11 Photo of the transformer prototype, soldered on the PCB

The transformer was manufactured in two prototypes by ICE Transformers, using a double E core equivalent to ETD 54/28/19, with 4 turns of the primary coil and 16 for the secondary. Litz wires with 50 µm strands were used for both the coils, allowing to minimize the losses due to skin effect. The characterization of the main design parameters for the transformer prototype mounted on the converter PCB is reported in Tab. 4.9. All the parameters are included in the target ranges set by specification.

A photo of the transformer prototype is illustrated in Fig. 4.11. The prototype measures approximately 55 mmx56 mmx46 mm, and is mounted on the PCB via a through-hole coil former.

4.3.2 Boost design

In both CCM and DCM operating modes, the voltage gain of a two-level boost is modulated by changing the pulse width of the low-side transistor conduction period, without modifying the switching frequency. The fixed frequency operation allows to simplify the input and output filter capacitors design, but these two operating modes suffer of efficiency limitations that led this design to consider the BCM. The main limitation of CCM is the strong unbalance of conduction and switching losses between the two transistors (considering a synchronous boost), especially at higher duty cycles operation. In addition, the control-to-output transfer function of a boost in CCM operation is characterized by a RHP zero that complicates the stabilization of the voltage control loop. The low-side transistor never experiences soft switching, while the high-side transistor turns on at zero voltage, thanks to the polarity of the boost inductor current that flows through the body diode during the deadtime before the turn on. The main issue of DCM operation, instead, is the high current stress due to the increased RMS values in all the converter components. In addition, the DCM is unlocked only for conventional boost converters with a high-side diode, which may significantly affect the conversion efficiency at heavy loads.

For these reasons, the BCM was considered an optimal trade-off, allowing to exploit the soft turn on switching of both transistors while limiting the current stresses compared to the DCM. In the conventional BCM (denoted by C-BCM), the high-side MOSFET M_{HS} turns off when the inductor current falls to zero, as shown in Fig. 4.5a. As a result, depending on the load, the switching frequency $f_{\mathrm{sw,b}}$ of the PWM signals is not pre-defined, but changes as a function of the working point, the required voltage gain and the selected boost inductance L_{b}. Its expression is based on the computation of the average inductor current $\bar{I}_L$:

$$\bar{I}_L = \frac{I_{\mathrm{peak}}}{2} = \frac{1}{2}\frac{V_{\mathrm{in}}}{L_{\mathrm{b}}} D T_{\mathrm{sw,b}} = \frac{1}{2}\frac{V_{\mathrm{in}} D}{L_{\mathrm{b}} f_{\mathrm{sw,b}}}, \tag{4.49}$$

where I_{peak} is the peak value of the triangular current. At the same time, assuming a 100 % efficiency of the converter:

$$V_{\mathrm{in}}\bar{I}_L = V_{\mathrm{ob}} I_{\mathrm{out}} \longrightarrow \bar{I}_L = \frac{V_{\mathrm{ob}}}{V_{\mathrm{in}}} I_{\mathrm{out}} = G_1 I_{\mathrm{out}} = \frac{I_{\mathrm{out}}}{1-D} \tag{4.50}$$

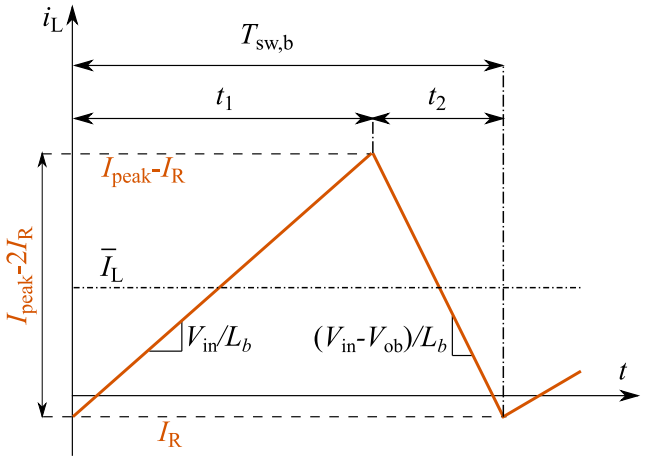


Fig. 4.12 Inductor current waveform in the ZVS-BCM operation, labelled with the main current and time variables for the computation of the switching frequency.

By equating (4.49) and (4.50), the switching frequency becomes:

$$f_{sw,b} = \frac{V_{in}}{2L_b I_{out}} D(1-D)\,. \tag{4.51}$$

As anticipated in Section 4.2, extending the conduction of M_{HS} after the zero-crossing of the inductor current, it is more likely to achieve the ZVS turn-on of the low-side transistor M_{LS}. This alternative operating mode is denoted in this work by ZVS-BCM to highlight the beneficial soft-switching of both the converter transistors, independently on the working point. To compute the impact of this period extension on the switching frequency and converter losses, let's assume that the inductor current i_L is a triangular current sweeping from $I_R < 0$ and $I_{peak} - I_R$, where I_{peak} is the previously computed peak current of the C-BCM. Fig. 4.12 shows a representative qualitative inductor current waveform, highlighting the main time and current values required to compute $f_{sw,b}$. The deadtime is assumed to be negligible compared to the switching period, to ease the computation. During time t_1 (conduction of the low-side transistor), the current slope is $\frac{V_{in}}{L_b}$, leading to:

$$\frac{V_{in}}{L_b} t_1 = I_{peak} - 2I_R \longrightarrow t_1 = \frac{L_b}{V_{in}} \left(I_{peak} - 2I_R\right)\,. \tag{4.52}$$

During t_2 (conduction of the low-side transistor), on the other hand:

$$-\frac{V_{\text{in}}-V_{\text{ob}}}{L_{\text{b}}}t_2 = I_{\text{peak}} - 2I_{\text{R}} \longrightarrow t_2 = \frac{L_{\text{b}}}{V_{\text{ob}}-V_{\text{in}}}\left(I_{\text{peak}} - 2I_{\text{R}}\right). \tag{4.53}$$

By definition, the switching period is the sum of t_1 and t_2. Combining (4.52), (4.53) and 4.49:

$$T_{\text{sw,b}} = t_1 + t_2 = \frac{2L_{\text{b}}}{V_{\text{in}}D}\left(\bar{I}_L - I_{\text{R}}\right). \tag{4.54}$$

For compactness of notation, we can define $\alpha > 0$:

$$\alpha = 1 - \frac{I_{\text{R}}}{\bar{I}_L}. \tag{4.55}$$

α represents the relative impact of the negative current I_{R} compared to the average inductor current. Intuitively, this parameter will affect the converter stresses and the switching frequency. The updated boost switching frequency can be computed by inverting (4.54):

$$f_{\text{sw,b}} = \frac{1}{T_{\text{sw,b}}} = \frac{V_{\text{in}}D}{2L_{\text{b}}\left(\bar{I}_L - I_{\text{R}}\right)} = \frac{V_{\text{in}}D}{2L_{\text{b}}\bar{I}_L\left(1-\frac{I_{\text{R}}}{\bar{I}_L}\right)} = \frac{V_{\text{in}}D\left(1-D\right)}{2L_{\text{b}}I_{\text{out}}\alpha}. \tag{4.56}$$

It is relevant to notice that, in presence of a negative current extension of the ZVS-BCM, the updated expression of $f_{\text{sw,b}}$ is simply scaled by a factor α compared to the C-BCM. From the design perspective, it may be more comfortable to express $f_{\text{sw,b}}$ as function of the boost gain $G_1 = \frac{1}{1-D}$, rather than the duty cycle D:

$$f_{\text{sw,b}} = \frac{V_{\text{in}}}{2L_{\text{b}}I_{\text{out}}\alpha}\frac{G_1 - 1}{G_1^2}. \tag{4.57}$$

According to (4.27), the required I_{R}, and, consequently, α, depend on the equivalent output parasitic capacitance C_{oss} of the selected transistors. This is strongly non-linear and is usually characterized as a function of the output voltage in the transistor datasheet. More representative values of capacitance to be used in (4.27) are the charge-equivalent or time-equivalent capacitances, which embed in a single value the non-linearity of the parasitics.

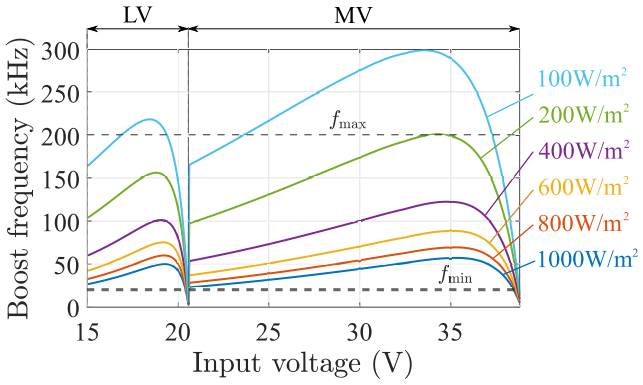


Fig. 4.13 Boost frequency as function of input voltage at various irradiance conditions, for $L_b = 33\,\mu H$.

The boost design is mainly based on the LV and MV operation, since the boost is controlled to be off in the HV mode. Once the turns ratio n is set from (4.29), the boost voltage gain in MV and LV modes follows:

$$G_1 = \begin{cases} G_{TOT} - 4n = \frac{V_{out}}{V_{in}} - 4n, \; V_{in} \in \text{LV mode} \\ G_{TOT} - 2n = \frac{V_{out}}{V_{in}} - 2n, \; V_{in} \in \text{MV mode} \end{cases} . \tag{4.58}$$

According to (4.56), for a given power-voltage curve of a PV panel, the required boost gain G_1 and a required I_R imposed by the transistors selection, the boost inductance L_b becomes the only design variable that determines the switching frequency. More in details, there is an inverse relationship between $f_{sw,b}$ and L_b. In this work, L_b is selected to bound $f_{sw,b}$ within 20 kHz and 200 kHz for most of the uniform irradiance scenarios, considering the electrical characteristic of a target PV module[3] The lower bound is set to limit interference in the audio bandwidth, while the upper bound to limit the hard-switching turn-off losses of the transistors and the frequency-related core losses of the inductor.

Various design iterations led to $L_b = 33\,\mu H$, effectively meeting the switching frequency constraints. To illustrate the behaviour of $f_{sw,b}$, an example at various representative irradiance conditions and $I_R = -500\,mA$ is shown in Fig. 4.13. As it can be predicted by (4.57), the lowest frequencies are obtained when $G_1 \to 1$ (immediately below the threshold voltages V_{th}^- and V_{th}^+), and in correspondence of the highest boost gains (at $V_{in} = 15\,V$ and immediately above V_{th}^-). However, the

[3]Datasheet available at: https://www.enfsolar.com/pv/panel-datasheet/crystalline/61873.

current stresses are expected to be minimized in the first cases, while maximized in the latter.

The current stresses in the boost components can be computed by recurring to the definition of RMS currents in (4.33). The RMS current stresses expressions for the inductor, low-side transistor and high-side transistor are reported in , respectively, where $I_{\text{peak}} = 2\bar{I}_L$ and $\beta = \sqrt{\frac{3+\alpha^2}{4}}$ for compactness of notation.

$$I_{\text{L,RMS}} = \frac{I_{\text{peak}}}{\sqrt{3}}\beta \tag{4.59}$$

$$I_{\text{LS,RMS}} = \sqrt{\frac{D}{3}}I_{\text{peak}}\beta \tag{4.60}$$

$$I_{\text{HS,RMS}} = \sqrt{\frac{1-D}{3}}I_{\text{peak}}\beta \tag{4.61}$$

The current stresses of the output capacitor C_{b} can be derived in the assumption that the output current I_{out} is purely DC and the capacitor conducts only the AC contribution of the high-side current:

$$I_{\text{C}_\text{b},\text{RMS}} = \sqrt{I_{\text{HS,RMS}}^2 - I_{\text{out}}^2} = \sqrt{\frac{1}{3G_1}\left(2G_1 I_{\text{out}}\beta\right)^2 - I_{\text{out}}^2} = I_{\text{out}}\sqrt{\frac{4}{3}G_1\beta^2 - 1} \tag{4.62}$$

The boost inductor should be selected to meet the required inductance and to sustain the worst-case peak current $I_{\text{peak}} - I_{\text{R}}$ without saturating. To avoid excessive heating, the rated current on the inductor datasheet should not be exceeded.

The peak voltage stress of both the transistors and output capacitor is linked to the maximum voltage that the boost is required to generate $V_{\text{ob,max}}$. This condition occurs just above V_{th}^-, where the boost gain is maximum:

$$V_{\text{ob,max}} = V_{\text{out}} - 2nV_{\text{th}}^- = V_{\text{out}} - 2n\frac{V_{\text{out}}}{4n+1} = \frac{2n+1}{4n+1}V_{\text{out}}\,. \tag{4.63}$$

In the HV mode, where the boost is off, both the inductor and high-side transistor conduct the DC current I_{out}, and $V_{\text{ob}} = V_{\text{in}}$. Tab. 4.10 summarizes the main voltage and current stresses of the boost components.

Table 4.10 Steady-state voltage and current stresses of the boost components in the MV / LV modes (equivalent expressions) and HV mode.

Converter component	Peak voltage stress		RMS current stress	
	LV / MV	HV	LV / MV	HV
Inductor L_b	$V_{in}(G_1-1)$	/ (no switching)	$\frac{I_{peak}}{\sqrt{3}}\beta$	I_{out} (DC)
Low-side transistor M_{LS}	$V_{in}G_1$	V_{in} (off)	$\sqrt{\frac{D}{3}}I_{peak}\beta$	/ (off)
High-side transistor M_{HS}	$V_{in}G_1$	/ (on)	$\sqrt{\frac{1-D}{3}}I_{peak}\beta$	I_{out} (DC)
Capacitor C_b	$V_{in}G_1$	V_{in}	$I_{out}\sqrt{\frac{4}{3}G_1\beta^2-1}$	/ (no AC current)

The only missing variable to be designed is the output capacitance value. This should be set to maintain the output voltage ripple induced by the triangular current stress below a pre-defined value, also in the worst-case condition. The minimum C_{in} relies on the computation of the charge ΔQ that the capacitor should supply and sink at every switching cycle to maintain a stable output voltage. An approximated expression derives from the integration of the triagular capacitor current during the high-side transistor conduction:

$$\Delta Q \approx \frac{1}{2}(1-D)T_{sw,b}\cdot\left(I_{peak}-I_R-I_{out}\right)=\frac{L_b I_{out}^2}{V_{in}}\alpha G_1\left(1+\frac{\alpha G_1}{G_1-1}\right) \tag{4.64}$$

From (4.64), ΔQ increases in the working points characterized by high output current and boost gain. By denoting ΔV_{ob} the maximum tolerated voltage ripple, the output capacitance should satisfy:

$$C_b > \frac{\Delta Q}{\Delta V_{ob}}=\frac{L_b I_{out}^2}{\Delta V_{ob}V_{in}}\alpha G_1\left(1+\frac{\alpha G_1}{G_1-1}\right). \tag{4.65}$$

Considering the worst case working point characterized by $V_{in}=20.5\,\text{V}/P_{out}=400\,\text{W}$ and a 2 % tolerated voltage ripple around the rated V_{ob}, the computed minimum capacitance is $\approx 8.1\,\mu\text{F}$, rounded to $10\,\mu\text{F}$. A film capacitor was selected, in order to reduce the ESR and to improve the long-term reliability.

The input capacitance, which should filter the AC current contributions of both the SRC and boost, was designed as the last component. The following assumptions were made to compute its RMS current stresses:

- the MV mode is the voltage range in which the highest powers are expected, therefore this mode is considered for the worst-case current stresses;
- the magnetizing current is considered to be negligible compared to the resonant contribution of i_{prim}. As a consequence, the total current supplied to the full-bridge is $|i_{\text{prim}}| \approx \pi I_{\text{out}} n |\sin \omega_{\text{res}} t|$;
- the input current supplied by the PV panel is considered to be constant: $\bar{I}_{\text{in}} \approx G_{\text{TOT}} I_{\text{out}}$
- the current balance at the input node holds, thus: $i_{C_{\text{in}}}(t) = \bar{I}_{\text{in}} - |i_{\text{prim}}(t)| - i_{\text{L}}(t)$.

The total AC contribution $I_{\text{SRC,RMS,AC}}$ from the SRC becomes:

$$\begin{aligned} I_{\text{SRC,RMS,AC}} &= \sqrt{I^2_{\text{prim,RMS}} - \bar{I}^2_{\text{SRC,in}}} = \sqrt{\left(\frac{\pi n I_{\text{out}}}{\sqrt{2}}\right)^2 - (2nI_{\text{out}})^2} \\ &= I_{\text{out}} \sqrt{\frac{n^2\pi^2}{2} - 4n^2} = 2nI_{\text{out}} \sqrt{\frac{\pi^2}{8} - 1} \end{aligned} \tag{4.66}$$

The total AC contribution $I_{\text{b,RMS,AC}}$ from the boost becomes:

$$\begin{aligned} I_{\text{b,RMS,AC}} &= \sqrt{I^2_{\text{L,RMS}} - \bar{I}^2_{\text{L}}} = \sqrt{\left(\frac{I_{\text{peak}}}{\sqrt{3}}\beta\right)^2 - (G_1 I_{\text{out}})^2} \\ &= \sqrt{\left(\frac{2G_1 I_{\text{out}}\beta}{\sqrt{3}}\right)^2 - (G_1 I_{\text{out}})^2} = G_1 I_{\text{out}} \sqrt{\frac{4}{3}\beta^2 - 1}\,. \end{aligned} \tag{4.67}$$

Assuming that the spectra of the AC currents supplied to the SRC and boost are decoupled, the total RMS current of the input capacitor becomes:

$$\begin{aligned} I_{C_{\text{in}},\text{RMS}} &= \sqrt{I^2_{\text{SRC,RMS,AC}} + I^2_{\text{b,RMS,AC}}} \\ &= I_{\text{out}} \sqrt{4n^2 \left(\frac{\pi^2}{8} - 1\right) + G_1^2 \left(\frac{4}{3}\beta^2 - 1\right)}\,. \end{aligned} \tag{4.68}$$

Since the first term under the square root in (4.68) is constant, it follows that the harshest current stresses occur in correspondence of the highest boost gains. When selecting a commercial part, it is essential to consider that the capacitor must tolerate

these stresses without overheating. The rated voltage of the capacitor should be higher that the maximum input voltage, i.e., the open-circuit voltage of the target PV panel.

The design of the required capacitance to maintain a stable voltage requires to evaluate how a voltage ripple across a PV panel could deteriorate the power harvesting from it. Compared to single-stage inverters, in which the input capacitance is responsible to filter out the harmonics at twice the grid frequency (e.g.: 100 Hz), in dual stage converters the filter requirements of the input capacitor are significantly relaxed, because limited to the switching frequency [175]. According to previous studies, the minimum filter capacitance across the PV panel should be designed to limit the reduction of power induced by the AC voltage ripple [176, 175]. Given the strong non-linearity of the PV electrical characteristic, the reduction of power is not straightforward to quantify: an approximated approach based on a small signal impedance was proposed in [177].

At the same time, it is important to consider that a more conservative design with a larger capacitance increases the settling time of the closed-loop MPPT control, i.e. the time required for the converter to reach the new steady state after a step of the reference voltage [178].

In this work, following the guidelines in [176], C_{in} was designed to maintain the maximum voltage ripple across the PV panel below 8.5 % of the rated MPP voltage, associated to a power reduction limited to 2 % of the rated power. In general, defining the maximum voltage ripple ΔV_{in} and the charge exchanged with the converter stages ΔQ_{in}, the minimum C_{in} can be computed as:

$$C_{\text{in}} > \frac{\Delta Q_{\text{in}}}{\Delta V_{\text{in}}}\,. \tag{4.69}$$

Considering the different shape and frequency of the current stresses excited by the two stages of the IPOS architecture, an analytical solution of ΔQ_{in} cannot be found. However, by design choice, the current stresses of the boost are minimized in correspondence of the rated PV panel working point. As a consequence, it can be assumed that a minimum C_{in} value can be computed by only considering the AC current stresses of the SRC, i.e. of $|i_{\text{prim}}(t)|$. According to the Fourier analysis, the amplitude of the most dominant harmonic contribution of $|i_{\text{prim}}(t)|$ is $\frac{4}{3} n I_{\text{out}}$ at

Table 4.11 Selected components for the converter prototype.

Component	Value	Part number
Full-bridge MOSFETs M_{1-4}	N/A	STL120N10F8
Transformer core	N/A	ETD 54/28/19, N97
Transf. primary coil	N/A	4 turns, 2400 x AWG 44
Transf. secondary coil	N/A	16 turns, 225 x AWG 41
Rectifier diodes D_{1-2}	N/A	STTH10R04G-TR
Rectifier MOSFETs $M_{\text{aux},1-3}$	N/A	STB45N30M5
Resonant capacitors $C_{\text{r1-r2}}$	68 nF	R76PI268050H7J
Output capacitors $C_{\text{o1-o2}}$	3.3 µF	R76PR4330AA30K
Boost MOSFETs $M_{\text{HS-LS}}$	N/A	STB45N30M5
Boost inductor L_{b}	33 µH	AGP4233-333ME
Boost output capacitor C_{b}	10 µF	R75MW51004030J
Input capacitor C_{in}	37.6 µF	8x CB182D0475JBC

frequency $2f_{\text{sw}}$. This leads to the following computation of ΔQ_{in}:

$$\Delta Q_{\text{in}} = \int_0^{\frac{1}{2}\frac{1}{2f_{\text{sw}}}} \frac{4}{3} n I_{\text{out}} \sin\left(2\pi \cdot 2f_{\text{sw}} t\right) dt = \frac{4}{3} n I_{\text{out}} \frac{1}{2\pi f_{\text{sw}}} = \frac{2nI_{\text{out}}}{3\pi f_{\text{sw}}}. \tag{4.70}$$

Assuming 5 % voltage ripple superimposed to the rated $V_{\text{in}} = 36.5\,\text{V}$, i.e. 1.8 V, the constraint on the minimum capacitance using (4.69) becomes $C_{\text{in}} > 17\,\mu\text{F}$. This analytical approach only provides an order of magnitude of the required capacitance, but a more systematic approach should be based on simulations to evaluate ΔQ_{in} in a more comprehensive way. Based on simulations, the final selected capacitance was $C_{\text{in}} = 37.6\,\mu\text{F}$. The final list of selected components for the PCB prototype is reported in Tab. 4.11.

4.4 Control design

4.4.1 General control architecture of PPO

In PPO applications, as described in Chapter 2.2, multiple step-up DC-DC converters are connected in parallel to the same DC rail that feeds a grid inverter or local DC loads. A general and simplified block diagram of the control architecture is shown in Fig. 4.14. A relevant advantage of the PPO architecture is that a potential fault at the grid inverter can be simultaneously detected by each PPO without inter-communication among the DC-DC stages. If the grid inverter enters a fault state that prevents the regulation of the DC rail voltage (350 V or 400 V), the fluctuations of this voltage can simultaneously be detected and handled by all the PPO stages. This phenomenon can occur, for instance, when the grid is de-energized, or when the grid inverter experiences an internal fault. In SPO, on the other hand, the single optimizer stage may not be able alone to detect a potential fault at the inverting stage, and communication among the SPO is needed to stop the energy harvesting from the PV plant.

In general, the control block diagram of a PPO consists of two nested control loops, as shown in Fig. 4.14: an external, low bandwidth controller performs the MPPT, while an internal high bandwidth controller regulates the PV module voltage. The MPPT controller does not require a high bandwidth because the electrical characteristic of the PV panel changes according to relatively slow variations in irradiance, temperature and shading scenarios. In most of the simplest and most popular MPPT algorithms, such as the Perturb & Observe (P&O) and Incremental Conductance (InC) approaches, the MPPT measures the instantaneous power at a certain time, compares it with the previously measured power, and updates the reference voltage V_{in}^{*} towards a higher power working point [179, 180]. The inner voltage regulator, on the other hand, updates the control variable / variables to minimize the voltage error $\varepsilon = V_{\text{in}}^{*} - V_{\text{in}}$. The control variables, such as the pulse-width, switching frequency, or phase shift, are then translated by a modulator into a sequence of gate signals G_i. The voltage regulator, as anticipated, should include a fault detection control that detects anomalies at the output voltage V_{out} and turns off the converter. It is relevant to point out that, differently from other applications, in this context the output voltage is regulated by the following converter stage (the grid inverter), while the PPO aims at regulating the input voltage across the

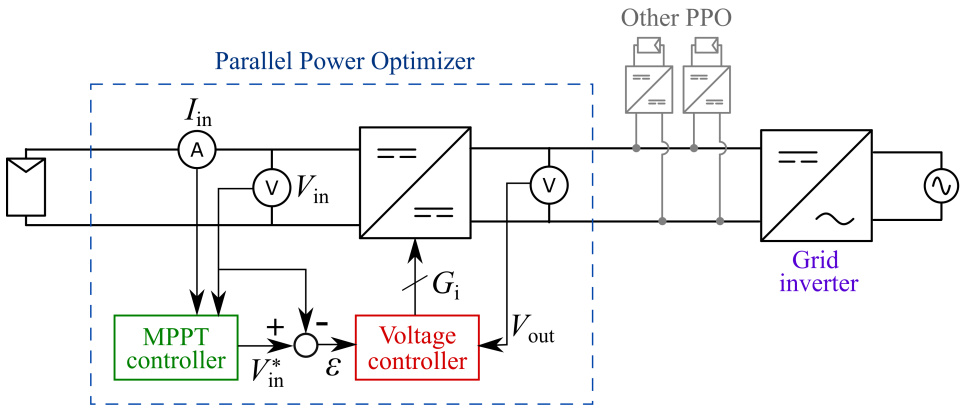


Fig. 4.14 General control block diagram of a PPO with MPPT control.

PV panel or, in other words, aims at modifying the voltage gain to perform the MPPT.

4.4.2 Multi-mode control approach of the proposed converter

While the MPPT controller is independent from the specific PPO converter topology, the design of the voltage controller strongly depends on it. The first step consists in the identification of the control variables allowing to modulate the voltage gain. In this specific case, being the converter characterized by multiple operating modes, different control variables exist according to the range of the input voltage.

As anticipated in Sections 4.2 and 4.3, the voltage gain modulation in the LV and MV modes is performed by the synchronous boost, since the SRC operates with fixed gain at the resonance frequency. The boost is operated in the variable frequency BCM, exploiting a ZCD circuit to achieve the ZVS of the low-side transistor. In this operating mode, the on time T_{ON} is exploited to modulate the gain, while the switching frequency is determined by the working point and not defined *a priori*. In the HV mode, on the other hand, the boost is off and the gain modulation is performed by modifying the phase shift Φ of the SRC full-bridge legs. An additional control variable of the converter, which modifies the SRC gain in a discrete way, is represented by the rectifier mode, which can be either VDR or VQR. The combination of these variables allows the converter to operate in the whole target voltage range.

According to this preliminary discussion, a more detailed block diagram of the voltage controller suited for the proposed converter topology is shown in Fig. 4.15.

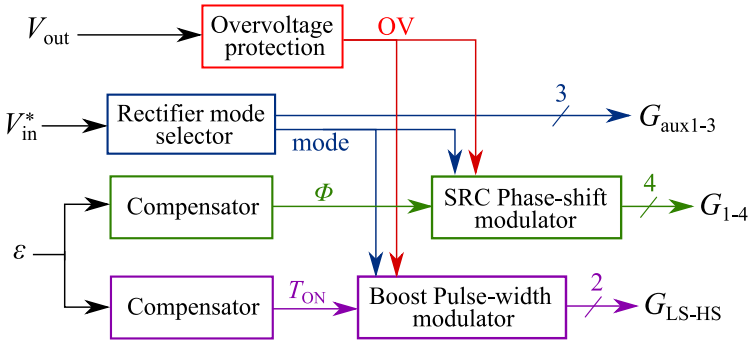


Fig. 4.15 Block diagram of the voltage regulator for the specific IPOS converter proposed in this work. $\varepsilon = V^*_{in} - V_{in}$ is the error between the reference and the measured input voltages, Φ is the phase shift between the two legs of the SRC full-bridge, T_{ON} is the on-time of the low-side boost transistor, *OV* is the overvoltage flag.

The block diagram represents an expanded view of the controller block of Fig. 4.14. Specifically, the nine transistors (M_{aux1} is considered like a single transistor) of the topology can be split into three groups, driven by three different modulators. The conduction state of the rectifier auxiliary MOSFETs M_{aux1}, M_{aux2} and M_{aux3}, which determines the topology of the rectifier, is handled on the basis of the reference voltage V^*_{in}. The voltage error ε is passed to two different compensators, which update the required control variables of the boost and SRC, namely T_{ON} and Φ. The control variables update should also be based on the working mode: for instance, in both the LV and MV modes Φ should be kept null to maximize the performance of the SRC, while the boost gate signals should be kept off in the HV mode. Specific modulators translate the control variables into gate signals for the two conversion stages. An overvoltage protection that monitors V_{out} should generate an overvoltage flag *OV* to turn off the converter when needed.

The rest of this section is devoted to a mathematical analysis of the relationship between the voltage gain at steady state and the control variables.

In the LV and MV modes, the SRC gain is fixed and depends uniquely on the rectifier mode. This stage can be controlled in open loop with fixed frequency and null phase shift. The required boost gain, defined in (4.58), is determined by T_{ON}. At the same time, as anticipated, the required negative inductor current $I_R < 0$ to assist the ZVS of M_{LS} can be controlled by properly tuning the extension time dt_{ext}. Considering the negative slope $-\frac{V_{ob}-V_{in}}{L_b}$ of the inductor current during the conduction

of the high side transistor M_{HS}:

$$\frac{di_{\mathrm{L}}}{dt} = -\frac{V_{\mathrm{ob}} - V_{\mathrm{in}}}{L_{\mathrm{b}}} \longrightarrow dt_{\mathrm{ext}} = -L_{\mathrm{b}} \frac{I_{\mathrm{R}}}{V_{\mathrm{ob}} - V_{\mathrm{in}}} = -L_{\mathrm{b}} \frac{I_{\mathrm{R}}}{V_{\mathrm{in}}(G_1 - 1)}. \tag{4.71}$$

As in the CCM, the boost gain in the BCM mode depends on the duty cycle D:

$$G_1 = \frac{1}{1-D} \longrightarrow D = 1 - \frac{1}{G_1} = \frac{G_1 - 1}{G_1}. \tag{4.72}$$

The duty cycle can be related to the control variable T_{ON} through the switching frequency, the expression of which was derived in (4.57):

$$T_{\mathrm{ON}} = \frac{D}{f_{\mathrm{sw,b}}} = \frac{G_1 - 1}{G_1} \cdot \frac{2L_{\mathrm{b}} I_{\mathrm{out}} \alpha}{V_{\mathrm{in}}} \frac{G_1^2}{G_1 - 1} = \frac{2L_{\mathrm{b}}}{V_{\mathrm{in}}} \left(G_1 I_{\mathrm{out}} - I_{\mathrm{R}} \right), \tag{4.73}$$

from which:

$$G_1 = \frac{1}{I_{\mathrm{out}}} \left(\frac{V_{\mathrm{in}}}{2L_{\mathrm{b}}} T_{\mathrm{ON}} + I_{\mathrm{R}} \right). \tag{4.74}$$

Eq. (4.73) suggests that, to obtain a desired G_1, a larger T_{ON} is required at heavier loads or when the ZVS condition is harder to achieve (at higher $|I_{\mathrm{R}}|$).

The gain modulation in the HV mode is performed by the PSM, whose detailed operation and modelling was proposed in [168]. The PSM was already exploited in another multi-mode PPO to modulate the gain in a voltage range located below the rated input voltage [90, 89]. Since the operating principle is not new, the expression of the voltage gain in a SRC working in PSM is provided here without further derivation:

$$G_2(\Phi) = n \left[-A \left(\frac{2}{\pi Q} - 1 \right) + \sqrt{A^2 \left(\frac{2}{\pi Q} - 1 \right)^2 + \frac{8A}{\pi Q}} \right], \tag{4.75}$$

where, Q is the quality factor of the secondary-side resonant tank, as expressed in (4.76), n is the turns ratio and A is a function of the phase shift defined for compactness of notation in (4.77).

$$Q = \frac{8\pi L_{\mathrm{k}} f_{\mathrm{res}}}{R_{\mathrm{SRC}}} \tag{4.76}$$

$$A(\Phi) = \frac{1}{2}\left[1 - \cos\left(\pi - \frac{\Phi\pi}{180}\right)\right]. \tag{4.77}$$

The definition of Q relies on the computation of the equivalent AC resistance seen at the input port of the VDR R_{SRC}, which is expressed in (4.78).

$$R_{\mathrm{SRC}} = \frac{2}{\pi^2}\frac{V_{\mathrm{oSRC}}}{I_{\mathrm{out}}}. \tag{4.78}$$

Notice that (4.75) refers to an SRC equipped with a VDR, indeed $G_2(\Phi \to 0^\circ) = 2n$. According to (4.77), an increasing phase shift reduces the voltage gain of the SRC. In the extreme case of 180°, as expected, the voltage gain becomes $G_2(\Phi \to 180^\circ) = 0$. The voltage gain also depends on the resonant tank design and on the load condition: more precisely, for the same phase shift Φ, more significant gain reductions can be obtained at heavier loads (lower R_{SRC}) and with an increased L_{k}. From the transformer design point of view, a worse coupling between the primary and secondary coils allows to relax the phase shift requirements to obtain a target voltage gain. However, as anticipated, the proposed SRC converter is primarily designed to operate in its best efficiency condition, i.e., at resonance, for most of the input voltage range.

An analytical expression of $\Phi(G_2)$ cannot be obtained from (4.75): once the design parameters and the working condition is set, Eq. (4.75) must be numerically solved to determine the required phase shift.

Eqs. (4.79) and (4.80) summarize the voltage gain expressions of the boost and SRC in the three operating modes, expressed as functions of the corresponding control variables. For any input voltage condition, the equation $G_1 + G_2 = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}}$ must always hold.

$$G_1 = \begin{cases} \frac{1}{I_{\mathrm{out}}}\left(\frac{V_{\mathrm{in}}}{2L_{\mathrm{b}}}T_{\mathrm{ON}} + I_{\mathrm{R}}\right), \ V_{\mathrm{in}} \in \text{LV mode} \\ \frac{1}{I_{\mathrm{out}}}\left(\frac{V_{\mathrm{in}}}{2L_{\mathrm{b}}}T_{\mathrm{ON}} + I_{\mathrm{R}}\right), \ V_{\mathrm{in}} \in \text{MV mode} \\ 1, \ V_{\mathrm{in}} \in \text{HV mode} \end{cases} \tag{4.79}$$

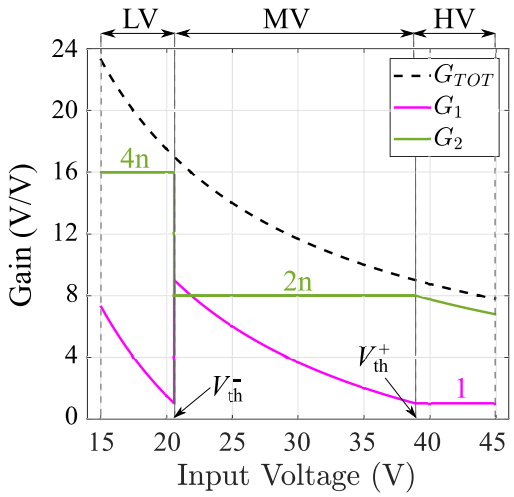


Fig. 4.16 Behaviour of the total converter gain G_{TOT}, boost gain G_1 and SRC gain G_2 in the three operating modes.

$$G_2 = \begin{cases} 4n, \ V_{\text{in}} \in \text{LV mode} \\ 2n, \ V_{\text{in}} \in \text{MV mode} \\ n\left[-A\left(\frac{2}{\pi Q}-1\right)+\sqrt{A^2\left(\frac{2}{\pi Q}-1\right)^2+\frac{8A}{\pi Q}}\right], \ V_{\text{in}} \in \text{HV mode} \end{cases} \tag{4.80}$$

Fig. 4.16 shows the behaviour of the required voltage gains of the two converter stages and the total converter gain, as function of the input voltage.

The expressions of the two main control variables, namely T_{ON} and Φ, are expressed in (4.81) and (4.82) for the whole voltage range.

$$T_{\text{ON}} = \begin{cases} \frac{2L_{\text{b}}}{V_{\text{in}}}\left(G_1 I_{\text{out}} - I_{\text{R}}\right), \ V_{\text{in}} \in \text{LV mode} \\ \frac{2L_{\text{b}}}{V_{\text{in}}}\left(G_1 I_{\text{out}} - I_{\text{R}}\right), \ V_{\text{in}} \in \text{MV mode} \\ 0, \ V_{\text{in}} \in \text{HV mode} \end{cases} \tag{4.81}$$

$$\Phi = \begin{cases} 0, \ V_{\text{in}} \in \text{LV mode} \\ 0, \ V_{\text{in}} \in \text{MV mode} \\ f^{-1}\left(G_2(\Phi)\right), \ V_{\text{in}} \in \text{HV mode} \end{cases} \tag{4.82}$$

As predicted by (4.57), at very low power operation, i.e., at low irradiance conditions, the switching frequency of the boost may increase far above the selected maximum limit, $f_{\mathrm{sw,b,max}} = 200\,\mathrm{kHz}$, causing undesirably high core losses in the inductor and turn-off losses in the boost MOSFETs which may jeopardize the light load efficiency. To limit this issue, the boost control is designed to switch to a low power mode in which the switching frequency is upper-bounded to $f_{\mathrm{sw,b,max}} = 200\,\mathrm{kHz}$. In this mode, the expression of T_{ON} becomes (4.83):

$$T_{\mathrm{ON}} = \frac{D}{f_{\mathrm{sw,b,max}}} = \frac{1}{f_{\mathrm{sw,b,max}}}\left(1 - \frac{1}{G_1}\right). \tag{4.83}$$

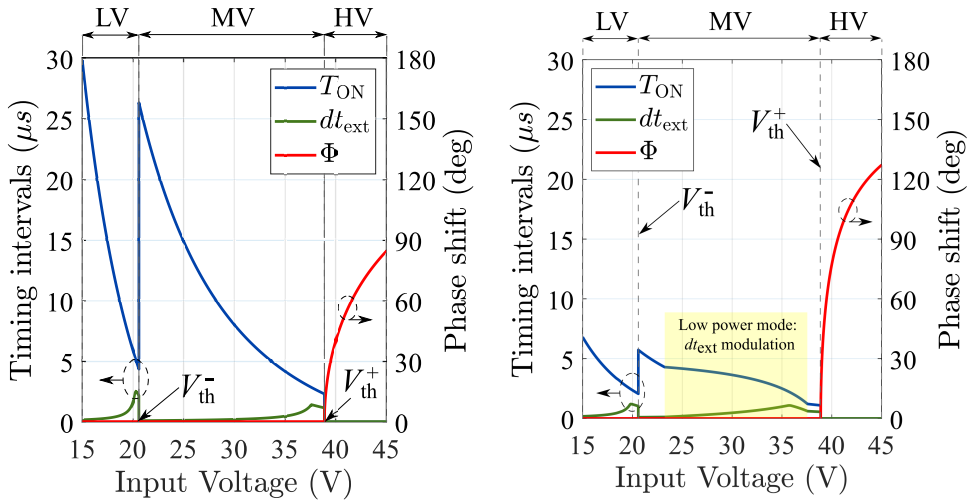
As the frequency is fixed, T_{ON} cannot be used to modulate the gain at varying load conditions. Therefore, in this low power mode dt_{ext} is modified to adjust the voltage gain depending on the working point. Exploiting the triangular shape of the inductor current, it is possible to derive:

$$\begin{gathered} G_1 I_{\mathrm{out}} - \frac{1}{2}\frac{V_{\mathrm{in}}}{L_{\mathrm{b}}} T_{\mathrm{ON}} = dt_{\mathrm{ext}} \frac{V_{\mathrm{in}}\,(1 - G_1)}{L_{\mathrm{b}}} \longrightarrow \\ dt_{\mathrm{ext}} = \frac{1}{G_1 - 1}\left(\frac{T_{\mathrm{ON}}}{2} - \frac{L_{\mathrm{b}} G_1 I_{\mathrm{out}}}{V_{\mathrm{in}}}\right), \end{gathered} \tag{4.84}$$

where T_{ON} is expressed by (4.83). Intuitively, dt_{ext} at low power must increase to shift down the inductor current, as in the case of a constant-frequency CCM operation. The ZVS of both transistors is preserved, limiting the impact of switching losses at low power operation.

As an example, Fig. 4.17a shows the evolution of the control variables T_{ON} and Φ, on the target input voltage range for a constant 300 W power, according to (4.81) and (4.82). The behaviour of dt_{ext} according to (4.71) is also reported, assuming $I_{\mathrm{R}} = -500\,\mathrm{mA}$ on the entire voltage range.

As can be seen, a strong discontinuity in T_{ON} is evident at the LV-MV threshold voltage, where the SRC rectifier morphs between VQR and VDR. The discontinuity coincides with the gain step of the SRC between the two modes. The transition between MV and HV modes is much smoother, since the boost moves between minimum gain to the off state, whereas the phase shift gradually increases from 0. To provide another representative example at lighter loads, Fig. 4.17b shows the



(a) (b)

Fig. 4.17 Graphical representation of the control variables for the two stages in the three operating modes of the proposed converter. (a) Evolution of the control variables T_{ON}, dt_{ext} and Φ, for $P_{out} = 300\,W$; (b) Evolution of the control variables T_{ON}, dt_{ext} and Φ, for $P_{out} = 50\,W$.

evolution of the control variables on the target voltage range for a constant 50 W power. The graphs show that the same boost voltage gain can be achieved with reduced T_{ON} in the LV and MV modes, while an increased phase shift is required for the SRC in the HV mode, due to the reduced quality factor. In the 23 V–38 V range, the low power mode of the boost avoids exceeding the 200 kHz frequency upper limit by modulating dt_{ext} according to (4.84).

As the main focus of the experimental tests in this work was to validate the operating principle and performance of the new topology, the characterization was performed by relying on the open-loop controller schematically shown in Fig. 4.18. The controller is specifically designed to test the steady-state performances of the converter, thus the computation of the required control variables for a specific reference input voltage and power condition, defining the working point of the PV panel, is performed off-line. The controller is responsible of generating suitable gate signals according to the given control variables. Note that the boost modulator takes as input the resulting frequency $f_{sw,b}$ computed by (4.57). As a protection feature, the controller monitors the output voltage V_{out} and turns off the converter control signals in case of overvoltages.

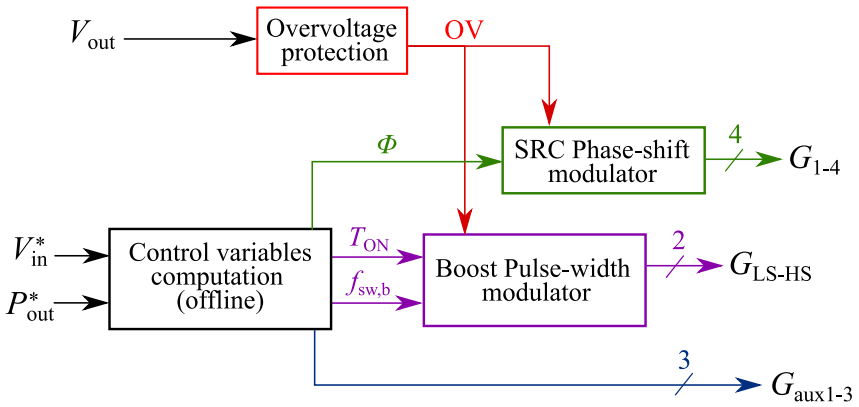


Fig. 4.18 Block diagram of the open-loop controller implemented to test the converter operation and performance.

Soft Transition Strategy between LV and MV Modes

The discontinuity of the SRC and boost gains in correspondence of the MV–LV mode transition must be addressed with care. Although this transition is not expected to occur frequently, since it is well away from the rated input voltage, its analysis is crucial to prevent severe electrical stresses that could compromise the converter reliability. In particular, the SRC is the most critical stage, as it processes the highest fraction of the input power and sustains harsher voltage stresses: for this reason, this section focuses on its behavior during the transition between LV and MV modes.

During the start-up phase, it is known that resonant converters exhibit significant inrush currents while charging the output filter capacitors [181]. Similarly, the VDR–VQR transition involves the charge and discharge of C_{o1} and C_{o2}.

From a control standpoint, the transition corresponds to a change in the conduction state of the auxiliary MOSFETs Maux1, M_{aux2} and M_{aux3}. In the VQR-to-VDR case, turning off M_{aux1} enables the gradual discharge of both output capacitors from $2nV_{in}$ to nV_{in}. Fig. 4.19a illustrates the main simulated waveforms observed during this transition: the control voltages of the auxiliary MOSFETs, the resonant capacitor voltages v_{Cr1} and v_{Cr2}, and the transformer's primary and secondary currents, i_{prim} and i_{sec}, respectively. The simulations are performed in SIMetrix [4] using the SPICE models of the components in the prototype bill of materials. The turn-off of M_{aux1} immediately redistributes the currents, raising the DC voltages of the resonant capacitors from $\frac{V_{oSRC}}{4}$ to $\frac{V_{oSRC}}{2}$. Until v_{oSRC} settles at $2nV_{in} \approx 164\,\text{V}$, the reduced

[4] https://www.simetrix.co.uk/ (accessed Jan. 21, 2026).

quality factor of the resonant tank damps both transformer currents. As a result, the transition does not induce dangerous overvoltages or overcurrents, ensuring safe operation. In closed-loop operation, the boost stage must compensate for the drop in SRC gain by increasing its duty cycle.

Conversely, the transition from VDR to VQR charges the output capacitors from a total $2nV_{\text{in}}$ to the new steady-state voltage $4nV_{\text{in}}$. In this case, the continuous currents keep flowing through the body diodes of M_{aux2} and M_{aux3} after they are turned off, causing no significant modification in the rectifier currents and voltages. Instead, the turn-on of M_{aux1} excites large resonant overcurrents due to the temporarily high quality factor of the tank, similarly to what happens at the start-up. As shown in Fig. 4.19b, the simulated primary current peaks at approximately 81 A, around nine times its steady-state value. Despite the short duration of the event, such stresses can accelerate the degradation or even cause the failure of the SRC components.

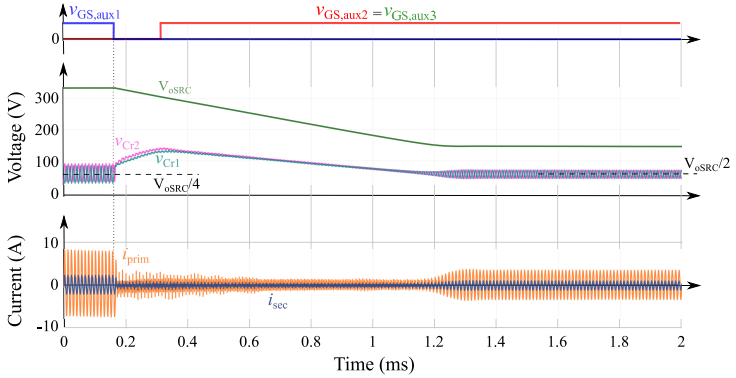
To alleviate this problem, a soft-transition algorithm is designed for the MV-to-LV transition: the duty cycle of the gate signal to M_{aux1} is gradually increased from 0% to 100%. Its frequency is twice the SRC switching frequency, to ensure the balance of the current stresses in the rectifier during the transition, as described in [182]. A representative example of the auxiliary gate signals is depicted in Fig. 4.20.

Cycle-skipping approach for light loads efficiency improvement

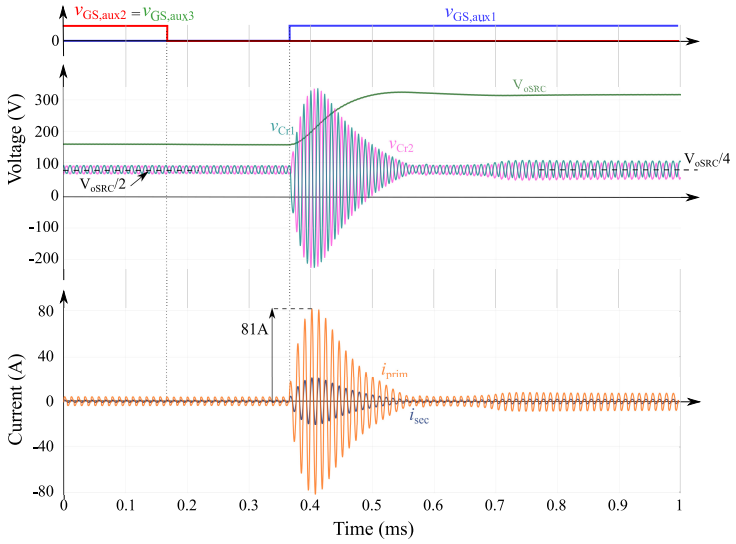
At light loads, the SRC efficiency is usually penalized by voltage- and frequency-dependent losses, such as the hysteresis losses in the magnetic core of the transformer and the gate-driving losses. Using a simplified approach, the magnetic hysteresis losses in a core subjected to a sinusoidal excitation can be modelled using the empirical Steinmetz equation [183]:

$$\rho_{\text{SE}} \propto f_{\text{sw}}^{\alpha_{\text{SE}}} \hat{B}^{\beta_{\text{SE}}} \tag{4.85}$$

where ρ_{SE} is the loss density in the magnetic material, $\hat{B}$ is the peak flux density, and α_{SE} and β_{SE} are material-dependent empirical parameters. More complex and generalized models derived from the Steinmetz model were later developed to include non sinusoidal and PWM excitations [184, 185].



(a)



(b)

Fig. 4.19 Simulated main voltage and current waveforms involved in the topology-morphing of the SRC rectifier: control voltages of the auxiliary MOSFETs M_{aux1}, M_{aux2} and M_{aux3}, resonant capacitors voltages and SRC output voltage V_{oSRC}, primary and secondary transformer currents. (a) Transition from the LV mode (VQR) to the MV mode (VDR). (b) Transition from the MV mode (VDR) to the LV mode (VQR).

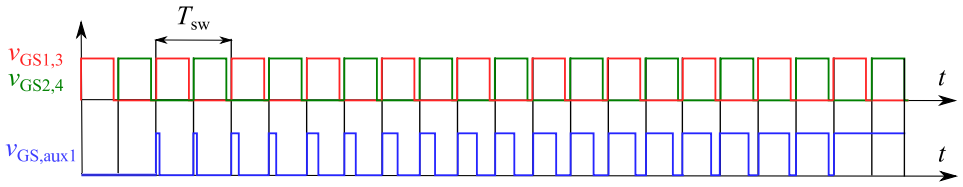


Fig. 4.20 Control signal waveforms for the full-bridge transistors M_{1-4} and the auxiliary MOSFET M_{aux1} during the soft transition from VDR to VQR.

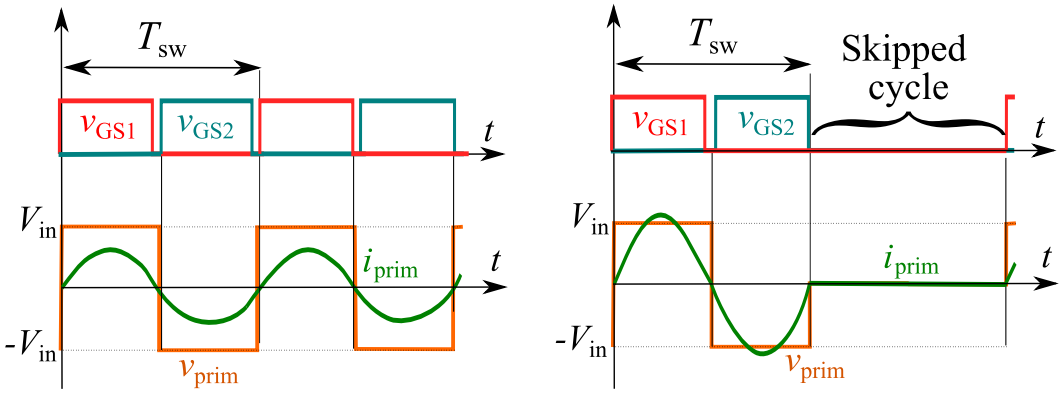


Fig. 4.21 Comparison of the qualitative waveforms of the control voltages of M_1 and M_2, and transformer primary current and voltage, with and without cycle skipping. (a) Rated frequency operation; (b) 1-cycle skipping.

On the other hand, by denoting as V_{CC} the supply voltage of a gate driver, and Q_G the total gate charge to be supplied for the complete turn on of a MOSFET, the gate driving losses can be estimated by:

$$P_{driving} = V_{CC} Q_G f_{sw} \,. \tag{4.86}$$

Eqs. (4.85) and (4.86) suggest that these contributions of loss do not scale with the load, and thus lead to a more significant impact at light loads. In a PV application, where lower irradiance conditions occur systematically within a day, the mitigation of the efficiency drop at reduced load conditions is crucial to ensure a satisfactory weighted efficiency.

Various techniques such as the cycle- or half-cycle skipping [90, 124] were introduced for this purpose: all of them are based on modifying the switching pattern so as to lower the effective switching frequency, resulting in a reduction of the

frequency-related losses. In this work, a preliminary experimental characterization was performed to determine the most effective technique between the half-cycle skipping and the one-cycle skipping in reducing the SRC losses at light loads. The results highlighted the better performance of the one-cycle skipping, consisting in generating the switching pulses only every two periods. Figs. 4.21a and 4.21b show the qualitative waveforms of the control voltages for the $M_1 - M_2$ leg of the full-bridge, and the transformer primary current and voltage, at the rated frequency operation and with the one-cycle skipping approach. At the rated 36.5 V voltage, the approach allows to save approximately 1.4 W at 5 % of the rated power, and approximately 1.25 W at 10 % of the rated power.

The physical implementation of the firmware on a microcontroller is presented in Section 4.5.2.

4.5 Experimental results

4.5.1 Schematic and layout design

The schematic and layout of the PCB prototype were designed in *Altium Designer*[5]. Fig. 4.22 shows an intuitive block diagram of the implemented schematic of the converter prototype which highlights its main domains, blocks and the main connections. As it can be seen, the schematic is composed of four sheets, devoted to the different sections of the converter. While this section only describes the functionality of the blocks in Fig. 4.22, the pictures of the full schematic sheets can be found in Appendix A.

Sheet 1 includes the part of the schematic devoted to the synchronous boost, including the power circuit (inductor, high- and low-side MOSFETs, output capacitor), the half-bridge gate driver (with a bootstrap network to implement the floating voltage supply for M_{HS}) and the ZCD circuit (for the correct implementation of the BCM).

In previous works, different implementations of the ZCD circuit were explored for synchronous boost or Power-Factor Correction (PFC) AC-DC converters: most of them are based on the acquisition of the current through a combination of a low bandwidth Hall-effect sensor and a high bandwidth current transformer [186], a sense resistor [187], a current transformer designed to be driven to saturation [188], a senseFET [189]. In the mentioned cases, the acquired signal is compared to a reference voltage to detect the transition instant through the zero. A sensorless approach is exploited in [190], where all the timing intervals of the BCM operation are computed on the basis of the input and output voltages, and the target load power, without sensing the inductor current. In this prototype, the implemented ZCD circuit consists of a 1 MHz Tunnel Magneto-Resistive (TMR) isolated current sensor followed by a high-speed comparator with propagation delays lower than 10 ns. The TMR sensor generates an output voltage proportional to the inductor current, which is then compared to its offset value to generate a digital signal corresponding to the polarity of i_{L}. The falling edge of this digital signal is supposed to be used as a trigger event by the digital controller to activate the negative current extension time, until i_{L} reaches I_{R}. For the purpose of the open-loop experimental characterization,

[5] https://www.altium.com/altium-designer (accessed Jan. 20th, 2026).

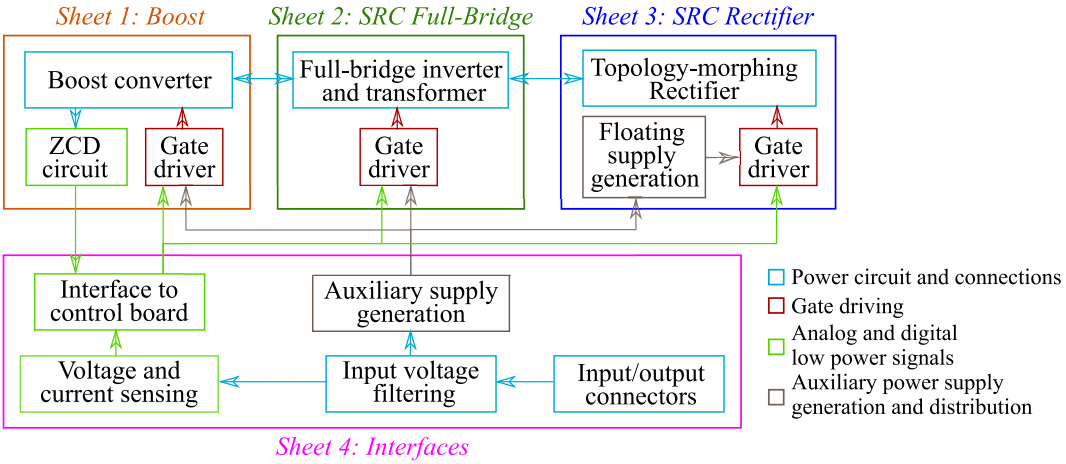


Fig. 4.22 Block diagram of the schematic of the converter prototype, highlighting the main blocks and connections, and the division into the four sheets in *Altium Designer*.

a similar approach to [190] was used, in which the timing intervals were computed offline according to the desired voltage gain and power, without recurring to the ZCD circuit.

Sheet 2 includes the part of the schematic related to the SRC full-bridge and transformer. The four MOSFETs of the full-bridge are driven by a gate driver with four independent channels. External gate resistors were added in series to the MOSFETs gates to limit the peak current sourced / sunk by the gate driver within its specified limits, reported in datasheet.

Sheet 3 is devoted to the topology-morphing rectifier of the SRC. The sheet includes the power circuit, as well as the three gate drivers required for the auxiliary MOSFETs and the auxiliary power supplies that generate the floating voltages.

Finally, *Sheet 4* includes the sections of the schematic devoted to the connections of the PCB with the external source and load, the interface with the control board, to the analog sensing circuits to acquire the input voltage and current and the output voltage, to the input DC filtering capacitors, and to the generation of the auxiliary power supply for the full-bridge and boost gate drivers.

A PCB prototype was designed on the basis of the schematics presented so far. A four-layer stack-up was selected to gain a greater flexibility in the components placement and signals routing. The size of the resulting PCB is 240 mm by 154 mm, with 1.6 mm thickness. It is important to say that the maximization of the power

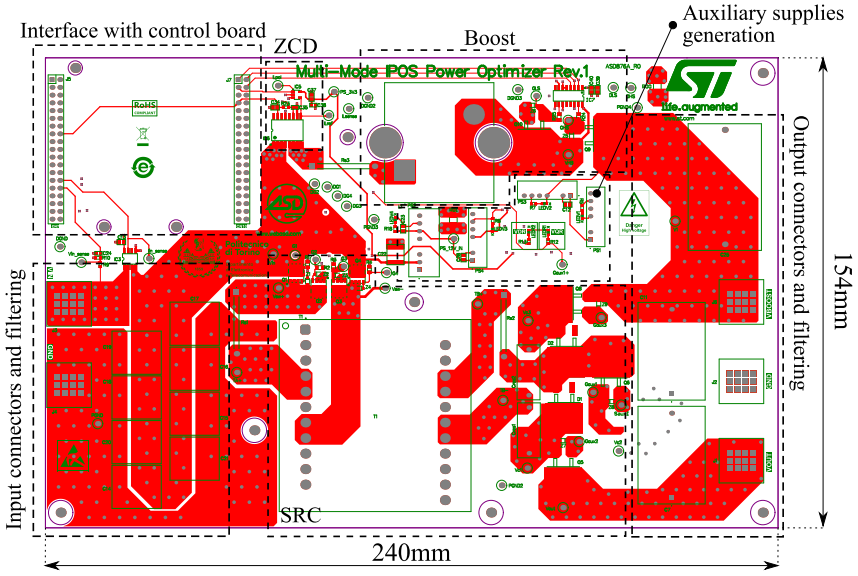


Fig. 4.23 Layout of the top layer of the PCB prototype.

density was out of the scope of this proof of concept. Due to the novelty of the converter topology, the primary goals of the layout design were to ensure its correct operation and high performances, while offering the possibility of monitoring the main currents and voltages through testpoints and shunt resistors. In general, the layout design focused on minimizing the resistive and inductive parasitics of the traces, by optimizing the components placement and tuning the traces widths. Specific attention was devoted to the gate drivers, due to the dangerous impact that parasitic inductances may have on the driven transistors due to overvoltages and ringing: the length of the gate and source traces was minimized to reduce the loop inductances as much as possible.

Fig. 4.23 shows the top-layer view of the PCB, highlighting the areas of the top layer devoted to each main part of the schematic. On the upper left corner of the board, the two headers ensure the connection with the NUCLEO development board. The SRC is located in the lower part of the PCB, while the boost components are located in the upper right one. Surface-Mount Devices (SMD) were selected for most of the semiconductor and capacitive components, while the transformer, boost inductor and output film capacitors exhibit through-hole packages. Most of the components of the converter are soldered on the top layer.

Fig. 4.24 illustrates the first of the two inner layers of the PCB, devoted primarily to the routing of low power signals and supply traces which could not fit on the top

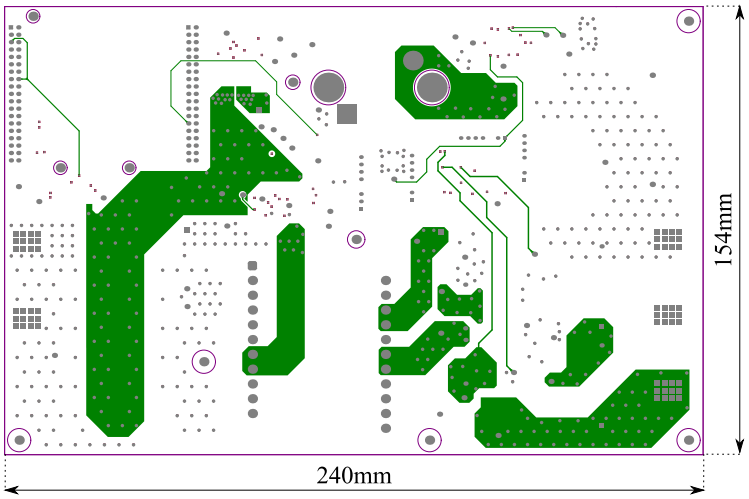


Fig. 4.24 Layout of the first inner layer of the PCB prototype.

layer. To enhance the heat dissipation on the largest copper area possible, some high current traces / planes of the top layer are connected through uniformly distributed thermal vias to equal copper planes located in this inner layer. The same approach is also exploited in the bottom layer, where the copper areas can exchange more effectively the dissipated heat with the air. In addition, this approach allows to distribute on a larger conductive area the current, leading to a reduction of the equivalent trace resistance.

Fig. 4.25 shows the layout of the second inner layer, which is entirely occupied by the ground planes, beside in correspondence of the two magnetic components of the converter, the boost inductor and SRC transformer. As anticipated the digital ground plane, developed in the upper and left part of the layout, is electrically connected to the power ground of the converter, extended through the remaining surface area. The maximization of the ground plane allows to minimize the loop inductances introduced by the return paths of the converter.

Finally, Fig. 4.26 shows the layout of the bottom layer, devoted to the placement of the SRC gate drivers and voltage partition networks on the input and output voltages. As for the first inner layer, reinforced copper traces and planes were located in the bottom layer to improve the thermal and electrical performance of the high current paths.

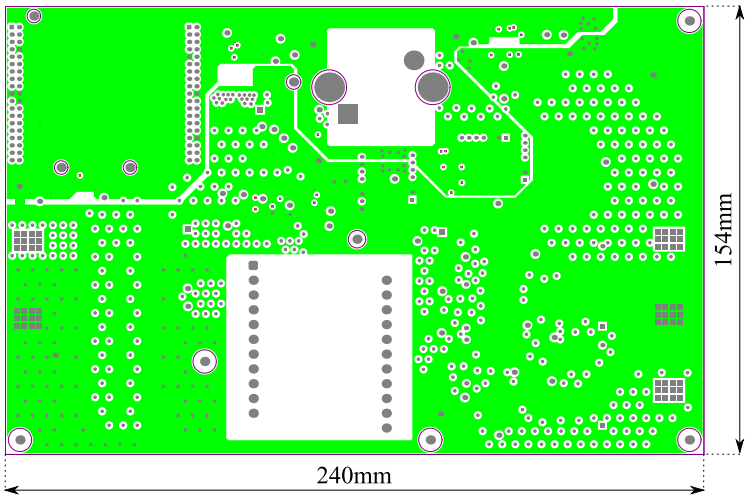


Fig. 4.25 Layout of the inner ground layer of the PCB prototype.

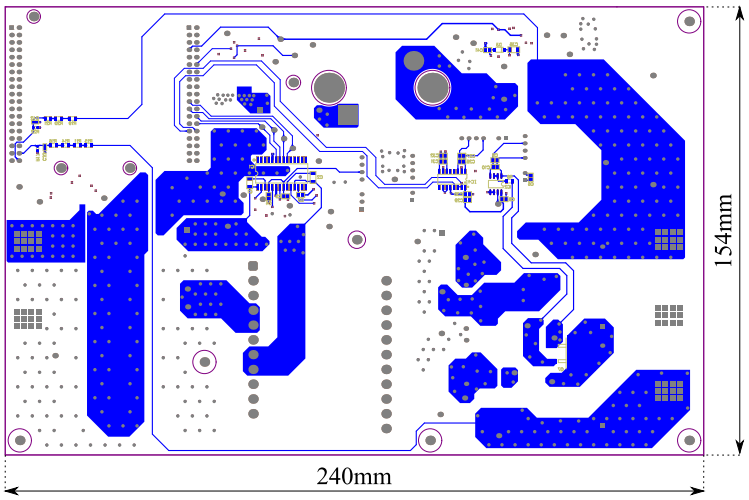


Fig. 4.26 Layout of the bottom layer of the PCB prototype.

The layout design and components placement was commissioned to an external company, *ASD*[6]. A picture of the PCB prototype with the bill of materials in Tab. 4.11 is shown in Fig. 4.27.

[6]https://www.webasd.com/

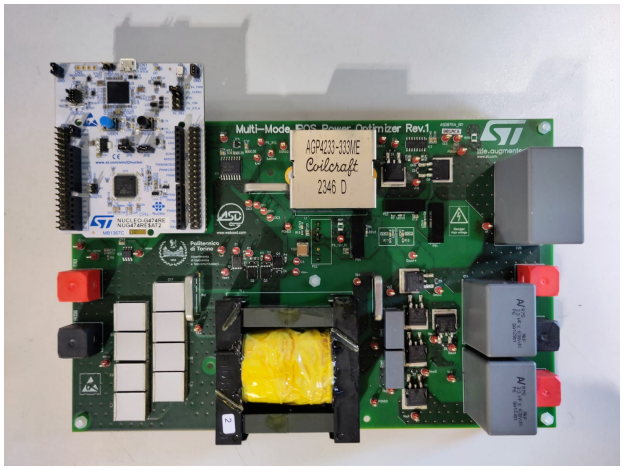


Fig. 4.27 PCB prototype of the proposed converter.

4.5.2 Microcontroller implementation

A development board, STMicroelectronics NUCLEO-G474RE[7] was selected for the implementation of the open loop control: the adoption of a development board significantly simplifies the hardware design, since the auxiliary circuits to burn the firmware, to supply the microcontroller and to interface it to external systems are integrated in an already optimized and compact board. This solution is suitable to test a proof of concept in which the design focus is not the maximization of the power density. The development board includes a STM32G474RE microcontroller[8], a high performance microcontroller equipped with a Arm Cortex-M4 32-bit RISC core, a 512 kB Flash memory, and 128 kB SRAM. The main peripherals used for the targeted applications are the four 12-bit ADC channels, used to acquire the analog signals from the voltage and current sensors of the converter, and the high-resolution timer (HRTIM), characterized by a maximum 184 ps resolution, used for the generation of the PWM signals for the full-bridge and boost MOSFETs.

The microcontroller was programmed by using the Integrated Design Environment (IDE) specifically developed for STM32 microcontrollers, STM32CubeIDE[9]. The IDE allows to speed up the microcontroller programming by integrating in a unique environment the peripherals configuration platform, the libraries of macros

[7]https://www.st.com/en/evaluation-tools/nucleo-g474re.html (accessed Jan. 21, 2026).

[8]https://www.st.com/en/microcontrollers-microprocessors/stm32g474re.html (accessed Jan. 21, 2026).

[9]https://www.st.com/en/development-tools/stm32cubeide.html (accessed Jan. 21, 2026).

and the debugging feature, and is compliant with multiple operating systems. At the beginning of a new project, the software allows to select the target microcontroller and configure its peripherals from the STM32CubeMX. It is also possible to start from one of many example projects already available to use.

Fig. 4.28 shows the pinout view of the target microcontroller in STM32CubeMX environment. The used pins are coloured green: some of them are reserved to the connection with the external oscillators (the pins denoted by *RCC_OSC*) and to the connection with the programmer and debugger ST-link through UART protocol. The other green pins are free to be configured with high flexibility. More specifically:

- the input pins *Vin*, *Iin*, *Vb* and *Vout* collect the analog signals coming from the analog sensors of V_{in}, I_{in}, V_{ob} and V_{out}, respectively; these input voltage and current signals are converted by 12-bits ADC and used to generated the PWM signals in a closed-loop controller, whereas the other two signals are monitored for overvoltage protection purposes;
- the output pins *G1*, *G2*, *G3*, *G4* are used to drive the full-bridge MOSFETs and are connected to four synchronized channels of the HRTIM;
- the output pins *GLS* and *GHS* are used to drive the boost MOSFETs and are connected to two synchronized channels of the HRTIM;
- the GPIO output pins *Gaux1* and *Gaux2* are used to drive the auxiliary MOSFETs of the topology-morphing rectifier;
- the GPIO input pin *iLpol* collects the digital signal generated by the ZCD network, to be used for the implementation of the variable frequency BCM.

In the open-loop controller designed to characterize the converter performances, only the *Vout* analog signal is actually monitored to provide a safe overvoltage protection. The *iLpol* is also not considered in this first session of tests, since the switching frequency and pulse-width of the boost signals are calculated off-line for each working point using the control equations defined previously.

The HRTIM channels work as Finite-State Machines (FSM), in which the output signal, high or low, is controlled according to the instantaneous comparison of a 16-bit counter and up to four values stored in compare registers. These registers can be designed to store the count numbers associated to the timing of the edges of the

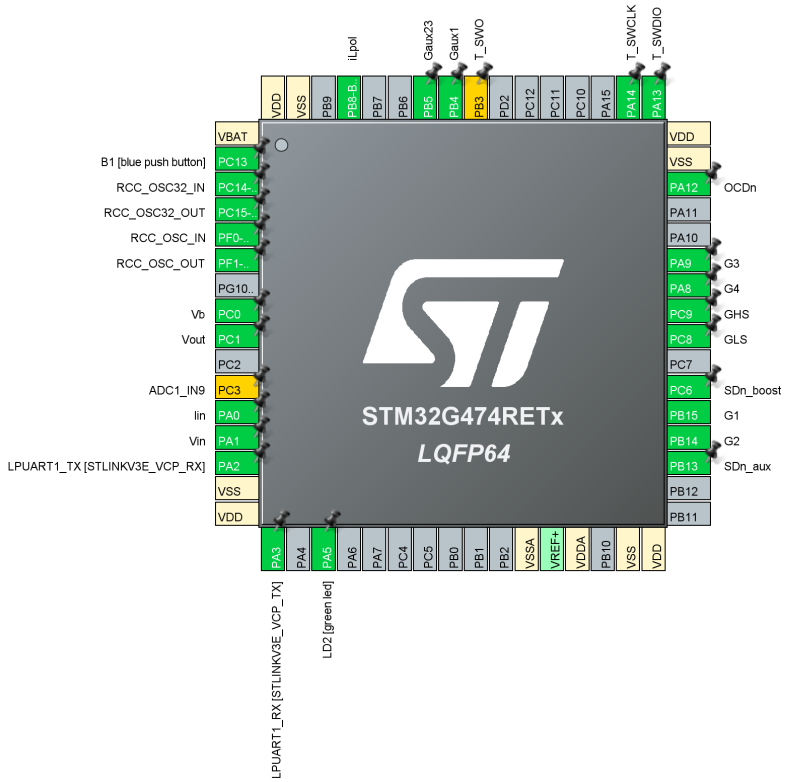


Fig. 4.28 Pinout view of the target microcontroller in STM32CubeMX environment.

PWM signals: in this way, four compare registers can be used to generate two PWM signals for a half-bridge. The counter frequency, denoted by f_{cnt} can be increased compared to the base core frequency, 170 MHz, up to 5.44 GHz. The counter reset can be set to a proper value N_{period} that allows to realize the desired switching period T_{sw}:

$$N_{\text{period}} = f_{\text{cnt}} \cdot T_{\text{sw}} \,. \tag{4.87}$$

More in general, each compare register is programmed to store a 16-bit number N_x associated to the time instant T_x at which it is desired to force a transition of a PWM signal, according to the formula:

$$N_x = f_{\text{cnt}} \cdot T_x \,. \tag{4.88}$$

STM32CubeIDE allows to configure the output channels of the HRTIM to be set and reset in correspondence of the compare values N_x.

When the initial configuration of the peripherals is complete, the IDE generates a template of the *main* file, already including the library import for the specific microcontroller, and the lines of code associated to the initial configuration performed in the Graphical User Interface (GUI). The microcontroller was programmed in C by using the Hardware Abstraction Layer (HAL) macros, higher level and intuitive macros that allow to easily act on the peripherals registers without a detailed knowledge of their address in memory and the role of each single bit.

Without entering the details of the code, the *main* is structured into four main parts:

- an initial part including the definition of variables and constants, and the initial configuration of the peripherals. The constant signals to control the conduction state of the auxiliary MOSFETs of the rectifier are set in this phase according to the voltage of the target working condition;
- a soft-startup phase in which the pulse-width of the boost gate signals is progressively increased, in order to charge gradually the output capacitance C_b to the desired steady-state value. During this phase, the full-bridge gate signals are kept off;
- a soft-startup phase for the full-bridge, in which the phase shift Φ between the legs of the full-bridge is gradually decreased from 180° to the final steady state value (0° is case of LV or MV modes, a different positive Φ in case of HV mode). As anticipated, the soft-startup approaches allow to limit significantly the impact of the initial inrush currents that may damage the converter components.
- the infinite loop of the *main* is actually empty, since there is no implemented closed-loop control in this test phase. Both the MPPT control and the input voltage regulation should update the control variables here, in a practical PV application.

Outside the *main* function, two Interrupt Service Routines (ISR) are defined: one is triggered periodically by another timer and is responsible to monitor V_out by reading the corresponding ADC value and comparing it with a maximum tolerated voltage, 380 V; the other is triggered asynchronously by pressing the user button *B1* and interrupts the generation of the PWM signals.

4.5.3 Experimental waveforms

The experimental tests, as mentioned, were primarily aimed at characterizing the performances of the converter and the effectiveness of its operating principle across the three operating ranges. As such, the experimental setup included:

- a programmable 1000 V/30 A DC power supply, EA-PSI 91000-30[10], compliant with the voltage and current specifications of the target PV panel;
- a programmable bidirectional 1000 V/$\pm$30 A power supply EA-PSB 9500-30[11], used as a constant current sink at the output of the converter;
- a 2-channel power analyzer, Zes Zimmer LMG500-2[12], to characterize the efficiency of the converter;
- a 4-channel, 12-bit, 1 GHz digital oscilloscope, Teledyne HDO6000B[13], to monitor and acquire the converter waveforms.

In this section, the main experimental waveforms of the SRC and boost converters are reported to validate the correct operation of the proposed PPO in its three operating regions, at steady state. The SRC waveforms include the control and output voltages of MOSFET M_2, namely v_{GS2} and v_{DS2}, and the voltage and current at the primary side of the transformer, namely v_{prim} and i_{prim}. For the boost, the waveforms include the control voltages of the low-side and high-side transistors, namely $v_{GS,LS}$ and $v_{GS,HS}$, the switching node voltage v_{sw} (which also coincides with the drain-source voltage of M_{LS}) and the inductor current i_L.

In the final part of this section, exploiting the soft-transition algorithm presented before, the main waveforms of the SRC are presented during the MV-LV and LV-MV modes transitions, to validate the effectiveness of the algorithm in reducing the transient current stresses.

[10] https://elektroautomatik.com/shop/en/products/programmable-dc-laboratory-power-supplies/discontinued-series/series-psi-9000-3u-br-3.3kw-up-to-15kw/445/laboratory-power-supply-0..1000v/0..30a

[11] https://elektroautomatik.com/shop/en/products/programmable-dc-laboratory-power-supplies/discontinued-series/bidirectional-dc-laboratory-power-supplies-psb-9000-3u/819/bi-directional-power-supply?c=2602

[12] https://www.zes.com/en/Products/Predecessor-Products/Energy-and-Power-Meters/LMG500

[13] https://it.teledynelecroy.com/oscilloscope/hdo6000.aspx

LV mode

Fig. 4.29 shows the main experimental waveforms of the SRC and boost in a working point belonging to the LV mode, namely $V_{\text{in}} = 20\,\text{V}$ and $P_{\text{out}} = 300\,\text{W}$.

The SRC waveforms in Fig. 4.29a show a near-ZVS of M_2, highlighting that the primary current is insufficient to completely discharge its output capacitance during the deadtime. As it can be seen, i_{prim} experiences a temporary linear rise / fall immediately after the full-bridge legs switching, which is not predicted by the theoretical waveforms in Figs. 4.6 and 4.8. The main consequence is that the switching period must be shortened to ensure the desired primary current when the full-bridge transistors switch. This behaviour, observed also in [127], is linked to the non-instantaneous switch of the rectifier diodes, while the presented analysis assumed ideal components [191].

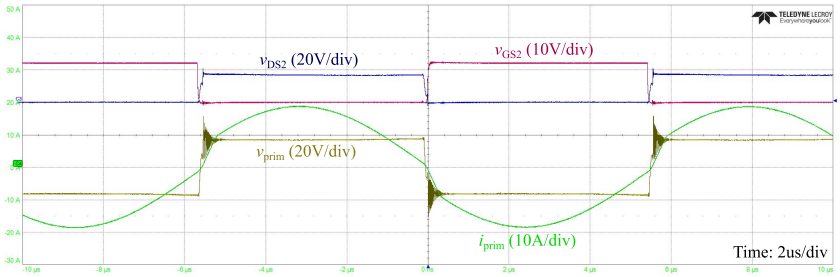
The boost waveforms in Fig. 4.29b show the typical triangular inductor current of a variable-frequency BCM. The negative current extension (in the example, $I_{\text{R}} = -500\,\text{mA}$ allows to achieve a full ZVS turn on of the low-side MOSFET, as desired. Both transistors, thus, turn on with minimized switching losses.

MV mode

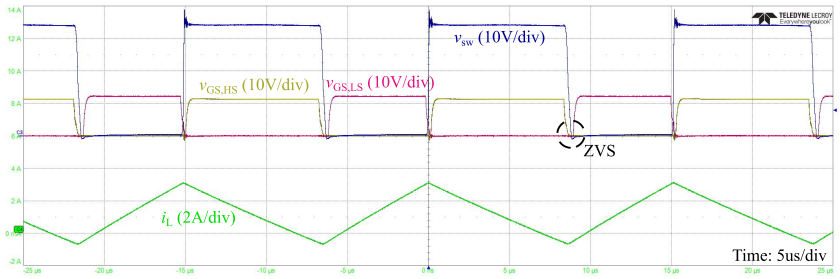
Fig. 4.30 shows the main experimental waveforms of the SRC and boost in a working point belonging to the MV mode, namely $V_{\text{in}} = 36.5\,\text{V}$ and $P_{\text{out}} = 300\,\text{W}$.

Also in this case, the SRC waveforms in Fig. 4.30a show a near-ZVS turn on of M_2, and the impact of the rectifier parasitic capacitances on the primary current shape. Notice that, although the operating power in the circuit is the same, the peak primary current in the MV mode is halved compared to Fig. 4.29a. Due to the increased gain of the SRC, indeed, more severe current stresses are expected in all its components in the LV mode.

The boost waveforms in Fig. 4.30b show that, also in this case, with $I_{\text{R}} = -500\,\text{mA}$, the negative current extension time allows to achieve a full ZVS turn on of the low-side transistor.



(a)



(b)

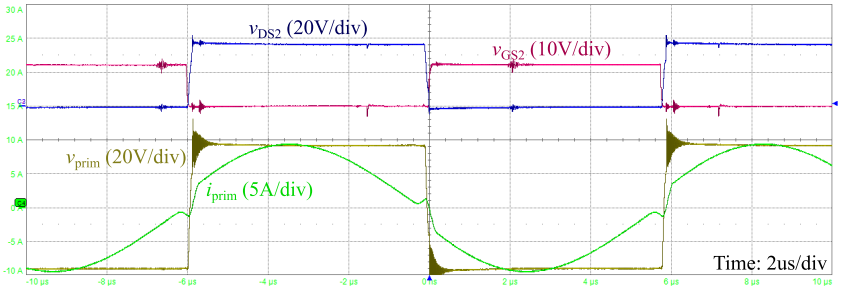
Fig. 4.29 Main SRC and boost waveforms in the LV mode: $V_{in} = 20\,V$, $P_{out} = 300\,W$: (a) SRC waveforms (v_{GS2}, v_{DS2}, v_{prim} and i_{prim}); (b) boost waveforms ($v_{GS,LS}$, $v_{GS,HS}$, v_{sw} and i_L).

HV mode

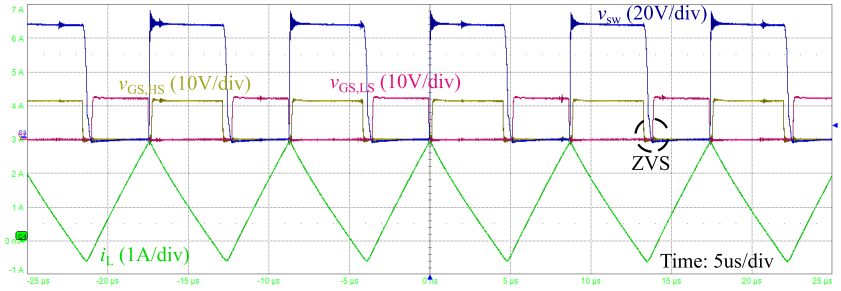
Fig. 4.31 shows the main experimental waveforms of the SRC and boost in a working point belonging to the MV mode, namely $V_{in} = 43\,V$ and $P_{out} = 300\,W$, where the boost is kept off and the PSM is exploited to achieve the correct total gain.

The SRC waveforms in Fig. 4.31a show that the $\Phi = 70°$ phase shift induces a discontinuous current operation, which forbids the achievement of the ZVS turn on condition for M_2. In addition, it introduces higher order harmonics in the transformer current that increase its winding losses.

Fig. 4.31b shows the boost waveforms in the off state. In all the working points of the HV mode, both the inductor and the body diode of the high-side transistor conduct the DC output current I_{out}. The conduction losses in these two components are the only loss contributions in the boost.



(a)



(b)

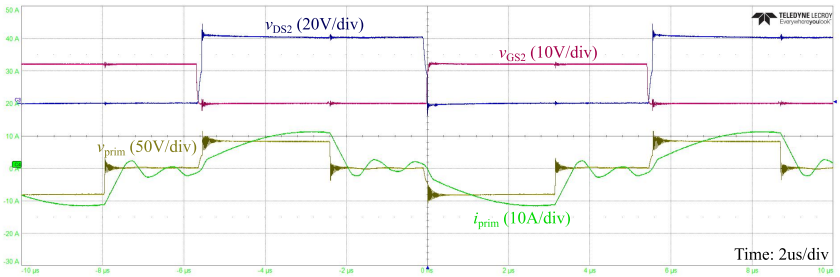
Fig. 4.30 Main SRC and boost waveforms in the MV mode: $V_{in} = 36.5\,V$, $P_{out} = 300\,W$: (a) SRC waveforms (v_{GS2}, v_{DS2}, v_{prim} and i_{prim}); (b) boost waveforms ($v_{GS,LS}$, $v_{GS,HS}$, v_{sw} and i_L).

LV-MV transients

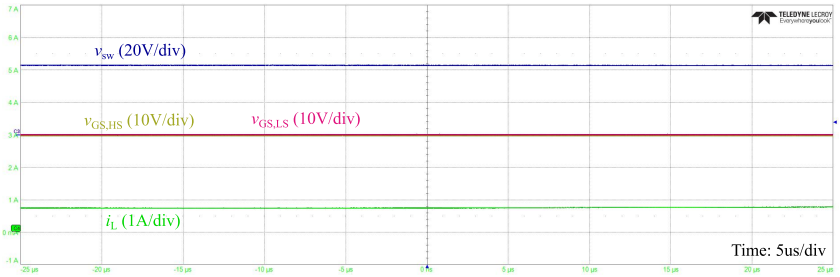
Fig. 4.32 shows the main experimental waveforms of the SRC involved in the transition between LV and MV, in the same working point previously simulated and described in Fig. 4.19, namely $V_{in} = 20\,V$, $P_{out} = 100\,W$. The experimental waveforms refer to the primary transformer current i_{prim}, the output voltage of the SRC V_{oSRC}, and the control signals of the auxiliary MOSFETs $v_{GS,aux1-2}$.

More specifically, Fig. 4.32a illustrates the transient from the LV to the MV mode, in which the rectifier topology morphs from VQR to VDR. As previously described and proven experimentally, a smooth discharge of the SRC output capacitors is enabled when M_{aux1} is turned off, during which the resonant current is damped. No overcurrent is experienced during the mode transition.

On the other hand, Fig. 4.32b shows the transient from the MV to LV mode, in which the rectifier topology morphs from VDR to VQR. In this case, to avoid the dangerous overcurrents observed in Fig. 4.19a, the control signal $v_{GS,aux1}$ gradually increases its duty cycle from 0 % to 100 %, according to the described soft-transition



(a)



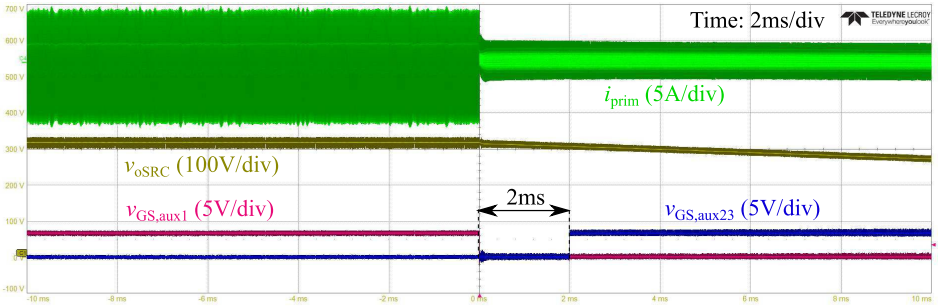
(b)

Fig. 4.31 Main SRC and boost waveforms in the LV mode: $V_{in} = 43\,V$, $P_{out} = 300\,W$: (a) SRC waveforms (v_{GS2}, v_{DS2}, v_{prim} and i_{prim}); (b) boost waveforms ($v_{GS,LS}$, $v_{GS,HS}$, v_{sw} and i_L).

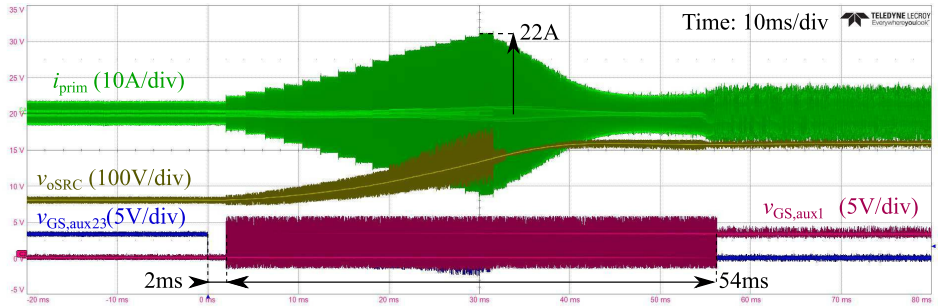
approach. Its successful implementation allows to limit the peak resonant current at 22 A, compliant with the steady-state peak primary currents observed in other working points. In this specific implementation of the soft-transition algorihtm, the control signal takes $\approx 54\,ms$ to stabilize at the "high" value, during which the MPPT controller should not update the reference voltage. A further model-based optimization of the algorithm could be investigated in the future to speed up the transient while still ensuring a safe topology-morphing.

4.5.4 Efficiency characterization

The efficiency of the converter was characterized in open-loop, in a quasi-static way, by modifying at any test the control variables to achieve the correct voltage gain at the desired transferred power condition. This approach allowed to validate the static gain equations and focus the attention on the steady-state performances of the converter prototype.



(a)



(b)

Fig. 4.32 Experimental waveforms of the primary side transformer current i_{prim}, the output voltage of the SRC V_{oSRC}, and control signals of the auxiliary MOSFETs $v_{GS,aux1-2}$, during the mode transitions between LV and MV modes, at $V_{in} = 20\,V$ and $P_{out} = 100\,W$: (a) Transition from LV to MV mode; (b) Transition from MV to LV mode.

Fig. 4.33 shows the converter efficiency at the input voltage $V_{in} = V_{th}^{+} = 39\,V$, the input voltage at which, by design choice, the efficiency peak is expected, since the boost realizes a minimum voltage gain close to 1, while the SRC still operates at resonance. The efficiency is characterized at constant input voltage and varying output power, at the power steps required to compute the EURO and CEC efficiencies. The x-axis is normalized to the rated 700 W power. As anticipated, the one-cycle skipping technique was implemented to improve the part-load efficiency at 5 % and 10 % of the rated power (continuous line): the experimental results show an efficiency improvement of around 2.5 % and 1.2 % at the two working powers, respectively, validating the effectiveness of this method. The measured EURO efficiency at this voltage is 96.81 %, while the CEC efficiency is 97.15 %. In general, the converter exhibits an efficiency $> 96\,\%$ between the 20 % and 100 % of the rated power, with a 97.8 % peak at 50 %. The limited efficiency drop is justified by the fact that most of the power is processed by the SRC, whereas PWM converters usually exhibit a

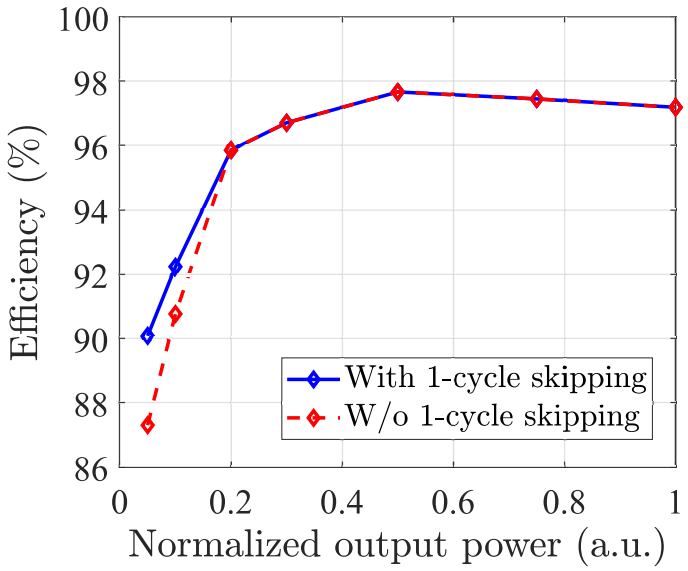


Fig. 4.33 Converter efficiency VS normalized output power, at 39 V.

significant efficiency drop at heavier loads [75, 104].

Fig. 4.34 shows the behaviour of the converter efficiency as a function of the input voltage in the proposed MPPT range, at two illustrative power levels, namely 200 W and 400 W. It is important to highlight that, differently from the previous case, the characterization of the efficiency vs input voltage is an artificial and indirect way to characterize the performance of a PV-fed converter under variable shading and temperature scenarios. During a real-life application, indeed, the MPPT controller will force the converter to span the PV curve on variable power working points: however, due to the difficulty to find a universal figure of metrics to quantify the wide-range performance of a converter, this approach is commonly adopted in the literature [95, 91, 63]. To the author's knowledge, a single work identified a custom power profile to reproduce a more realistic PV curve in which to test the proposed converter [90].

As shown in Fig. 4.34, the efficiency curve is always maintained above 90 % in the entire range. Considering the characteristic bell-shaped power-voltage curve of a PV module, the higher power level 400 W was tested only on a restricted MPPT range, 33 V–45 V. This range is sufficient to highlight that the peak efficiencies are obtained in the neighborhood of the rated voltage, and decrease moving away from

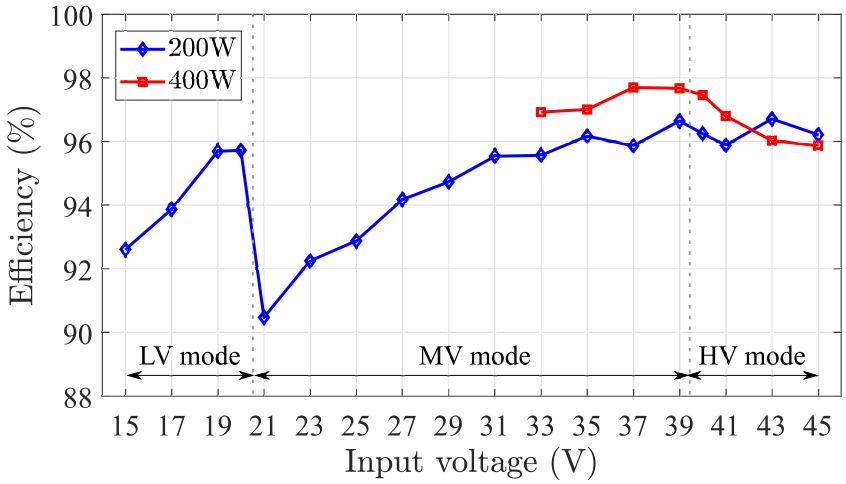


Fig. 4.34 Converter efficiency VS input voltage, at two representative power levels (200 W and 400 W).

it: in the MV mode, the efficiency drop is due to the increased power processed by the boost, while in the HV mode due to the increased current stresses related to the PSM. The efficiency curve characterized at 200 W power allows to appreciate the correlation between the converter performance and the fraction of power processed by the boost: as expected, the efficiency exhibits local maxima when the boost gain (and power) is minimum, and viceversa.

Fig. 4.35 shows the loss breakdown of the converter at three representative working points in the different operating modes, coherent with some of the tested working points of Fig. 4.34. Due to the difficulty of characteristing the loss breakdown experimentally, the results refer to simulations performed in Simetrix[14] using the SPICE models of the components used in the prototype, available in Tab. 4.11. The transformer was modelled through an equivalent parallel resistance for the core losses, while the AC winding resistances was estimated using Tourkhani's model [192] applied on the winding geometry, arrangement and the type of Litz wire adopted for the transformer prototype.

At $V_{in} = 36.5\,V / P_{out} = 400\,W$ (MV mode), the boost processes a low fraction of the input power ($\approx 16.6\,\%$), resulting in a high converter efficiency. The transformer and diodes represent the main sources of losses. At $V_{in} = 17\,V / P_{out} = 200\,W$ (LV

[14] https://www.simetrix.co.uk/.

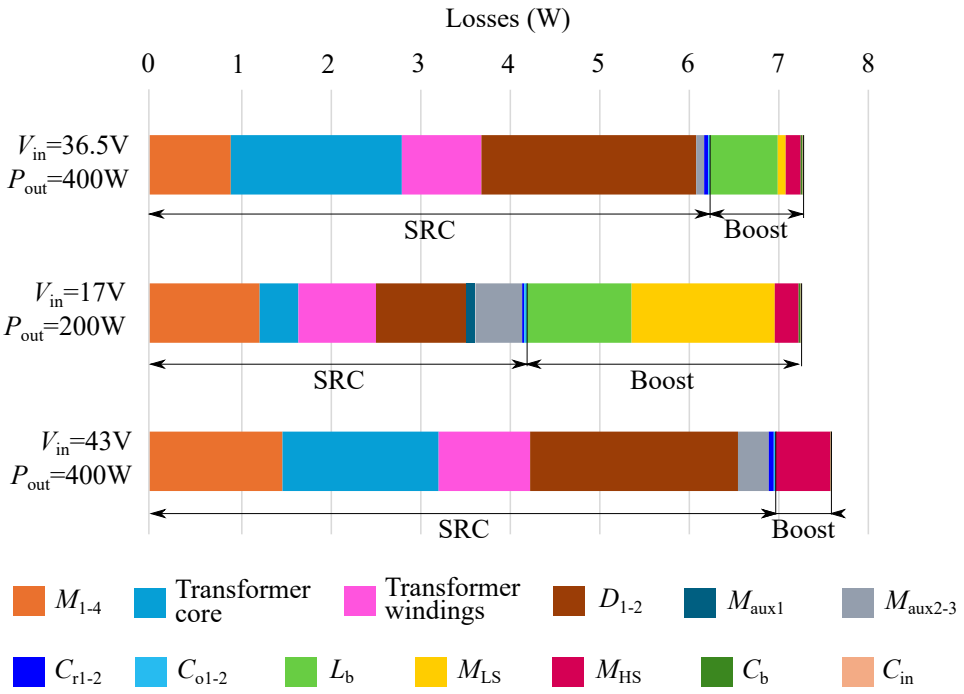


Fig. 4.35 Simulated loss breakdown of the converter at three representative working points: $V_{in} = 36.5\,V/P_{out} = 400\,W$ (MV mode), $V_{in} = 17\,V/P_{out} = 200\,W$ (LV mode), and $V_{in} = 43\,V/P_{out} = 400\,W$ (HV mode).

mode), despite the halved operating power, the VQR doubles the current stresses at the primary side of the transformer compared to a VDR, resulting in increased conduction losses in the full-bridge MOSFETs and in the transformer windings. The boost gain increases to ≈ 4.6, resulting in more significant losses in the inductor and low-side MOSFET. The auxiliary MOSFETs of the rectifier impact more in the VQR rather than in the VDR, due to the continuous conduction of M_{aux1} and the alternate conduction through the body diodes of M_{aux2} and M_{aux3}. At $V_{in} = 43\,V/P_{out} = 400\,W$ (HV mode), the only relevant loss contribution of the boost is the high-side MOSFET, which conducts a continuous current through its body diode. For the same power, increased conduction losses are measured in the full-bridge MOSFETs and transformer windings, due to the PSM that introduce higher order harmonics compared to the resonant operation. In this case as well, the rectifier diodes and the transformer exhibit the major contributions to the converter losses.

4.5.5 Comparison with the state of the art

Given the experimental results presented above, it is relevant now to compare the features and performance of the proposed converter solution with the state of the art: more specifically, this section tries to extract general observations from the comparison of multiple works based on different conversion techniques, with the goal of highlighting limitations and advantages.

Tab. 4.12 compares the proposed converter with other power optimizers exhibiting similar specifications. The converters are compared based on the step-up technique, number of components, rated power, peak and CEC efficiencies at the rated voltage, and performance on the target MPPT range.

Multiple considerations can be done:

- the PWM converters based on voltage multipliers and / or switched capacitors [110, 75] suffer of a high number of passive components. Nevertheless, they allow to achieve high peak efficiencies at the rated voltage, but are designed to operate on a relatively narrow MPPT range (25 V–40 V);
- the multi-mode converters in [89, 90, 95] and the proposed one are designed to operate on the widest voltage ranges: with a 3:1 ratio between the upper and lower boundaries, the proposed converter operates on the second widest MPPT range after [90];
- the asymmetric IPOS solutions [126–128] employ more switches and at least two magnetic components, due to the two stages. Among these, the proposed converter achieves the highest peak efficiency 97.8 %, 2.5 % more than [126], and, at the same time, the widest voltage range.

In order to provide a more comprehensive benchmarking, the scatter plots presented in Chapter 3 are here reported again, with the addition of the figures of merit of the proposed converter. Fig. 4.36a considers the measured CEC efficiency (at the rated voltage) and gain range of several converters analyzed in the literature review, while Fig. 4.36b considers the rated power and gain range, as figures of merit of the wide-range operation. The plots highlight that the multi-mode proposed IPOS converter is aligned with the best performing state of the art solutions in terms of weighted efficiency and extension of voltage gain. Its rated power, 700 W, is among

Table 4.12 Comparison of the proposed power optimizer with other state of the art solutions. Legend: VM (Voltage Multipliers), SC (Switched Capacitors), MM (Multi-mode), MS (Multi-stage), A-IPOS (Asymmetric IPOS), TM (Topology-morphing), SRC (Series Resonant Converter), L (inductor), CL (coupled inductors), T (Transformer).

Reference	[110]	[75]	[89]	[90]	[95]	[124]	[126]	[127]	[128]	Proposed
Step-up technique	VM	VM, SC	MM SRC	MM SRC	TM LLC	Cascaded MS	A-IPOS	A-IPOS	A-IPOS	MM A-IPOS
Isolation	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
Number of switches	4	1	5	5	6	6	6	6	6	9
Number of diodes	7	8	2	2	7	2	2	2	4	2
Number of magnetic components	6 L	1 CL	1 T	1 T, 1 CL	1 T	1 T, 1 L	1 T, 1 L	1 T, 1 L	2 T, 1 L	1 T, 1 L
Number of capacitors	9	8	4	5	8	4	6	3	11	6
Rated power	1 kW	200 W	300 W	300 W	300 W	250 W	200 W	250 W	400 W	700 W
Peak efficiency at rated voltage	97.9 %	97.1 %	97.9 %	97.4 %	95.6 %	96.3 %	95.3 %	95.0 %	94.0 %	97.8 %
CEC efficiency at rated voltage	97.45 %	N/A	97.50 %	96.80 %	N/A	95.5 %	N/A	N/A	N/A	97.15 %
Input voltage range	25 V – 40 V	25 V – 40 V	22 V – 36 V	10 V – 60 V	20 V – 50 V	20 V – 45 V	32 V – 40 V	24 V – 37 V	24 V – 44 V	15 V – 45 V
Output voltage	400 V	400 V	315 V	400 V	500 V	400 V	400 V	240 V	400 V	350 V
Min / max efficiency in the voltage range	97.2% – 97.9%	92.7% – 95%	95.5% – 97.5%	79% – 97.4%	94.5% – 95.5%	95.0% – 97.0%	94.7% – 95.3%	92.3% – 95.0%	92.0% – 94.0%	90.5% – 96.7%

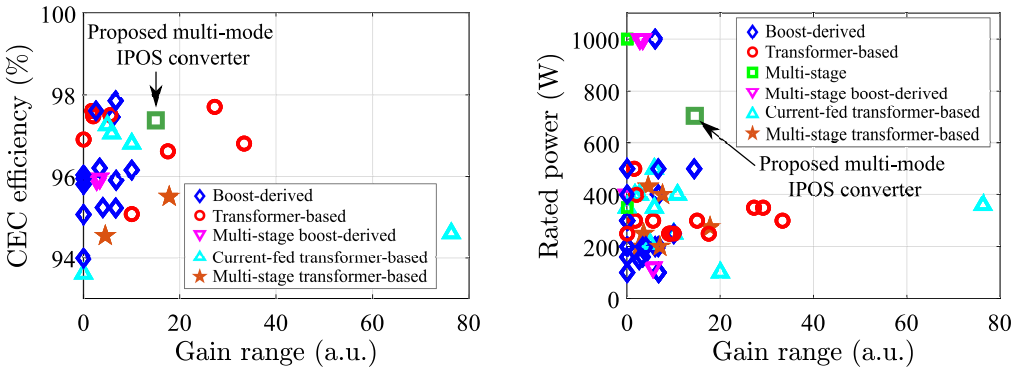


Fig. 4.36 Scatter plots of some relevant figures of merit for the proposed multi-mode IPOS converter and the state-of-the-art topologies (a) CEC efficiency and gain range; (b) Rated power and gain range.

the highest among the considered converters, which, in most cases, are designed for 60-cell, 300 W–400 W monofacial Silicon PV modules, widespread commercial solutions. The proposed converter, on the other hand, was designed to be compliant also to the most advanced and recent heterojunction bifacial PV modules, exhibiting superior conversion efficiencies and up to 700 W power at STC.

4.6 Conclusions

This chapter has introduced a new converter topology for wide-range PPO applications. From the identification of the main desirable features of power converters designed for the target application, a preliminary simulation-based comparison of different multi-stage topologies was presented, highlighting the promising benefits of the asymmetric IPOS architecture to improve the converter efficiency through an optimal power splitting between two stages.

The identified promising asymmetric IPOS topology, consisting of a fixed-gain LLC and a conventional two-level boost, was further refined by including a topology-morphing rectifier, to extend the target MPPT range while relaxing the design constraints on the boost. The topology was optimized for the highest efficiency possible on a target input voltage and power range, compliant with a commercial PV module. For this reason, the LLC was modified into a SRC operating at resonance, and a synchronous boost was adopted, operating in the BCM to improve the switching performance of its MOSFETs. A multi-mode control approach, based on the topology-morphing rectifier and on the switching scheme of the SRC full-bridge, was designed to effectively operate in the wide proposed input voltage range.

In general, the proposed converter shares with the multi-mode converters the possibility to operate on a wide MPPT range, while optimizing the power splitting between the two IPOS-connected stages to achieve a high peak and weighted efficiency at a desired rated voltage. The IPOS architecture improves the design flexibility of the converter, allowing to simultaneously and independently optimize the SRC and boost stages.

A prototype was designed, built and tested on the entire voltage range and up to the rated power. The open-loop testing was aimed at validating the multi-mode converter operation and characterize its efficiency on many working points. A particular attention was devoted to the analysis and implementation of a soft mode transition algorithm, to ensure a reliable transient operation of the converter when it is supposed to switch between two modes. The converter prototype exhibits a measured CEC efficiency of 97.15 %, one of the highest performances at the rated voltage among similar works of the state of the art. At the same time, the characterization over the wide 15 V–45 V input voltage range determined a high efficiency above 90.5%%, peaking in the neighborhood of the rated voltage.

The proposed solution was introduced to be a valid and credible alternative for PPO applications, thanks to its inherent features. The integration of multiple design approaches was proved to be effective in achieving the desired goals. The future steps of this work could go in the direction of further refining the proposed solution by:

- considering the use of WBG devices for a further improvement of efficiency and power density;
- integrating the control hardware directly in the PCB board, or a daughter board;
- include cost-aware and reliability-aware design considerations, which will be the object of the next chapter.

Chapter 5

Reliability-Constrained Optimization of the Proposed Converter

As anticipated, part of the effort of this PhD was devoted to the investigation of novel optimization approaches to tackle the hard integration of conflicting objectives (cost, efficiency, reliability) in the design of high step-up DC-DC converters for PV applications. Among the different objectives, reliability introduces some challenges in both the modelling and experimental validation, giving rise to a variety of approaches in the literature to tackle its inclusion in optimization processes. The goal of this chapter is to present the outcomes of a new methodology that addresses the simultaneous optimization of a DC-DC converter in terms of cost and efficiency, while considering a lifetime constraint based on real mission profiles. The rest of this chapter is structured as follows:

- Section 5.1 introduces the different adopted approaches to include reliability in the literature, underlining their limitations;
- Section 5.2 introduces in a systematic way all the relevant characteristics and key features of the proposed off-line design optimization methodology, namely the definition of the objective function and lifetime constraints, the description of the converter adopted as the case study, the various modelling contributions, and the search algorithm used to find the optimal solution;
- Section 5.3, starting from the identified optimal solution based on the optimization procedure, describes the steps for the prototype design, including its

full schematic and layout, the design of a custom high-frequency transformer, the firmware design to test the converter performance;

- Section 5.4 presents the experimental results on the prototype of the converter based on the optimal identified solution. The results mainly aim at validating the converter operation and performance, with a specific eye on the thermal performance of the semiconductor devices;
- Section 5.5 draws the conclusions and potential future steps of this work.

This work was developed in collaboration with the Department of Energy of Aalborg University and its outcomes were presented at the international conference IEEE Applied Power Electronics Conference (APEC) 2025 [193]. A journal paper including the most recent advancements and the experimental results is going to be submitted in the near future.

5.1 Introduction

As mentioned in Chapter 1, the decreasing cost and technological improvements of PV modules is gradually increasing the share of cost and failures associated to the power conversion stage. Cost and reliability-aware design considerations can foster even more the penetration of distributed PV systems, in the countries energy mix. So far in this work, little or no attention was devoted to these two critical design constraints, which are, on the other hand, essential for the successful commercialization of a power converter. This chapter focuses on a further optimization of the proposed converter topology introduced in Chapter 4, with a specific eye on cost, efficiency and reliability. Many aspects of this second project are shared with the previously presented content and will not be repeated again, such as the context of module-level power converters (MLPC), with their features and different architectures, and the inherent characteristics of PV generators according to the environmental conditions. Based on that common background, this chapter will describe a new proposed design optimization methodology for the IPOS power optimizer discussed so far.

Before introducing the main aspects of the proposed optimization approach, it is relevant to mention, based on a literature review, the different approaches in which the reliability analysis was considered in the design of power converters for MLPC PV applications: the treatment of reliability in this work represents, indeed, a distinctive and innovative aspect of the investigation.

Reliability analysis not included in the design

In most of the cases presented in the literature review (Chapter 3), the reliability analysis is not considered at all when a new power converter topology is proposed. This observation is probably connected to multiple considerations, such as:

- when presenting a new converter topology, it is usually considered more relevant to focus the attention on the improved performances and the distinctive features in terms of electrical stress reduction, lower component count, improved gain, and so on. A similar consideration can be done for the cost of the converter, which is normally neglected at all when designing a single prototype;

- as described, the reliability analysis is an inherently statistical discipline, based on semi-empirical models trying to estimate, on a statistical basis, the degradation of components until their failure. The lifetime models employed in this discipline are affected by tolerances and are extracted in a laboratory environment that does not reproduce the actual mission profiles that the converter or its components will be required to sustain;

- the degradation of components is, as said, mainly linked to repeated thermal stresses, induced by the losses in the components themselves. When considering a single converter topology, it can be deduced that, with no focus on cost, the most efficient and expensive devices can be selected among the commercially available ones: in other terms, it is assumed that more efficient devices will consequently lead to enhanced converter lifetime.

In most of the papers mentioned in Chapter 3, the design of MLPC mainly focuses on a single objective function, namely, the conversion efficiency. In other cases, however, when introducing multiple conflicting objectives such as cost and power density, more complex and iterative design approaches must be developed to make sure that the identified solution actually represents an effective trade-off of the objective functions. This complex task was addressed in many works in the form of single- or multi-objective optimization problems, often relying on metaheuristic approaches. Their use in power electronics was, up to few years ago, mainly limited to the optimization of control algorithms, but is experiencing an increasing diffusion in off-line topology design phases [194]. Compared to deterministic approaches, metaheuristic population-based search algorithms, like Genetic Algorithms (GA), and Particle Swarm Optimization (PSO) are more scalable, simpler and more suited to complex optimization problems involving non-linear objective functions and discrete design variables. They exhibit an improved convergence speed compared to trajectory-based search algorithms (like simulated annealing), but a potentially higher computational burden.

Multiple works focused on the design optimization of elementary DC-DC topologies like boost [195, 196] or buck-boost [197, 198] converters to be employed in SPO architectures. The objective functions in these cases include power density [195, 197, 196], weighted efficiency [195, 198], and cost [198]. In some cases, due to the flexible number of panels in a string, the number of conversion stages is the design variable to optimize the objective function [195].

Concerning the PPO architecture, main focus of this work, previous works proposed the multi-objective optimization of efficiency and power density of high-gain PWM topologies derived from the boost converter, namely a boost equipped with a voltage multiplier [199], and an interleaved boost [200]. The converter cost was also considered in the objective function in [199].

Post-layout reliability analysis

In other works, reliability is still not included in the design procedure of a new converter topology, but is the object of a post-layout assessment on a prototype, to estimate its lifetime. This approach is adopted in DC-AC large-scale inverters [141, 201] and usually takes into account the most-critical components, namely the electrolytic capacitors and the power modules. On the other hand, this approach is less common in MLPC: in [202], a detailed post-layout reliability assessment, based on the experimental characterization of the thermal impedances of each component and on two real mission profiles, was performed on a micro-inverter originally proposed and prototyped two years before [90]. In [203], a reliability assessment was performed on a buck-boost SRC prototype comparing the FIDES [139] and Military Handbook [136] approaches. In some cases, like in [202], a modified control strategy can be implemented to enhance the converter reliability, without re-designing the prototype.

Reliability included as objective function in the design optimization

Few works included reliability as one of the multiple objective functions to be optimized. This is the case, for instance, of [204], where the Mean Time Between Failures (MTBF), the converter cost and the weighted efficiency were considered as the three conflicting objectives for a low-gain boost converter used as a SPO. Regarding PPO architectures, a high-gain quadratic boost was optimized in terms of peak efficiency and MTBF for in [205], while multiple isolated DC-DC converter topologies (flyback, full-bridge, push-pull) were the object of an optimization based on volume, weighted efficiency and failure rate in [206]. Only catastrophic and random failure modes were considered for the reliability assessment in these works. Following the discussion introduced in Chapter 1, it is relevant to remind that the Military Handbook approach adopted in the previous works, which is based on

empirical failure rates, does not consider the failure modes associated to the aging of the converter components due to the repeated thermal stresses along the converter lifetime. It is also relevant to underline that the intrinsic conflict between enhanced reliability and low cost was addressed, only partially, in [204].

The inclusion of degradation-related failure modes in the reliability assessment was only addressed in a large-scale PV inverter [207], where the yearly lifetime consumption (LC) of the power modules, also denoted as accumulated damage, was considered as objective function to be minimized.

This work aims at filling a gap in the literature, addressing the previously presented limitations:

- it is important to include both reliability and cost already in the design procedure, for a more comprehensive optimization of power converters that does not only consider its performance;
- a reliability assessment that includes also the physics of degradation of the converter components allows to get more insights on the potential failures of the converter;
- the analysis of thermal stresses induced by the converter operation on a real PV mission profile provides a more realistic estimation of the converter lifetime.

For these reasons, this work introduces, as a novelty, the converter lifetime as a constraint, and not as an objective function to be optimized: in this way, the design procedure focuses on optimizing the other objective functions, better clarified later in this work, but always keeping an eye on the minimum target lifetime, which should at least match the warranty time of the corresponding PV panels [41]. The reliability assessment, in this work, considers the failure modes associated to the degradation of components, and induced by the converter operation on a real annual mission profile. It is worth noting that the design methodology proposed in this work is general and can be adapted to different case studies, once the modelling of the converter components is performed.

5.2 Proposed design optimization methodology

This structured section describes all the distinctive elements of the proposed optimization methodology, including the objective function, the identification of the solution space for a given case study, the various modelling contributions, the description of the reliability constraint and of the search algorithm, and the implementation of the optimization procedure in a Matlab application.

5.2.1 Definition of the objective function

The analysis of the state-of-the-art revealed that the main goals for MLPC design are cost, efficiency, power density and reliability. Cheap, efficient and reliable power converters, more precisely, allows to maximize the energy production and minimize the payback time of the initial PV system investment. The power density is directly connected to the cost of the converter: the cost of capacitors, magnetic components and the protection case is, intuitively, proportional to their size. A higher frequency operation, thus, which allows to decrease the size of the passive components, would at the same time decrease their cost. Reliability is ultimately connected to the lifetime costs of the converter: a reliable MLPC, indeed, reduces or eliminates the replacements costs and the revenue losses due to the unavailability of the PV system.

The objective function was, thus, built in a way to integrate both cost and performance figures of merit:

$$u(S) = \frac{\text{Cost}}{\eta_{\text{EURO}}}. \tag{5.1}$$

The European efficiency η_{EURO} was previously defined[1] as a wide-spread figure of merit for the average performance of a PV-fed power converter during an ordinary day in the middle-Europe climate. The objective function $u(S)$ depends on the trial solution S, which consists of a set of trial design variables. The set of potential trial solutions is denoted as the solution space $\mathbb{S}$. Without additional constraints, the

[1] https://www.pvsyst.com/help/component-database/grid-inverters/grid-inverters-main-interface/grid-inverters-efficiency-curve/european-or-cec-efficiency.html (Accessed Nov. 6, 2025).

optimal solution S_{opt} is defined as the solution that minimizes $u(s)$:

$$u(S_{\text{opt}}) = \min\{u(S \in \mathbb{S})\}. \tag{5.2}$$

The numerator of $u(S)$ consists of the cost of the power converter: to be precise, its complete cost includes some terms that are constant to different trial solutions, such as the cost of the microcontroller that implements the control. According to the specific case study, there may be the possibility to neglect some terms that do not affect it significantly or only focus on the most critical ones.

The denominator of $u(S)$, on the other hand, is defined as the EURO efficiency of the trial converter solution S at the rated voltage of the PV panel:

$$\eta_{\text{EURO}} = \sum_i \kappa_i \eta(P_{\text{in},i}), \tag{5.3}$$

where $\kappa_i \in [0.03, 0.06, 0.13, 0.1, 0.48, 0.2]$ are the weighting factors, while $\eta(P_{\text{in},i})$ is the evaluation of the converter efficiency at the following discrete power levels: $P_{\text{in},i} \in [0.05, 0.1, 0.2, 0.3, 0.5, 1] \cdot P_{\text{in,rated}}$. $\eta(P_{\text{in},i})$ can be further expanded to highlight the impact of the converter losses:

$$\eta(P_{\text{in},i}) = 1 - \left(\sum_{\text{comp}} P_{\text{loss,comp}}(P_{\text{in},i}) \right) / P_{\text{in},i}, \tag{5.4}$$

where $P_{\text{loss,comp}}(P_{\text{in},i})$ is the power loss of the specific component *comp* at the power level $P_{\text{in},i}$. Chapter 5.2.4 describes the various contributions of modelling adopted in this work to evaluate, from a specific trial solution S^*, the corresponding $u(S^*)$.

5.2.2 Definition of the case study

The expressions introduced so far for the computation of the cost and weighted efficiency of a converter are of general validity: in order to identify the key design variables constituting the solution space $\mathbb{S}$ and analyze their impact on the objective function, it is now crucial to single out a specific case study.

This work was devoted from its beginning to the investigation of partial-power processing IPOS converters for PPO, leading to the original, multi-mode converter

topology presented in the previous chapter, and shown in Fig. 5.2a. The prototype built from the design specifications of a commercial PV module led to satisfactory performances in terms of conversion efficiency, on a wide voltage range and power range. At the same time, it is relevant to investigate more deeply the impact of the relatively high number of semiconductor devices (two transistors in the boost, 7 transistors and two diodes in the SRC) on the cost and reliability of the converter. The adoption of the proposed converter as a case study for the proposed optimization approach serves two main purposes:

- it allows to investigate more systematically the simultaneous design of the two stages in the IPOS architecture. For instance, it allows to evaluate how the unbalanced distribution of power between the two stages impacts on the cost of the converter and its reliability, and not only on its efficiency;
- it allows to directly address one of the main potential limitations of the proposed converter, namely, the number of semiconductor devices.

As said, the optimization procedure includes a reliability assessment based on three real mission profiles, namely, time-series of solar irradiance and ambient temperature data referred to three different locations, for one year. The plots of the irradiance and ambient temperature profiles are shown in Fig. 5.1a (Aalborg, Denmark), Fig. 5.1b (Turin, Italy), and Fig. 5.1c (Arizona, United States of America). The reason behind the considerations of three different mission profiles lies in the investigation of what is their impact on the optimal power converter design. The selected locations reflect three different climates, characterized by specific features: the Aalborg climate is characterized by a significant difference in the number of daylight hours between Summer and Winter, and the coolest temperatures among the mission profiles; the Arizona mission profile, on the opposite, is characterized by almost constant irradiance peaks throughout the entire year, with the highest temperatures, also exceeding 40 °C in many Summer days; Turin represents a good tradeoff, both in terms of seasonal temperatures and variations in irradiance between Winter and Summer months. The experimental data for the Aalborg mission profile were extracted at the PV laboratory of the Department of Energy of Aalborg University, while the data referred to Turin were measured at the Department of Energy "Galileo Ferraris" of Politecnico di Torino. The data for the Arizona mission profile

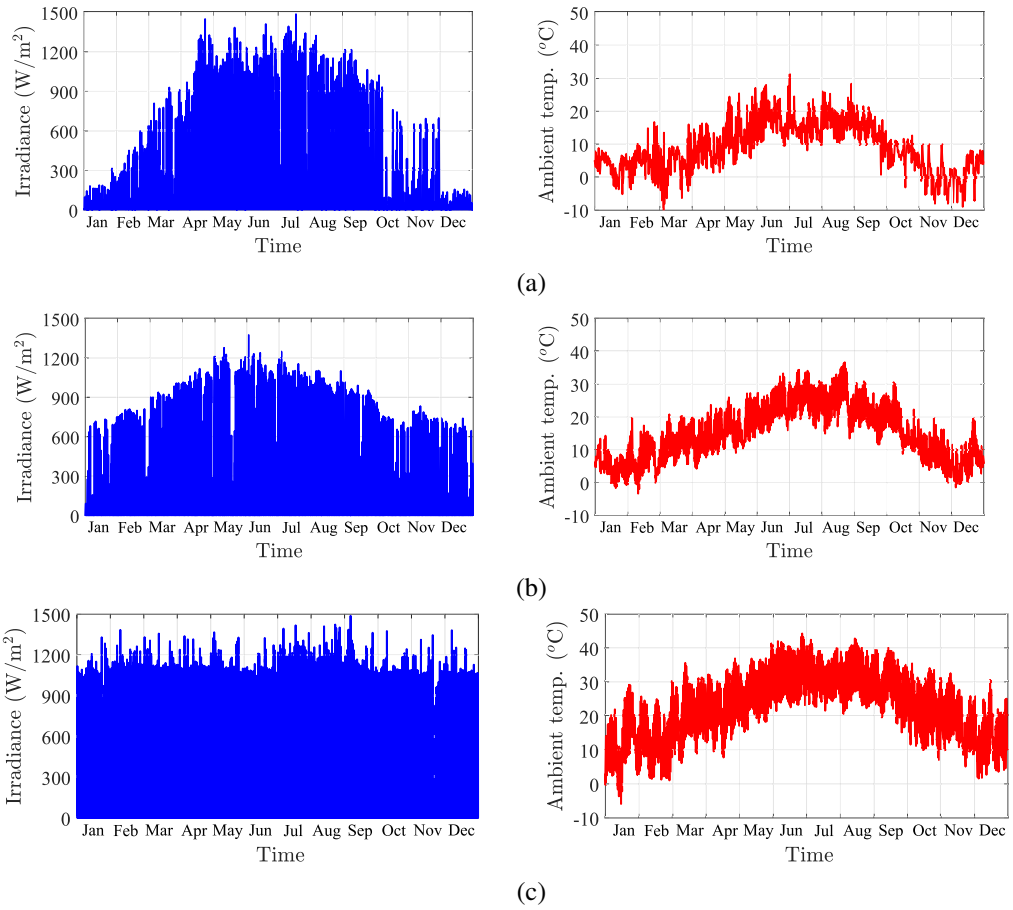


Fig. 5.1 Experimental annual mission profiles of solar irradiance and ambient temperature used for the proposed converter optimization, referred to three different locations: (a) Aalborg (Denmark); (b) Turin (Italy); (c) Arizona (United States of America).

are available online[2]. The inspection of the three mission profiles already suggests that the degradation of the converter components may be faster in Arizona, due to the highest ambient temperatures and most frequent irradiance peaks, which reflect on most frequent PV power peaks.

Unfortunately, the available mission profiles do only consider uniform irradiance conditions, and do not allow to evaluate the eventual shift of the MPP voltage of the PV panel due to partial shading scenarios. As a result, based on those mission profiles, the proposed multi-mode converter would always operate in the neighborhood of the rated MPP voltage, where the rectifier would constantly work as a VDR. This will be more evident as soon as the PV panel model is presented, allowing to extract the

[2]https://midcdmz.nrel.gov/apps/daily.pl?site=UAT&live=1 (Accessed Nov. 7, 2025).

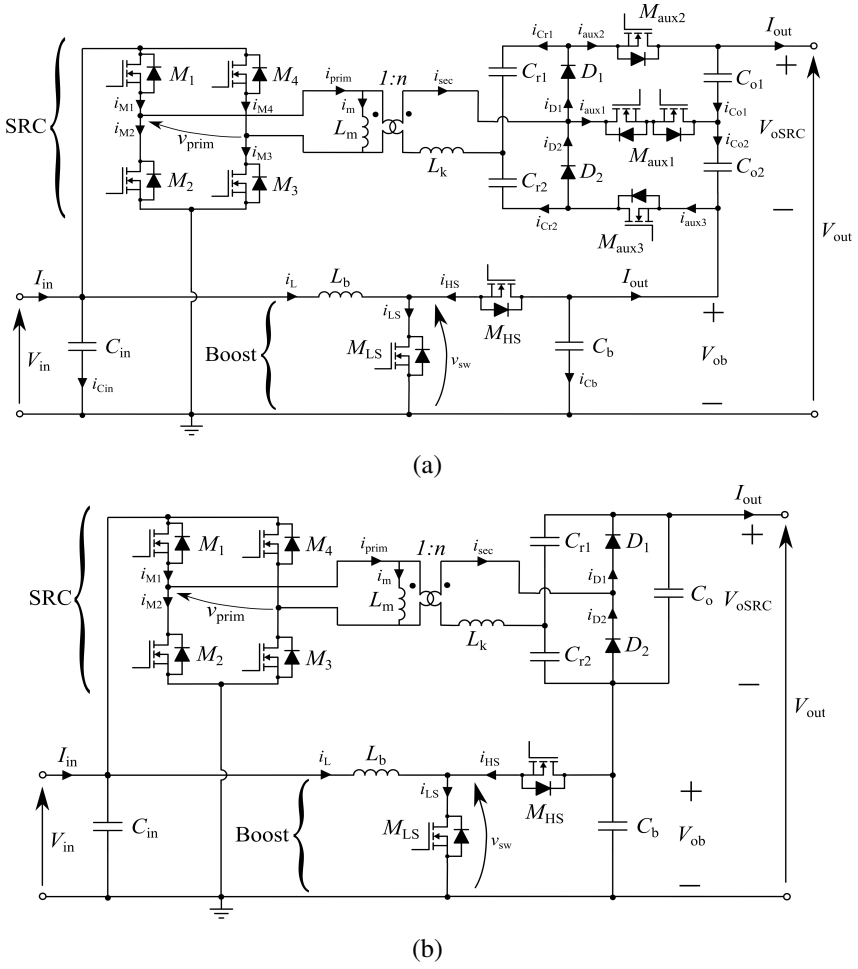


Fig. 5.2 Comparison of the schematics of the proposed converters used for the efficiency-oriented design in Chapter 4 and for the multi-objective reliability-constrained optimization in this chapter: (a) Multi-mode IPOS converter with topology-morphing rectifier; (b) Simplified single-mode IPOS converter.

working input voltages and powers of the converter. For this reason, the proposed optimization is performed on the simplified converter topology shown in Fig. 5.2b. In the modified converter topology, the topology-morphing rectifier of the original design is replaced by a conventional VDR.

The operating principle of the converter is still based on the resonant operation of the SRC, ensuring its best performance, and on the gain modulation performed by the synchronous boost, operating in the BCM. The modelling of the converter waveforms and the electrical stresses are briefly recalled in Section 5.2.4. It is relevant to recall that, in an IPOS architecture, the share of power processed by the

Table 5.1 Main electrical specifications and thermal ratings of the target PV module used for the optimization.

Specification	Symbol	Value
Power at MPP (STC)	$P_{\mathrm{MPP,STC}}$	470 W
Voltage at MPP (STC)	$V_{\mathrm{MPP,STC}}$	36.48 V
Current at MPP (STC)	$I_{\mathrm{MPP,STC}}$	12.89 A
Open circuit voltage (STC)	$V_{\mathrm{oc,STC}}$	44.11 V
Short circuit current (STC)	$I_{\mathrm{sc,STC}}$	13.70 A
Module efficiency (STC)	η_{PV}	24.5 %
Temperature coefficient of P_{max}	γ_P	$-0.24\,\%/^{\circ}\mathrm{C}$
Temperature coefficient of V_{oc}	γ_V	$-0.20\,\%/^{\circ}\mathrm{C}$
Temperature coefficient of I_{sc}	γ_I	$0.044\,\%/^{\circ}\mathrm{C}$

two stages is proportional to their voltage gain. By denoting G_1 the boost gain and G_2 the SRC gain, the following relationship holds:

$$\frac{P(G_2)}{P(G_1)} = \frac{G_2}{G_1}\,. \tag{5.5}$$

Since the SRC works as a DC transformer with gain $2n$, (5.5) can be rewritten as:

$$\frac{P(G_2)}{P(G_1)} = \frac{2n}{\frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} - 2n}\,. \tag{5.6}$$

A target monocrystalline Silicon PV module, 3SHMBTBA-470 manufactured by 3SUN, was selected as reference, characterized by a rated voltage $V_{\mathrm{MPP,STC}} = 36.5\,\mathrm{V}$ and a rated power $P_{\mathrm{MPP,STC}} = 470\,\mathrm{W}$ at STC[3]. The main electrical specifications and temperature degradation rates of the target PV module are reported in Tab. 5.1.

5.2.3 Identification of the solution space

The computation of the objective function depends on the specific trial design solution of the converter topology shown in 5.2b. Without preliminary considerations and constraint, the size of the solution space $\mathbb{S}$ would become extremely large and hard to

[3]https://www.3sun.com/content/dam/threesun/documents/technical/3SUN_M40BOLD.pdf (Accessed Nov. 7, 2025).

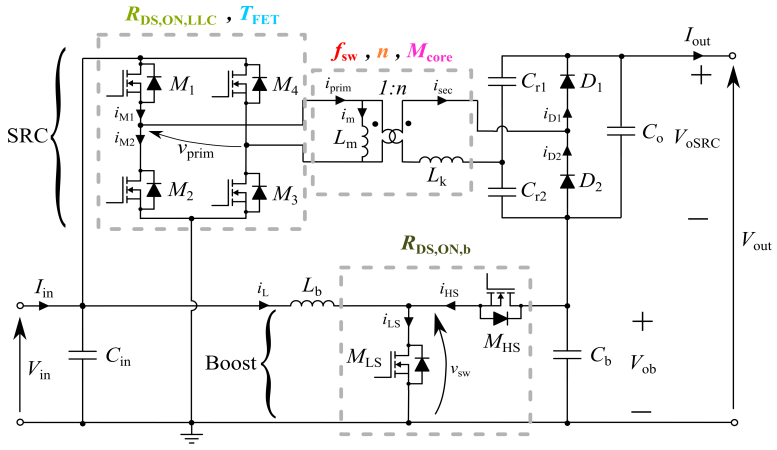


Fig. 5.3 Schematic of the asymmetric IPOS-PPO topology adopted as case study for the optimization. The design variables to be optimized are highlighted.

handle for a search algorithm. The Reduced Order Modelling approach was adopted to identify the minimum number of design parameteres to be optimized [206], to restrict the size of $\mathbb{S}$. The main principle behind the Reduced Order Modelling is that all the intermediate variables, parameters or quantities to compute the objective function can be expressed as functions of a limited number of design parameters. The selected design parameters exhibit the most significant impacts in terms of cost, efficiency and reliability.

Preliminary considerations allowed to identify the following minimal set of design parameters, which are also illustrated in Fig. 5.3:

- the conduction resistance $R_{\mathrm{DS,ON,SRC}}$ and technology T_{FET} of the SRC transistors. As it will be clarified, these two parameters affect both the cost and the switching performances of a transistor, and not only the their conduction losses;
- the resonance frequency f_{res} (ideally coinciding with the full-bridge switching frequency f_{sw}). The resonance frequency has an impact on the core size, cost and losses, on the winding losses, on the turn-OFF switching losses of the full-bridge transistors, and on the input-output DC filter capacitors of the SRC;
- the turns ratio n and core material M_{core} of the SRC transformer. In Chapter 4, the turns ratio n was designed to minimize the power processed by the synchronous boost stage in the neighborhood of the rated PV panel voltage. Here, for a more systematic analysis, n, which is responsible for splitting the

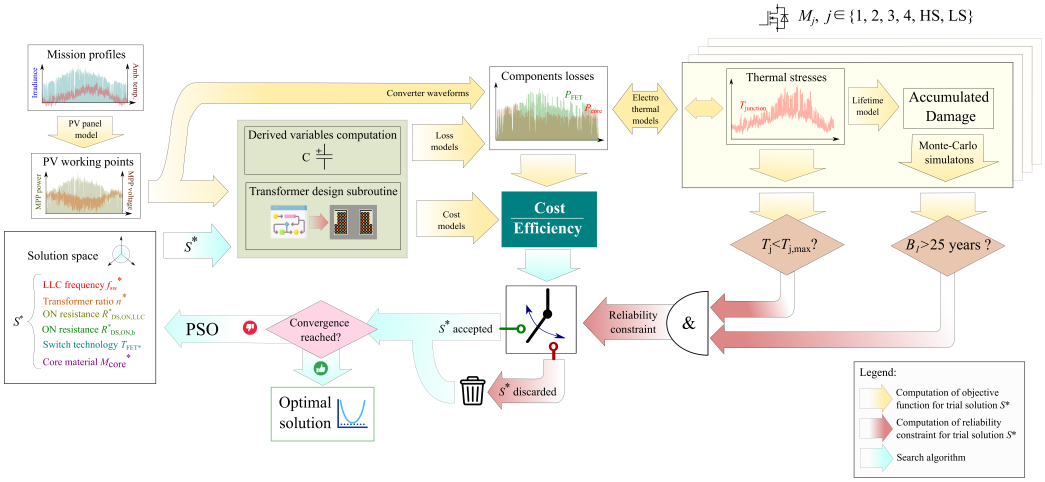


Fig. 5.4 Block diagram of the proposed optimization approach.

power between the IPOS converter stages, is instead selected as one of the variables of the solution space, to be optimized. The core material M_{core} affects the AC core losses of the transformer;

- the conduction resistance $R_{\text{DS,ON,b}}$ of the boost transistors. As well as $R_{\text{DS,ON,SRC}}$, both cost and losses can be expressed as functions of $R_{\text{DS,ON,b}}$. From the analysis of commercial parts for the boost transistors performed during this work, it was considered that the enhanced switching performance of GaN transistors compliant with the boost voltage ratings were not sufficient to justify their limited availability and significantly higher costs. This is the reason why only superjunction Silicon MOSFETs were considered for the boost devices.

Formally speaking, a specific set of the six design variables constitutes the trial solution S^*, belonging to the six-dimensional solution space $\mathbb{S}$:

$$S^* = \{R^*_{\text{DS,ON,SRC}}, T^*_{\text{FET}}, f^*_{\text{sw}}, n^*, M^*_{\text{core}}, R^*_{\text{DS,ON,b}}\}\,. \tag{5.7}$$

The following section describes all the relevant cost and loss models derived from the identified minimal set of design variables.

5.2.4 Modelling

Fig. 5.4 shows the block diagram of the proposed optimization algorithm, including all its constitutive elements and the required links between blocks. The block diagram highlights what kind of modelling contributions are needed for both the evaluation of the objective function and the computation of the converter lifetime. The mission profiles (constraint) and the trial design parameters set S^* from the solution space (inputs) are fed into the algorithm to compute the objective function $u(S^*)$. These calculations are based on several models that and are described in this section:

- a PV panel model is needed to derive its working points (MPP voltages and powers) from the time-series of solar irradiance and ambient temperature;
- the steady-state converter modelling is required to extract the electrical stresses of every components at every working point;
- the trial solution S^* is fed to a set of equations to derive additional variables, such as the required capacitance of the filter capacitors. A specific design subroutine was developed for the transformer sizing;
- cost models are needed to compute the numerator of the objective function, i.e., the total cost of the converter;
- suitable loss models must be developed to compute the converter losses (and, thus, its efficiency) from the electrical stresses of every component

The right-hand side of the block diagram is devoted to the computation of the reliability constraint, used as a selector to accept or discard the trial solution S^* from the next iterations of the search algorithm. Details on the implementation of the reliability constraints are provided in Chapter 5.2.5. A more detailed description of the implemented search algorithm is instead presented in 5.2.6.

PV module modelling

The maximum power working point of a PV panel, as introduced in Chapter 1.1, depends on irradiance and the panel temperature, which significantly affect its electrical characteristic. In this work, a conventional linear model allows to extract,

at each time step k of the mission profile, the optimal working point of the PV panel $V_{\mathrm{MPP,k}}$, $P_{\mathrm{MPP,k}}$, according to (5.8) and (5.9):

$$V_{\mathrm{MPP,k}} = V_{\mathrm{MPP,STC}} \left[1 + \gamma_V \left(T_{\mathrm{panel,k}} - T_{\mathrm{STC}}\right)\right], \tag{5.8}$$

$$P_{\mathrm{MPP,k}} = P_{\mathrm{MPP,STC}} \frac{G_k}{G_{\mathrm{STC}}} \left[1 + \gamma_P \left(T_{\mathrm{panel,k}} - T_{\mathrm{STC}}\right)\right], \tag{5.9}$$

where $T_{\mathrm{panel,k}}$ and G_k are the panel temperature and solar irradiance at the time step k (mission profiles), $T_{\mathrm{STC}} = 25\,^{\circ}\mathrm{C}$ and $G_{\mathrm{STC}} = 1000\,\mathrm{W/m^2}$ are the STC panel temperature and solar irradiance. An additional model is needed to derive the panel temperature from the mission profiles. This work exploited an empirical linear model defined in [208] for roof-mounted PV modules:

$$T_{\mathrm{panel,k}} = T_{\mathrm{amb,k}} + 0.028\,^{\circ}\mathrm{C/Wm^{-2}} \cdot G_k\,. \tag{5.10}$$

For simplicity, the converter is assumed to track perfectly the MPP of the panel (ideal MPPT efficiency). In addition, it is assumed that the time required to move between two consecutive MPPs is negligible compared to the one-minute time step of the measured mission profiles: it this way, the electrical stresses of the converter components are only computed at steady-state, and the transient behaviour is not considered. This is a reasonable assumption, because the electrical transients of power converters usually exhibit time constants significantly lower than one minute. Using (5.8) and (5.9), it is now possible to compute the time-series of the MPP voltages and powers for the three mission profiles, shown in Figs. 5.5a, 5.5b and 5.5c. As it can be seen, according to (5.9), the MPP power profiles recalls the irradiance time-series shown in Figs. 5.1a, 5.1b and 5.1c: the variations of irradiance, indeed, impact in a proportional way the intensity of photo-generated current. Power peaks above 600 W can be observed in Aalborg and Arizona mission profiles. The MPP voltage, on the other hand, is affected by variations in the PV panel temperature. In all the mission profiles, the MPP voltage is bounded between 33 V and 39 V: this the mathematical proof that, when considering only uniform irradiance conditions, PPOs can be designed to work on a limited input voltage range. As a result, the decision to simplify the proposed multi-mode IPOS converter into a single-mode one, where the SRC is equipped with a simple VDR, is justified.

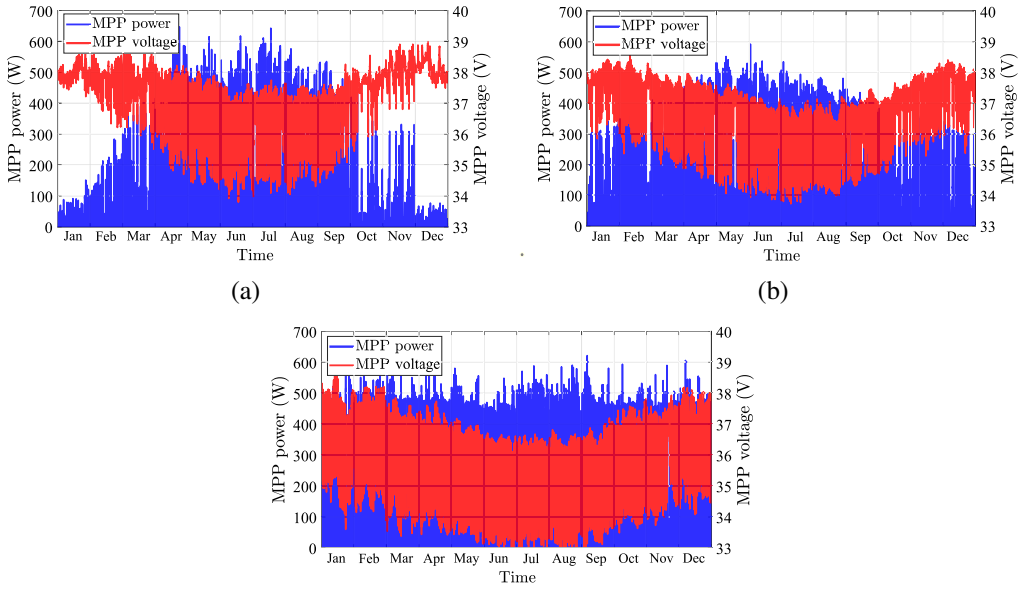


Fig. 5.5 Time-series of the MPP powers and voltages for the three mission profiles, derived from (5.9) and (5.8): (a) Aalborg mission profile; (b) Turin mission profile; (c) Arizona mission profile.

Converter steady-state modelling

Fig. 5.6 shows the qualitative waveforms of the main voltages and currents of the circuit. The waveforms reproduce perfectly the operation of the previously proposed multi-mode IPOS converter in the MV mode, except for the auxiliary MOSFETs M_{aux1}, M_{aux2} and M_{aux3}, which were removed in the topology under investigation. The full mathematical derivation of the waveforms is not repeated, but the main characteristics are recalled.

The SRC full-bridge transistors operate at 50% duty cycle, 180° phase shift and at the resonance frequency of the resonant tank, resulting in sinusoidal transformer currents and uniform electrical stresses among the inverter transistors and among the rectifier diodes. The synchronous boost is operated in the variable-frequency BCM. A ZCD circuit and the precise timing of the control signals for the low-side and high-side transistors allows to achieve the ZVS of the low-side transistor.

Following the block diagram of Fig. 5.4, the working points of the PV panel should be translated into corresponding electrical stresses of the converter components which, in turns, should be converted into loss profiles. Also in this case, the

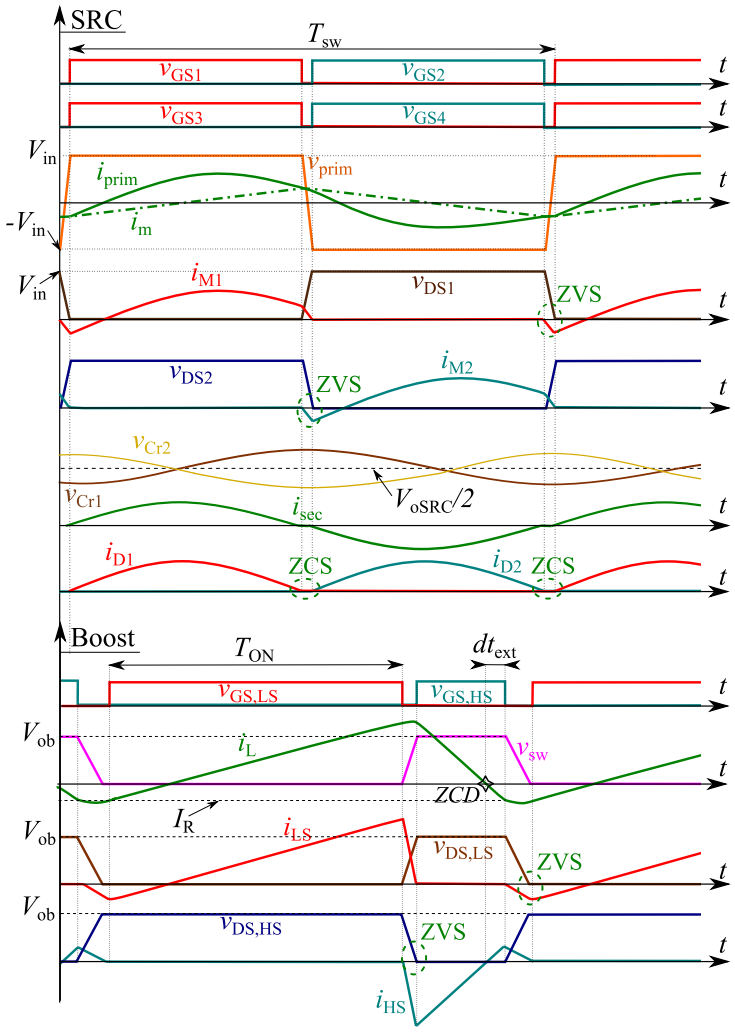


Fig. 5.6 Qualitative waveforms of the proposed IPOS-PPO.

full derivation of the peak voltage stresses and average or RMS current stresses is not repeated, since it was already presented in Chapter 4.3. Table 5.2 lists the main peak voltage, RMS and average current stresses of the converter components, based on the equations and parameters derived in Chapter 4.3. Notice that $T_{sw,b}$ is the switching period of the synchronous boost.

Table 5.2 Comparison of the steady-state voltage and current stresses of the SRC and boost components of the proposed IPOS topology.

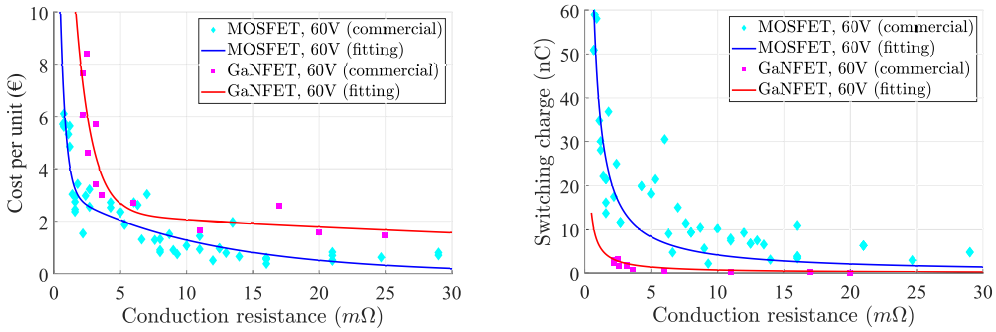
Converter component	Peak voltage stress	RMS current stress	Average current stress
Full-bridge transistors M_{1-4}	V_{in}	$\frac{n\pi}{\sqrt{2}}I_{\text{out}}$	$\frac{n\pi}{\sqrt{2}}I_{\text{out}}$
Transformer primary winding	V_{in}	$\frac{n\pi}{\sqrt{2}}I_{\text{out}}$	0
Transformer secondary winding	$\frac{V_{\text{oSRC}}}{2}+\frac{I_{\text{out}}}{2f_{\text{res}}C_{\text{r}}}$	$\frac{\pi}{\sqrt{2}}I_{\text{out}}$	0
Rectifier diodes D_{1-2}	V_{oSRC}	I_{out}	I_{out}
Resonant capacitors $C_{\text{r1-r2}}$	$\frac{V_{\text{oSRC}}}{2}+\frac{I_{\text{out}}}{2f_{\text{res}}C_{\text{r}}}$	$\frac{\pi}{2\sqrt{2}}I_{\text{out}}$	0
Output capacitor C_{o}	V_{oSRC}	$I_{\text{out}}\sqrt{\frac{\pi^2}{8}-1}$	0
Inductor L_{b}	$V_{\text{in}}\,(G_1-1)$	$\frac{I_{\text{peak}}}{\sqrt{3}}\beta$	$\frac{I_{\text{peak}}}{2}$
Low-side transistor M_{LS}	$V_{\text{in}}G_1$	$\sqrt{\frac{D}{3}}I_{\text{peak}}\beta$	$\frac{I_{\text{peak}}}{2}\frac{T_{\text{ON}}}{T_{\text{sw,b}}}$
High-side transistor M_{HS}	$V_{\text{in}}G_1$	$\sqrt{\frac{1-D}{3}}I_{\text{peak}}\beta$	$\frac{I_{\text{peak}}}{2}\left(1-\frac{T_{\text{ON}}}{T_{\text{sw,b}}}\right)$
Capacitor C_{b}	$V_{\text{in}}G_1$	$I_{\text{out}}\sqrt{\frac{4}{3}G_1\beta^2-1}$	0

Semiconductor devices: cost and loss modelling

The intermediate green block between the trial variable set S^* and the computation of the objective function is responsible for computing all the intermediate design variables of the converter that do not explicitly appear in the solution space. This block is responsible, for instance, to compute the derived variables allowing to estimate the cost and loss of the devices.

Regarding the converter transistors, two different sets of commercial components were taken into account for the SRC and boost switches, respectively. Given the peak voltage stresses across the SRC full-bridge devices M_{1-4} (equal to V_{in}), 60 V-rated components were considered, in both Silicon and Gallium Nitride technology. Both the cost-per-unit and the switching charge Q_{sw} (linked to the switching losses of the devices) can be expressed as functions of the rated ON-resistance $R_{\text{DS,ON,SRC}}$ and the device technology T_{FET}. Proper fitting functions were derived based on the analysis of cost-per-unit and Q_{sw} of 45 Si superjunction MOSFETs and 15 GANFETs, selected among the active components on Digikey[4]. Fig. 5.7a illustrates the fitting of the cost-per-unit of the commercial devices, while Fig. 5.7b shows the fitting of the switching charge. It is relevant to remind that the SRC transistors are supposed to turn ON at zero-voltage, if the magnetizing inductance of the transformer

[4]https://www.digikey.com/ (accessed Jan. 22, 2026).



(a) (b)

Fig. 5.7 Cost-per-unit and switching charge models used in the optimization procedure, based on the analysis of commercial 60 V-rated devices (Si MOSFETs and GaNFETs): (a) Cost-per-unit as function of $R_{\mathrm{DS,ON,SRC}}$, parametrized on the device technology; (b) Switching charge as function of $R_{\mathrm{DS,ON,SRC}}$, parametrized on the device technology.

is properly designed. As a result, the switching losses only involve the turn-OFF of the transistors, which can be approximately expressed (with a linear approximation) by:

$$P_{\mathrm{switching}} = \frac{1}{2} t_{\mathrm{OFF}} f_{\mathrm{sw}} V_{\mathrm{OFF}} I_{\mathrm{ON}} \,, \tag{5.11}$$

where t_{OFF} is the switching time, $V_{\mathrm{OFF}} = V_{\mathrm{in}}$ is the output voltage after the switching, and $I_{\mathrm{ON}} = \frac{V_{\mathrm{in}}}{4 L_{\mathrm{magn}} f_{\mathrm{sw}}}$ is the turn-OFF current, coinciding ideally with the peak of the triangular magnetizing current. From Q_{sw}, t_{OFF} can be derived as [209]:

$$t_{\mathrm{OFF}} = R_{\mathrm{gate}} \cdot \frac{Q_{\mathrm{sw}}(R_{\mathrm{DS,ON,SRC}})}{V_{\mathrm{Miller}}} \,, \tag{5.12}$$

where the gate resistance R_{gate} and the Miller voltage V_{Miller} were still obtained based on the datasheet of the components in the analyzed set. On the other hand, the conduction losses can be expressed as:

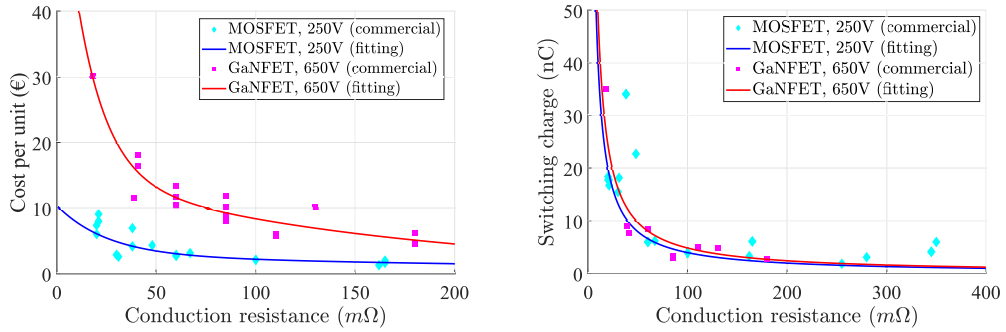
$$P_{\mathrm{conduction}} = R_{\mathrm{DS,ON,SRC}} \cdot \alpha_{\mathrm{R}}(T_{\mathrm{j}}) I_{\mathrm{RMS}}^2 \,, \tag{5.13}$$

where the thermal degradation coefficient $\alpha_{\mathrm{R}}(T_{\mathrm{j}})$ will be better detailed in Section 5.2.5, since it involves the definition of specific models linking the electrical and thermal domains that are essential for a reliable estimation of the components lifetime.

The presented plots and models already underlines a fundamental trade-off between cost and losses, and conduction and switching performances, for which the optimal selection of a component is not a straightforward process. As expected, the GaN technology ensures better switching performances at an increased cost per unit for the same $R_{DS,ON,SRC}$, compared to Si devices. For both the device technologies, the minimization of the conduction losses (minimization of $R_{DS,ON,SRC}$) corresponds unavoidably to increased switching losses (increased Q_{sw} and t_{OFF}). The latter point, indeed, is connected to the fact that both the conduction and switching performances are related (in an inverse way) to the die area of the device [209, 210].

A similar approach was adopted to model the cost and losses of the boost devices, characterized by higher voltage stresses that depend on the specific selection of n. Commercial 250 V Si superjunction MOSFETs and 650 V GaN High Electron Mobility Transistors (HEMTs) were selected for the modelling. Notice that the higher (oversized) voltage ratings of GaN HEMTs is due to the limited availability of lower-voltage HEMTs at the time of this analysis. Fig. 5.8a illustrates the fitting of the cost-per-unit of the commercial devices, while Fig. 5.8b shows the fitting of the switching charge, both expressed as functions of the variable $R_{DS,ON,b}$ of the solution space. It is possible to observe that the significantly higher voltage ratings of GaN HEMTs increases significantly their cost-per-unit but with an imperceptible enhancement of the switching charge: this is the reason why only Si MOSFETs were considered for the optimization of the boost devices, as anticipated previously. The switching times, the conduction and switching loss models can be derived by using the same approach as the SRC devices.

The SRC rectifier diodes were not object of the optimization: according to Tab. 5.2, indeed, their current stresses, ultimately related to their conduction losses do not depend on the specific power spitting between the SRC and the boost in the IPOS architecture. As such, the diodes were selected after the rest of the converter design to minimize their forward voltage drop, and to be compliant with their current and voltage stresses.



(a) (b)

Fig. 5.8 Cost-per-unit and switching charge models used in the optimization procedure, based on the analysis of commercial 250 V-rated Si MOSFETs and 650 V-rated GaN HEMTs): (a) Cost-per-unit as function of $R_{\mathrm{DS,ON,b}}$, parametrized on the device technology; (b) Switching charge as function of $R_{\mathrm{DS,ON,b}}$, parametrized on the device technology.

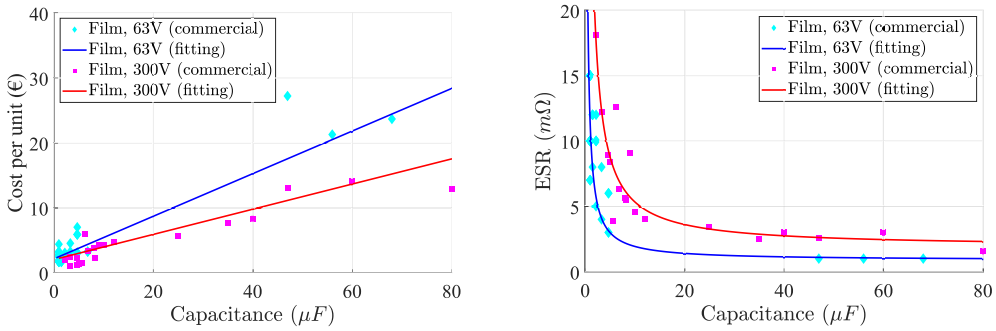
DC filter capacitors: cost and loss modelling

The intermediate green block between the trial variable set S^* and the computation of the objective function is also responsible for computing the required DC filter capacitances (the input capacitance C_{in}, the boost and SRC output capacitances C_{b} and C_{o}, respectively) according to the design equations already presented in Chapter 4.3. From the analysis of 63 V-rated film capacitors (for the input capacitor C_{in}) and 300 V-rated film capacitors (for the boost output capacitor C_{b}), it was possible to derive fitting functions that relate both the cost-per-unit and the ESR of capacitors to their capacitance, which are shown in Fig. 5.9a and Fig. 5.9b, respectively. Electrolytic capacitors were not considered in this design, due to their well-known reduced reliability compared to the film technology [134]. Once the required capacitance value is designed, the corresponding ESR is computed from the model and the conduction lossesin the capacitors are computed as:

$$P_{\mathrm{capacitor}} = ESR \cdot I_{\mathrm{RMS}}^2 \,. \tag{5.14}$$

Transformer: cost and loss modelling

A specific attention is devoted to the design of the custom high-frequency transformer. The design of a transformer extends beyond the selection of the turns ratio, core



(a) (b)

Fig. 5.9 Cost-per-unit and ESR models used in the optimization procedure, based on the analysis of commercial 63 V-rated film capacitors and 300 V-rated film capacitors: (a) Cost-per-unit as function of capacitance, for the two voltage ratings; (b) ESR as function of capacitance, for the two voltage ratings.

material and operating frequency (inputs of the trial solution S^*), as it involves the definition of the number of turns, core size, type of winding, and so on. This is the reason why a specific design optimization subroutine was developed for the transformer inside the outer converter optimization loop, as shown in Fig. 5.4. The general goal of this optimization subroutine is to single out, for a specific trial variable set S^* and among many potential alternatives, the design of the transformer optimizing an ad hoc objective function, the cost-to-power ratio CPR_{T}:

$$CPR_{\mathrm{T}}(AP, N_1) = \frac{\mathrm{C}_{\mathrm{core}} + \mathrm{C}_{\mathrm{bobbin}} + \mathrm{C}_{\mathrm{coils}}}{P_{\mathrm{rated}} - P_{\mathrm{core}} - P_{\mathrm{windings}}}, \tag{5.15}$$

where the numerator consists of the sum of the core, bobbin and coils costs, whereas the denominator is the transformer output power, obtained by subtracting the total transformer losses from the input power, at the rated operation. Additional constraints are added in the transformer design subroutine: the transformer temperature should never exceed $T_{\mathrm{max}} = 100\,^{\circ}\mathrm{C}$, and the maximum flux density should be kept below the saturation B_{sat}.

The procedure was described in [193] and is here recalled in its essential steps:

- relying on the reduced order modelling approach, two degrees of freedom were identified as the key design parameters to express the cost and losses of the transformer: the number of turns of the primary winding N_1, and the area product AP, common geometrical parameter embedding essential information

on the size of the core. This means that the cost, and the core and winding losses can be expressed in terms of the three variables n^*, M^*_{core} and f^*_{sw}, and the two additional design parameters N_1 and AP;

- many different design alternatives exist in the solution space identified by AP and N_1: first of all, it is important to identify a set of constraints that allows to bound the domain;

- *Flux density constraint*: for a specific AP^*, N_1 must be sufficiently large to keep the flux density ΔB across the magnetic cross-section A_{e} lower than a recommended maximum value. As a rule of thumb, this maximum value is the one that causes in the core approximately $100\,\text{mW/cm}^3$ loss density [211]):

$$N_1 > \frac{V_{\text{in,max}}}{2 f_{\text{sw}} \Delta B_{\text{max}} A_{\text{e}}(AP^*)} \tag{5.16}$$

- *Window area constraint*: for a specific AP^*, the primary and secondary coils, with conductor cross section A_{cond} must fit in the available window area A_{w} [212]:

$$N_1 < \frac{K_{\text{w}} A_{\text{w}}(AP^*)}{2A_{\text{cond}}}, \tag{5.17}$$

  where $K_{\text{w}} = 0.3$ is a typical window utilization factor when Litz wire windings are used [213].

- *Magnetizing inductance constraint*: the ZVS operation of the SRC switches bounds the maximum magnetizing inductance L_{magn} of the transformer. At the same time, smaller L_{magn} values increase the conduction losses in the full-bridge devices. For a specific AP^* and inductance factor A_{L} (function of AP^*), N_1 should be large enough to obtain the required L_{magn}:

$$N_1 > \sqrt{\frac{L_{\text{magn}}}{A_{\text{L}}(AP^*)}}. \tag{5.18}$$

The previous constraints depend on many derived variables, such as the geometrical parameters $A_{\text{e}}(AP^*)$, $A_{\text{w}}(AP^*)$ and $A_{\text{L}}(AP^*)$ which were fitted from a set of commercial EE and ETD cores using power functions of the area product, AP. Tab. 5.3 reports the fitting functions to express the magnetic effective area A_{e}, the window

Table 5.3 Empirical fitting functions for the main geometrical parameters of the EE and ETD cores under investigation. AP should be expressed in cm^4.

A_e (cm^2)	$0.9677 \cdot AP^{\frac{1}{2}}$
A_w (cm^2)	$1.043 \cdot AP^{\frac{1}{2}}$
l_e (cm^2)	$7.041 \cdot AP^{\frac{1}{4}}$
MTL (cm^2)	$5.846 \cdot AP^{\frac{1}{4}}$
V_e (cm^2)	$7.445 \cdot AP^{\frac{3}{4}}$

Table 5.4 Empirical parameters of the Steinmetz Equations to compute the core losses for the three identified ferrites.

Material	ρ_{SE} (kW/m^3)	α_{SE} (a.u.)	β_{SE} (a.u.)
N27	153.1	1.969	2.737
N87	51.96	1.936	2.539
N97	51.97	1.858	2.363

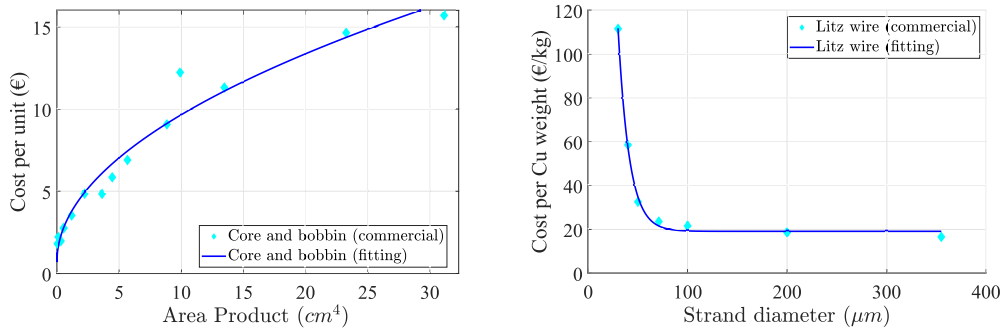
area A_w, the effective magnetic path length l_e, the mean turn length MTL and the effective core volume V_e.

The maximum flux density ΔB_{max}, on the other hand, is specific for a certain material, and is thus a function of M_{core}. TDK "Magnetic Design Tool"[5] was used to derive, for three different ferrite materials (N27, N87 and N97), the ΔB_{max} corresponding to the maximum loss density. The selected ferrite core materials were identified among others for their availability in many different core sizes. The tool expresses the loss functions graphs in terms of Steinmetz Equations depending on the empirical parameters ρ_{SE}, α_{SE}, and β_{SE}, whose values are reported in Tab. 5.4.

For square-wave input voltage excitations (as in the present case), the core loss density can be expressed as:

$$\rho(f_{\mathrm{sw}}, \Delta B) = \frac{\pi}{4} \rho_{\mathrm{SE}}(100\,\mathrm{kHz}, 100\,\mathrm{mT}) \cdot \left(\frac{f_{\mathrm{sw}}}{100\,\mathrm{kHz}} \right)^{\alpha_{\mathrm{SE}}} \left(\frac{\Delta B}{2 \cdot 100\,\mathrm{mT}} \right)^{\beta_{\mathrm{SE}}} . \quad (5.19)$$

[5] https://tools.tdk-electronics.tdk.com/mdt/index.php/pl_flux_density (accessed Nov. 11, 2025).



(a) (b)

Fig. 5.10 Main cost models for the core and windings of the custom transformer. (a) Core and bobbin cost, expressed as function of the area product AP; (b) Litz wire cost-per-weight, expressed as function of the strand diameter.

Inverting (5.19), the maximum $\Delta B_{\max}$ associated to the $100\,\mathrm{mW/cm^3}$ core loss is:

$$\Delta B_{\max} = 200\,\mathrm{mT}\left[\frac{100\,\mathrm{mW/cm^3}}{\frac{\pi}{4}\rho(100\,\mathrm{kHz},\,100\,\mathrm{mT})}\left(\frac{100\,\mathrm{kHz}}{f_{\mathrm{sw}}}\right)^{\alpha}\right]^{\frac{1}{\beta}} \tag{5.20}$$

The cost model for the core and bobbin ($C_{\mathrm{core}} + C_{\mathrm{bobbin}}$) was derived by fitting the cost of commercial EE and ETD cores, widely adopted in power electronics applications, and available in different sizes and materials. Fig. 5.10a shows the fitting of the sum of core and bobbin costs for a set of 15 commercial parts. It can be observed that the cost trend follows $\sqrt{AP}$: in other terms, since $A_{\mathrm{e}} \propto \sqrt{AP}$, there is an approximately direct proportionality between the core magnetic area and the core cost. For the transformer windings, the cost model C_{windings} for Litz wire coils is based on the cost model provided in [214], depending on the overall windings weight ω_{Cu} and diameter d_{s} of the copper strands. The cost-per-weight can be expressed as a negative exponential function of the strand diameter, as shown in Fig. 5.10b.

Regarding the denominator of the objective function CPR_{T} in (5.15), it is necessary to model the core losses P_{core} and the winding losses P_{windings}. The core losses can be computed from the Steinmetz Equation $P_{\mathrm{core}} = V_{\mathrm{e}} \cdot \rho(f_{\mathrm{sw}}, \Delta B)$, where $\rho(f_{\mathrm{sw}}, \Delta B)$ is expressed in (5.19). The winding losses can be analytically computed by:

$$P_{\mathrm{windings}} = R_{\mathrm{prim}} F_{\mathrm{prim}} I_{\mathrm{prim}}^2 + R_{\mathrm{sec}} F_{\mathrm{sec}} I_{\mathrm{sec}}^2\,, \tag{5.21}$$

where $R_{\text{prim}}/R_{\text{sec}}$ are the DC resistances of the primary/secondary coils, whereas $F_{\text{prim}}/F_{\text{sec}}$ is a resistance increase factor that includes both the skin and proximity effects [213]:

$$F_i \approx 1 + \frac{5N_{\text{layers}}^2 N_{\text{s},i} - 1}{45} \left(1.37 \frac{d_{\text{s}}}{2\delta_f}\right)^4 , i \in \{\text{prim}, \text{sec}\} . \tag{5.22}$$

Notice that the increase in the winding resistance is linked to the number of strands $N_{\text{s},i}$, the number of adjacent Litz wire layers carrying the same current N_{layers} and by the ratio between the strand diameter and the skin depth d_{s}/δ_f [213]. To limit the impact of the AC losses in the windings, the transformer design subroutine selects the strand diameter d_{s} to be $1/3$ of the skin depth.

To summarize the procedure, the transformer optimization subroutine consists in an inner optimization problem. Among many potential alternative designs, characterized by different sizes AP and number of turns N_1, the optimal transformer is the one that minimizes an ad hoc objective function, given the set of inputs n^*, f_{sw}^*, and M_{core}^*. A deterministic search is implemented to find the optimal couple of primary turns N_1 and area product AP: the cost and loss of the core and windings can be expressed in terms of this minimal set of material-related and geometry-related parameters. It is relevant to observe that, similarly to what happens for the semiconductor devices, the optimal transformer design is not straightforward: an increased frequency operation (larger f_{sw}) would decrease the core size (and cost) but would require to select thinner and more expensive Litz wire strands.

The main cost and loss models of the converter components described so far are listed in Tab. 5.5 and Tab. 5.6, respectively, which highlight what are the "primitive" parameters (the variables of the solution space $\mathbb{S}$) and the main derived functions / intermediate variables on which the models are based. The empirical parameters of the cost models are listed in Tab. 5.7.

5.2.5 Implementation of the lifetime constraint

The reliability constraint implemented in this work only applies to the power transistors of the converter. The approach considers both the failures due to instantaneous

Table 5.5 List of the main cost models adopted in the optimization algorithm.

Component	Primitive parameters	Derived parameters	Cost model
SRC FETs M_{1-4}	$R_{\mathrm{DS,ON,SRC}}$, T_{FET}	-	$b_1 e^{d_1 R_{\mathrm{DS,ON,SRC}}} + b_2 e^{d_2 R_{\mathrm{DS,ON,SRC}}}$
Boost FETs $M_{\mathrm{LS-HS}}$	$R_{\mathrm{DS,ON,b}}$	-	$b_3 e^{d_3 R_{\mathrm{DS,ON,b}}} + b_4 e^{d_4 R_{\mathrm{DS,ON,b}}}$
Input capacitor C_{in}	f_{sw}, n	C_{in}	$c_1 + c_2 \cdot C_{\mathrm{in}}$
Boost capacitor C_{b}	n	C_{b}	$c_3 + c_4 \cdot C_{\mathrm{b}}$
Transformer core and bobbin	f_{sw}, n, M_{core}	AP	$g_1 + g_2 AP^{\frac{1}{2}}$
Transformer windings	f_{sw}, n	d_{s}, ω_{Cu}, N_1, N_2	$g_3 + \omega_{\mathrm{Cu}} \cdot \left[g_4 + g_5 e^{g_6 d_{\mathrm{s}}} \right]$

Table 5.6 List of the main loss models adopted in the optimization algorithm.

Component	Primitive parameters	Derived parameters	Loss model
SRC FETs M_{1-4}	$R_{\mathrm{DS,ON,SRC}}$, T_{FET}, f_{sw}	t_{OFF}, α_{R}	$R_{\mathrm{DS,ON,SRC}} \alpha_{\mathrm{R}}(T_{\mathrm{j}}) I_{\mathrm{RMS}}^2 + \frac{1}{2} t_{\mathrm{OFF}} f_{\mathrm{sw}} V_{\mathrm{OFF}} I_{\mathrm{ON}}$
Boost FETs $M_{\mathrm{LS-HS}}$	$R_{\mathrm{DS,ON,b}}$	t_{OFF}, α_{R}	$R_{\mathrm{DS,ON,b}} \alpha_{\mathrm{R}}(T_{\mathrm{j}}) I_{\mathrm{RMS}}^2 + \frac{1}{2} t_{\mathrm{OFF}} f_{\mathrm{sw}} V_{\mathrm{OFF}} I_{\mathrm{ON}}$
Input capacitor C_{in}	f_{sw}, n	C_{in}, $ESR(C_{\mathrm{in}})$	$ESR(C_{\mathrm{in}}) I_{\mathrm{RMS}}^2$
Boost capacitor C_{b}	n	C_{b}, $ESR(C_{\mathrm{b}})$	$ESR(C_{\mathrm{b}}) I_{\mathrm{RMS}}^2$
Transformer core and bobbin	f_{sw}, n, M_{core}	AP, N_1, V_{e}, α_{SE}, β_{SE}, ρ_{SE}	$\frac{\pi}{4} K_{\mathrm{core}} V_{\mathrm{e}}(AP) \rho_{\mathrm{SE}} f_{\mathrm{sw}}^{\alpha_{\mathrm{SE}}} \Delta B^{\beta_{\mathrm{SE}}}$
Transformer windings	f_{sw}, n	N_1, N_2, R_{prim}, F_{prim}, R_{sec}, F_{sec}	$R_{\mathrm{prim}} F_{\mathrm{prim}} I_{\mathrm{prim,RMS}}^2 + R_{\mathrm{sec}} F_{\mathrm{sec}} I_{\mathrm{sec,RMS}}^2$

excessive heating and to the wear-out induced by the repeated thermal cycles during the lifetime of the semiconductor devices, and it is based on models that take into account the physics of the degradation. As shown in Fig. 5.4, the reliability constraint actually consists of two conditions to be met simultaneously: the maximum junction temperature of every transistor should never exceed the maximum temperature reported in the datasheet, and the converter lifetime, expressed in terms of B_1, should be larger than 25 years. If at least one of the two conditions is not met, the current trial solution S^* is discarded and not re-iterated in the search algorithm.

Table 5.7 Empirical parameters of the cost models in Table 5.5.

Parameter	Value	Parameter	Value
b_1	23.84 €(Si) / 39.36 € (GaN)	c_2	0.328 €/μF
b_2	3.236 €(Si) / 2.346 € (GaN)	c_3	2.017 €
b_3	7.62 €(Si)	c_4	0.194 €/μF
b_4	2.791 €(Si)	g_1	0.704 €
d_1	$-2.467\,\mathrm{m\Omega^{-1}}$ (Si) / $-0.821\,\mathrm{m\Omega^{-1}}$ (GaN)	g_2	2.83 €/cm^2
d_2	$-0.091\,\mathrm{m\Omega^{-1}}$ (Si) / $-0.013\,\mathrm{m\Omega^{-1}}$ (GaN)	g_3	0.5 €
d_3	$-0.0393\,\mathrm{m\Omega^{-1}}$ (Si)	g_4	19.04 €/kg
d_4	$-0.003\,\mathrm{m\Omega^{-1}}$ (Si)	g_5	1323 €/kg
c_1	2.128 €	g_6	$-886\,\mathrm{cm^{-1}}$

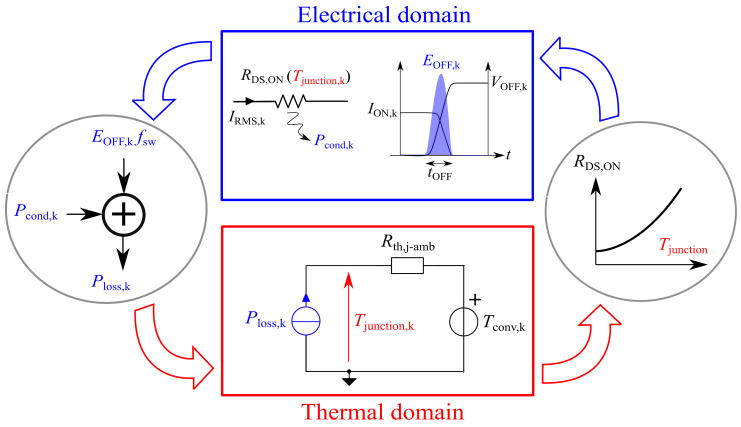


Fig. 5.11 Graphical representation of the coupling between electrical and thermal domains for the computation of the thermal stresses of the converter transistors.

In both cases, the computation of the two reliability constraints is based on the simulation of the yearly profile of the devices junction temperatures. A suitable electro-thermal model must be defined to couple the electrical domain, in which the electrical stresses are translated into power losses, and the thermal domain, in which the dissipated power is translated into a temperature increase.

The coupling between the electrical and thermal domains is graphically represented in Fig. 5.11. At each time step k of the mission profile, the conduction losses and switching losses are computed and summed, according to the loss model in Tab.

5.6:

$$P_{\text{loss,k}} = R_{\text{DS,ON}}(T_{\text{junction,k}})I^2_{\text{RMS,k}} + E_{\text{OFF}} f_{\text{sw}} \,. \tag{5.23}$$

The total dissipated power is modelled, in an equivalent thermal circuit, as an independent current generator. In the thermal domain, the dissipated power generates a corresponding increase in the junction temperature depending on the instantaneous converter temperature $T_{\text{conv,k}}$ and the junction-to-converter thermal resistance $R_{\text{j,amb}}$:

$$T_{\text{junction,k}} = T_{\text{conv,k}} + R_{\text{th,j-amb}} P_{\text{loss,k}} \,. \tag{5.24}$$

Since the converter is expected to be enclosed in a case and not in open air, it would be incorrect to assume the air temperature in the thermal model. The ambient temperature inside the case is not easy to estimate, as it is affected, intuitively, also by the PV panel temperature and converter losses: in this work, $T_{\text{conv,k}}$ is computed by using the empirical model derived in [215]. In the article, the authors developed a linear regressive model based on the analysis of the correlation between a microinverter temperature and the most statistically relevant variables: ambient temperature, PV module temperature, irradiance and electrical power:

$$T_{\text{conv,k}} = -0.232 + 0.676 \cdot T_{\text{amb,k}} + 0.365 \cdot T_{\text{panel,k}} + 0.002 \cdot G_k - 0.0095 \cdot P_{\text{in,k}} \,. \tag{5.25}$$

As expressed in (5.25), the converter temperature is mainly dependent on the ambient and PV module temperatures. Given the 1 min time-step of the mission profiles, much longer than the typical time constants of the junction temperature transients, the equivalent thermal circuit does not include capacitive effects and can be modelled as a resistive circuit.

As expressed in (5.23), the conduction resistance used for the computation of the conduction losses is a function of the junction temperature. More specifically, by fitting the typical behaviour of $R_{\text{DS,ON}}$ versus T_{junction} from both Si and GaN transistors datasheet, exponential functions were derived to model this interdependence. This exponential term, denoted as α_{R}, is computed at each time step depending on the current junction temperature and is multiplied to the rated $R_{\text{DS,ON}}$.

The thermal resistance $R_{\text{th,j-amb}}$ mainly dependent on the device package and layout design: a systematic analysis would require to consider, for each trial solution S^*, a corresponding layout design and multiphysics simulations to estimate more

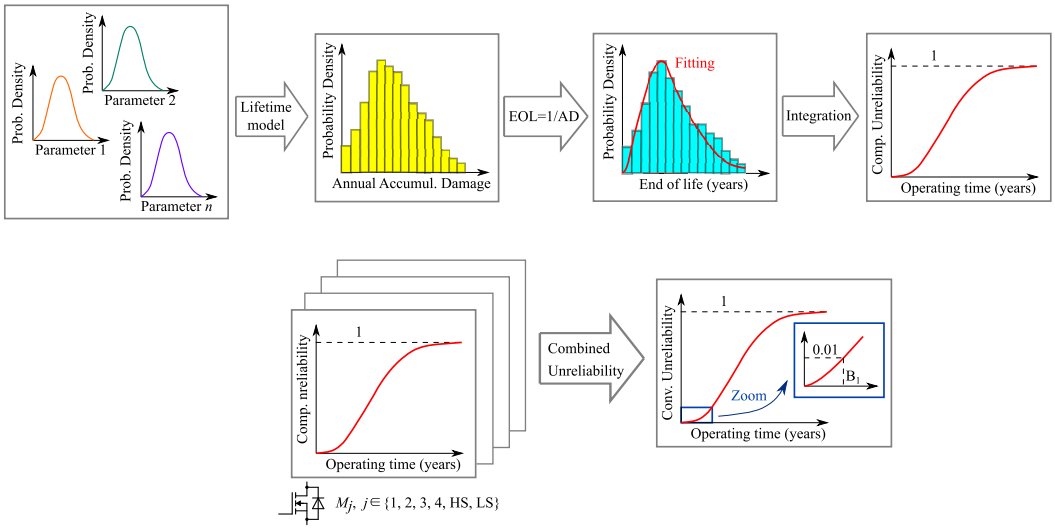


Fig. 5.12 Block diagram of the Monte-Carlo approach adopted for the computation of the converter lifetime. Legend: EOL = End-of-lifetime.

accurately the thermal resistance. This approach is clearly too time-consuming for an iterative optimization algorithm and could be adopted only once after the converter design is finalized. In this work, to simplify the analysis, worst-case values of $R_{\mathrm{th,j-amb}}$ were selected from the most common packages in the database of the SRC and boost transistors. No heat-sink is considered in the design. The simultaneous solution at each time step of the coupled equations (5.23) and (5.24) provides the time series of the power losses and junction temperature for each converter transistor.

As shown in Fig. 5.4, the first reliability constraint to be met is that the junction temperature of any converter switch must never exceed the maximum datasheet value $T_{\mathrm{j,max}}$ (175 °C for Si devices, 150 °C for GaN devices). The second condition is that the converter lifetime, represented by the parameter B_1, must be larger than 25 years. The lifetime estimation procedure was described in details in Chapter 3.2: the junction temperatures profiles are decomposed into elementary thermal cycles, which are counted using the rainflow counting algorithm; each thermal cycle is converted through a lifetime model into a corresponding damage, and all contributions are summed linearly into AD; Monte-Carlo simulations are run to derive the distribution function of the end-of-life (EOL), to take into account the tolerances of the lifetime model parameters.

Table 5.8 Lifetime model parameters used in the computation of the expected switches lifetime.

Model parameter	Value
A	$4.9283 \cdot 10^{13} \pm 10\%$
B	$-5.2776 \pm 10\%$
E_a	$812\,\mathrm{eV} \pm 10\%$

A block-diagram of the Monte-Carlo approach used to compute the converter lifetime is shown in Fig. 5.12. The computation of the *AD* for each transistor is repeated many times, by sampling, at each time, the parameters of the lifetime model from normal distribution functions, to take into account their tolerances. The lifetime estimation in this work is based on the lifetime model proposed in [148], which was derived through accelerated aging tests on discrete power MOSFETs using the increase of the $R_{\mathrm{DS,ON}}$ as degradation precursor:

$$N_{\mathrm{f},i} = A \cdot \Delta T_{\mathrm{j},i}^{B} \cdot \exp\left(\frac{E_\mathrm{a}}{k_\mathrm{B}\left(\overline{T}_{\mathrm{j},i} + 273\right)}\right), \tag{5.26}$$

where the empirical parameters A, B and E_a are reported in Tab. 5.8, k_B is the Boltzmann constant, $\Delta T_{\mathrm{j},i}$ and $\overline{T}_{\mathrm{j},i}$ are the peak-to-ripple and average value of the elementary thermal cycle i. The $\pm 10\%$ tolerance of the empirical parameters describes the 95 % confidence bound of the normal distribution from which the parameters are sampled.

The repeated simulations with different values of model parameters allow to obtain a histogram of *AD*. By definition, since the mission profiles used in the simulations refer to one year operation, the lifetime, or End-of-lifetime (EOL) of a component can be computed as:

$$EOL = \frac{1}{AD}. \tag{5.27}$$

The application of (5.27) allows to translate the distribution of *AD* into a corresponding histogram of *EOL*. The histogram is then fitted with a suitable PDF: Weibull or Gamma distributions are usually exploited for this purpose. The resulting PDF represents the probability density that a component fails at a certain time. Thus, the integration of this function provides the unreliability of the component, namely

a statistical estimation of the fraction of components failed at a certain time. This approach is performed for all the transistors of the circuit, leading to the components unreliability functions for the SRC transistors U_{SRC}, and boost transistors $U_{\mathrm{b,LS}}$ and $U_{\mathrm{b,HS}}$. Once these are derived, the converter unreliability for the trial solution S^* is computed as:

$$U_{S^*} = 1-(1-U_{\mathrm{SRC}})^4(1-U_{\mathrm{b,LS}})(1-U_{\mathrm{b,HS}})\,. \tag{5.28}$$

The global assumption behind this method is that the converter reliability is mainly constrained by the transistors lifetime: otherwise, other terms should be considered in the converter unreliability function. In this work, the lifetime B_1 of the converter solution S^* is defined as the time after which the first 1 % of the converters have failed, popular indicator to express the reliability of a power converter [134]:

$$U_{S^*}(B_1) = 0.01\,. \tag{5.29}$$

Coming back to the block diagram of the optimization methodology, the inclusion of the lifetime constraints modifies the definition of optimal solution compared to (5.2): S_{opt} is the solution that minimizes the objective function u while still meeting the two reliability constraints:

$$S_{\mathrm{opt}}\ \text{such that}\begin{cases} u(S_{\mathrm{opt}}) = \min\{u(S\in\mathbb{S})\} \\ B_1(S_{\mathrm{opt}}) > 25\,\text{years} \\ T_{\mathrm{j}}(M_k) < T_{\mathrm{j,max}},\ \forall k\in\{1,2,3,4,\mathrm{LS},\mathrm{HS}\} \end{cases} \tag{5.30}$$

5.2.6 Search algorithm: implementation of PSO

The exhaustive search of the optimal solution in the solution space was excluded due to its computational burden. In addition, due to the presence of the reliability constraint, significant regions of the solution space that are not actually acceptable would be explored in any case. For these reasons, a metaheuristic approach was exploited to explore the solution space in a faster and smarter way. The PSO was selected among other search algorithms for its simple implementation and for its effectiveness when the objective function is non linear or discontinuous [206]. In addition, it only relies on a limited number of user-defined parameters, reducing the sensitivity of the user choices. On the other hand, one of the main limitations

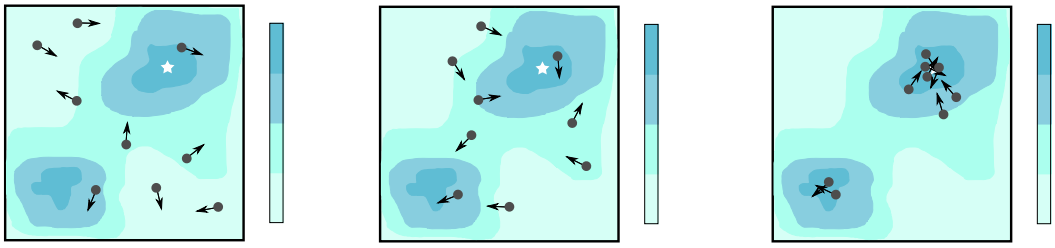


Fig. 5.13 Schematic representation of the PSO in a simplified 2D solution space, at three different iterations. The square represents the domain of all the potential solutions: the areas inside the square are coloured according to the corresponding evaluation of the objective function. The star represents the solution optimizing the objective function. The particles move inside the solution space, from random positions (first iteration), gradually concentrating around the optimal solution and a local sub-optimal one.

of the PSO is the possibility to converge to local solutions in case of non-convex optimization problems.

The principle of the PSO algorithm is schematically represented in Fig. 5.13, showing a simplified 2D case. The particles, which have their own speed, move inside the square domain in search of the optimal solution that minimizes or maximizes the objective function. The star represents the global optimal solution. As schematically shown, from initial random positions and speeds, the particles gradually concentrate around the global optimal solution and a local, sub-optimal one.

At each iteration of the algorithm, the population of particles, i.e. the trial converter solutions, move inside the solution space with a speed that depends on their previous speeds, and the "attraction" to the individual and global optimal solutions. As shown in Fig. 5.4, the single particle $\mathbf{S}^*$ can be represented by a vector of six coordinates:

$$\mathbf{S}^* = [f_{\mathrm{sw}}^*, n^*, M_{\mathrm{core}}^*, R_{\mathrm{DS,ON,SRC}}^*, T_{\mathrm{FET}}^*, R_{\mathrm{DS,ON,b}}^*]\,. \tag{5.31}$$

In mathematical terms, at the iteration m, the speed of the particle $\mathbf{S}_\mathbf{m}^*$, denoted by $\mathbf{V}_\mathbf{m}^*$, is computed as:

$$\mathbf{V}_\mathbf{m}^* = \omega \mathbf{V}_{\mathbf{m-1}}^* + k_1 r_1 \left(\mathbf{S_{best}} - \mathbf{S}^*\right) + k_2 r_2 \left(\mathbf{G_{best}} - \mathbf{S}^*\right), \tag{5.32}$$

where ω (inertia coefficient), k_1 (cognitive coefficient) and k_2 (social coefficient) are the user-defined parameters of the PSO, $r_1 \in [0, 1]$ and $r_2 \in [0, 1]$ are random numbers, $\mathbf{S_{best}}$ is the optimal solution found so far by the particle $\mathbf{S}^*$, whereas $\mathbf{G_{best}}$ is the global optimal solution found so far by the entire swarm. The definition of ω, k_1 and k_2 affects both the convergence speed and the fraction of the solution space that can be explored. The next position of the particle is thus computed as a vector sum:

$$\mathbf{S^*_{n+1}} = \mathbf{S^*_n} + \mathbf{V^*_n}. \tag{5.33}$$

It is important to notice that, if the particle at the position $\mathbf{S^*_{n+1}}$ does not meet the reliability constraint, it comes back to the previous acceptable position $\mathbf{S^*_n}$. The algorithm stops when the objective function remains stable after a sufficient number of iterations, decided by the user. The PSO-based optimization procedure implemented in this work is summarized in the flowchart shown in Fig. 5.14. After the first iteration, whose goal is to initialize a population of particles in the solution space meeting the reliability constraints, the algorithm proceeds in successive iterations until the convergence criterion is satisfied. At every iteration, the tentative new position of a particle is discarded if it does not meet the reliability constraints.

5.2.7 Matlab implementation of a GUI

The Matlab code implementing the complete algorithm is reported in Appendix B. To increase the accessibility and ease of use of the developed algorithm, a custom Matlab application was implemented with an intuitive Graphical User Interface (GUI). While the models of the converter components cannot be accessed by the user, the main constraints and user-defined parameters can be manually specified to satisfy custom design requirements. The first tab of the GUI, shown in Fig. 5.15a, includes the description of the algorithm and the target IPOS converter topology to be optimized. The user can specify the datasheet parameters of a desired PV module and can select one of three mission profiles, namely Turin (Italy), Aalborg (Denmark), and Arizona (United States of America).

In the second tab, shown in Fig. 5.15b, the PSO coefficients, convergence criteria and the boundaries of the solution space can be defined by the user. By default, the range of n is derived by the algorithm according to the feasible SRC gains, while $M_{\text{core}} \in \{\text{N27}, \text{N87}, \text{N97}\}$ and $T_{\text{FET}} \in \{\text{Si}, \text{GaN}\}$ are set by default. In addition,

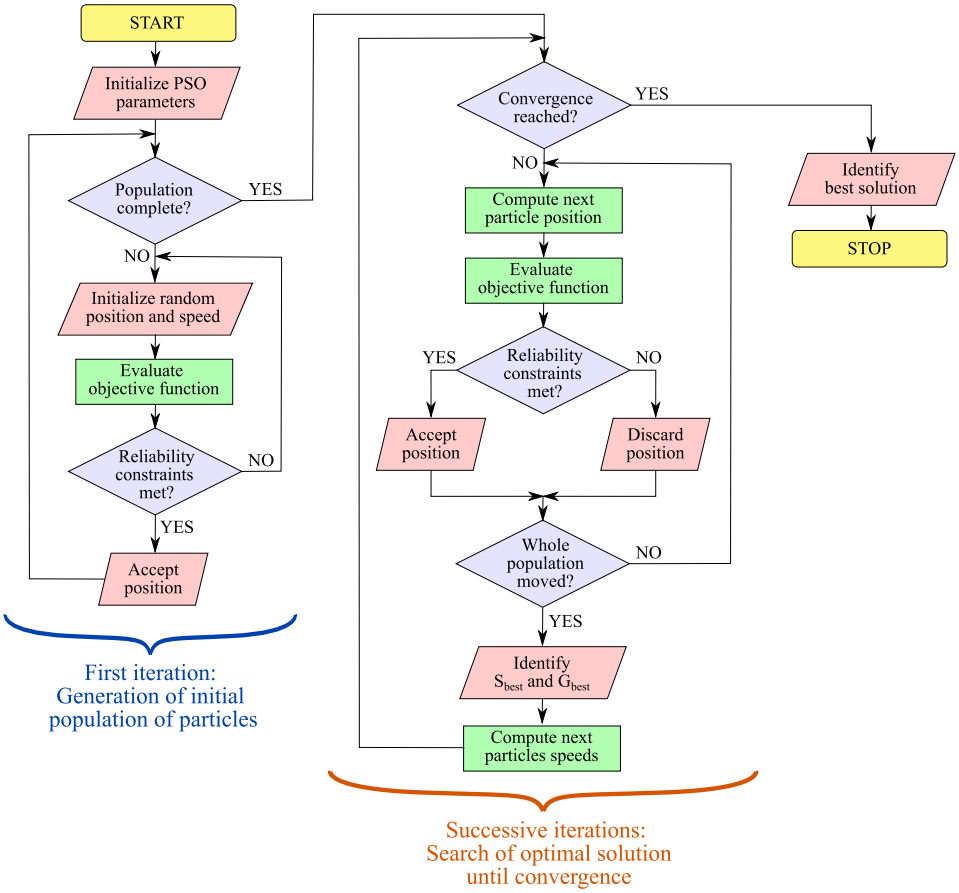
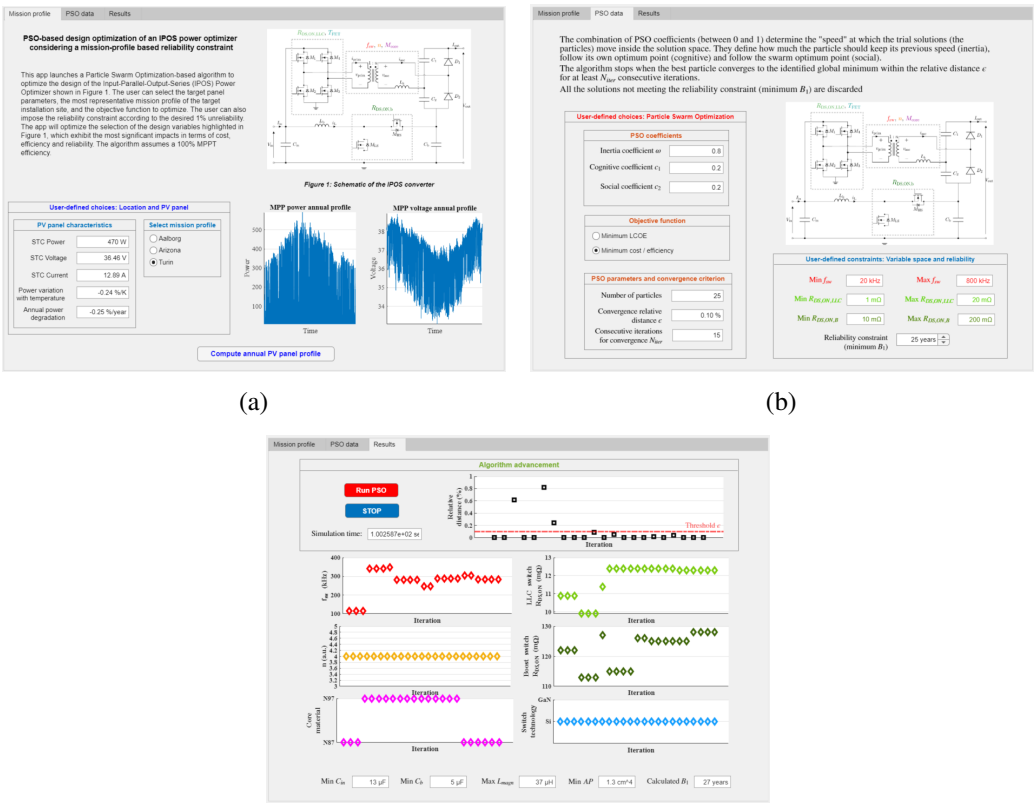


Fig. 5.14 Flowchart of the proposed PSO-based search algorithm

according to the required reliability, the value of B_1 can be set. Regarding the objective function, the app allows to select between the cost / efficiency ratio, and the more conventional LCOE.

In the third tab, shown in Fig. 5.15c, the GUI displays the convergence of the solution iteration after iteration, and the evolution of the optimal variable set, i.e., the variable set of the "particle" in the swarm minimizing the objective function.



(a) (b)

(c)

Fig. 5.15 Pictures of the three tabs of the custom GUI application. (a) "Mission profile" tab: definition of the target PV module and mission profile; (b) "PSO data": definition of user parameters for the PSO; (c) "Results" tab: real-time evolution of the algorithm convergence and display of the global optimal solution.

5.3 Simulation results and hardware design

As explained in details in Chapter 5.2, the optimization algorithm already embeds most of the design equations for a suitable selection of the components. The result of the algorithm, however, is a set of key variables which must be translated into a hardware prototype. This section starts presenting the simulation results of the optimal identified solution by the PSO, and describes the further steps towards a hardware implementation.

5.3.1 Simulation results of optimization algorithm

For all the simulations, the PSO parameters were selected as a tradeoff between convergence speed and exploration of the solution space: $\omega = 0.8$ (inertia coefficient), $k_1 = 0.2$ (cognitive coefficient) and $k_2 = 0.2$ (social coefficient). A population of 25 particles was considered, and the algorithm was designed to stop when the relative distance between the optimal objective functions of two consecutive populations was lower than 0.1% for at least 10 consecutive iterations. Since the first population is randomly generated and the particles speed depends on the random terms k_1 and k_2, the algorithm was run multiple times to reduce their impact on the results. The target converter lifetime B_1 was imposed to be larger than 25 years, and the solution space was bounded as follows: $f_{\text{sw}} \in [20\,\text{kHz}, 700\,\text{kHz}]$, $n \in [3.2, 4]$, $M_{\text{core}} \in \{\text{N27}, \text{N87}, \text{N97}\}$, $T_{\text{FET}} \in \{\text{Si}, \text{GaN}\}$, $R_{\text{DS,ON,SRC}} \in [1\,\text{m}\Omega, 20\,\text{m}\Omega]$, $R_{\text{DS,ON,b}} \in [10\,\text{m}\Omega, 200\,\text{m}\Omega]$. The ranges of the conduction resistances were set according to the dataset of commercially available transistors.

The range of n was set by imposing that the boost gain G_1 is always bounded between $G_{1,\text{min}} = 1$ (minimum achievable gain in a boost converter) and $G_{1,\text{max}} = 5$ (corresponding to approximately half of power processed by the boost at the rated MPP voltage) for all the MPP voltages of the mission profiles. Considering that the SRC is supposed to work at resonance, with gain equal to $2n$, the total IPOS converter gain is expressed by:

$$G_{\text{tot}} = \frac{V_{\text{out}}}{V_{\text{in}}} = 2n + G_1 \,. \tag{5.34}$$

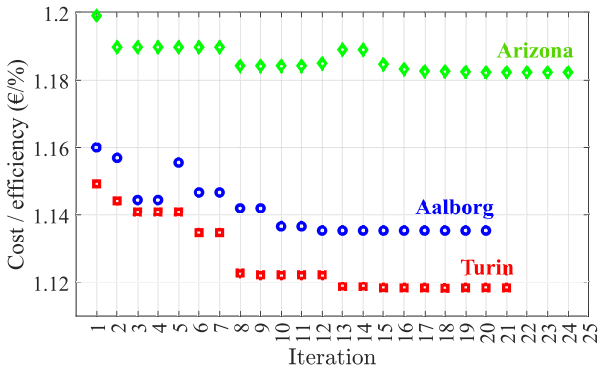


Fig. 5.16 Evolution, iteration after iteration, of the optimal objective function found by the population of particles, for the three mission profiles.

Consequently, imposing the boundaries of G_1 leads to the derivation of the interval of admissible n:

$$\begin{cases} G_1 = \frac{V_{\text{out}}}{V_{\text{in}}} - 2n \leq G_{1,\max} \\ G_1 = \frac{V_{\text{out}}}{V_{\text{in}}} - 2n \geq G_{1,\min} \end{cases} \longrightarrow \frac{1}{2}\left(\frac{V_{\text{out}}}{V_{\text{in,min}}} - G_{1,\max}\right) \leq n \leq \frac{1}{2}\left(\frac{V_{\text{out}}}{V_{\text{in,max}}} - G_{1,\min}\right) \tag{5.35}$$

Fig. 5.16 shows the evolution of the optimal objective function found by the population of particles at each iteration, for the three mission profiles. As it can be seen, the mission profile has an impact on the optimal objective function: the largest cost-efficiency ratio is found for the Arizona mission profile, characterized by the harshest environmental conditions which requires more expensive devices to meet the reliability constraint. The simulation time using an AMD Ryzen 5 3500U processor was around 15 minutes for Turin and Aalborg, and around 25 minutes for Arizona, for which the identification of the initial population surviving the reliability constraint required more time.

The optimal parameters sets and the associated B_1 found by the PSO are reported in Tab. 5.9. The results allow to extract multiple considerations:

- the optimal switching frequency range for the three mission profiles, mainly affecting the cost and size of the transformer and input capacitor, is only slightly dependent on the mission profile. The N27 ferrite, which is optimized for lower frequencies, is discarded from all the solutions;

Table 5.9 Results of the optimization algorithm for three different mission profiles: Aalborg (Denmark), Turin (Italy), Arizona (USA).

Mission profile	f_{sw}	n	M_{core}	T_{FET}	$R_{DS,ON,SRC}$	$R_{DS,ON,b}$	B_1
Aalborg	270 kHz	4	N87	Si	8.4 mΩ	150 mΩ	28 years
Arizona	240 kHz	4	N87	Si	8.5 mΩ	44 mΩ	26 years
Turin	270 kHz	4	N87	Si	12.3 mΩ	107 mΩ	26 years

- for all the mission profiles, the preferred FET technology is Silicon which, despite the worse switching performance for the same $R_{DS,ON}$, exhibits more competitive costs. With the rapidly increasing maturity of GaN technology, this result may probably be overcome in few years.

Above all, the most relevant observation concerns the optimal turns ratio, which for all the cases was $n = 4$, the largest in the admissible range identified by (5.35). According to (5.34), the largest n minimizes the boost gain in the target voltage range. This result is relevant because it allows to justify and validate the initial claims for the adoption of this converter topology, based on the asymmetric IPOS approach. The largest n corresponds, indeed, to the most unbalanced power splitting between the SRC and boost stages. The optimization results confirm that the minimization of the power processed by the boost not only corresponds to an improvement of the converter efficiency, but also reduces the cost and size of the DC filtering capacitors and improves the reliability of the converter.

As shown in the last column of the table, the computed lifetimes of the optimal solutions are slightly larger than the specified target. This result is expected, because in general the PSO privileges cheaper semiconductor devices, associated to a lower converter reliability. The results would be significantly different if the converter lifetime was included among the objective functions. The optimal FETs conduction resistances strongly depends on the mission profile. The Arizona mission profile, characterized by almost daily high irradiance and temperature peaks, the minimum conduction resistances are obtained for both the SRC and boost devices.

It is also relevant to observe that the average ambient temperature of a mission profile directly affects the electrical stresses of the SRC and boost transistors. According to (5.8), indeed, lower ambient temperatures increase the MPP voltage, reducing the boost gain requirement and, consequently, the electrical stresses on

its devices. This result is evident in the Aalborg case, where the lower average temperatures result in more relaxed $R_{\mathrm{DS,ON,b}}$.

Clearly, the suggested parameters set should be considered as a starting point for the selection of real components. Other constraints, such as the components availability or space limitations, should be taken into account while designing a real prototype. If the location of the PV installation is not known *a priori*, the worst case optimal solution should be considered.

To prove that the optimal $R_{\mathrm{DS,ON}}$ of the converter transistors allow to never exceed the maximum junction temperatures, Figs. 5.17a, 5.17b and 5.17c show the time-series of the junction temperatures of the semiconductor devices. The most conservative $R_{\mathrm{DS,ON,SRC}} = 8.4\,\mathrm{m\Omega}$ and $R_{\mathrm{DS,ON,b}} = 44\,\mathrm{m\Omega}$ were selected so as to be compliant with the lifetime constraint. The simulations were run for T_{FET} =Si, $f_{\mathrm{sw}} =$ 250 kHz and $n = 4$. As shown in the figures, the maximum junction temperature 175 °C is never exceeded by any transistor in any mission profile.

5.3.2 SRC design

The main design equations and expressions of the electrical stresses of the SRC components are an integral modelling part of the proposed optimization algorithm. The selection of the components for a physical prototype was based on the worst-case electrical stresses in the worst-case mission profile (Arizona). The selection of the SRC MOSFETs was, clearly, based on the recommended optimal $R_{\mathrm{DS,ON,SRC}}$ identified by the algorithm, rounded to the closest available value among the commercial parts. A 9 mΩ N-channel MOSFET was selected for M_{1-4}, STMicroelectronics STL50N6F7[6]. From the MOSFET selection, the computation of the maximum magnetizing inductance to achieve their ZVS turn-on follows [170]:

$$L_{\mathrm{m}} < \frac{t_{\mathrm{dead}}}{8 C_{\mathrm{oss,eq}} f_{\mathrm{sw}}}, \tag{5.36}$$

where $C_{\mathrm{oss,eq}}$ is the charge-equivalent output parasitic capacitance of a single MOSFET. This was computed by fitting the experimental non-linear $C_{\mathrm{oss}}(v)$ (reported in the device datasheet) with a double exponential function, and using (5.37) to impose

[6]https://www.st.com/resource/en/datasheet/stl50n6f7.pdf.

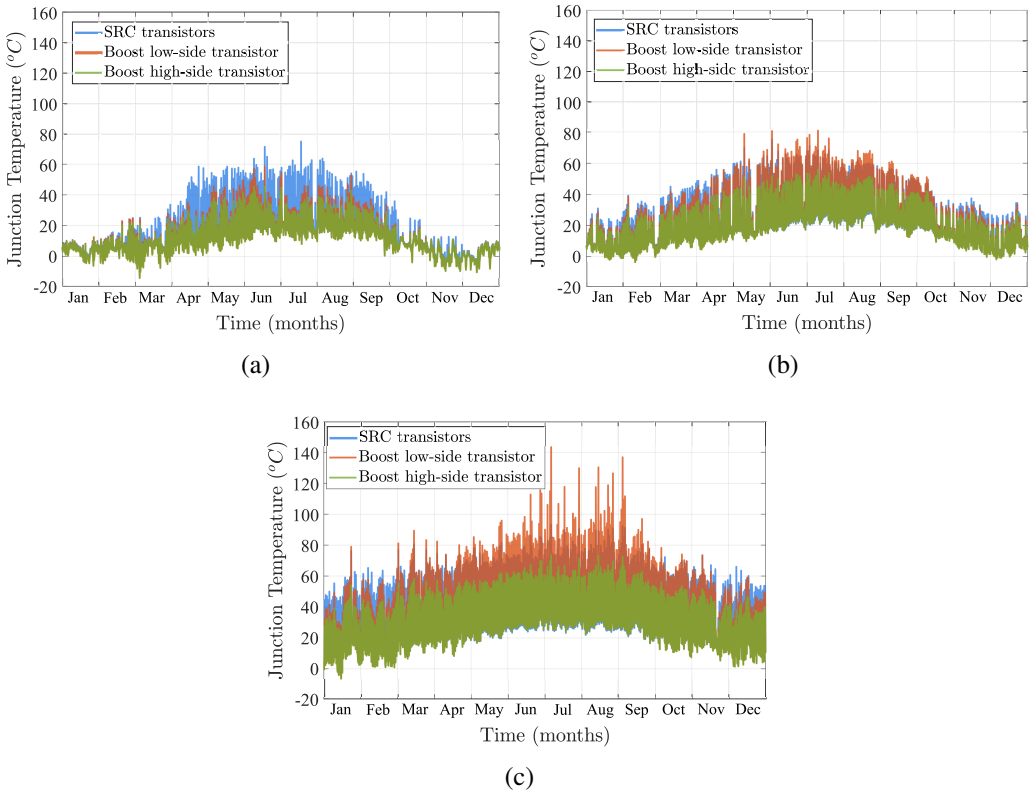


Fig. 5.17 Simulated junction temperature profiles of the SRC, boost low-side and boost high-side MOSFETs according using the optimal $R_{\mathrm{DS,ON,SRC}} = 8.4\,\mathrm{m\Omega}$ and $R_{\mathrm{DS,ON,b}} = 44\,\mathrm{m\Omega}$ from the worst-case mission profiles: (a) Junction temperatures referred to Aalborg mission profile; (b) Junction temperatures referred to Turin mission profile; (c) Junction temperatures referred to Arizona mission profile.

that $C_{\mathrm{oss,eq}}$ stores the same charge as $C_{\mathrm{oss}}(v)$:

$$C_{\mathrm{oss,eq}}(v)\cdot v = \int_0^v C_{\mathrm{oss}}(v')dv' \longrightarrow C_{\mathrm{oss,eq}}(v) = \frac{1}{v}\int_0^v C_{\mathrm{oss}}(v')dv'\,. \tag{5.37}$$

For the specific selected MOSFET:

$$C_{\mathrm{oss,eq}}(v) \approx \frac{3.198\cdot\left(1-e^{-0.111v}\right)+29.34\cdot\left(1-e^{-0.0302v}\right)}{v}\,[\mathrm{nF}]\,, \tag{5.38}$$

which, evaluated for $v = V_{\mathrm{in}} \in [30\,\mathrm{V}, 40\,\mathrm{V}]$, gives $C_{\mathrm{oss,eq}} \in [595, 686]\mathrm{pF}$. With $f_{\mathrm{res}} = 250\,\mathrm{kHz}$ and assuming that the deadtime is 80 ns (2 % of the switching period), (5.36) results in a maximum tolerated $L_{\mathrm{magn}} = 58\,\mu\mathrm{H}$. A more conservative value

$L_{\text{magn}} = 40\,\mu\text{H}$ was considered for the transformer prototype design.

The only relevant missing parameters to be designed, and whose design equations are not included in the algorithm, are the resonant tank parameters. For the computation of the high-frequency losses in the transformer and the hard-switching turn-off losses in the full-bridge FETs, only the resonant frequency is needed, independently on the values of the leakage inductance and resonant capacitances. For a practical implementation, the same design equation already derived in Chapter 4.3 can be used, namely (4.48), which imposes a minimum capacitance value to limit the worst-case sinusoidal voltage ripple below V_{oSRC}:

$$C_{\text{r}} > \frac{1}{2f_{\text{res}}} \left(\frac{I_{\text{out}}}{V_{\text{oSRC}}} \right)_{\text{max}} . \tag{5.39}$$

From this equation, the leakage inductance of the transformer, seen at the secondary port, can be evaluated as:

$$L_k = \frac{1}{(2\pi f_{\text{res}})^2 \cdot 2C_{\text{r}}} . \tag{5.40}$$

Custom transformer design

The specifications for the design of the custom high-frequency transformer are reported in Tab. 5.10: some of them, such as the rated frequency and turns ratio, come directly from the optimal parameters identified by the optimization algorithm; other, such the maximum current, voltage and power ratings, depend on the worst-case electrical stresses, according to the mission profile; the magnetizing and leakage inductances were derived, finally, based on the above-mentioned design equations. The maximum AC resistances of the windings were given to limit the winding losses below 2 % of the rated transferred power.

The transformer was manufactured in two prototypes using the core ETD 34/17/11, with 4 turns of the primary coil and 16 for the secondary. A Litz wires consisting of 2400 strands with 50 µm diameter was used for the primary coil, while a Litz wire with 225 strands of 71 µm diameter for the secondary. The characterization of the main design parameters for the transformer prototype mounted on the converter PCB is reported in Tab. 5.11. Beside the magnetizing inductance, which

Table 5.10 Design specifications of the custom SRC transformer.

Design specification	Value
Rated frequency	250 kHz
Rated power	420 W
Configuration	1 primary coil, 1 secondary coil
Turns ratio $n = \frac{N_2}{N_1}$	4
Peak primary voltage	40 V
Maximum primary current (RMS / peak)	12.8 A / 18 A
Peak secondary voltage	320 V
Maximum secondary current (RMS / peak)	3.2 A / 4.5 A
Leakage inductance seen at the secondary coil	10 µH–20 µH
Magnetizing inductance seen at the primary coil	32 µH–40 µH
Target primary winding AC resistance	<25 mΩ
Target secondary winding AC resistance	<400 mΩ
Isolation type	Basic

Table 5.11 Main parameters of the transformer prototype.

Parameter	Measured value
Magnetizing inductance seen at the primary coil	42.5 µH
Leakage inductance seen at the secondary coil	15.5 µH
Primary winding DC resistance	1.2 mΩ
Secondary winding DC resistance	17.8 mΩ

slightly exceeds the given specification, the rest of the parameters are included in the target ranges. A picture of the transformer prototype mounted on the PCB is shown in Fig. 5.18.

5.3.3 Boost design

The main design equations for the selection of the boost components were already integrated in the optimization algorithm, as well as for the SRC. As in the previous IPOS project, the BCM operation was selected for its beneficial reduction of the switching losses in the low-side MOSFET M_{LS}, thanks to the inherent ZVS turn-on.

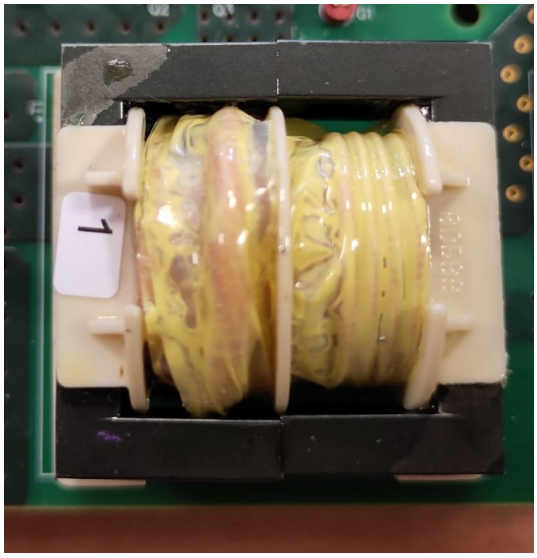


Fig. 5.18 Picture of the transformer prototype

50 mΩ-400 V N-channel MOSFETs, STB41N40DM6AG[7] were selected, due to the current unavailability of off-the-shelf STMicroelectronics components with lower $R_{DS,ON}$ and rated voltage at the time of the definition of the bill of materials. An accurate thermal design is needed to minimize the thermal resistance between junction and ambient, so as to still be able to meet the reliability constraints.

It is relevant to observe that the inductor design was not included in the optimization procedure, but was assumed to be a fixed component. Its inductance value, $L_b = 33\,\mu H$, was indeed selected according to preliminary investigation on the switching frequency in the BCM. As explained in details in Chapter 4.3, the operating frequency in a boost controlled in the BCM depends on the load and voltage gain and can be designed to be bounded in a certain range by properly selecting the inductance, according to (4.57). The choice of a fixed inductor component, effectively representing a constraint in the algorithm, simplifies the search of the optimal solution and reduces the need of a custom magnetic design to the transformer alone.

The sizing of the input and output DC filter capacitors of the boost was based on (4.69) and (4.65), respectively.

[7] https://www.st.com/resource/en/datasheet/stb41n40dm6ag.pdf

Table 5.12 Selected components for the converter prototype designed according to the optimal solution.

Component	Value	Part number
SRC switches M_{1-4}	N/A	STL50N6F7
Transformer core	N/A	ETD 34/17/11, N97
Transf. primary coil	N/A	4 turns, 2400 x AWG 44
Transf. secondary coil	N/A	16 turns, 225 x AWG 41
Resonant capacitors C_{r1-r2}	15 nF	R76PF215050H3J
Rectifier diodes D_{1-2}	N/A	STTH10R04G-TR
SRC output capacitor C_o	1 µF	R75PR4100AA30K
Boost switches M_{HS-LS}	N/A	STB41N40DM6AG
Boost inductor L_b	33 µH	74437529203330
Boost capacitor C_b	10 µF	R75MW51004030J
Input capacitor C_{in}	23.5 µF	5x CB182D0475JBC

The complete bill of materials for both the SRC and boost converters is reported in Tab. 5.12.

5.4 Experimental results

5.4.1 Schematic and layout design

The schematic and layout of the PCB prototype were designed in *Altium Designer*[8]. As it was done for the prototype in Chapter 4, this section describes the block diagram of the implemented schematic, while the pictures of the complete schematic sheets can be found in Appendix A. The main domains, blocks and connections of the schematic, which consists of four sheets, are illustrated in Fig. 5.19.

Due to the similarity of the topologies, the block diagram exhibits only minor differences with respect to the one presented in Fig. 4.22. The only relevant difference is the VDR replacing the topology-morphing rectifier in *Sheet 3*, which does not require additional floating supply voltages or gate drivers. The rest of the block diagram is essentially analogous: *Sheet 1* includes the synchronous boost with its gate driver and ZCD circuit (implemented in the same way), *Sheet 2* contains the full-bridge inverter and transformer of the SRC, and *Sheet 4* includes the remaining parts of the schematic, devoted to the auxiliary power supply generation, filtering of the input voltage, acquisition of the critical electrical quantities for the control, and connections with the control board, source, and load.

The layout of the PCB prototype was designed on the basis of the schematic presented so far. The size of the resulting four-layer PCB is 210 mm by 129 mm, with 1.6 mm thickness. The PCB area is approximately 27 % smaller than the PCB prototype of the multi-mode IPOS converter, especially because of the smaller boost inductor and SRC transformer, the reduced number of input DC-filter capacitors and the absence of the topology-morphing rectifier.

The primary goals of the layout design were to ensure the correct operation and to validate the expected performances of the proposed optimized converter, while offering the possibility of monitoring the main currents and voltages through test-points and shunt resistors. In general, the layout design focused on minimizing the resistive and inductive parasitics of the traces (especially around the gate driver), by optimizing the components placement and tuning the traces widths. Specific attention was devoted to the maximization of the copper areas below the thermal pads

[8]https://www.altium.com/altium-designer (accessed Jan. 20th, 2026).

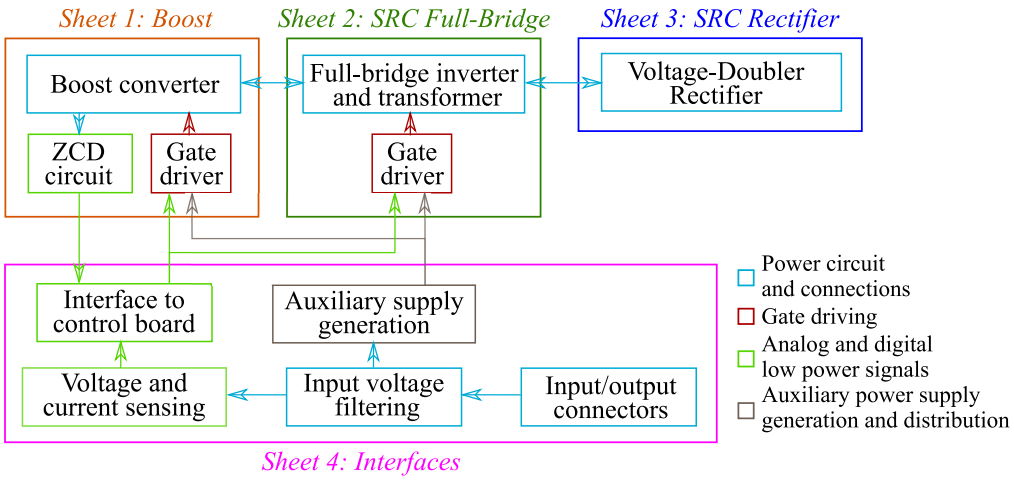


Fig. 5.19 Block diagram of the schematic of the converter prototype, highlighting the main blocks and connections, and the division into the four sheets in *Altium Designer*.

of the SMD semiconductor devices, which directly affect their junction-to-ambient thermal resistances.

Fig. 5.20 shows the top-layer view of the PCB, highlighting the areas devoted to each main part of the schematic. On the upper left corner of the board, the two headers ensure the connection with the NUCLEO development board. The SRC is located in the lower part of the PCB, while the boost components are located in the upper right one. The transformer, boost inductor and output film capacitors exhibit through-hole packages, while all the power semiconductor devices were selected in SMD packages for their improved thermal conductivity: no heat-sink, indeed, is designed for the prototype, and the generated heat must be dissipated uniquely through the PCB. Most of the components of the converter are soldered on the top layer.

Fig. 5.21 illustrates the first of the two inner layers of the PCB, devoted primarily to the routing of supply traces for both the 3.3 V and 12 V supply voltages, and to reinforcement copper planes to enhance the heat dissipation of some critical high current traces / planes of the top layer. The exploitation of copper areas on multiple layers, interconnected by uniformly distributed thermal vias allows to reduce the equivalent resistance of the traces and ensure an improved distribution oh heat. The same approach is also exploited in the bottom layer, where the copper areas can exchange more effectively the dissipated heat with the air, improving the thermal conductivity of the PCB.

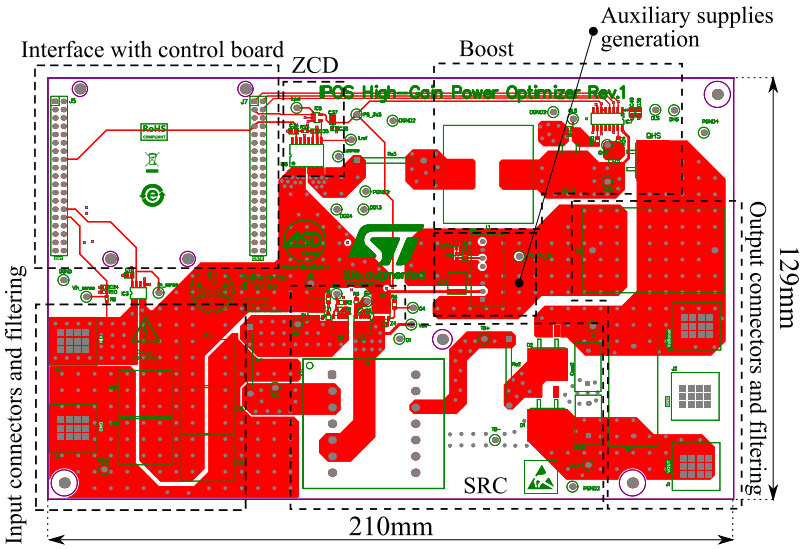


Fig. 5.20 Layout of the top layer of the PCB prototype.

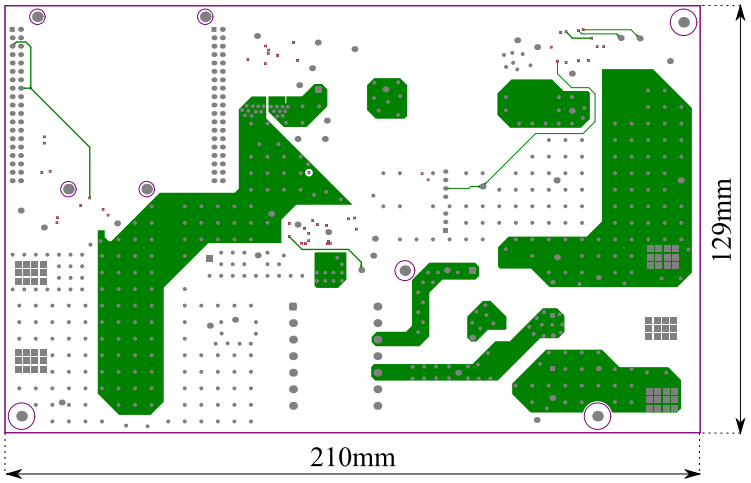


Fig. 5.21 Layout of the first inner layer of the PCB prototype.

Fig. 5.22 shows the layout of the second inner layer, which is entirely occupied by the ground planes, except for the areas below the two magnetic components of the converter, the boost inductor and SRC transformer. The digital ground plane, developed in the upper and left part of the layout, is electrically connected to the power ground of the converter, extended through the remaining surface area. The surface maximization of the ground plane allows to minimize the loop inductances in the return paths of the converter.

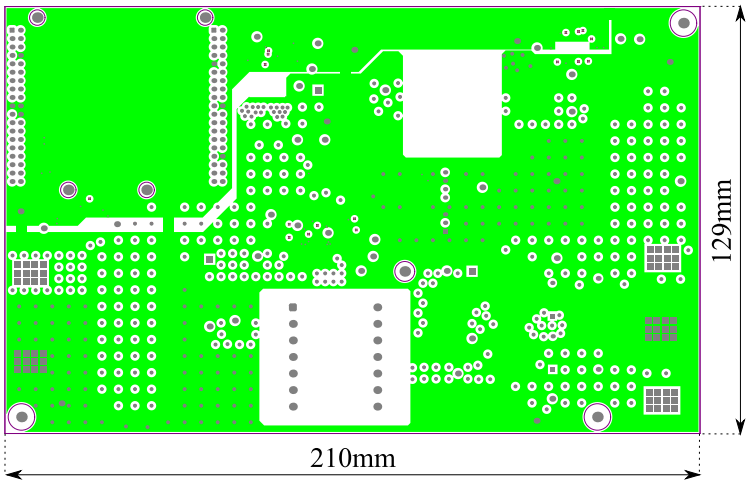


Fig. 5.22 Layout of the inner ground layer of the PCB prototype.

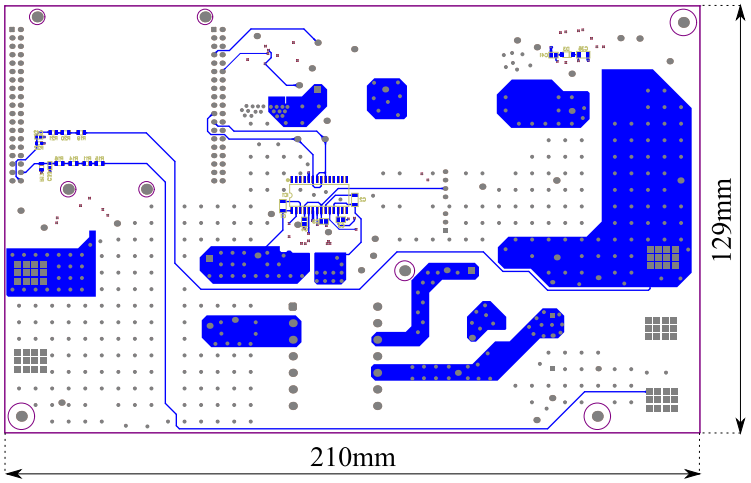


Fig. 5.23 Layout of the bottom layer of the PCB prototype.

Finally, Fig. 5.23 shows the layout of the bottom layer, devoted primarily to the placement of the gate driver of the SRC full-bridge MOSFETs, and of the voltage partition networks on the input and output voltages. As for the first inner layer, reinforced copper traces and planes were located in the bottom layer to improve the thermal and electrical performance of the high current paths.

A picture of the PCB prototype, assembled by the external company *ASD*[9], is shown in Fig. 5.24.

[9]https://www.webasd.com/

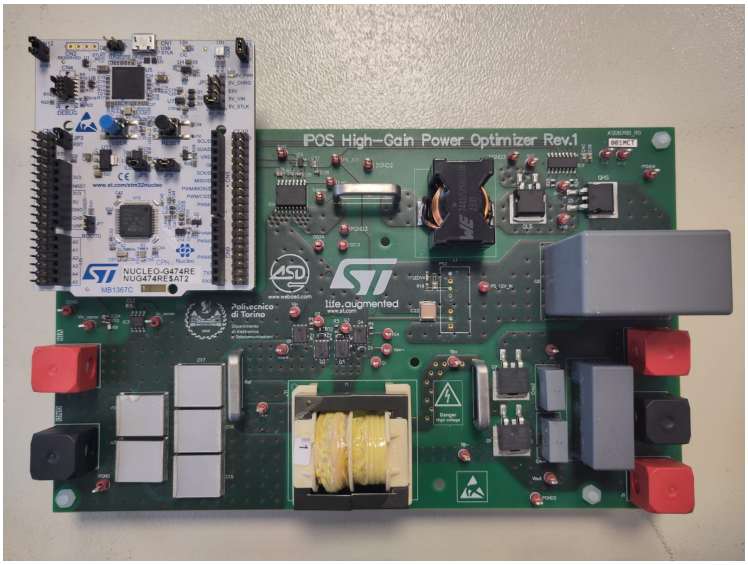


Fig. 5.24 Photo of the PCB prototype used for the experimental characterization.

5.4.2 Control design and implementation

The primary goal of the experimental validation of a prototype was, as in the previous case, the characterization of the converter performances. In this project, given the additional focus on the converter reliability, the measurements of the components temperatures were needed as well to validate the thermal models used in the optimization.

For these purposes, open-loop tests were run at various operating conditions. The converter operation, as explained, reproduces exactly the MV mode of the previously proposed IPOS multi-mode converter (SRC operating at resonance with VDR, boost in BCM). As a consequence, the voltage gain depends on the conduction time T_{ON} of the boost low-side MOSFET, as derived in (4.74), and the resulting switching frequency of the BCM operation can be expressed by (4.57). The physical implementation consisted in setting the correct timing intervals of the gating signals for the synchronous boost to achieve the target voltage gain at the each load condition.

As in the previous case, the development board STMicroelectronics NUCLEO-G474RE[10] was programmed in STM32CubeIDE to generate the PWM signals. Fig. 5.25 shows the pinout view of the target microcontroller in STM32CubeMX environment. A more detailed description of the configuration of the pins can be

[10]https://www.st.com/en/evaluation-tools/nucleo-g474re.html

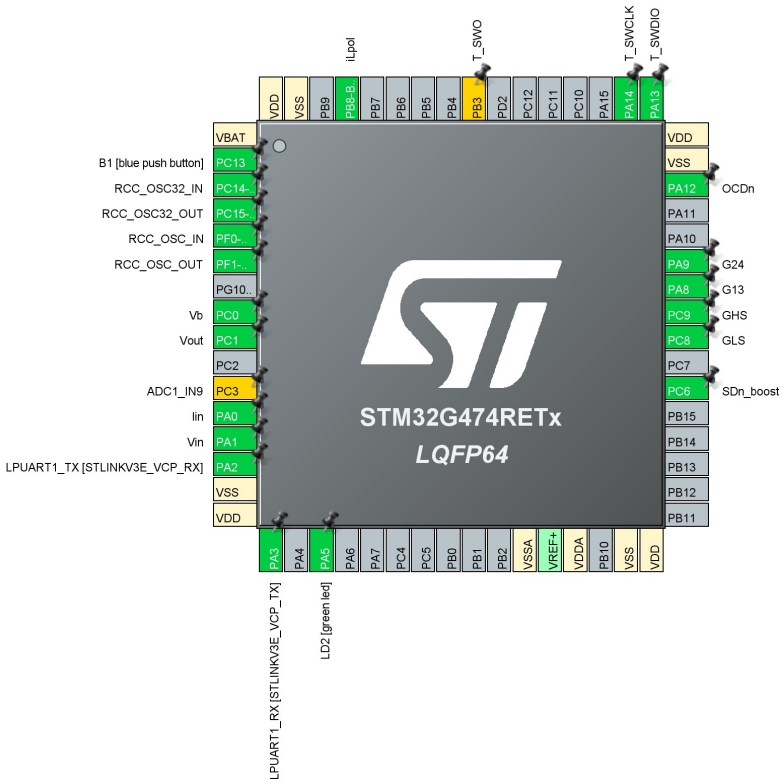


Fig. 5.25 Pinout view of the target microcontroller in STM32CubeMX environment.

found in Section 4.5.2, as the two implementations are mostly identical: the only relevant difference is that the GPIO pins previously devoted to drive the auxiliary MOSFETs of the topology-morphing rectifier are not used here. The organization and tasks of the firmware code are the same.

5.4.3 Experimental waveforms

Preliminary experimental tests on the hardware prototype shown in Fig. 5.24 were carried out in a laboratory of the System Research and Applications (SRA) division of the Catania site of STMicroelectronics. The definitive characterization tests, on the other hand, were performed in a laboratory at the Department of Energy of Politecnico di Torino, using the same experimental setup described in Section 4.5. In addition, the infrared thermo-camera Fluke FLK-TIS75+[11] was used to monitor the case temperatures of the converter transistors.

[11] https://www.fluke.com/it-it/prodotto/termocamera/tis75plus#

In this section, the main experimental waveforms of the SRC and boost converters are reported to validate the correct operation of the proposed PPO, at steady state. The SRC waveforms include the control and output voltages of MOSFET M_2, namely v_{GS2} and v_{DS2} (both referred to the common power ground), and the voltage and current at the primary side of the transformer, namely v_{prim} and i_{prim}. For the boost, the waveforms include the control voltages of the low-side and high-side transistors, namely $v_{GS,LS}$ and $v_{GS,HS}$, the switching node voltage v_{sw} (which also coincides with the drain-source voltage of M_{LS}) and the inductor current i_L.

Fig. 5.26 shows the experimental waveforms characterized at $V_{in} = 35\,V$ (close to the rated MPP voltage), and at two different operating powers, namely at half of the rated power (220 W) and at the rated PV power (440 W).

Figs. 5.26a and 5.26b show the boost and SRC waveforms at 220 W, respectively. At $V_{in} = 35\,V$, the boost realizes a gain equal to 2, corresponding to processing around 20 % of the total input power; in a complementary way, the SRC processes the remaining 80 %. The SRC waveforms show a near-ZVS of M_2, highlighting that the primary current is insufficient to completely discharge its output capacitance during the deadtime. The linear rise/fall of i_{prim} in correspondence of the switching of the full-bridge legs, not predicted by the theoretical waveforms in Fig. 5.6, was already observed in the experimental results of the proposed multi-mode IPOS converter, and is linked to the non-instantaneous switching of the rectifier diodes [191].

Figs. 5.26c and 5.26d show the boost and SRC waveforms at 440 W, respectively. The boost waveforms are characterized by the typical triangular current of the inductor. While the duty cycle is still close to 50 %, as in Fig. 5.26a, both the ON-time and the switching period are increased due to the increased power. It should be noted that the negative current extension exploited for the BCM allows to achieve a full ZVS of the low-side transistor in both the power conditions, with $I_R = -0.8\,A$. The SRC waveforms underlines a full ZVS turn on of M_2, which completely eliminates the ringing on v_{prim} and v_{DS2}.

5.4.4 Efficiency characterization

The converter efficiency was characterized experimentally in the designed target power and input voltage range. Before presenting the efficiency graphs, it is relevant

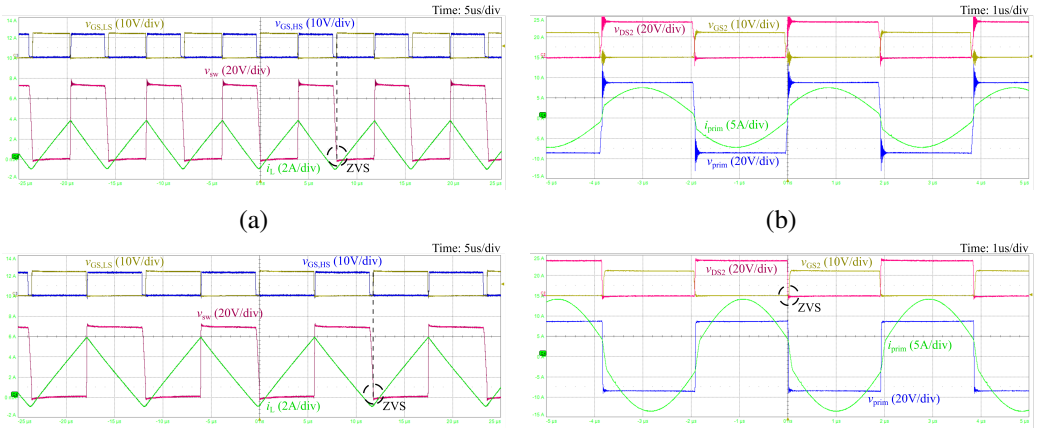


Fig. 5.26 Main experimental waveforms of the boost and SRC stages of the converter prototype. For the boost converter, the waveforms refer to the inductor current i_L, low side MOSFET M_{LS} gate and output voltages ($v_{GS,LS}$ and $v_{DS,LS}$, respectively) and high side gate-source voltage $v_{GS,HS}$. For the SRC, the waveforms refer to MOSFET M_2 gate-source and output voltage ($v_{GS,2}$ and $v_{DS,2}$, respectively), transformer primary voltage v_{prim} and current i_{prim}. (a) Boost waveforms, half power 220 W; (b) SRC waveforms, half power 220 W; (c) Boost waveforms, rated power 440 W; (d) SRC waveforms, rated power 440 W.

to remind, as it was done for the multi-mode IPOS converter, that resonant converters such as the SRC exhibit some frequency-dependent losses that affect negatively the light load efficiency. In order to improve the efficiency at reduced operating powers, several techniques based on half cycle [124] or complete cycles [90] skipping were developed. Fig. 5.27 shows the qualitative waveforms of the control voltages of MOSFETs M_1 and M_2 (of the SRC full-bridge), and the primary voltage and current of the high-frequency transformer. More in details, at the rated operation (Fig. 5.27a), the control voltages are complementary, and all the waveforms exhibit a T_{sw} periodicity. The one-cycle skipping approach, shown in Fig. 5.27b, consists in skipping one complete cycle every two, resulting in a doubled fundamental period of all the electrical waveforms. In other terms, the effective duty cycle of the control voltages is reduced from 50 % to 25 %. On the other hand, Fig. 5.27c shows the qualitative waveforms referred to the half-cycle skipping technique, consisting in applying a further 90° phase delay of the control voltages M_2. In both the cases, the overall effect is to halve the effective fundamental frequency of the converter. It is relevant to notice that, for the same load, the current stresses of the transformer and transistors need to increase to cope with the discontinuous power transfer. At lighter loads, where the current stresses would be low in any case, the stress increase is fully

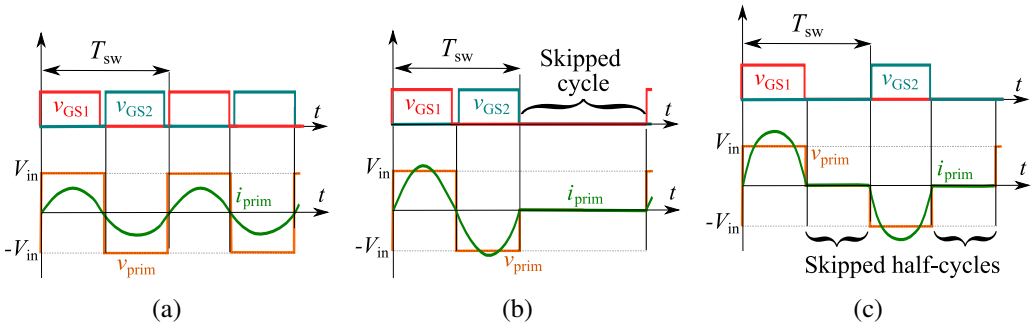


Fig. 5.27 Comparison of the qualitative waveforms of the control voltages of M_1 and M_2, and transformer primary current and voltage, with different approaches to light-load efficiency enhancement: (a) Rated frequency operation; (b) One-cycle skipping; (c) Half-cycle skipping.

compensated by the reduced frequency-dependent losses (core and driving losses), resulting in an effective efficiency enhancement, as it will be shown. Fig. 5.28 shows the experimental waveforms of the control and output voltages of M_2 (in order to verify the presence of soft-switching), and of the primary transformer current i_{prim} using the above mentioned techniques: rated frequency operation (Fig. 5.28a), one-cycle skipping (Fig. 5.28b) and half-cycle skipping (Fig. 5.28c). The waveforms were extracted for the same operating condition: $V_{in} = 36.5\,V$, $P_{out} = 88\,W$ (20 % of the rated power). As highlighted qualitatively, it is possible to observe that the peak resonant current of the transformer is almost doubled in the one-cycle and half-cycle skipping cases, compared to the rated operation. Except for a near-ZVS turn-on of M_2 highlighted in Fig. 5.27c, in general the cycle-skipping techniques do not preserve the soft switching.

Fig. 5.29 shows the measured converter efficiency as a function of the operating power, at the rated MPP voltage of the target PV panel, $V_{in} = 36.5\,V$. The efficiency was characterized in correspondence of the discrete power levels used to compute the EURO and CEC efficiency. As it can be seen, the one-cycle skipping technique was implemented at 5 %, 10 % and 20 % of the rated power, resulting in significant efficiency enhancement (almost 6 % improvement at the lowest power level). The converter exhibits almost 95 % EURO efficiency and around 95.3 % CEC efficiency. It is relevant to observe that the one-cycle skipping enhances by 0.9 % the EURO efficiency, which privileges more the light-load performance of a converter. The peak efficiency, 96 %, is measured at 50 % of the rated power.

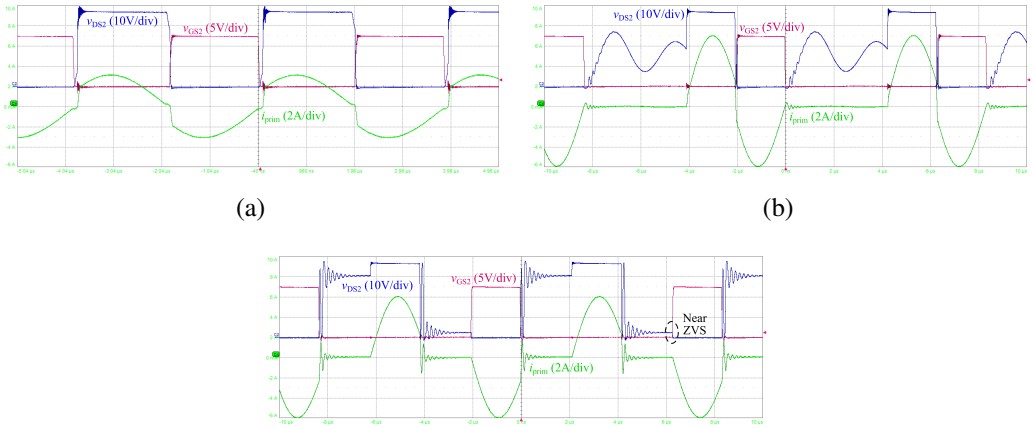


Fig. 5.28 Experimental waveforms ($v_{GS,2}$, $v_{DS,2}$ and i_{prim}) of different cycle-skipping approaches to improve the light-load efficiency of the SRC of the proposed converter. The waveforms refer to the rated $V_{in} = 36.5\,V$ and to 20 % of the rated power, $P_{out} = 88\,W$: (a) Normal operation (no cycle skipping); (b) One-cycle skipping; (c) Half-cycle skipping.

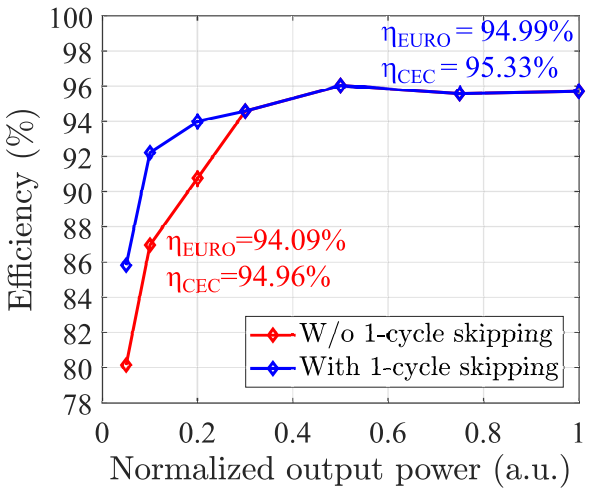


Fig. 5.29 Measured efficiency VS output power, at the rated input voltage $V_{in} = 36.5\,V$. At lighter loads, the one-cycle skipping technique allows to significantly enhance the conversion efficiency.

Fig. 5.30 shows the measured efficiency and share of power processed by the boost as functions of the input voltage (in a voltage range compliant with the simulated mission profiles, 33 V–38 V) and at different power levels (20 %, 50 % and 100 % of the rated power). The combined plots allow to extract relevant information on the impact of the SRC and boost losses as function of the working point. For instance, at 20 % of the rated power, the lowest efficiency is characterized at $V_{in} = 38\,V$,

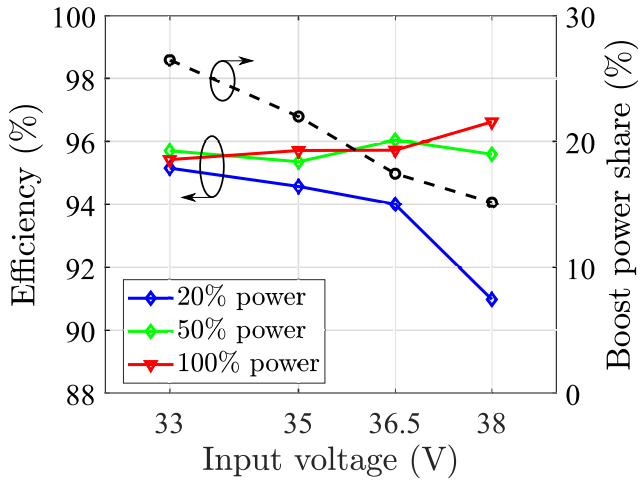


Fig. 5.30 Measured efficiency and share of power processed by the boost as functions of the input voltage, at different power levels.

where the transformer core losses are more dominant. At the rated power, on the other hand, the efficiency monotonically decreases from 38 V to 33 V, in accordance with the increased power processed by the boost.

Fig. 5.31 illustrates the simulated loss breakdown of the converter, at $V_{\text{in}} = 36.5\,\text{V}$ and 440 W power. Due to the absence of current shunts in each converter branch, it was not possible to characterize it experimentally. The simulations were performed in Simetrix[12] using an equivalent parallel resistance to emulate the transformer core losses, while its windings resistances were estimated using Tourkhani's model [192]. The pie plot highlights that most of the losses are obtained in the SRC, as it processes most of the input power. Beside the transformer, which accounts alone for slightly less than 50 % of the total losses, the SRC MOSFETs and diodes are components contributing the most in terms of losses. The measured total losses in the same operating point were around 18.6 W, around 16 % more than the simulated one, probably due to the losses in the PCB traces and the simplified transformer models.

[12] https://www.simetrix.co.uk/.

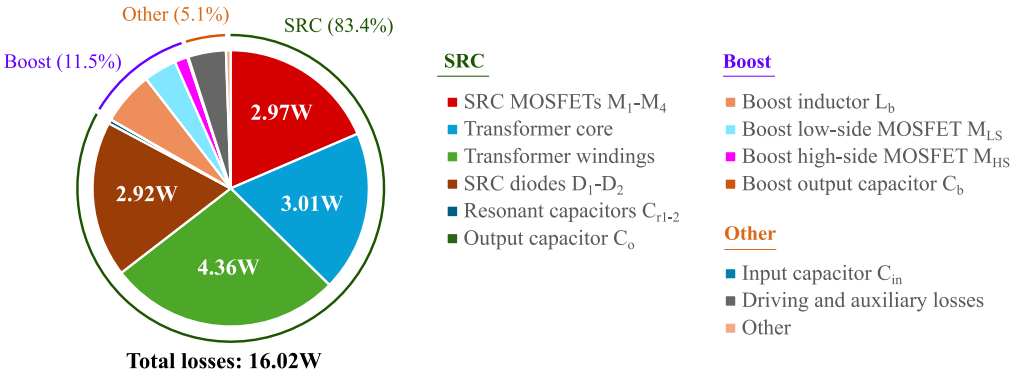


Fig. 5.31 Simulated loss breakdown of the converter at the rated PV panel MPP ($V_{\text{in}} = 36.5\,\text{V}$, $P = 440\,\text{W}$.

5.4.5 Thermal characterization

The final part of the converter characterization involves the measurement of the temperatures of the semiconductor devices, whose variations, as seen, are directly associated to their degradation. Unfortunately, a direct measurement of the junction temperatures would require to access the die with thermocouples or optical fibers, an invasive procedure due to the packaging of the device, or to monitor in a more complex way other quantities that are directly or indirectly related to the junction temperatures [216]. In the latter case, specific setup or control approaches are needed, which may conflict with the rated operation of the converter devices.

A simplified and preliminary approach was adopted here: a thermocamera was used to measure the case temperatures of M_2 (representative of all the SRC MOSFETs, given their uniform stresses), M_{LS} and M_{HS}. By means of simulations, the goal was to try to relate the numerical and experimental results and try to validate the thermal model used in the optimization algorithm. This approach is too simplified to offer a reliable estimation of the junction temperatures, but it can be helpful to extract relevant qualitative information on the distribution of losses, more aware insights on the impact of the layout, and highlight the fundamental limitations of the adopted models, which could serve the purpose of further future refinements of this methodology.

Fig. 5.33 shows the interpolation of the measured case temperatures of MOSFETs M_2, M_{LS} and M_{HS} at different working points, identified by the input voltage V_{in} and output power. For each working point, the control variable T_{ON} was set to achieve the desired voltage gain and obtain the target $V_{\text{out}} = 350\,\text{V}$. In absence of load, the case

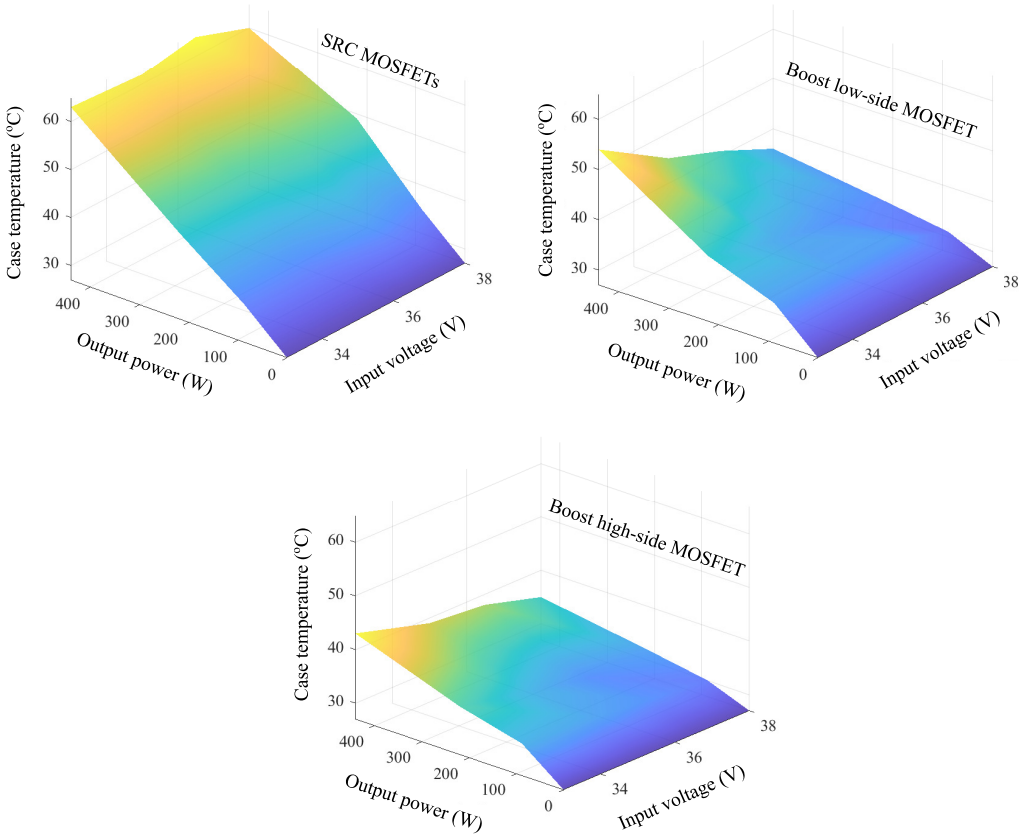


Fig. 5.32 Experimental characterization of case temperatures for the SRC MOSFETs (M_2, specifically), the boost low-side and boost high-side MOSFETs, at different operating conditions ($P_{\text{out}} \in [0\,\text{W}, 440\,\text{W}]$, $V_{\text{in}} \in [33\,\text{V}, 38\,\text{V}]$) and the same ambient temperature, 27 °C.

temperatures coincided with the ambient temperature in the laboratory, 27 °C. All the characterizations were performed the same day, waiting for a sufficient time between two consecutive tests to allow the complete cooldown of the converter components. What is possible to observe at first sight is that the SRC temperature seems to be independent from the input voltage: this is a consistent result, since the current stresses of the full-bridge MOSFETs (and, as a consequence, their conduction losses) only depend on the load power, as highlighted in Tab. 5.2. On the other hand, as already mentioned in Fig. 5.30, decreasing the input voltage means increasing the boost power, resulting in increased losses in its components, especially at heavier loads.

Fig. 5.33 allows to better appreciate the trend of the case temperatures, and to compare the experimental results with the numerical results of case temperatures,

computed on the basis of the worst-case $R_{\text{th,j}-\text{amb}}$ (60 °C/W for the SRC MOSFETs, in a PowerFlat package 5 mmx6 mm, and 42 °C/W for the boost MOSFETs, in a D2PAK package). In particular, for the numerical computation of the case temperature $T_{\text{case,k}}$ (where $k \in \{2, \text{LS}, \text{HS}\}$, the heating of the surrounding components was assumed to not affect it:

$$T_{\text{case,k}} \approx T_{\text{amb}} + P_{\text{loss,k}} \cdot \left(R_{\text{th,j}-\text{amb}} - R_{\text{th,j}-\text{case}}\right), \tag{5.41}$$

where $P_{\text{loss,k}}$ is the computed loss of component k using the loss models in Tab. 5.6. This is a strong assumption, especially for power-dense prototypes. The simultaneous integration of all the heating contributions would require complex multiphysics simulations to extract the thermal impedance of each node of an equivalent thermal circuit.

Fig. 5.33a shows the experimental and numerical case temperatures of M_2. As highlighted previously, the trend is mainly affected by the load power and only marginally by the input voltage. The numerical results highlight a distinctive parabolic trend, related to the squared relationship between the conduction losses and the load power, which actually does not reproduce the experimental results. A potential explanation for this is that the SRC MOSFETs are located close to the high-frequency transformer, as shown in the prototype photo in Fig. 5.24, whose heating may reasonably affect the actual case temperature.

Fig. 5.33b shows the results for the boost low-side MOSFET. The numerical results significantly differ from the measured ones, especially at the heaviest loads. Considering the worst case scenario of $V_{\text{in}} = 33\,\text{V}$, the displacement seems to suggest that the thermal design in the layout (through the maximization of the copper areas) was effective in reducing the thermal resistance way below the limit value 42 °C/W. On the other hand, the worse thermal performance at $V_{\text{in}} = 38\,\text{V}$ may be related to the heating of the nearby boost inductor.

Finally, Fig. 5.33c shows the results for the boost high-side MOSFET, highlighting the closest matching between experimental and numerical results. This phenomenon may be related to the fact that M_{HS} is located close to the border of the PCB (see Fig. 5.24), allowing to improve the heating dissipation by convection and to increase the distance from other heated components. Both the trend and

absolute values of the experimental case temperatures are in good agreement with the numerical results.

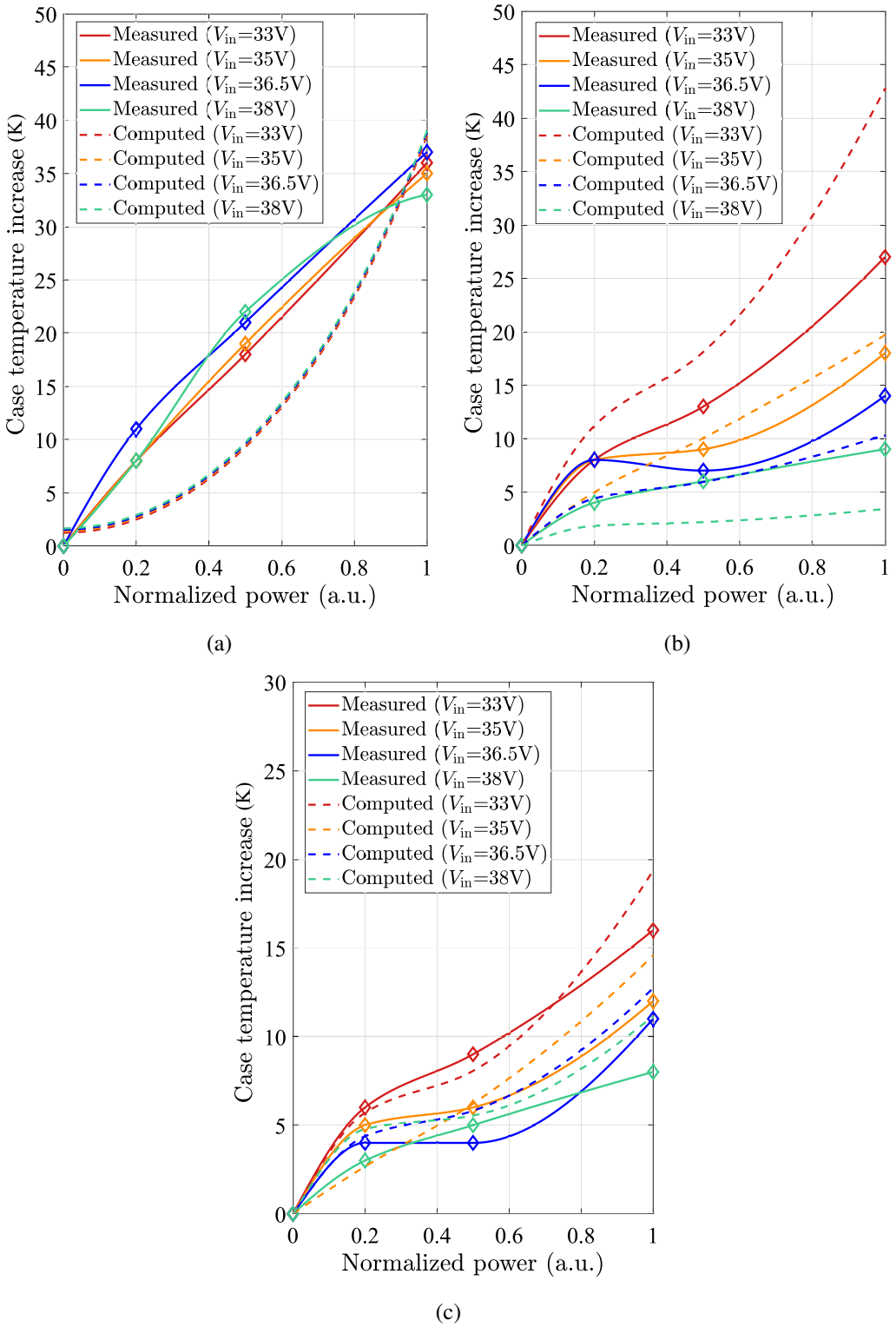


Fig. 5.33 Comparison of experimental and calculated case temperatures for the SRC MOSFETs (M_2, specifically), the boost low-side and boost high-side MOSFETs, for the validation of the thermal model used in the optimization algorithm. The measurements and computations refer to the same operating conditions ($P_{out} \in [0\,\text{W}, 440\,\text{W}]$, $V_{in} \in [33\,\text{V}, 38\,\text{V}]$) and the same ambient temperature, 27 °C: (a) SRC MOSFET M_2; (b) Boost low-side MOSFET M_{LS}; (c) Boost high-side MOSFET M_{HS}.

5.5 Conclusions

This chapter has introduced an innovative design optimization methodology intended for PV-fed power converters, which integrates conventional conflicting objectives such as cost and efficiency. One of the main innovative features of the proposed method consists in integrating the reliability assessment of trial power converter solutions within the optimization algorithm, in terms of an estimation of the converter lifetime. However, differently from previous solutions, which either excluded completely the reliability from the design procedure or included it as an objective function to be optimized (leading to potentially cost-ineffective solutions), in this work the reliability assessment is treated as a constraint to accept or discard a trial converter solution for the following iterations of the algorithm.

In addition, the reliability assessment is based on lifetime models representing the physical degradation of the semiconductor devices due to the repeated thermal stresses, representing a more realistic physics-based approach to model the failures of the converter components, rather than only considering catastrophic random failure modes. Real mission profiles of annual irradiation and ambient temperature from three different locations were inputted in the algorithm for a more representative estimation of the thermal stresses of the semiconductor devices due to the hourly, daily, and seasonal variations of environmental conditions.

The developed methodology was applied to the specific case study of an asymmetric IPOS power optimizer based on a simplified modification of the IPOS multi-mode converter presented in Chapter 4, consisting of an SRC and a synchronous boost stages. After defining the objective function, the minimal number of key design variables of the converter was identified to constitute the solution space, namely the combination of all the potential converter solutions.

Significant attention was devoted to the modelling of the PV source, the electrical stresses of the power converter, cost and losses of the converter components based on the analysis of commercially available parts, and to the reliability of the trial converter according to the simulated thermal stresses of its components. The search algorithm, based on the PSO, was run for the three mission profiles, representative for different climate scenarios, in order to be able to extract meaningful mission profile-dependent considerations. The simulation results revealed that the objective function was optimized for converters solutions in which silicon devices with relatively high

conduction resistance were preferred: Gallium Nitride solutions were discarded for the less competitive costs, result that should probably be reviewed in the upcoming years. Independently from the mission profile, the results also revealed that a strongly unbalanced power processing between the SRC and boost stages is beneficial not only from the efficiency point of view (result already pointed out in the previously presented work), but also from the cost and reliability perspectives.

A PCB prototype was designed and built based on the optimal solution in the worst-case scenario. Open-loop tests were carried out to validate the performance of the optimal converter, showing a EURO efficiency of 95 % at the rated MPP voltage of the target PV panel, 36.5 V. The measurement of the case temperatures of the semiconductor devices during the operation of the converter in different working points allowed to extract some qualitative considerations on the distribution of thermal stresses and to highlight the limitations of the validity of the thermal models used in the algorithm, due to the increased complexity of the heat dissipation mechanisms introduced by the PCB layout.

It is worth noticing that the optimal results are largely affected by the adopted models and by the assumptions made to simplify the problem. Despite this, the developed framework integrates systematically multiple conflicting objectives to assist the design phase, and provides valuable insights on how the main design parameters affect performance, cost and reliability. Beside the specific case study, the proposed methodology has a general validity for other converter topologies or applications in which it is relevant to assist the converter design with reliability-aware considerations.

Chapter 6

A Quasi-resonant PV-fed Battery Charger for Off-grid Applications

As anticipated in Chapter 1 and in Chapter 3, part of the research activities of this PhD program was devoted to the investigation of a new high-efficiency solution for a PV-to-ESS power converter. This chapter illustrates the main steps from the conceptualization of the topology to the experimental characterization of a prototype, and is organized as follows: Section 6.1 describes the design specifications and the derivation of the converter topology, Section 6.2 illustrates the operating principle of the converter in its two operating modes, also providing the analytical derivation of its static characteristic, Section 6.3 derives the electrical stresses of each component and describes an *ad-hoc* hardware design procedure, Section 6.4 presents the main experimental results of a 100 watt PCB prototype, while Section 6.5 draws the conclusion of this work.

The content of this chapter represents the extension of the work originally introduced in [217], whose further developments were presented at the international conference EUROCON [218] and were published in the peer-reviewed journal IEEE Access [219].

6.1 Specifications and topology definition

This section presents the proposed converter topology, highlighting its distinctive and innovative features relative to the current state of the art. Given the analysis of the previous works in this research field, the investigation of a new topology aims at combining the main advantages and overcoming, as far as possible, their limitations. The idea of this work is based on a previously developed grid-connected battery charger [220] that employs a small resonant inductance to enable the ZVS of the input MOSFETs, without introducing additional voltage or current stress on the semiconductor devices. The converter can be engineered to achieve the soft commutation over a wide input power range, making it a promising candidate for photovoltaic PV-fed battery charging applications. The converter topology introduced in [220] is shown in Fig. 6.1a: it consists of a half-bridge inverter, composed of MOSFETs M_1 and M_2, and capcitors C_1 and C_2, a step-down transformer T_1, a center-tapped rectifier composed of diodes D_3 and D_4, and an output inductive filter L_o to smoothen the charging current for the battery. Diodes D_1 and D_2 are added to clamp the maximum voltage across the half-bridge capacitors, ensuring an inherent maximum power transfer limitation. The relatively small resonant inductor (20 µH in the work) is added to assist the ZVS of the half-bridge MOSFETs, namely, to discharge their output parasitic capacitances during the deadtime. The unfiltered rectified grid is represented as an ideal rectified sine wave voltage source, whereas the load low-voltage battery is modelled with an equivalent Thevenin representation. The battery charger in [220] is clearly designed for a different application, for which it offers unity power factor, galvanic isolation and an intrinsic power limitation. However, the straightforward frequency modulation control and the possibility to achieve the soft commutation on a wide range of operating powers makes it an interesting candidate for the PV-to-ESS application.

This work re-engineered the converter topology and the design of its components to adapt it to the different application. The topology investigated in this work is shown in Fig. 6.1b. Differently from Fig. 6.1a, the updated schematic includes an additional input filter capacitor, to stabilize the operating point of the PV panel, removes the transformer, since the galvanic isolation is not needed for the current application, and replaces the diode-based center-tapped rectifier with an active full-wave rectifier, composed of MOSFETs M_{3-6}, aiming at improving the conversion efficiency. The half-bridge structure, the output filter inductor, the clamping diodes

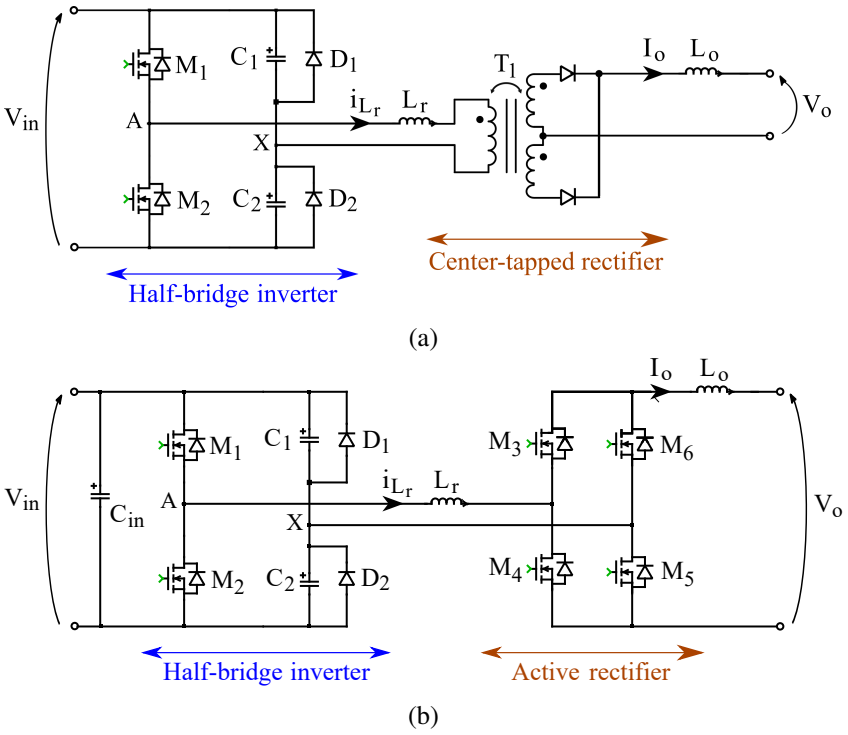


Fig. 6.1 Comparison of the battery charger topologies in [220] and in the proposed solution. (a) Grid-fed battery charger proposed in [220]; (b) PV-fed battery charger proposed in this work.

Table 6.1 Target specifications and design parameters of the converter.

Design specification / parameter	Value
Rated input voltage $V_{\text{in,rated}}$	28.5 V
Battery voltage range $V_{\text{batt,min}} - V_{\text{batt,max}}$	12 V–13.5 V
Target efficiency η_{target}	>90%
Rated power P_{rated}	100 W
Power range meeting the ZVS condition	30 W–100 W

and the additional small inductance are preserved in the new topology. The control of the power flow from the source to the load is still based on the frequency modulation.

The main target specifications of the converter are listed in Tab. 6.1. The input power and voltage levels are compliant with thin-film PV modules such as the Copper Indium Gallium Selenide (CIGS) modules Unisun FLEX-03N [221] or Bluesun BSM-FLEX-130N [222]. Lead-acid 12 V batteries are considered as

reference loads for this application. Given the voltage constraints that will be detailed in Section 6.2, not all the PV panels are compliant with any battery selection.

6.2 Converter operation

M_1 and M_2 are controlled with 180° phase shift and 50% duty cycle, so as to ensure a symmetric operation of the converter in the two half switching periods. A dead time t_{dead} is introduced between the conduction periods of the MOSFETs to avoid cross-conduction. The active rectifier provides a full-wave rectification of the intermediate AC voltage generated between nodes A and X, and must be controlled to be in phase with the half-bridge inverter. Despite the additional driving complexity, an active rectifier eliminates the voltage drops of a diode bridge, improving the conversion efficiency at low voltage loads.

The inductor L_r, originally present in [220], is connected to the switching node A to assist the ZVS turn-ON of M_1 and M_2, by resonating with their output parasitic capacitances.

Unlike in conventional half-bridge converters, where capacitors C_1 and C_2 are designed to maintain a stable voltage at the floating node X, in this converter they are designed to be alternately charged and discharged between 0 V and V_{in} by the output current I_o. As in [220], the clamping action of D_1 and D_2 limits the maximum energy that each capacitor can store and release in a switching cycle. The result is that the voltage at node X features a distinctive trapezoidal shape, giving the name to the Discontinuous Voltage Mode (DVM) [220].

The investigation of the operating principle revealed that the converter, under certain circumstances of switching frequency and load voltage, can exit the DVM. This second working mode was not previously studied and required to be properly modelled, in order to predict the influence of the control variable and load parameters on the available power transfer. Since the converter enters this second working mode only above a source- and load-dependent switching frequency, it will be referred to as *High frequency* (HF) mode, to be distinguished from the *Low frequency* (LF) mode.

For the analysis of the converter operation in a switching cycle for both the operating modes, the following assumptions are made:

- the input capacitor C_{in} is sufficiently large to maintain a constant DC input voltage V_{in};

- the output filter inductor L_o is sufficiently large to maintain a constant DC output current I_o;
- the half-bridge MOSFETs M_1 and M_2 are ideal, except for their output parasitic capacitances C_{s1} and C_{s2} (with $C_{s1} = C_{s2} = C_s$), involved in the soft switching;
- the forward voltage drops of the clamping diodes and MOSFETs body diodes are neglected;
- the reactive components C_1, C_2, C_{in}, L_r and L_o are lossless and ideal;
- the converter operation is perfectly symmetric in the two half periods: for this reason, the following discussion will be limited to half period.

6.2.1 Low frequency mode (LF)

Let's assume that the half-period starts when M_1 is turned ON. The two state variables for the converter analysis are the voltage across capacitor C_2, namely V_X, and the current, i_{Lr} through the inductor L_r. The voltage across C_1, $V_{in} - V_X$, is not an independent variable since V_{in} is assumed to be constant. The two capacitors are connected in parallel from the point of view of the AC analysis. At the beginning of the half-period, $V_X(0) = 0\,V$ and $i_{Lr}(0) = I_o$. The three MOSFETs M_1, M_3 and M_5 are turned ON, conducting the constant output current I_o as well as the inductor L_r. On the other hand, M_2, M_4 and M_6 are OFF. Since there is a direct power transfer between source and load during this phase, it is here named the ***Power Transfer*** phase (PT). At the floating node X, I_o splits between C_1 and C_2 (with $C_1 = C_2 = C$):

$$i_{Lr} = C_2 \frac{dV_X}{dt} - C_1 \frac{d}{dt}(V_{in} - V_X) = 2C \frac{dV_X}{dt}. \tag{6.1}$$

According to (6.1), V_X increases linearly from 0 V to V_{in}, since the output current gradually charges C_2 and discharges C_1:

$$V_X(t) = \frac{I_o}{2C} t. \tag{6.2}$$

Since no voltage drop appears across L_r, the rectifier primary voltage V_p decreases with the same rate:

$$V_p(t) \approx V_{DS2} - V_X = V_{in} - \frac{I_o}{2C} t. \tag{6.3}$$

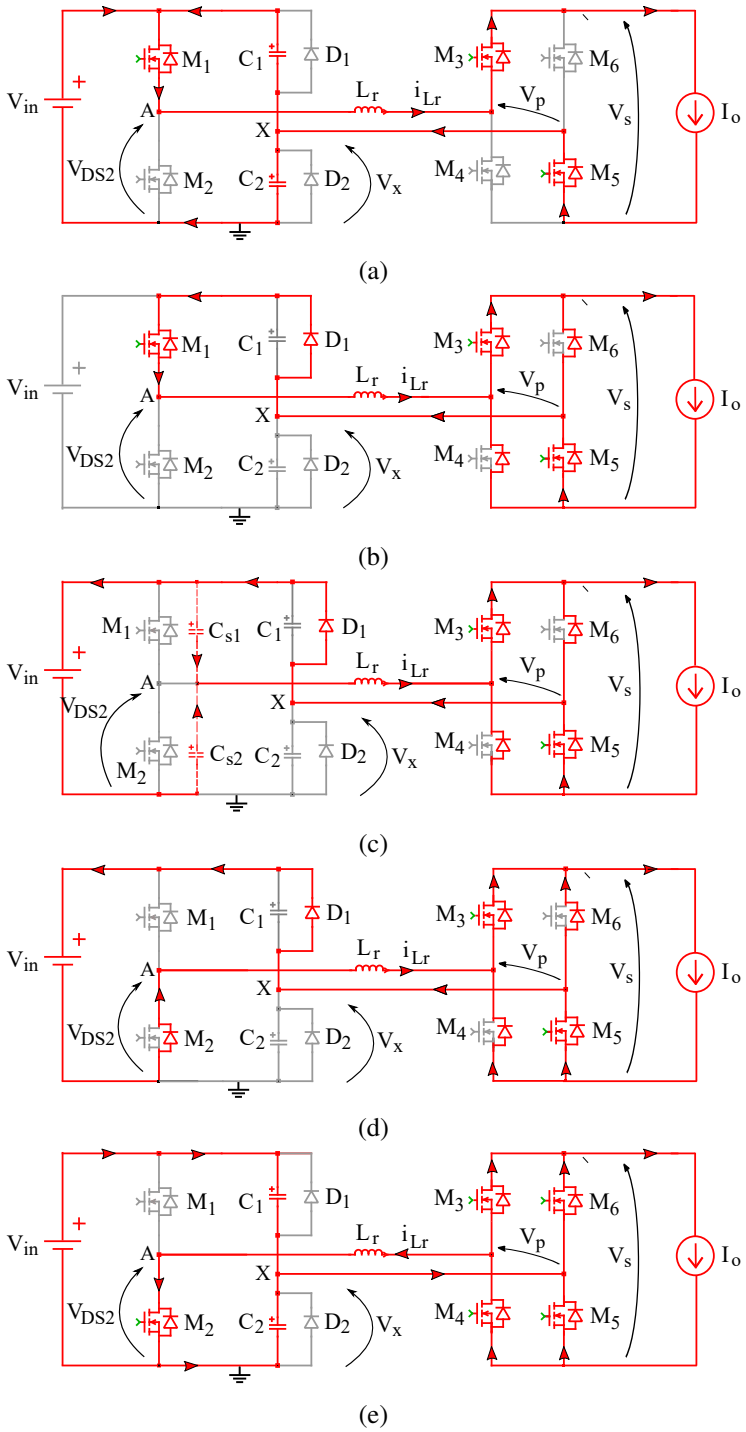


Fig. 6.2 Equivalent circuits of the qR charger during a half-period, in the LF region. (a) PT mode. (b) CC mode. (c) CR mode: L_r resonates with the output parasitic capacitances of M_1 and M_2. (d) CR mode: the body diode of M_2 starts conducting. (e) CR mode: M_2 is turned ON and L_r is forced to be discharged.

The rectifier secondary voltage V_s coincides with V_p for the entire half-period, becoming $-V_p$ in the other half. This phase ends when $V_X = V_{in}$: its duration ΔT_{PT} can be computed from (6.2):

$$\Delta T_{PT} = \frac{2CV_{in}}{I_o}. \tag{6.4}$$

The equivalent circuit of the converter during the PT phase is shown in Fig. 6.2a.

After time ΔT_{PT}, the clamping diode D_1 gets forward biased and clamps $V_X = V_{in}$, thereby preventing any further increase of the C_2 voltage. M_1, M_3 and M_5 are still turned ON. During this phase, i_{Lr} recirculates through the free-wheeling current path created by D_1. V_p becomes null and forces the body diodes of M_4 and M_6 to turn ON. It is relevant to observe that the tun ON occurs at zero current (ZCS). I_o starts splitting between the two legs of the active rectifier. The free-wheeling circulation of the output current gives the name to this phase, the ***Current Circulating*** phase (CC), shown in Fig. 6.2b. During the CC phase, no power is temporarily extracted from the supply or transferred to the battery. Its duration is not fixed a priori, but it depends on the control variable, the switching frequency.

The CC phase ends when M_1 is turned OFF and the deadtime begins. At the beginning of the next phase, $i_{Lr} = I_o$ and $V_X = V_{in}$. During the deadtime, L_r starts resonating with the MOSFETs output capacitances C_{s1} and C_{s2}, with $C_{s1} = C_{s2} = C_{s1}$. For simplicity, the output capacitances are assumed to be constant and equal. For this reason, this phase is called the ***Crossover Resonant*** phase (CR). In response of the resonance, V_{DS2} starts decreasing towards 0 V, and can only reach 0 V if the energy previously stored in L_r is sufficient to charge C_{s1} up to V_{in}. This condition translates into a lower boundary for L_r:

$$L_r > \frac{2C_s V_{in}^2}{I_o^2}. \tag{6.5}$$

The equivalent circuit of the converter during the resonance is shown in Fig. 6.2c. If (6.5) is met, V_{DS2} reaches 0 V and the body diode of M_2 gets forward-biased, as shown in Fig. 6.2d. The voltage $V_X = V_{in}$ (almost constant during this short phase) forces L_r to discharge linearly:

$$i_{Lr} = I_o - \frac{V_X}{L_r}t = I_o - \frac{V_{in}}{L_r}t. \tag{6.6}$$

The difference between i_{Lr} and I_{o} flows through the body diodes of M_4 and M_6. By applying the Kirchhoff Current Law (KCL) at the input and output nodes of the rectifier, the source-to-drain currents of M_{3-6} derive consequently:

$$i_{\mathrm{M_3}} = i_{\mathrm{M_5}} = \frac{I_{\mathrm{o}}}{2} + \frac{i_{\mathrm{Lr}}}{2} \tag{6.7}$$

$$i_{\mathrm{M_4}} = i_{\mathrm{M_6}} = \frac{I_{\mathrm{o}}}{2} - \frac{i_{\mathrm{Lr}}}{2}. \tag{6.8}$$

If the deadtime t_{dead} is sufficiently short, M_2 is turned ON while its body diode is still conducting: in this condition, the ZVS is achieved. The maximum allowed deadtime $t_{\mathrm{dead,max}}$ to achieve ZVS is limited by the time required for the full discharge of C_{s2} (denoted by t_1), plus the time for i_{Lr} to become null:

$$t_{\mathrm{dead,max}} \approx t_1 + \frac{L_{\mathrm{r}} I_{\mathrm{o}}}{V_{\mathrm{in}}}. \tag{6.9}$$

After this time, indeed, L_{r} starts resonating again with C_{s1} and C_{s2}, and the ZVS condition is lost.

If M_4 and M_6 are turned ON synchronously with M_2, they also meet the ZVS condition. In the last phase of the half period, shown in Fig. 6.2e, thus, only M_1 is OFF, while all the other MOSFETs are turned ON. As suggested by (6.7), there exists an optimal time instant at which the currents flowing through M_3 and M_5 fall to 0: with an accurate control of the driving signals, the ZCS turn OFF of M_3 and M_5 could be turned OFF at zero current (ZCS). This condition occurs when $i_{\mathrm{Lr}} = -I_{\mathrm{o}}$. The CR phase, and the first half of the period, are concluded when M_3 and M_5 are turned OFF.

Fig. 6.3 summarizes the key converter waveforms over a complete switching cycle. It is noteworthy that the duration of the CR phase has been intentionally exaggerated to enhance clarity. In practical scenarios, the CR phase accounts for only a small portion of the half-cycle, typically 2% or less. The waveforms in the LF mode reproduce the the DVM operation described in [220].

In the LF mode, since the capacitors C_1 and C_2 are alternately charged and discharge between 0 V and V_{in} independently from the switching frequency, they

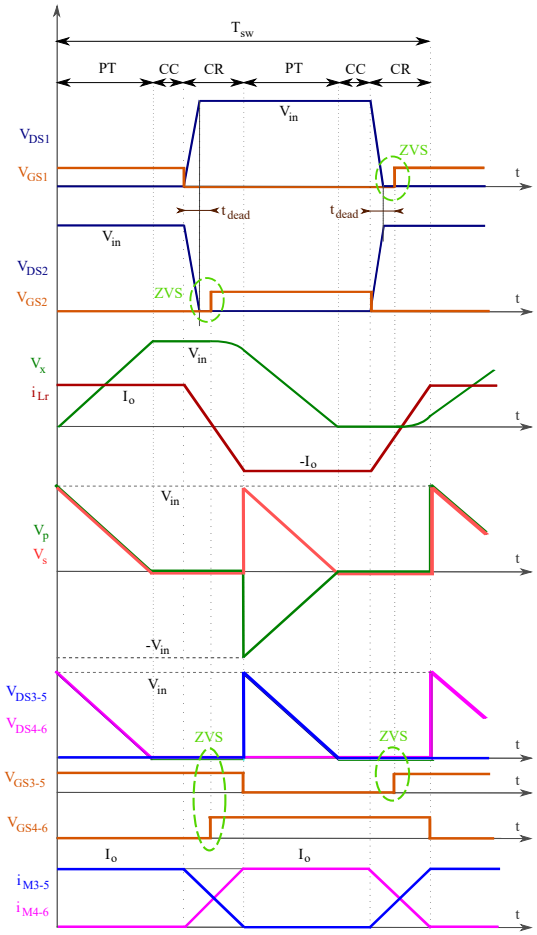


Fig. 6.3 Main voltage and current waveforms in a switching period, in the LF mode.

always store and release in a period the same amount of energy $\mathscr{E}_{\mathrm{C}}$, defined by:

$$\mathscr{E}_{\mathrm{C}} = \frac{1}{2} C V_{\mathrm{in}}^2 \,. \tag{6.10}$$

As already derived in [220], the transferred power P_{out} exhibits a linear dependence on the switching frequency f_{sw}:

$$P_{\mathrm{out}} = 2 C V_{\mathrm{in}}^2 f_{\mathrm{sw}} \,. \tag{6.11}$$

According to (6.11), the converter can be modelled as a voltage- and frequency-dependent power generator, whose transferred power is independent from the battery state of charge: this principle is indeed exploited in [220] to provide an intrinsic charging power limitation, also in case the battery is initially fully discharged.

However, the power transfer is subjected to a voltage constraint imposed on the PV source: at steady-state, assuming no voltage drop across L_o, the average value of the triangular-shaped V_s coincides with the charging voltage of the battery. As a consequence, to ensure a positive power flow, the following voltage constraint holds:

$$V_{in} > 2V_{batt}\,. \tag{6.12}$$

6.2.2 High frequency mode (HF)

At sufficiently low frequencies, the converter always works in the LF mode. For certain combinations of frequency and battery voltages, however, the half-switching period is no more sufficient for the output current to completely charge / discharge the capacitors C_1 and C_2. When these conditions occur, the voltage V_X assumes a triangular shape still centered at $\frac{V_{in}}{2}$, but with a reduced ripple. For certain fixed input and battery voltage values, it will be proved later in this section that there exists a maximum frequency at which the converter works according to the waveforms of the LV mode. Above this frequency, the converter starts operating in the HF mode.

At the beginning of the half-period, equivalently to the the ***Power Transfer*** phase (PT) of the LF mode, the constant output current I_o flows through M_1, M_3 and M_5, charging C_2 and discharging C_1. While the initial condition for $i_{Lr} = I_o$ still holds, the initial V_X voltage is different from 0 V:

$$V_X(0) = \frac{V_{in}}{2} - \Delta V\,, \tag{6.13}$$

where $\Delta V \in \left(0, \frac{V_{in}}{2}\right)$ is not known a priori. As described later in this section, ΔV is a function of the input voltage, the battery voltage and the switching frequency: its analytical derivation is crucial to quantify the available charge stored in C_1 and C_2, which is transferred to the load at each switching cycle. I_o determines the linear slope of voltages V_X and V_p:

$$V_X(t) = \frac{V_{in}}{2} - \Delta V + \frac{I_o}{2C}t \tag{6.14}$$

$$V_p(t) \approx V_{DS2} - V_X = \frac{V_{in}}{2} + \Delta V - \frac{I_o}{2C}t. \tag{6.15}$$

The equivalent circuit of the converter in the PT phase is shown in Fig. 6.4a and coincides with the corresponding one of the LF mode. At the end of the PT phase, when M_1 is turned OFF, it can be assumed that $V_{\mathrm{X}} = \frac{V_{\mathrm{in}}}{2} + \Delta V < V_{\mathrm{in}}$, based on the symmetry of the converter operation.

When M_1 turns OFF, differently from the LF mode, V_{X} is not sufficient to forward bias the clamping diode D_1: as a result, the CC phase is absent in the HF mode. At the beginning of the ***Crossover Resonant*** phase, L_{r} starts resonating with C_{s1} and C_{s2}, causing the fall of voltage V_{DS2} until the body diode of M_2 gets forward biased, as shown in Fig. 6.4b. As in the LF case, this condition occurs only if (6.5) is met. During the fast V_{DS2} fall, V_{X} is assumed to be constant. Concurrently, the body diodes of M_4 and M_6 get forward biased and start sinking current from L_{r}, as in the LF region: as a result, both V_{p} and V_{s} are null.

Once the body diode of M_2 gets forward biased, V_{DS2} is clamped to 0 V and L_{r} starts resonating with C_1 and C_2. The behaviour of the state variables during this phase can be mathematically described by combining the Kirchhoff Current and Voltage Laws applied to the equivalent circuit in Fig. 6.4c. The combination of the two equations translates into the following linear system:

$$\begin{cases} 2C\frac{dV_{\mathrm{X}}}{dt} - i_{\mathrm{Lr}} = 0 \\ V_{\mathrm{X}} + L_{\mathrm{r}}\frac{di_{\mathrm{Lr}}}{dt} = 0\,, \end{cases} \tag{6.16}$$

whose resonance frequency is $\omega_{\mathrm{res}} = \frac{1}{\sqrt{2CL_{\mathrm{r}}}}$, and whose initial conditions are $i_{\mathrm{Lr}}(0) = I_{\mathrm{o}}$ and $V_{\mathrm{X}}(0) = \frac{V_{\mathrm{in}}}{2} + \Delta V$. The system can be solved by re-arranging the equations into a unique second-order ODE with the above-mentioned initial conditions:

$$\begin{cases} V_{\mathrm{X}}(t) = \left(\frac{V_{\mathrm{in}}}{2} + \Delta V\right)\cos\omega_{\mathrm{res}}t + \frac{I_{\mathrm{o}}}{2C\omega_{\mathrm{res}}}\sin\omega_{\mathrm{res}}t \\ i_{\mathrm{Lr}}(t) = I_{\mathrm{o}}\cos\omega_{\mathrm{res}}t - 2C\omega_{\mathrm{res}}\left(\frac{V_{\mathrm{in}}}{2} + \Delta V\right)\sin\omega_{\mathrm{res}}t\,. \end{cases} \tag{6.17}$$

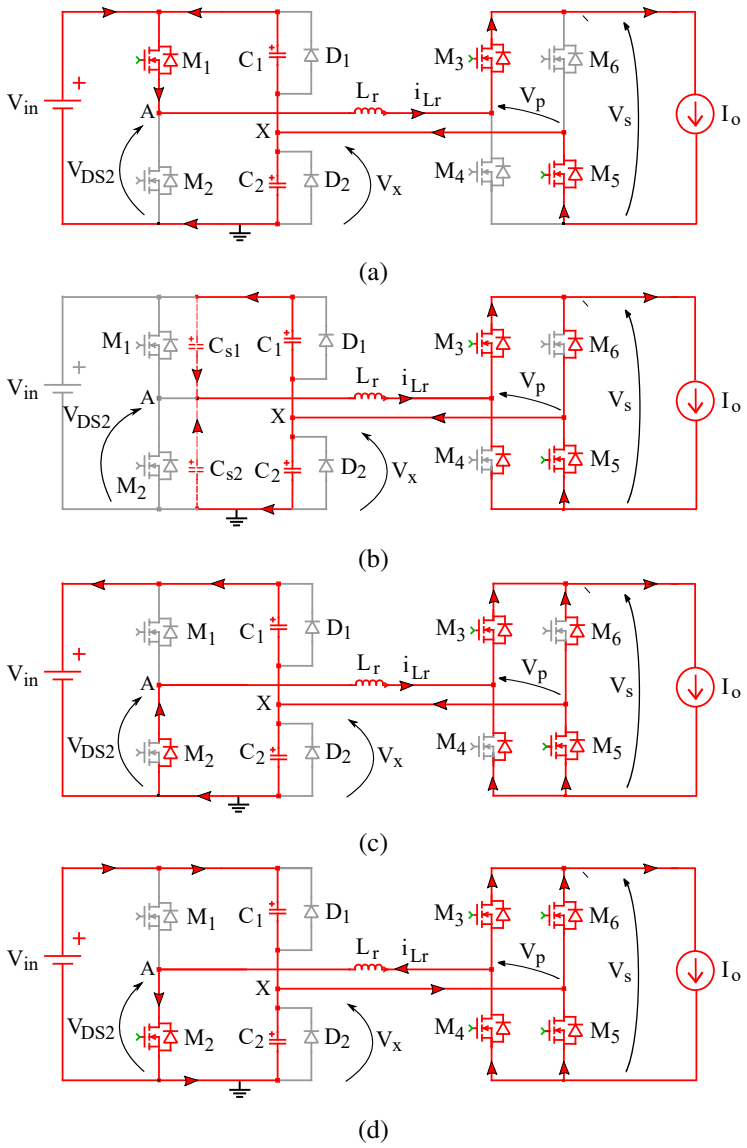


Fig. 6.4 Equivalent circuits of the qR charger during a half-period, in the HF region. (a) PT mode. (b) CR mode: L_r resonates with the output parasitic capacitances of M_1 and M_2. (c) CR mode: the body diode of M_2 starts conducting. (d) CR mode: M_2 is turned ON and L_r is forced to be discharged.

In practical cases, the duration of the CR phase is short enough to exploit a first-order Taylor approximation of (6.17) without committing significant mistakes:

$$\begin{cases} V_{\mathrm{X}}(t) \approx \frac{V_{\mathrm{in}}}{2} + \Delta V \\ i_{\mathrm{Lr}}(t) \approx I_{\mathrm{o}} - 2C\omega_{\mathrm{res}}^2 \left(\frac{V_{\mathrm{in}}}{2} + \Delta V \right) t \,. \end{cases} \tag{6.18}$$

The distribution of the currents in the rectifier MOSFETs and the conditions for their ZVS turn ON are equivalent to the LF mode case. The maximum allowed deadtime still ensuring the ZVS of M_2 can be computed from in (6.9). After the deadtime, M_2, M_4 and M_6 are turned ON synchronously, as shown in Fig. 6.4d. The soft-switching of all the converter transistors, allows to minimize their switching losses.

The time t_2 required by i_{Lr} to completely reverse (from I_{o} to $-I_{\mathrm{o}}$) can be computed assuming its approximated solution:

$$t_2 \approx \frac{2I_{\mathrm{o}}}{2C\omega_{\mathrm{res}}^2 \left(\frac{V_{\mathrm{in}}}{2} + \Delta V \right)} = \frac{2L_{\mathrm{r}}I_{\mathrm{o}}}{\frac{V_{\mathrm{in}}}{2} + \Delta V} \,. \tag{6.19}$$

Fig. 6.5 shows the main converter waveforms in a complete switching cycle, in the HF mode.

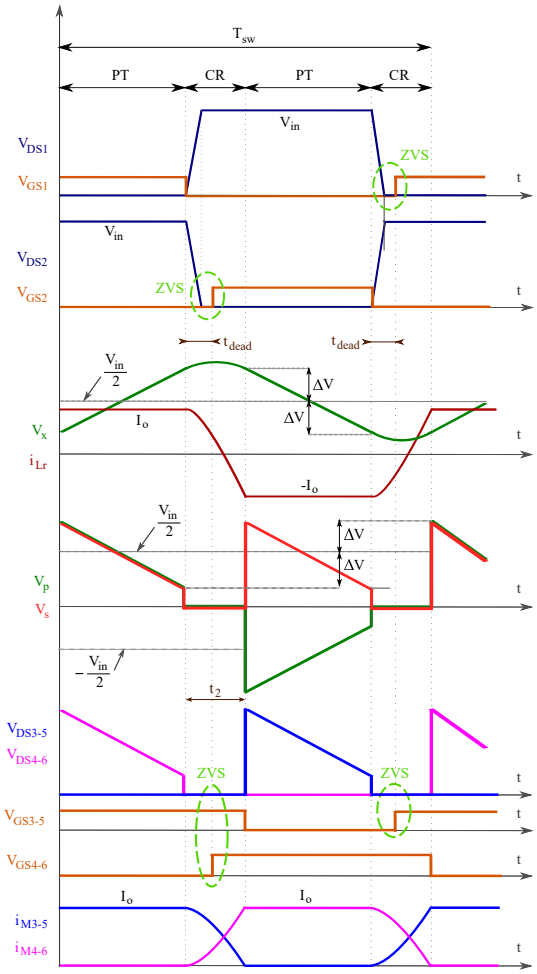


Fig. 6.5 Main voltage and current waveforms in a switching period, in the HF more.

In contrast to the LF mode, where the charge stored and released by the capacitors depends solely on the input voltage ($C \cdot V_{\text{in}}$), in the HF mode it exhibits a more complex and non-linear relationship. The static characteristic $P_{\text{out}}(f_{\text{sw}})$ in the HF region can be obtained by averaging the trapezoidal output voltage of the rectifier, which coincides with the charging voltage across the battery. As described, V_{s} exhibits the following behaviour:

$$V_{\text{s}}(t) = \begin{cases} \frac{V_{\text{in}}}{2} + \Delta V - \frac{I_{\text{o}}}{2C}t & \text{if } t \in \text{PT phase} \\ 0 & \text{if } t \in \text{CR phase}\,. \end{cases} \tag{6.20}$$

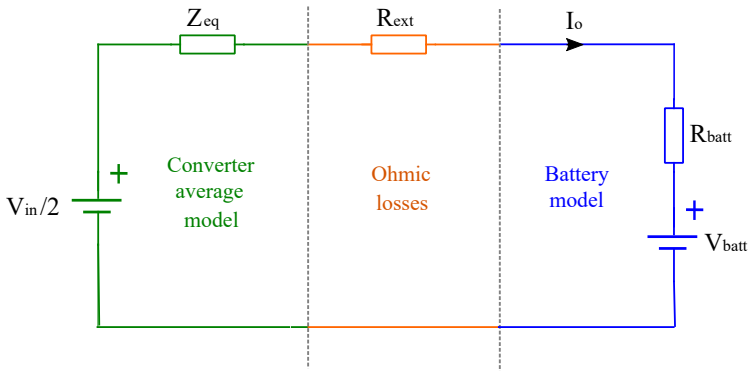


Fig. 6.6 Averaged simplified equivalent circuit of the converter in the HF region.

Assuming that the CR phase duration coincides with t_2, expressed in (6.19), the average value of V_s follows:

$$\overline{V_s} = \frac{2}{T_{sw}} \int_0^{\frac{T_{sw}}{2}} V_s(t)\, dt = \frac{2}{T_{sw}} \frac{V_{in}}{2} \left(\frac{T_{sw}}{2} - t_2 \right) = \frac{V_{in}}{2} - Z_{eq} I_o \,,$$

where:

$$Z_{eq} = \frac{2 V_{in} L_r f_{sw}}{\frac{V_{in}}{2} + \Delta V} \,. \tag{6.21}$$

The averaged circuit of the converter in a switching cycle of the HF mode can then be modelled as a resistive loop in which the output of the active rectifier is represented with its Thevenin equivalent circuit, consisting of the constant voltage contribution $\frac{V_{in}}{2}$ and the equivalent resistance Z_{eq}, linked to the reactive impedance of L_r. Fig. 6.6 illustrates the equivalent circuit model of the output side of the converter: as shown, the battery is represented as a Thevenin equivalent model, consisting of the DC voltage source V_{batt} and the internal resistance R_{batt}, while the additional resistance R_{ext} combines the resistive losses in the output loop (such as the filter inductor, rectifier and cables losses). Since the average model is studied, no reactive elements are included in Fig. 6.6. For compactness of notation, the total ohmic losses are embedded in a unique resistance, $R_{ohm} = R_{ext} + R_{batt}$.

From the schematic of Fig. 6.6, the current flowing in the output loop can be easily derived:

$$I_o(\Delta V) = \frac{\frac{V_{in}}{2}(1 - \alpha_V)}{Z_{eq}(\Delta V) + R_{ohm}} \,, \tag{6.22}$$

where, for compactness of notation:

$$\alpha_{\mathrm{V}} = \frac{2V_{\mathrm{batt}}}{V_{\mathrm{in}}}\,. \tag{6.23}$$

Notice that the output current, which determines the transferred power, is function of the still unknown ΔV. The other parameters are supposed to be known in advance. Eq. (6.22) highlights that a positive charging current, and thus a positive power transfer from source to load, can only be obtained when $\alpha_{\mathrm{V}} < 1$, resulting in the same voltage constraint expressed in (6.12).

The derivation of the static characteristic relies, at this point, on the explicit derivation of ΔV. By integrating (6.1) in the PT phase, another equation relating I_{o} and ΔV can be found:

$$\int_0^{\frac{T_{\mathrm{sw}}}{2}-t_2} i_{\mathrm{Lr}}dt = 2C\int_0^{\frac{T_{\mathrm{sw}}}{2}-t_2}\frac{dV_X}{dt}dt \longrightarrow I_{\mathrm{o}}\left(\frac{T_{\mathrm{sw}}}{2}-t_2\right) = 4C\Delta V\,. \tag{6.24}$$

After some algebraic re-arrangements, the combination of (6.22) and (6.24) leads to a third-order equation with single unknown ΔV:

$$P_3\Delta V^3 + P_2\Delta V^2 + P_1\Delta V + P_0 = 0\,, \tag{6.25}$$

where:

$$P_3 = \frac{4R_{\mathrm{ohm}}^2}{V_{\mathrm{in}}} \tag{6.26}$$

$$P_2 = R_{\mathrm{ohm}}\cdot\left[4\left(R_{\mathrm{ohm}}+4L_{\mathrm{r}}f_{\mathrm{sw}}\right) - \frac{1-\alpha_{\mathrm{V}}}{4Cf_{\mathrm{sw}}}\right] \tag{6.27}$$

$$P_1 = V_{\mathrm{in}}\left(R_{\mathrm{ohm}}+4L_{\mathrm{r}}f_{\mathrm{sw}}\right)^2 + \frac{V_{\mathrm{in}}L_{\mathrm{r}}}{2C}\left(1-\alpha_{\mathrm{V}}\right)^2 - \frac{R_{\mathrm{ohm}}+2L_{\mathrm{r}}f_{\mathrm{sw}}}{2Cf_{\mathrm{sw}}}\frac{V_{\mathrm{in}}}{2}\left(1-\alpha_{\mathrm{V}}\right) \tag{6.28}$$

$$P_0 = -\left(\frac{V_{\mathrm{in}}\left(1-\alpha_{\mathrm{V}}\right)}{2}\right)^2\cdot\left[\frac{R_{\mathrm{ohm}}+4L_{\mathrm{r}}f_{\mathrm{sw}}}{4Cf_{\mathrm{sw}}\left(1-\alpha_{\mathrm{V}}\right)}+\frac{L_{\mathrm{r}}}{C}\right]. \tag{6.29}$$

To give an idea of the orders of magnitude of coefficients P_i, $i \in \{0,1,2,3\}$ and their dependence on the switching frequency, Fig. 6.7 shows their behaviour assuming the following known parameters, consistent with the final design which will be detailed in Section 6.3: $V_{\mathrm{in}} = 28.5\,\mathrm{V}$, $V_{\mathrm{batt}} = 12\,\mathrm{V}$, $R_{\mathrm{ohm}} = 0.2\,\Omega$, $L_{\mathrm{r}} = 330\,\mathrm{nH}$, and $C = 0.94\,\mu\mathrm{F}$.

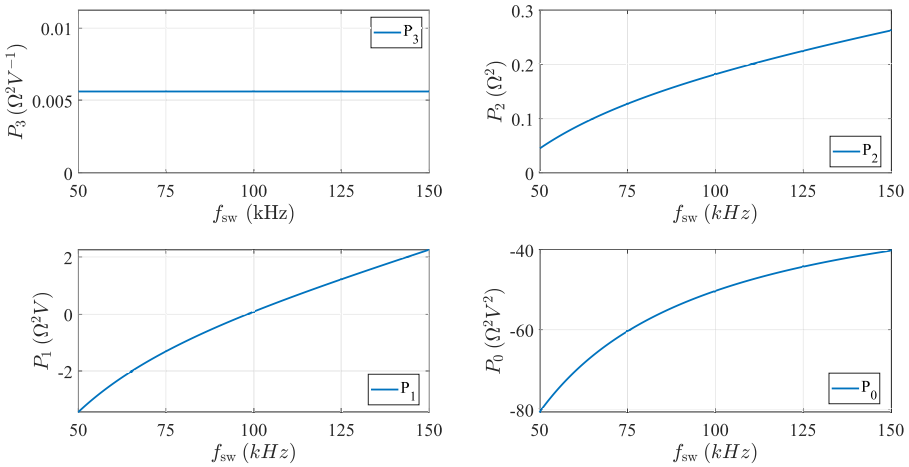


Fig. 6.7 Behaviour of the coefficients of the third-order equation (6.25), evaluated for the following parameters: $V_{\text{in}} = 28.5\,\text{V}$, $V_{\text{batt}} = 12\,\text{V}$, $R_{\text{ohm}} = 0.2\,\Omega$, $L_{\text{r}} = 330\,\text{nH}$, $C = 0.94\,\mu\text{F}$.

A conventional method to solve third-order equations is the Cardano's method [223], which, however, would lead to complex expressions for the solution ΔV. Without committing a significant mistake, a reasonable second-order approximation of (6.25) can be performed in case the second-order term $P_2(f_{\text{sw}})\Delta V^2$ is proved to be much larger than the third-order term $P_3\Delta V^3$, in the worst-case scenario (minimum frequency $f_{\text{sw,min}}$, maximum ΔV), i.e.:

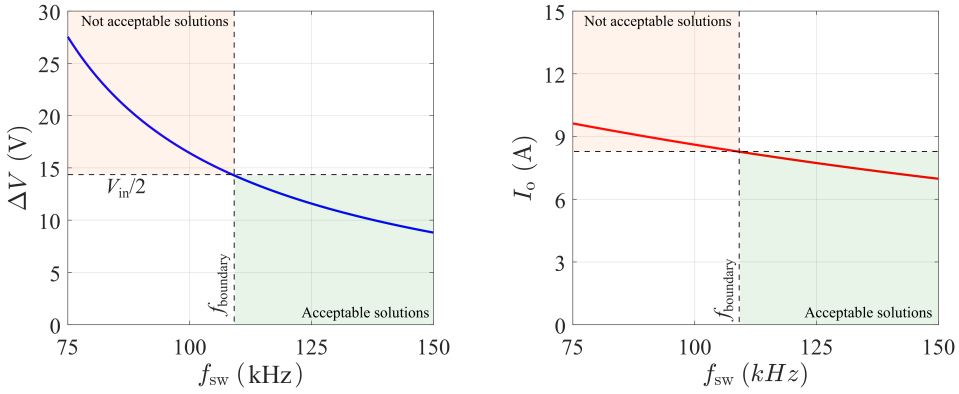
$$P_2(f_{\text{sw,min}})\Delta V_{\text{max}}^2 \gg P_3\Delta V_{\text{max}}^3 \longrightarrow \frac{P_2(f_{\text{sw,min}})}{P_3} \gg \frac{V_{\text{in}}}{2}. \tag{6.30}$$

If (6.30) holds, the third-order term can be neglected from (6.25) and the explicit solution of the resulting second-order equation $P_2\Delta V^2 + P_1\Delta V + P_0\Delta V = 0$ becomes:

$$\Delta V = \frac{-P_1 + \sqrt{P_1^2 - 4P_2P_0}}{2P_2}. \tag{6.31}$$

Once ΔV is computed, I_{o} follows from (6.22). As an example, their behaviour is shown, for the same design parameters mentioned above, in Figs. 6.8a and 6.8b, respectively. Notice that, since ΔV can only vary in the $0\,\text{V} - \frac{V_{\text{in}}}{2}$ range, (6.31) provides acceptable solutions only in the frequency range at which this constraint is met. The acceptable and not acceptable solutions are highlighted in Figs. 6.8a and 6.8b in green and red, respectively. The minimum frequency still satisfying

$\Delta V \in \left(0, \frac{V_{\text{in}}}{2}\right)$ is denoted by f_{boundary}, since it represents the boundary between LF and HF modes.



(a) (b)

Fig. 6.8 Frequency characteristic of ΔV and I_{o} resulting from the second-order approximation of (6.25), with $V_{\text{in}} = 28.5\,\text{V}$, $V_{\text{batt}} = 12\,\text{V}$, $R_{\text{ohm}} = 0.2\,\Omega$, $L_{\text{r}} = 330\,\text{nH}$, and $C = 0.94\,\mu\text{F}$. The green zone and red zone determine the range of acceptable and not acceptable solution, respectively.

Once I_{o} is known, the power transferred to the battery becomes:

$$P_{\text{out,HF}} = I_{\text{o}} \cdot (V_{\text{batt}} + R_{\text{batt}} I_{\text{o}}) \,. \tag{6.32}$$

Both ΔV and I_{o} decrease with increasing frequency with a hyperbolic-like trend. The intuitive explanation is that, in the HF mode, the inductive reactance offered by L_{r} increases the duration of the CR phase in the switching period, limiting the charge and discharge of capacitors C_1 and C_2 during the PT phase. As a result, the output power also decreases with frequency, significant difference with the LF mode. Moreover, since ΔV, and thus I_{o}, depends on the battery voltage, the output power decreases with increasing V_{batt}, leading to an automatic charging limitation in the last charging phases of the battery. In the LF mode, instead, the output power does not depend on the battery voltage.

The boundary frequency f_{boundary} can be derived imposing the continuity of the output power between LF and HF modes, i.e., equating (6.11) and (6.32):

$$P_{\text{out,LF}}(f_{\text{boundary}}) = P_{\text{out,HF}}(f_{\text{boundary}}) \,. \tag{6.33}$$

By definition, f_{boundary} is the frequency at which $\Delta V = \frac{V_{\text{in}}}{2}$: imposing this condition in (6.22) leads to a simplified expression of I_{o}:

$$I_{\text{o}}(f_{\text{boundary}}) = \frac{\frac{V_{\text{in}}}{2}(1-\alpha_V)}{2L_{\text{r}}f_{\text{boundary}}}. \tag{6.34}$$

The re-arrangement of (6.33) with (6.34) leads to a second-order equation, with solution:

$$f_{\text{boundary}} = \sqrt{\left(\frac{R_{\text{ohm}}}{4L_{\text{r}}}\right)^2 + \frac{\alpha_{\text{V}}(1-\alpha_{\text{V}})}{16CL_{\text{r}}}} - \frac{R_{\text{ohm}}}{4L_{\text{r}}}. \tag{6.35}$$

As an example, $f_{\text{boundary}}(V_{\text{in}} = 28.5\,\text{V}, V_{\text{batt}} = 12\,\text{V}, R_{\text{ohm}} = 0.2\,\Omega, L_{\text{r}} = 330\,\text{nH}, C = 0.94\,\mu\text{F}) = 71.53\,\text{kHz}$. By taking into account the different static characteristics $P_{\text{out}}(f_{\text{sw}})$ in the LF and HF modes, the transferred power can be globally expressed by:

$$P_{\text{out}} = \begin{cases} 2CV_{\text{in}}f_{\text{sw}}, & f_{\text{sw}} \leq f_{\text{boundary}} \\ (V_{\text{batt}} + R_{\text{batt}}I_{\text{o}}(f_{\text{sw}}))I_{\text{o}}(f_{\text{sw}}), & f_{\text{sw}} > f_{\text{boundary}} \end{cases} \tag{6.36}$$

Figs. 6.9a and 6.9b show the 3-D plots of the static characteristic of the converter as function of frequency and of the input or battery voltage, respectively, with $L_{\text{r}} = 330\,\mu\text{H}$, $C = 0.94\,\mu\text{F}$ and $R_{\text{ohm}} = 0.2\,\Omega$. The dashed lines represent the boundary between the LF and HF modes, corresponding to the maximum power transfer condition for a specific V_{in} or V_{batt}. Following (6.35), it is clear that an increase of V_{in} or reduction of V_{batt} move f_{boundary} at higher frequencies and larger powers can be achieved. On the contrary, an increased battery voltage during the charging process causes an automatic limitation of the transferred power. Due to the hyperbolic-like trend of the power in the HF mode, a wider frequency sweep is required to obtain the same range of operating powers.

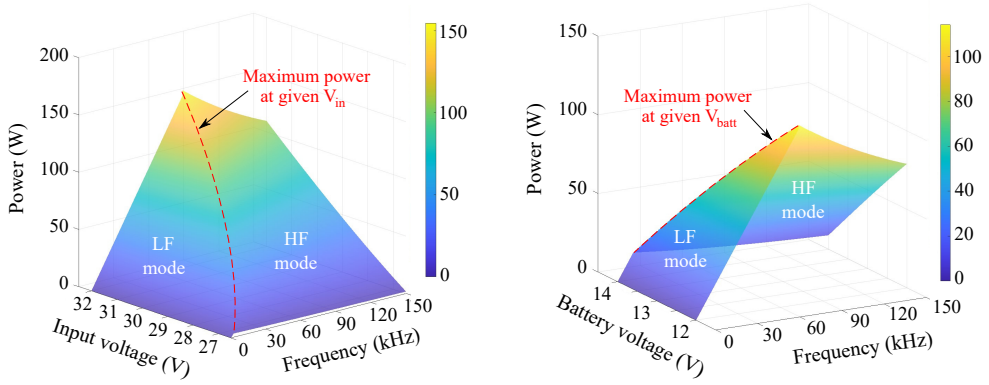


Fig. 6.9 Analytical 3-D plots of the static characteristic of the proposed converter. (a) Output power as function of V_{in} and f_{sw}, at $V_{\text{batt}} = 13.2\,\text{V}$; (b) Output power as function of V_{batt} and f_{sw}, at $V_{\text{in}} = 28.5\,\text{V}$.

6.3 Converter design

This section introduces a step-by-step design procedure for the proposed converter, taking into account the target PV source and battery specifications, and guiding the components selection on the basis of their worst-case electrical stresses. The design process begins with defining the target battery specifications, namely the minimum and maximum charging voltages, $V_{\text{batt,min}}$ and $V_{\text{batt,max}}$, the rated charging current $I_{\text{o,max}}$, and the internal resistance R_{batt}. The target specifications for this design are reported in Tab. 6.1. Considering the voltage constraint defined in (6.12), not all the PV modules are compatible with every battery configuration. For a 12 V lead-acid battery, as in the case of this work, only PV modules rated for at least 24 V can be considered. To ensure maximum power extraction and maintain a positive net power flow throughout the entire charging cycle, it is recommended that the MPP voltage and the open circuit voltage of the target PV panel satisfy (6.37) and (6.38):

$$V_{\text{MPP}} > 2V_{\text{batt,min}} \tag{6.37}$$

$$V_{\text{OC}} > 2V_{\text{batt,max}} \tag{6.38}$$

The design of the converter can be broadly split into three steps:

1. the selection of the power semiconductor devices, namely the half-bridge and rectifier MOSFETs and the clamping diodes, which is based on the worst-case electrical stresses at steady-state;
2. the selection of the DC filtering components, i.e., the input capacitor C_{in} and output inductor L_{o}, which is based on the derivation of the worst-case electrical stresses and on specific filtering requirements;
3. the design of dividing capacitors $C_{1,2}$ and resonant inductor L_{r}, which significantly affect the static characteristic.

6.3.1 Power semiconductor devices

Recalling the mathematical analysis of the converter waveforms, all the converter MOSFETs conduct the output current I_{o} for approximately half switching period (neglecting the duration of the CR phase), both in the LF and HF modes. Thus, their

peak and RMS currents are expressed by I_o and $\frac{I_o}{\sqrt{2}}$. The half-bridge MOSFETs M_1 and M_2 share with the clamping diodes D_1 and D_2 the same peak voltage V_{in}, bounded by the input capacitor. On the other hand, the absence of a capacitive filter at the input or output of the rectifier generates voltage spikes across the rectifier MOSFETs immediately after their turn-OFF. To be conservative, it is recommended to select M_{3-6} with a rated voltage at least large twice the input voltage, $2V_{in}$. The reason for these spikes is the resonance induced between their output capacitances and the resonant inductance L_r.

Since all MOSFETs turn ON under the zero-voltage condition, thereby minimizing the switching losses, a low conduction resistance $R_{DS,ON}$ is required to reduce conduction losses as well. $100\,V - 92\,A$ MOSFETs were selected for the prototype, driven by three half-bridge gate drivers.

D_1 and D_2 conduct a square-wave current with peak I_o exclusively in the LF mode, whose pulse width coincides with the duration of the CC phase ΔT_{CC}: this time interval can be approximately computed by subtracting from the half-period the duration of the PT phase ΔT_{PT}, expressed in (6.4):

$$\Delta T_{CC} = \frac{T_{sw}}{2} - \Delta T_{PT} = \frac{T_{sw}}{2} - \frac{2CV_{in}}{I_o}\,. \tag{6.39}$$

The average current of D_1 and D_2 follows from (6.39):

$$\bar{I}_{diode} = \frac{1}{T_{sw}} \int_0^{\Delta T_{CC}} I_o dt = \frac{I_o}{T_{sw}} \left(\frac{T_{sw}}{2} - \frac{2CV_{in}}{I_o} \right) = \frac{I_o}{2} - 2Cf_{sw}V_{in}\,. \tag{6.40}$$

Schottky-barrier diodes with 8 A rated current and 45 V breakdown voltage were selected.

Together with the MOSFETs, the selection of the gate drivers took into account the following criteria:

- galvanic insulation, necessary to isolate the digital domain (FPGA) and the power section domain;
- many gate drivers for half-bridge configurations provides the possibility to control two MOSFETs with a single control signal, thanks to the internal

generation of the deadtime. For this application, however, the need to adjust real-time the deadtime requires two independent inputs;

- a low propagation delay (no more than few tens of *ns*) is required to ensure a fast response of the power system to the digital signals generated by the FPGA.

The adopted MOSFETs can be completely turned ON with $V_{GS} = 5\,V$: three isolated half-bridge gate drivers were selected to drive the three legs of MOSFETs. The galvanic isolation is a necessary requirement, since the active rectifier and load exhibit a floating reference voltage with respect to the half-bridge and PV source. The floating supply for the high-side MOSFETs can be obtained with an external bootstrap circuits.

6.3.2 Dividing capacitors $C_{1,2}$ and resonant inductor L_r

The analysis of the converter operation and the static characteristic presented in Section 6.2 highlighted a significant dependence of the feasibility of the ZVS condition of $M_1 - M_2$ and of the maximum transferred power on C and L_r. According to (6.35), once the source and load specifications are set, the boundary frequency, and consequently the maximum transferred power, depends on both parameters. An *ad hoc* step-by-step design procedure was developed to guide the selection of C and L_r and is illustrated in Fig. 6.10

Once the half-bridge MOSFETs are selected, a lower bound for L_r can be set by imposing the ZVS condition expressed in (6.5) for a minimum output power $P_{min,ZVS}$:

$$L_r > 2C_s \left(\frac{V_{in,rated} V_{batt}}{P_{min,ZVS}} \right)^2 . \tag{6.41}$$

The minimum L_r expressed in (6.41) ensures the ZVS condition in the $P_{min,ZVS} - P_{rated}$ power range.

The second constraint on L_r comes from the effective requirement to harvest the rated power at the PV panel rated voltage. Given that the converter static characteristic reaches its absolute maximum at $f_{boundary}$, it is necessary to impose

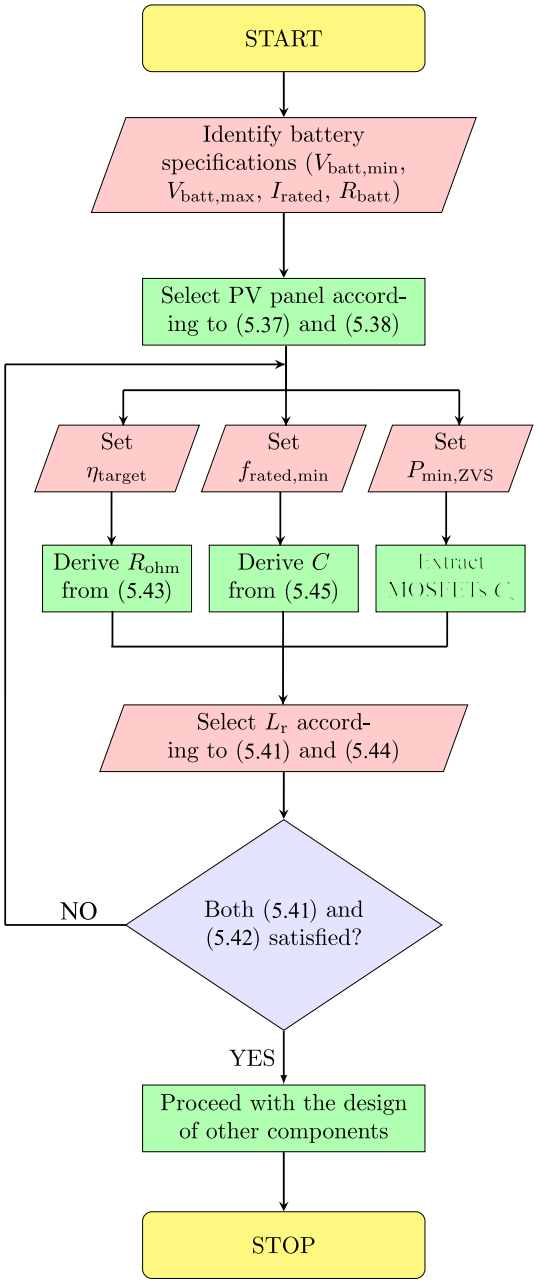


Fig. 6.10 Generalised design flowchart for the qR battery charger.

the following condition:

$$2CV_{\text{in,rated}}^2 \cdot f_{\text{boundary}}(R_{\text{ohm}}, \alpha_{\text{V}}, C, L_{\text{r}}) \geq P_{\text{rated}}\,. \tag{6.42}$$

Notice that α_V is computed at $V_{in,rated}$ and at a desired battery voltage ($V_{batt} = 12.5\,V$). On the other hand, a conservative initial value of R_{ohm}, which may not be known a priori, could be set from the desired target efficiency $\eta_{target} = 90\,\%$ at rated power:

$$R_{ohm} = (1 - \eta_{target}) \frac{P_{rated}}{I_{rated}^2}. \tag{6.43}$$

From (6.35) and (6.42), an upper bound of L_r can be computed:

$$L_r < C \cdot \left(\frac{V_{in,rated}^2}{P_{rated}} \right)^2 \left(\frac{\alpha_V(1-\alpha_V)}{4} - \frac{R_{ohm}}{R_{in,rated}} \right). \tag{6.44}$$

Until now, a lower and an upper bound for L_r was set, but C is still a degree of freedom. A preliminary selection of C can be made by specifying a minimum switching frequency $f_{rated,min} = 60\,kHz$ at which the rated power $100\,W$ is harvested in the LF mode, as expressed in (6.45): setting a minimum frequency for the rated operating point allows to relax the filtering requirements of the output inductor.

$$C = \frac{P_{rated}}{2 f_{rated,min} V_{rated}^2}. \tag{6.45}$$

Eq. (6.45) leads to the upper $1\,\mu F$ bound for C. At this point, the combination of (6.41) and (6.44) evaluated with $C = 1\,\mu F$ determines the range of admissible L_r ensuring, at the same time, the feasibility of the ZVS condition of M_1 and M_2 and the possibility to extract the rated power at the selected rated frequency. The evaluation of the two constraints on L_r leads to the admissible range $349\,nH - 468\,nH$ range. As illustrated in Fig. 6.10, in case the initial selection of C and L_r does not allow to meet (6.41) and (6.42) simultaneously, the process is iterated. In some cases, it may be necessary to relax the ZVS constraint, by increasing $P_{min,ZVS}$ or selecting MOSFETs with lower C_s.

Both C_1 ad C_2 conduct a symmetric square wave current with $\pm\frac{I_o}{2}$ peaks, and their peak voltage stress is limited by V_{in}. Low ESR and stable-capacitance Multi-Layer Ceramic Capacitors (MLCC) were selected, with $940\,nF$ capacitance, $50\,V$ rated voltage and $12\,A$ rated current.

L_r conducts a pure-AC symmetric square-wave current whose RMS value is I_o. A ferrite-core $330\,nH$ inductor was selected, exhibiting low DC resistance ($1.3\,m\Omega$),

36.5 A rated current, and 62 A saturation current. The selected inductance value is slightly outside the computed range, meaning that the ZVS condition will be met starting from a minimum output power slightly larger than the target $P_{\text{min,ZVS}}$.

6.3.3 DC filtering components

The design of the DC filtering components is based not only on the maximum electrical stresses at steady state, but also on the desired filtering requirements, namely, the maximum ripple voltage tolerated on the input PV source, and the maximum ripple current tolerated by the load battery. Provided that the proposed converter is frequency-modulated, the AC ripples are significantly influenced by the operating point. Since the worst-case filtering conditions occur at low frequencies, the LF mode is considered as the reference operating mode to derive the design equations for both the input capacitor and output inductor.

The input capacitor C_{in} is designed to provide a low-impedance path for the AC current, thus stabilizing the PV panel working voltage. In [176], a model-based approach recommends to limit the voltage ripple across a PV panel within the $8.5\,\%V_{\text{MPP}}$ in order to maintain the average extracted power above the $98\,\%P_{\text{MPP}}$. The impedance of the capacitor, coinciding with its ESR in case of electrolytic capacitors working at high frequencies, should be much smaller than the small-signal equivalent resistance of the target PV panel at the MPP [177]:

$$ESR \ll \left(\frac{dV_{\text{PV}}}{dI_{\text{PV}}}\right)_{\text{MPP}} \tag{6.46}$$

In this case, considering the target PV panel, $ESR < 540\,\text{m}\Omega$. The RMS current of C_{in} can be computed from the balance of currents at the input node. The total input current can be expressed by (6.47):

$$i_{\text{in}} = \begin{cases} \frac{I_{\text{o}}}{2}, & t \in [0, \Delta t_{\text{PT}}] \\ 0, & t \in [\Delta t_{\text{PT}}, \Delta t_{\text{PT}} + \Delta t_{\text{CC}}] \end{cases} \tag{6.47}$$

The RMS and average values, denoted by $I_{\text{in,RMS}}$ and $\bar{I}_{\text{in}}$, respectively, of the input current follow from (6.47):

$$I_{\text{in,RMS}} = \sqrt{\frac{1}{T_{\text{sw}}}\int_0^{T_{\text{sw}}} i_{\text{in}}(t)^2 dt} = \sqrt{\frac{2}{T_{\text{sw}}}\int_0^{\Delta t_{\text{PT}}} \left(\frac{I_{\text{o}}}{2}\right)^2 dt} = I_{\text{o}}\sqrt{\frac{\Delta t_{\text{PT}}}{2T_{\text{sw}}}} \tag{6.48}$$

$$\bar{I}_{\text{in}} = \frac{1}{T_{\text{sw}}}\int_0^{T_{\text{sw}}} i_{\text{in}}(t)dt = \frac{1}{T_{\text{sw}}}\int_0^{\Delta t_{\text{PT}}} \frac{I_{\text{o}}}{2}dt = I_{\text{o}}\frac{\Delta t_{\text{PT}}}{T_{\text{sw}}} \tag{6.49}$$

Assuming that the AC contribution of i_{in} is entirely supplied by C_{in}, its RMS current can be computed combining (6.48), (6.49) and (6.4):

$$I_{\text{C}_{\text{in}},\text{RMS}} = \sqrt{I_{\text{in,RMS}}^2 - \bar{I}_{\text{in}}^2} = 2CV_{\text{in}}f_{\text{sw}}\sqrt{\frac{I_{\text{o}}}{4CV_{\text{in}}f_{\text{sw}}} - 1}\,. \tag{6.50}$$

At the rated operating condition, $I_{\text{C}_{\text{in}},\text{RMS}} \approx 1.3\,\text{A}$. An Aluminum electrolytic capacitor was selected with 63 V rated voltage, 750 µF, 68 mΩ ESR and 2.5 A rated ripple current.

The output filter inductor L_{o} was designed to limit the current ripple superimposed to I_{o} below the 2.5 A safety limit recommended by [224] for Valve-Regulated Lead-Acid (VRLA) batteries with 50 A h capacity. The triangular voltage waveform across the inductor, $v_{\text{Lo}} = V_{\text{s}} - V_{\text{batt}}$, induces a parabolic AC current whose peak-to-peak ripple can be approximated by:

$$\Delta I_{\text{o}} \approx \frac{V_{\text{in}}}{16 f_{\text{sw}} L_{\text{o}}}\,. \tag{6.51}$$

A minimum 10.8 µH inductance is required to meet the constraint $\Delta I_{\text{o}} < 2.5\,\text{A}$. The inductor rated current should be larger than $I_{\text{o,max}}$. A ferrite-core 47 µH inductor with 8.8 mΩ DC resistance and 13 A saturation current was selected, allowing to limit the ripple current below 2.5 A down to 15 kHz.

A comprehensive summary of the voltage and current stresses of all the converter components is reported in Tab. 6.2.

The selected parts for the prototype are summarized in Tab.6.3.

Table 6.2 Summary of the main electrical stresses on all the converter components.

Converter component	Symbol	Peak voltage	Peak current	RMS current
Half-bridge MOSFETs	M_{1-2}	V_{in}	I_{o}	$\frac{I_{\text{o}}}{\sqrt{2}}$
Rectifier MOSFETs	M_{3-6}	$2V_{\text{in}}$	I_{o}	$\frac{I_{\text{o}}}{\sqrt{2}}$
Clamping diodes	D_{1-2}	V_{in}	I_{o} (only LF)	$\frac{I_{\text{o}}}{2} - 2Cf_{\text{sw}}V_{\text{in}}$ (average, only LF)
Resonant inductor	L_{r}	V_{in}	I_{o}	I_{o}
Dividing capacitors	C_{1-2}	V_{in}	$\frac{I_{\text{o}}}{2}$	$\frac{I_{\text{o}}}{2}$
Input filter capacitors	C_{in}	V_{in}	$2Cf_{\text{sw}}V_{\text{in}}$	$2CV_{\text{in}}f_{\text{sw}}\sqrt{\frac{I_{\text{o}}}{4CV_{\text{in}}f_{\text{sw}}} - 1}$
Output filter inductor	L_{o}	$V_{\text{in}} - V_{\text{batt}}$	I_{o}	I_{o}

Table 6.3 Main converter components for the physical prototype.

Converter component	Value	Part number
Half-bridge MOSFETs M_{1-2}	N/A	TPH4R10ANLL1Q
Rectifier MOSFETs M_{3-6}	N/A	TPH4R10ANLL1Q
Clamping diodes D_{1-2}	N/A	V8PAL45HM3_A/I
Resonant inductor L_{r}	330 nH	IHLP5050CEERR33M01
Dividing capacitors C_{1-2}	940 nF	C1812C944J5JLC7805
Input filter capacitors C_{in}	750 µF	UCZ1J751MNS1MS
Output filter inductor L_{o}	47 µH	74437529203470

6.4 Experimental results

6.4.1 Schematic and layout design

The schematic and layout of the PCB prototype were designed in *Altium Designer*[1]. In this section, a functional block diagram of the schematic is presented to illustrate its main blocks and their connections, while the pictures of the complete four sheets can be found in Appendix A. The block diagram is shown Fig. 5.19.

Sheet 1 includes both legs of the half-bridge inverter and the dual-channel gate driver for the two MOSFETs M_{1-2}.

Sheet 2 contains the synchronous rectifier of the converter, including the two half-bridge gate drivers required to drive the four MOSFETs M_{3-6}.

Sheet 3 includes the sections of the schematic devoted to the generation of the two supply voltages for the half-bridge and rectifier gate drivers, respectively, to the input current sensing, to the input and output connectors, and to the interface with the external development board *Terasic De1-SoC*[2]. The FPGA on this board was programmed to convert the analog signals from the voltage and current sensors, and to generate the PWM signals.

Finally, *Sheet 4* contains the sections of the schematic devoted to the acquisition of $v_{\mathrm{DS},2}$ and V_{in}. Originally, the proposed converter was supposed to be equipped with a dedicated control loop meant to tune the half-bridge deadtime in such a way to always provide the ZVS of M_1 and M_2 irrespectively of the working point (ZVS tracking control). The acquisition of the polarity of $v_{\mathrm{DS},2}$ during the deadtime served this purpose, and is implemented in the schematic as a comparator followed by a digital buffer isolator (to decouple the power and digital domains). The input voltage, on the other hand, is measured through a voltage divider followed by an isolated voltage amplifier. Although the PCB was equipped with all the necessary acquisition chains for both the ZVS-tracking control and the MPPT control, the converter was tested in open loop conditions, due to the unavailability of a PV characteristic emulator.

[1] https://www.altium.com/altium-designer (accessed Jan. 20th, 2026).

[2] https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&No=836 (accessed Jan. 22, 2026).

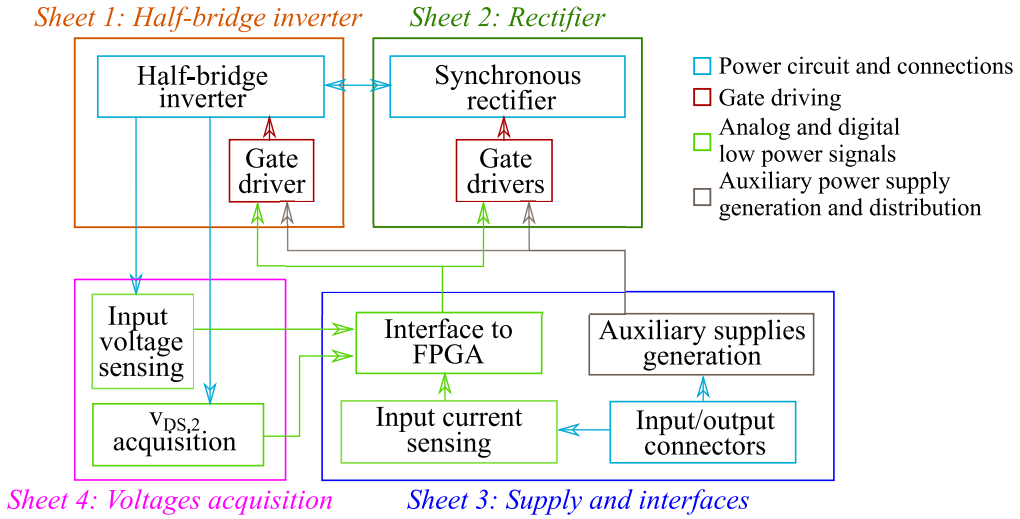


Fig. 6.11 Block diagram of the schematic of the converter prototype, highlighting the main blocks and connections, and the division into the four sheets in *Altium Designer*.

The circuit was printed on a 2-layer, 1.55 mm-thick FR4 board. The following list reports the main design criteria adopted for proper layout planning, components placing and trace routing:

1. the layout was planned to separate as much as possible the input, output and digital power domains. The ground planes in the bottom layer were designed to minimize the loop areas with the active traces in the top layer, to minimize the parasitic inductances;
2. the minimization of MOSFETs gate trace loops was a priority design criterion, to minimize the effect of stray inductances that may cause switching ringing;
3. traces carrying high-speed digital signals were routed as straight as possible, and entirely on the top-layer;
4. the analog outputs of the current and voltage sensors were located far from the high-frequency switching power nodes, to try reducing the EMI;
5. the width of the traces was also selected according to the expected current, preferring thinner traces (0.2 mm) for digital and analog signals, and up to few millimeters for large current power traces;
6. for convenience, the source and battery side connectors were placed at the opposite edges of the PCB, and as far as possible from the FPGA connector.

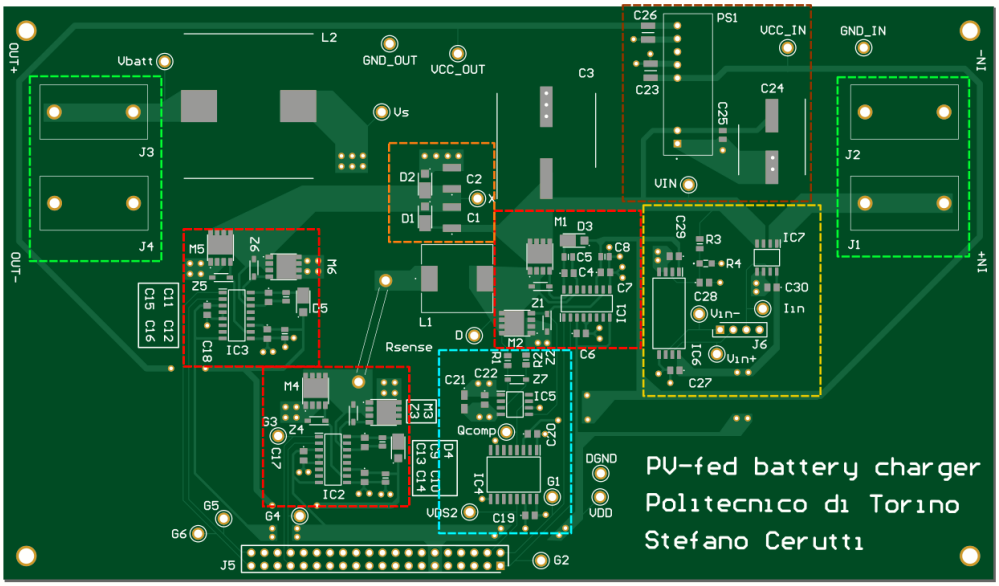
Fig. 6.12a shows the appearance of top layer of the final PCB layout, highlighting different functional clusters of components. Fig. 6.12b illustrates the bottom layer view of the PCB, highlighting the ground planes of the three power domains of the converter, namely the source, load and digital domains.

6.4.2 Experimental waveforms

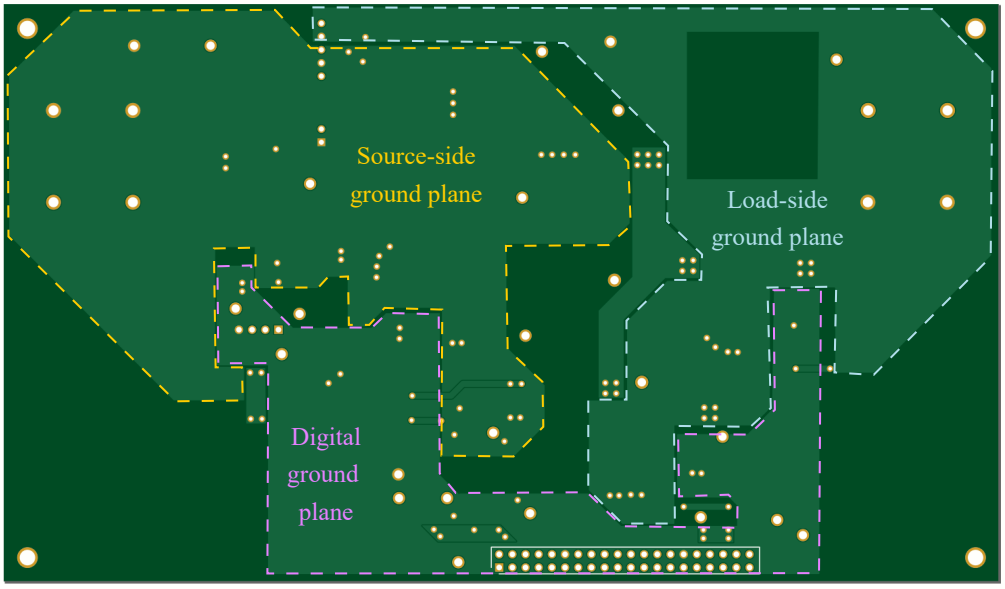
The designed PCB prototype, shown in Fig. 6.13a, was experimentally tested with the main purposes of validating the converter operation in its two working modes, the effectiveness of the analytical modelling of the static characteristic and the performance of the proposed converter. A DC power supply and DC electronic load were used to replace the PV panel and the low voltage battery in open loop tests. The driving signals for the MOSFETs were generated by an external FPGA Terasic Cyclone V SoC on a De1-SoC board, with the possibility to manually sweeping the switching frequency and deadtime. The complete experimental setup is shown in Fig. 6.13b.

Figs. 6.14a and 6.14b depict some of the relevant waveforms of the converter, namely the voltage V_X, the switching node voltage V_{DS2}, the resonant inductor current i_{Lr} and the rectifier output voltage V_s. Specifically, Fig. 6.14a refers to an operating point in the LF ($V_{in} = 27.5\,V$, $V_{batt} = 12\,V$, $f_{sw} = 50\,kHz$), characterized by the triangular waveform of V_X sweeping from $0\,V$ to V_{in}. Fig. 6.14b, on the other hand, refers to a working point in the HF mode ($V_{in} = 27.5\,V$, $V_{batt} = 12\,V$, $f_{sw} = 130\,kHz$), which can be distinguished by the reduced triangular ripple on V_X. In both cases, the duration of the CR mode is too short to be appreciated. Notice that i_{L_r} exhibits, in the second half of the switching period, an unexpected $\approx 330\,kHz$ oscillation superimposed to thesquare-wave behaviour, related to a spurious resonance of the filter inductor with the layout parasitics and not predicted in the converter modelling presented in Section 6.2.

A more detailed visualization of the of the soft commutation of the converter MOSFETs is presented in Fig. 6.15a, highlighting the ZVS turn ON of M_2, and Fig. 6.15b, highlighting the ZVS turn ON of M_4. Both the waveforms refer to the following operating point: $V_{in} = 27.5\,V$, $V_{batt} = 12\,V$, $f_{sw} = 50\,kHz$, $80\,ns$ dead time. More precisely, Fig. 6.15b does not show the output voltage V_{DS4}, but V_s, which

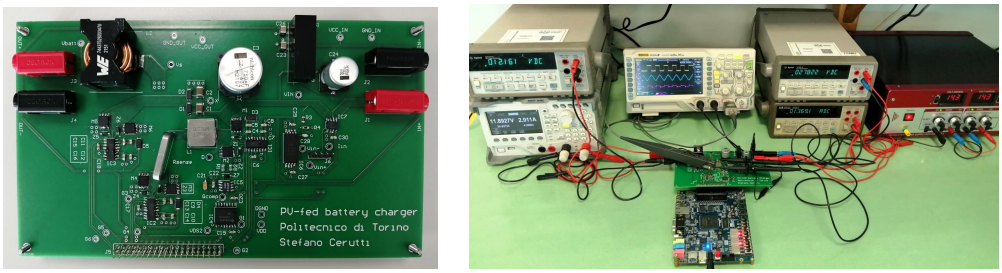


(a) Top layer.



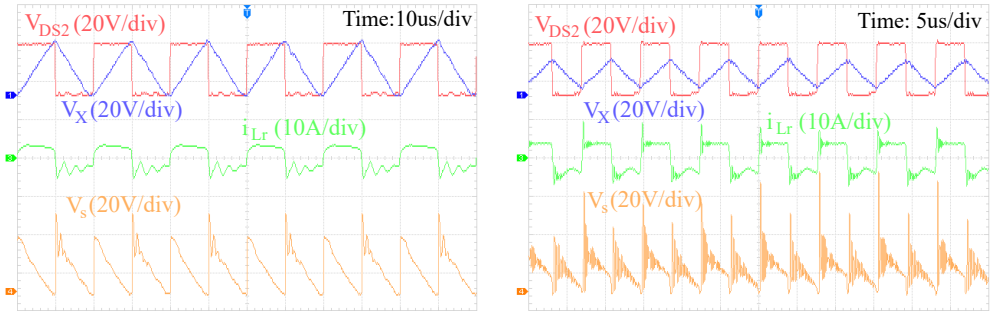
(b) Bottom layer.

Fig. 6.12 Top and bottom views of the PCB layout, with indications of the main components clusters and ground planes.



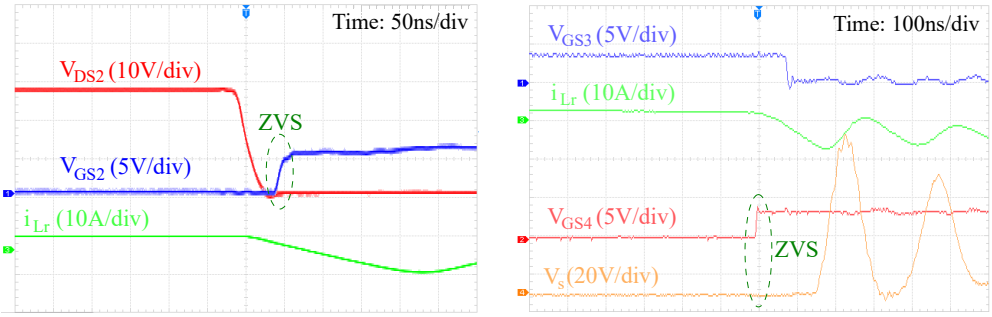
(a) (b)

Fig. 6.13 Pictures of the experimental setup: (a) Top layer view of the PCB prototype; (b) Picture of the testbench.



(a) (b)

Fig. 6.14 Main experimental waveforms of the converter at $V_{in} = 27.5\,V$ and $V_{batt} = 12\,V$, in the LF and HF modes: (a) Waveforms in the LF mode ($f_{sw} = 50\,kHz$); (b) Waveforms in the HF mode ($f_{sw} = 130\,kHz$.



(a) (b)

Fig. 6.15 Details of the soft commutation of M_2 and M_4 for $V_{in} = 27.5\,V$, $V_{batt} = 12\,V$, $f_{sw} = 50\,kHz$). (a) ZVS turn ON of M_2. (b) ZVS turn ON of M_4.

temporarily coincides with V_{DS4} during M_4 turn ON.

6.4.3 Validation of modelling

Another relevant goal of the tests was the validation of the analytical modelling of the static characteristic of the proposed converter, especially in the HF mode, for which no previous mathematical model was available.

Fig. 6.16 compares the experimental results of the measured output powers with the analytical static characteristics, derived by (6.11) (for the LF mode) and (6.32) (for the HF mode). The plots refer to two combinations of input and output voltages (27 V/12 V and 27.5 V/12 V) selected to clearly identify the two operating modes.

In the LF mode, the experimental results align closely with (6.11). For frequencies below 15 kHz, the resonant tank consisting of the inductor L_o and the half-bridge capacitors induces unwanted oscillations in the output current with resonance frequency around 16.9 kHz. As such low power conditions, the converter exits the DVM, and the output power can no longer be described by a linear function. In the HF mode, the measured output power exhibits a hyperbolic-like trend, as predicted. The values of R_{ohm} ensuring the best fitting were 173 mΩ (for the 27 V case) and 165 mΩ (for the 27.5 V case). At such conditions, the boundary frequencies $f_{boundary}$, computed by (6.35), are ≈ 66 kHz for $V_{in} = 27.5$ V, and ≈ 60 kHz for $V_{in} = 27$ V. A relevant remark is that, according to (6.31), the output power expression in the HF mode can be obtained in closed form, without resorting to nonlinear equation solvers. The HF characteristic presents minor deviations from the nominal curve, likely caused by the previously mentioned spurious resonance.

The closed-form modelling of the converter static characteristic relies on the assumption that the power source behaves like an ideal DC voltage generator with voltage V_{in}. In real PV applications, this assumption does not correspond to a realistic behaviour of a PV module. As a result, the real working point of the converter must take into account the non-linear I-V characteristic of the PV source, together with its dependence on the environmental conditions. Fig. 6.17 illustrates a simplified block diagram of the PV-converter system, in which the PV panel is represented by a non-linear current generator $I_{PV}(V_{PV}, T_{panel}, G)$, depending on its voltage V_{PV}, and on two external parameters, i.e. the panel temperature T_{panel} and solar irradiance G. The converter and battery block, instead, can be modelled as a non-linear resistance $R_{conv}(f_{sw}, V_{PV}, V_{batt})$ dependent on the switching frequency, input voltage and battery voltage. The working point of the system can be computed

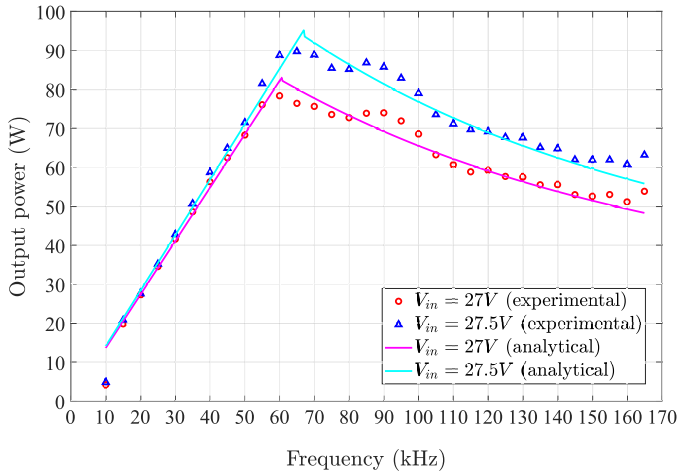


Fig. 6.16 Comparison of experimental results of static characteristics with the predicted analytical model, for $V_{\text{in}} = 27\,\text{V}/27.5\,\text{V}$ and $V_{\text{batt}} = 12\,\text{V}$.

by intersecting the non-linear characteristics of the PV source and converter for specific temperature, irradiance, switching frequency and battery voltage, i.e. by solving numerically the non-linear equation:

$$V_{\text{PV}} = I_{\text{PV}}(V_{\text{PV}}, T_{\text{panel}}, G) \cdot R_{\text{conv}}(f_{\text{sw}}, V_{\text{PV}}, V_{\text{batt}})\,. \tag{6.52}$$

An equivalent approach is to intersect the non-linear power-voltage curve of the PV panel with the analytical static characteristic of the DC-DC converter, either in the LF or HF mode:

$$P_{\text{PV}}(V_{\text{PV}}, T_{\text{panel}}, G) = P_{\text{conv}}(f_{\text{sw}}, V_{\text{PV}}, V_{\text{batt}})\,. \tag{6.53}$$

Notice that the only acceptable solutions are the ones meeting the $V_{\text{in}} > 2V_{\text{batt}}$ voltage constraint. As an example, the Bluesun Flex-03N-110W, whose main datasheet parameters are reported in Tab. 6.4, is considered as reference to show how the static characteristic of the converter can be coupled with the non-linear behaviour of a PV source. Fig. 6.18 shows some P-V curves of the same PV panel under different module temperatures and solar irradiance conditions, on the basis of the datasheet parameters. The power-voltage curves highlight the linear dependence of the peak power on the solar irradiance G, and the reduction of the MPP voltage at increasing T_{panel}.

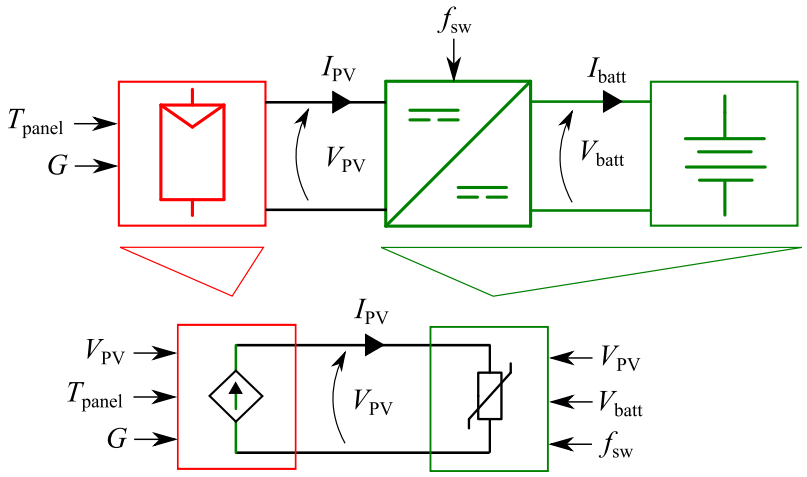


Fig. 6.17 Simplified block diagram of the interface between the PV source and converter-battery. From the point of view of the computation of the working point, the PV source can be represented as a non-linear dependent current generator, while the converter-battery blocks as a dependent resistor.

The numerical solution of (6.53) using the target PV module characteristic and considering the designed converter parameters leads to the non-linear static characteristic shown in Fig. 6.19. More in details, Fig. 6.19a considers fixed irradiance and battery voltage, and two different module temperatures, $T_{panel} = 25\,^{\circ}\text{C}$ and $T_{panel} = 50\,^{\circ}\text{C}$. Fig. 6.19b examines the impact of different irradiances on the static characteristic, with fixed mpdule temperature and battery voltage. In both cases, the plots show that there exists a boundary frequency between the LF and HF modes allowing to harvest the MPP power, in all the conditions. Fig. 6.19c shows the behaviour of the static characteristic for two different battery voltages, $V_{batt} = 12\,\text{V}$ and $14\,\text{V}$, with fixed irradiance and module temperature: in the latter case, the converter cannot harvest the MPP power, due to the power transfer limitations in the HF mode. In any case, the MPPT controller should update the control variable to always track the maximum achievable power.

6.4.4 Efficiency characterization

Fig. 6.20 shows relevant conversion efficiency plots under various operating conditions to emulate the performance of the PV-fed converter in an outdoor environment. The measured input and output powers account for gate driving losses, but exclude

Table 6.4 Main datasheet parameters of the target PV panel, Bluesun Flex-03N-110W.

Datasheet parameter	Symbol	Value
Rated power	P_{MPP}	110 W
Maximum power voltage	V_{MPP}	28.9 V
Maximum power current	I_{MPP}	3.81 A
Open circuit voltage	V_{OC}	37.1 V
Short circuit current	I_{SC}	4.50 A
Temperature coefficient of P_{MPP}	γ_{P}	$-0.38\,\%/^{o}C$
Temperature coefficient of V_{OC}	β_{V}	$-0.28\,\%/^{o}C$
Temperature coefficient of I_{SC}	α_{I}	$0.008\,\%/^{o}C$

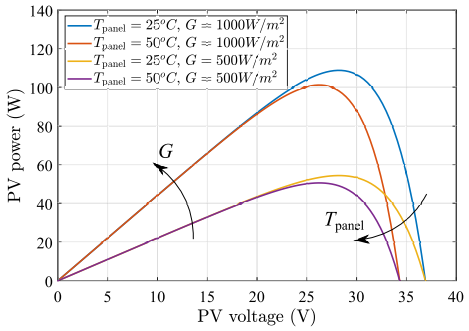
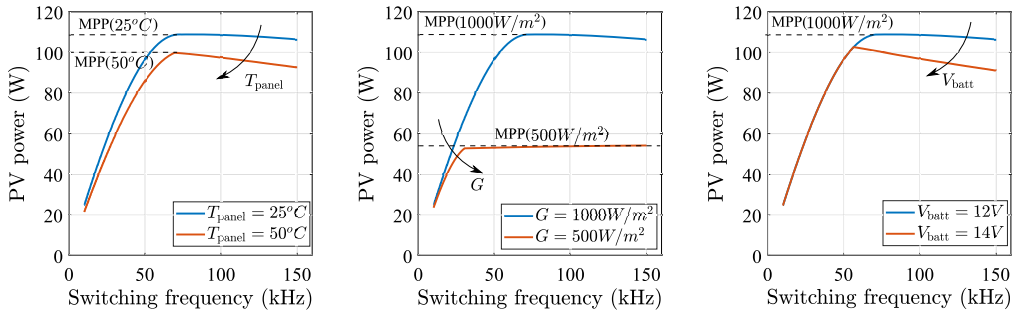


Fig. 6.18 P-V curves of the target PV panelunder different panel temperature and solar irradiance conditions.



(a) (b) (c)

Fig. 6.19 Static characteristics $P_{\text{PV}}(f_{\text{sw}})$ obtained by considering the non-linear P-V characteristic of the PV source, parametrized for different environmental and battery voltage conditions. (a) Varying module temperature, for fixed irradiance $G = 1000\,\text{W/m}^2$ and battery voltage $V_{\text{batt}} = 12\,\text{V}$; (b) Varying irradiance, for fixed module temperature $T_{\text{panel}} = 25\,^{\circ}\text{C}$ and battery voltage $V_{\text{batt}} = 12\,\text{V}$; (c) Varying battery voltage, for fixed irradiance $G = 1000\,\text{W/m}^2$ and module temperature $T_{\text{panel}} = 25\,^{\circ}\text{C}$.

the quiescent losses of the integrated circuits. The dead time was set to 80 ns, ensuring the achievement of ZVS for the input MOSFETs in most operating conditions.

Fig. 6.20a shows two efficiency plots as function of the output power at two input voltage conditions (27 V and 27.5 V), and fixed battery voltage, 12 V. The operating points in the LF and HF modes are highlighted in different colours and line styles. From the previous analysis, the power range covered in HF mode is limited unless very high switching frequencies are used. The efficiency curves remain nearly flat between 20 W and 90 W, with less than 2% efficiency drop. For the same output power, HF mode generally yields lower efficiencies due to the increased frequency-

dependent losses, such as the core losses in L_r and turn-OFF losses in M_1 and M_2. For frequencies below 15 kHz, when the transferred power falls below 20 W, the unwanted resonance among C_1, C_2 and L_o degrades the converter performance and prevents ZVS of the half-bridge MOSFETs.

Fig. 6.20b reports three efficiency curves as function of the input voltage, at 30 W, 50 W and 80 W output power, and $V_{batt} = 12$ V. The switching frequency is manually adjusted any time to achieve the desired output power. The converter achieves a peak 94% efficiency at $V_{in} = 27$ V and 30 W. The efficiency degrades at higher input voltages because of the hard-switching losses $P_{switching}$ of M_1 and M_2 at turn OFF, which can be estimated by:

$$P_{switching} \approx \frac{1}{2} f_{sw} t_{OFF} V_{IN} I_{OUT} . \tag{6.54}$$

In addition, the efficiency decreases at higher working powers for the larger conduction losses.

Fig. 6.20c shows some efficiency curves as function of the output power at various battery voltage conditions (between 12 V and 13.5 V) and at the rated input voltage, 28.5 V. The results show that the efficiency, in all the cases, is always above 90% for operating powers above 20 W. An increase in battery voltage causes $f_{boundary}$ to shift toward lower values, in accordance with (6.35), thereby inherently limiting the achievable charging power.

Fig. 6.20d reports three efficiency curves as function of the battery voltage at three power conditions (30 W, 50 W and 80 W) and $V_{in} = 28.5$ V. These measurements reproduce the realistic condition in which the battery is gradually charged according to a desired transferred power. Due to the lower conduction losses in all the components, the efficiency increases with V_{batt} for the same output power. According to Tab. 6.2, indeed, all the current stresses in the components depend on I_{out}, which is reduced at higher battery voltages. The converter achieves a peak 94.6% efficiency at 30 W and $V_{batt} = 13.5$ V.

A simulated breakdown of the losses in each converter component is reported in Fig. 6.21. The accurate loss models employed in the LTspice simulations allow to retrieve a reasonable estimation of the losses and to identify the main contributors. The simulations refer to the same operating conditions of the experimental waveforms

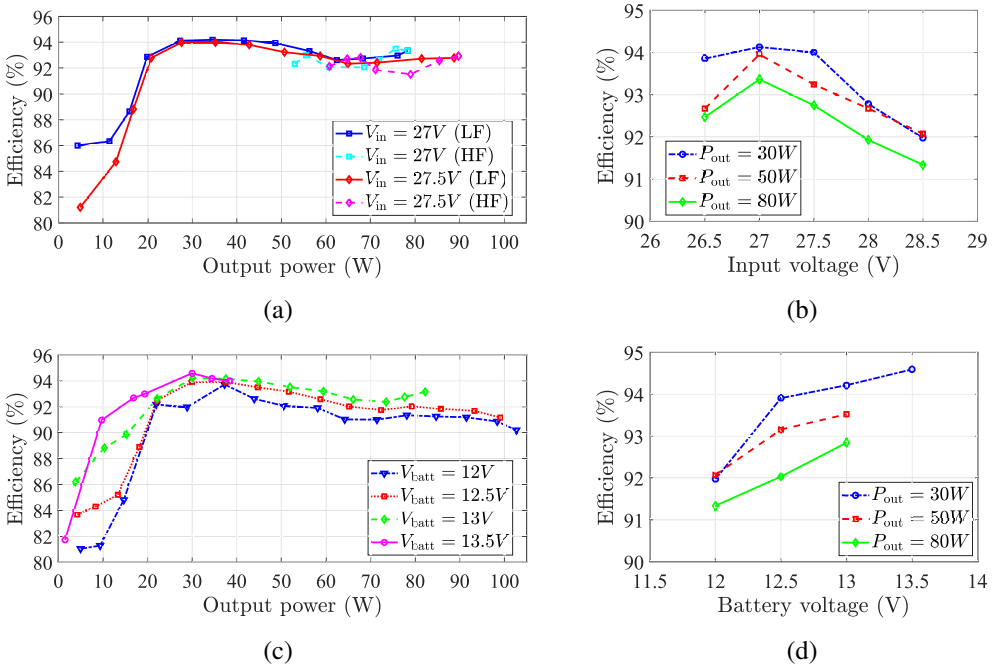


Fig. 6.20 Experimental efficiency plots at various input voltage, battery voltage and output power conditions. (a) Efficiency VS power at constant $V_{batt} = 12\,V$, at different V_{in} (27 V and 27.5 V); (b) Efficiency VS V_{in} at constant $V_{batt} = 12\,V$, at different power conditions (30 W, 50 W and 80 W); (c) Efficiency VS power at constant $V_{in} = 28.5\,V$, at different V_{batt} (from 12 V and 13.5 V); (d) Efficiency VS V_{batt} at constant $V_{in} = 28.5\,V$, at different power conditions (30 W, 50 W and 80 W).

reported in Figs. 6.14a and 6.14b, at fixed 70 W output power. Despite the losses of the clamping diodes in the LF mode, which are completely absent in the HF mode, the increased frequency causes larger dissipation in all the other components in the HF mode. The rectifier MOSFETs exhibit lower switching losses compared to the half-bridge switches, thanks to the soft switching in both the turn-ON (ZVS) and turn-OFF (nearly-ZCS).

Tab. 6.5 compares the proposed converter with state-of-the-art PV-fed battery chargers reported in the literature, with particular attention to the tested operating power range and the corresponding minimum and maximum efficiency values. The results show that the proposed solution achieves the highest efficiency over the widest power range among variable-gain converters, thereby confirming the initial claim of a high and flat efficiency profile.

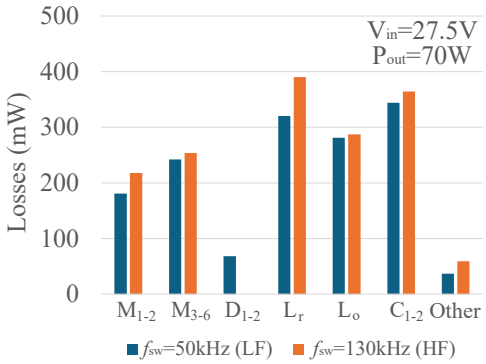


Fig. 6.21 Comparison of simulated power budget in the LF ($f_{sw} = 50\,kHz$) and HF modes ($f_{sw} = 130\,kHz$).

Table 6.5 Comparison of the proposed converter with the state of the art.

Reference	[149]	[156]	[157]	[154]	[158]	[160]	[220]	Proposed
Switching technique	Hard	Soft	Soft	Hard	Soft	Soft	Soft	Soft
Fixed/variable gain	Variable	Variable	Variable	Variable	Fixed	Fixed	Fixed	Variable
Control variable	Duty cycle	Switching frequency	Switching frequency	Duty cycle	Uncontrolled	Uncontrolled	Uncontrolled	Switching frequency
Tested voltage range	13.3 V–14.7 V	24 V	17 V–19 V	10 V–22 V	24 V	48 V	230 V (RMS)	26.5 V–28.5 V
Tested power range	3 W–27 W	5 W–20 W	4 W–48 W	10 W–80 W	80 W–90 W	10 W–100 W	15 W–65 W	20 W–100 W
Min / max efficiency	83.3 % / 89 %	81 % / 84 %	57 % / 85 %	N/A	87 % / 92 %	93.3 % / 95.3 %	80 % / 87 %	90.9 % / 94.6 %

6.5 Conclusions

This chapter has presented the analysis, design, and implementation of a new low-voltage battery charger for off-grid PV systems. One of the distinctive features of the proposed solution is the exploitation of a small resonant inductor assist the ZVS of the main MOSFETs, thereby minimizing switching losses and enhancing efficiency. With respect to the state of the art presented in Chapter 3.3, the proposed converter avoids the use of auxiliary networks typical of conventional quasi-resonant solutions, and at the same time is designed to track the MPP in a unique conversion stage, unlike other resonant solutions optimized for a single voltage conversion ratio. As a result, the proposed battery charger integrates the positive features of both quasi-resonant and resonant solutions, such as the simple control, the low component count and the gain modulation capability.

The topology of the converter analyzed in this work was derived from the adaptation of a grid-fed battery charger, offering the positive features of ZVS and intrinsic power limitation, to new specifications referred to the target PV application. The topology was further re-engineering with specific design choices to improve the conversion efficiency, such as the replacement of a passive rectifier with an active one.

A comprehensive mathematical analysis of the converter operation is provided for both the operating modes in which the converter can work. The modelling includes the derivation of the key electrical waveforms of the converter and the static characteristic, in order to predict the transferred power as function of the control variable, given a set of source and load parameters. The key design equations for the selection of the converter components are presented, to assist the designer according to the target source and load, and additional desired features such as the power range at which the ZVS condition should be achieved.

A 100 W, 28.5 V to 12 V PCB prototype was designed and tested to validate the accuracy of the mathematical modelling and the performances on a wide range of operating points. The experimental measurements of the static characteristic showed a high accuracy of the analytical modelling. The tests on the converter efficiency revealed a high and flat efficiency above 90% in the wide $20\,\mathrm{W} - 100\,\mathrm{W}$ power range, with a peak of 94.6 % at 13.5 V battery voltage. The soft commutation of the converter MOSFETs is ensured by design on a wide range, desirable feature for

outdoor PV applications in which the output power is significantly dependent on the environmental conditions.

The key benefits of the proposed solution, namely the reduced voltage stresses of the input components, the soft commutation of all the power devices and the low output current ripple, make it suitable for a MPPT battery charger for PV applications.

Future work could focus on a further refinition of the control algorithm, to embed the ZVS tracking and the MPPT control, and the experimental characterization on a real PV-battery testbench. These results will provide even stronger evidence of the positive features of the proposed solution in the field of PV-fed battery chargers.

Chapter 7

Thesis Conclusions

The work carried out in this PhD project focused on the relevant and urgent need to increase the sustainability and accessibility of the electrical energy generation, as demanded by the Agenda 2030 of the United Nations. More in details, by analyzing the continuous and increasing diffusion of the photovoltaic (PV) source within the countries energy mix, this work addressed the main role and requirements demanded by the power electronic conversion stage in enabling the collection and utilization of the electrical power from PV generators, and investigated innovative techniques to overcome the limitations of the current state-of-the-art solutions.

The introduction of the thesis highlighted the main features and characteristics of PV applications, with the specific goal of extracting the design requirements imposed to the power conversion stage. The analysis started from the equivalent circuit modelling of PV sources, and the description of its significant dependence on the environmental conditions, such as the solar irradiance, ambient temperature and uniformity of the shading. The role of power electronic converters was justified by the need of ensuring a reliable interface with the electrical grid or local off-grid loads, while accommodating the inherent variability of the electrical characteristic of PV generators. Different PV architectures were introduced and compared on the basis of multiple qualitative criteria, such as flexibility, cost, energy harvesting potential and robustness to power mismatches. General design requirements were highlighted, such as the conversion efficiency, reliability, cost effectiveness, and power density. At the same time, to cope with the changing environmental conditions,

the capability to operate with high efficiency on a wide range of operating conditions is an additional and desired requirement of power converters for this application.

Among the various PV architectures, module-level power converters (MLPC) such as microinverters and power optimizers were identified as the solutions providing the highest flexibility, which can help enhancing the penetration of the PV source in residential contexts. However, MLPC impose more demanding design requirements: this is especially true for the DC-DC conversion stage of microinverters and parallel power optimizers, which need to achieve a high step-up voltage conversion gain while ensuring a high efficiency, wide-range operation, reduced cost and high reliability. A solid and systematic analysis of the state of the art categorized the existing converters solutions while trying to identifying the common features, advantages and drawbacks of different techniques. This analysis served the purpose of guiding the implementation of new solutions to address the potential limitations of the existing converter topologies. A specific attention was also devoted to the reliability modelling of power converters, which is an often overlooked aspect of converters design, despite its significance.

The key technical contributions of this work were presented in Chapters 4, 5 and 6 and can be summarized as follows:

- a new high step-up DC-DC converter topology was presented and designed for PV applications that require particularly high conversion efficiencies and wide-range operation. To address these two targets, the proposed converter, described in details in Chapter 4, integrates in an innovative way the partial power processing and the multi-mode approaches. The converter consists in two stages, namely, a Series Resonant Converter (SRC) and a synchronous boost, connected in the Input-Parallel-Output-Series (IPOS) configuration, so as the SRC is designed to provide most of the voltage gain while operating at resonance, and the boost compensates for the remaining gain to ensure the Maximum Power Point Trackin (MPPT). This work presented the mathematical modelling of the converter operation and design workflow of the converter, followed by the experimental results on a 700 W prototype that validated the operation of the converter and demonstrated its good performances at the rated input voltage condition and over the target designed input voltage range,

15 V-45 V, and power range. The prototype showed a 97.15 % CEC efficiency at the rated voltage, superior to most of the converters designed for similar specifications in the state of the art. The multi-mode approach, allowing the SRC to always work at its highest efficiency point, ensures a reduced efficiency drop in the operating voltage voltage range.

- in Chapter 5, an optimization methodology that integrates cost, weighted efficiency and reliability was developed. Starting from the analysis of the previously proposed methodologies, it was highlighted that, while most of the design approaches focused on the optimization in terms of efficiency and power density, very few works included reliability in the design phase. When included, it is often done relying on empirical approaches that do not consider the physics of failures of the converter components, nor the mission profile. In this work, the developed methodology considers the weighted efficiency and cost as objective functions, and the trial converter solutions are discarded when they do not meet a lifetime constraint on 25 years. This lifetime constraint is computed on the basis of lifetime models that consider the physics of failure of semiconductor devices, and real mission profiles that allow to realistically simulate the thermal stresses of the converter components. The methodology was employed to optimize an IPOS converter consisting of a SRC and a synchronous boost: a 500 W prototype was designed and manufactured based on the optimal solution, found through the Particle Swarm Optimization. Experimental tests showed a 95.33 % CEC efficiency and thermal performances in line with the simulations. Fig. 7.1 reproduces the scatter plots presented in Chapter 3 to summarize the main performance parameters of the state of the art high step-up converters for PV applications: in addition, the plots include also the figures of merit of the two IPOS converters presented and tested in this work, to establish a comparison with the state of the art. Fig. 7.1a considers the CEC efficiency and gain range, while Fig. 7.1b considers the rated power and gain range, as figures of merit of the wide-range operation. The plots show that the multi-mode proposed IPOS converter is aligned with the best performing state of the art solutions in terms of weighted efficiency, extension of voltage gain and power range. Its rated power is compliant to the most advanced and recent heterojunction bifacial PV modules exhibiting superior conversion efficiencies. On the other hand, the optimized IPOS converter presented in Chapter 5 exhibits a reduced efficiency and gain range: the comparison is not

totally fair, since the design of this converter included the minimization of cost as part of the objective function, leading to cheaper components selection. Its power range is compliant with most of the commercial 60-cell and 72-cell PV modules.

- in Chapter 6, a new step-down DC-DC converter was proposed as a PV-fed battery charger for off-grid applications. The proposed quasi-resonant converter can achieve the soft-switching of its devices with a low component count and without increased electrical stresses, differently from other quasi-resonant converters designed for similar specifications. A 100 W prototype was designed and built according to realistic specifications of PV panels and low-voltage batteries, and was tested to validate the mathematical modelling of its operation and to characterize its performances. The converter showed a 94.5 % peak efficiency and a relatively flat efficiency behaviour in the 20 %-100 % load range, also thanks to the soft-switching of the semiconductor devices in most of the operating conditions. In addition, the experimental characterization of the static characteristic proved the accuracy of the analytical modelling proposed in this work.

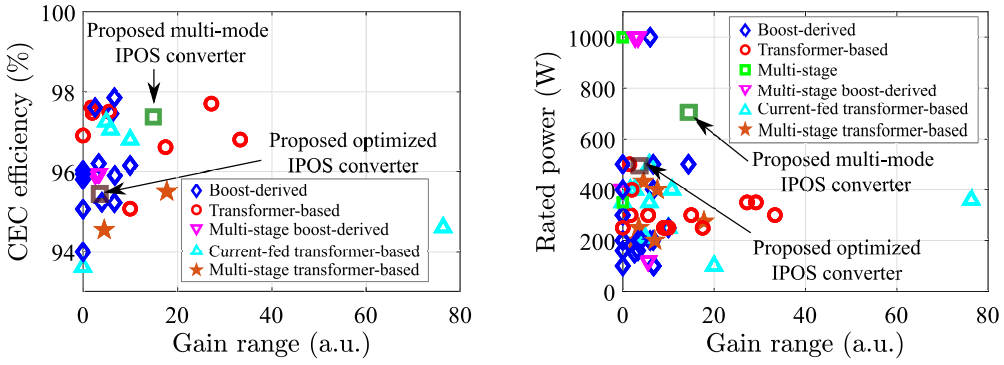


Fig. 7.1 Scatter plots of some relevant figures of merit for the proposed high step-up IPOS converters and the state-of-the-art topologies (a) CEC efficiency and gain range; (b) Rated power and gain range.

Despite the different specific key aspects of the three core projects presented in this work, some common elements can be identified. First of all, as mentioned, the PV application is the general frame above all the works, imposing specific constraints and desired features. The focus of all the developed converter solutions

always considered the efficiency, the wide-range operation, and the soft-switching of the semiconductor devices. Given the novelty of the proposed topologies, a significant attention was devoted to the mathematical modelling of the converters operation, voltage gain, and componets electrical stresses, which served as the basis for the development of ad hoc design workflows. In all the presented cases, to prove the competitiveness of the proposed solutions, a solid experimental validation on a physical prototype was necessary to validate the converters operation and performances.

A critical discussion must also consider the limitations of the new proposed solutions. The design of power electronic converters inherently involves trade-offs, as no predefined solution can offer superior characteristics across all the relevant figures of merit. As an example, wide-range converters may require costly semiconductor devices to sustain the electrical stresses across the whole power and voltage ranges. In the multi-mode IPOS converter, the main limitations can be found in the relatively large number of semiconductor devices and in the presence of two magnetic components.

Concerning the reliability-constrained optimal converter of Chapter 5, it is important to remark that the optimal solution strongly depends on the adopted models, based on the analysis of the commercial components available at the time of this work. It is necessary to expect that the optimal solutions will evolve in time with the changing cost and performance of the commercial components: from this point of view, for instance, it is reasonable that in few years, with the increasing maturity and decreasing costs of the GaN technology, GaN HEMTs may largely or totally replace Silicon MOSFETs, also in case of cost-constrained applications. In addition, the inherent tolerance on the lifetime models to assess the reliability of the converter cannot provide fully trustworthy results.

Finally, the quasi-resonant converter proposed in Chapter 6 is based on a topology that imposes strict design constraints in the selection of the PV source and/or battery, reducing its flexibility and its gain range. In addition, it was analyzed that the available power transfer depends on tolerances of passive components and resistive parasitics, which complicates its modelling and design.

More in general, a higher-level limitation of this research is linked to the difficulty of providing a totally fair comparison with the state of the art, due to the different design targets and specifications of the proposed converters in the literature. In addition, given the stronger focus on the novelty of the topologies and the limited time of the PhD, a lower attention was devoted to the control design and closed-loop testing of the converters, which is a mandatory requirement of solutions targeting real-world applications. The prototype characterization employing solar emulators or real PV panels would further validate the capability of the proposed converters to operate under real working conditions. These steps represent the natural milestones for future developments beyond the work presented in this thesis. As they were presented, some other elements are still missing before the potential commercial availability of the proposed solutions, such as a more careful power density-oriented optimization of the bill of material and PCB layout, a more thermal-aware design of the PCB and a design of the plastic case for the enclosing of the prototypes. From a power density perspective, for instance, the integration of a microcontroller in a dedicated custom control board may enhance the compactness of the prototype compared to the use of commercial development boards such as NUCLEO-STM32xx.

Concerning the impact of the results produced during the PhD, this research work was presented in multiple international IEEE conferences in the form of peer-reviewed articles. The modelling, design and experimental results of the quasi-resonant charger presented in Chapter 6 was published in IEEE Access, while two journal articles are right now under review. As inherent aspect of the academic research, the international recognition of the results of this work may contribute in further fostering the research in the direction of more sustainable technologies for the future. From the industry perspective, the industrial partner and co-founding company of this work, STMicroelectronics, has full interest in further strengthening this on-going collaboration, in perspective of achieving additional outcomes such as scientific publications and reference designs. This interest is also motivated by the perspective of collaboration with other third-party companies involved in cables and PV modules manufacturing located nearby the Catania site of STMicroelectronics.

In conclusion, this thesis provided multiple contributions to the advancement of power electronic converter design for PV applications by conceptualizing, modelling and validating innovative converter solutions and design methodologies that address

the key challenges imposed by the inherent characteristics of PV generators and the increasingly demanding requirements of modern power systems. This research combined multiple methodologies such as analytical modelling, simulations, and experimental tests, to extract both theoretical insights and practical considerations that can support the future development of high-efficiency and reliable PV conversion systems. Beyond the specific results achieved, the approaches and design principles introduced in this thesis offer a solid foundation for further academic and industrial research, in the broader frame and international effort toward the increasing integration of the PV generation in future energy systems.

References

[1] Renewables 2024. Technical report, IEA-Paris, 2024.

[2] Share of renewable electricity generation by technology, 2000-2030. Technical report, IEA-Paris, 2024.

[3] Department of Economic and Social Affairs. The sustainable development goals report 2024. Technical report, UN, 2024.

[4] Giampaolo Buticchi, Chi-Seng Lam, Ruan Xinbo, Marco Liserre, Davide Barater, Mohamed Benbouzid, Oriol Gomis-Bellmunt, Carlos Andrés Ramos-Paja, Chandan Kumar, and Rongwu Zhu. The role of renewable energy system in reshaping the electrical grid scenario. *IEEE Open Journal of the Industrial Electronics Society*, 2:451–468, 2021.

[5] Tole Sutikno, Watra Arsadiando, Aree Wangsupphaphol, Anton Yudhana, and Mochammad Facta. A review of recent advances on hybrid energy storage system for solar photovoltaics power generation. *IEEE Access*, 10:42346–42364, 2022.

[6] Md Ismail Hossain, Sowrov Komar Shib, Durjoy Roy Dipto, Tanay Banik, Abu Shufian, and Md Mukter Hossain Emon. Design and feasibility of off-grid photovoltaic charging stations for evs in remote areas. In *2024 International Conference on Innovation and Intelligence for Informatics, Computing, and Technologies (3ICT)*, pages 617–622, 2024.

[7] Jeffrey D. Sachs, Christian Kroll, Guillaume Lafortune, Grayson Fuller, and Finn Woelm. From crisis to sustainable development: the sdgs as roadmap to 2030 and beyond. sustainable development report 2022. Technical report, Cambridge University Press, 2022.

[8] Learn L. Chiloane, Muhammed Aswat, Yu-Chieh J. Yen, and Willie A. Cronje. A pv-supplied cooking solution using a hybrid electric-thermal energy storage system. In *2023 31st Southern African Universities Power Engineering Conference (SAUPEC)*, pages 1–5, 2023.

[9] Alexandros Arsalis, Panos Papanastasiou, and George E. Georghiou. Integration of a green hydrogen subsystem in a photovoltaic-battery nanogrid system. In *2022 2nd International Conference on Energy Transition in the Mediterranean Area (SyNERGY MED)*, pages 1–5, 2022.

[10] Akash Deep Verma, Virat Shishodia, Anuradha Tomar, and Prerna Gaur. Commercial solar pv off-grid battery charging/swapping station: Opportunity and solution for e-rickshaw. In *2023 2nd Edition of IEEE Delhi Section Flagship Conference (DELCON)*, pages 1–7, 2023.

[11] Hans S. Rauschenbach. *Solar Cell Array Design Handbook: The Principles and Technology of Photovoltaic Energy Conversion*. Springer Science, Dordrecht, Netherlands, 1980.

[12] Hatice Gül Sezgin-Ugranlı. Photovoltaic system performance under partial shading conditions: Insight into the roles of bypass diode numbers and inverter efficiency curve. *Sustainability*, 17(10), 2025.

[13] X.H. Nguyen. Matlab/simulink based modeling to study effect of partial shadow on solar photovoltaic array. *Environmental Systems Research*, 4, 2015.

[14] H. G. G. Nunes, F. A. L. Morais, J. A. N. Pombo, S. J. P. S. Mariano, and M. R. A. Calado. Bypass diode effect and photovoltaic parameter estimation under partial shading using a hill climbing neural network algorithm. *Frontiers in Energy Research*, 10, 2022.

[15] TC 82. Photovoltaic devices - part 3: Measurement principles for terrestrial photovoltaic (pv) solar devices with reference spectral irradiance data. Standard IEC 60904-3:2019, IET, 2019.

[16] TC 82. Terrestrial photovoltaic (pv) modules - design qualification and type approval - part 1: Test requirements. Standard IEC 61215-1:2016, IET, 2016.

[17] TC 82. Photovoltaic (pv) module safety qualification - part 1: Requirements for construction. Standard IEC 61730-1:2016, IET, 2016.

[18] Ellen David Chepp and Arno Krenzinger. A methodology for prediction and assessment of shading on pv systems. *Solar Energy*, 216:537–550, 2021.

[19] Mohammad Abdullah Al Mamun, Md Hasanuzzaman, and Jeyraj Selvaraj. Experimental investigation of the effect of partial shading on photovoltaic performance. *IET Renewable Power Generation*, 11(7):912–921, 2017.

[20] Evagelia V. Paraskevadaki and Stavros A. Papathanassiou. Evaluation of mpp voltage and power of mc-si pv modules in partial shading conditions. *IEEE Transactions on Energy Conversion*, 26(3):923–932, 2011.

[21] M.C. Alonso-García, J.M. Ruiz, and F. Chenlo. Experimental study of mismatch and shading effects in the i–v characteristic of a photovoltaic module. *Solar Energy Materials and Solar Cells*, 90(3):329–340, 2006.

[22] Kari Lappalainen and Seppo Valkealahti. Fluctuation of pv array global maximum power point voltage during irradiance transitions caused by clouds. *IET Renewable Power Generation*, 13(15):2864–2870, 2019.

[23] Samir Kouro, Jose I. Leon, Dimitri Vinnikov, and Leopoldo G. Franquelo. Grid-connected photovoltaic systems: An overview of recent research and emerging pv converter technology. *IEEE Industrial Electronics Magazine*, 9(1):47–61, 2015.

[24] Alexander Abramovitz and Doron Shmilovitz. Short survey of architectures of photovoltaic arrays for solar power generation systems. *Energies*, 14(16), 2021.

[25] Enrique Romero-Cadaval, Giovanni Spagnuolo, Leopoldo Garcia Franquelo, Carlos Andres Ramos-Paja, Teuvo Suntio, and Weidong Michael Xiao. Grid-connected photovoltaic generation plants: Components and operation. *IEEE Industrial Electronics Magazine*, 7(3):6–20, 2013.

[26] Ali Bidram, Ali Davoudi, and Robert S. Balog. Control and circuit techniques to mitigate partial shading effects in photovoltaic arrays. *IEEE Journal of Photovoltaics*, 2(4):532–546, 2012.

[27] Branislav Stevanović, Emanuel Serban, Santiago Cóbreces, Pedro Alou, Martin Ordonez, and Miroslav Vasić. Dc/dc stage contribution to bus voltage in 1000- and 1500-v grid-connected solar inverters. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 10(5):6252–6265, 2022.

[28] Engin Karatepe, Takashi Hiyama, Mutlu Boztepe, and Metin Colak. Power controller design for photovoltaic generation system under partially shaded insolation conditions. In *2007 International Conference on Intelligent Systems Applications to Power Systems*, pages 1–6, 2007.

[29] T. Shimizu, M. Hirakata, T. Kamezawa, and H. Watanabe. Generation control circuit for photovoltaic modules. *IEEE Transactions on Power Electronics*, 16(3):293–300, 2001.

[30] Ye Yuanmao, K. W. E. Cheng, and Y. P. B. Yeung. Zero-current switching switched-capacitor zero-voltage-gap automatic equalization system for series battery string. *IEEE Transactions on Power Electronics*, 27(7):3234–3242, 2012.

[31] Samir Soua and Guillaume Barbier de Préville. Mvdc for modern grids: Enabling flexibility and resilience. Technical report, General Electric Vernova, 2024.

[32] Huili YE, Miao ZHU, Xiuyi LI, and Xu CAI. Quantitative analysis and performance comparison of dc pv power collection network with different configurations. In *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, pages 1905–1910, 2020.

[33] Boris Dumnić, Elizaveta Liivik, Bane Popadić, Frede Blaabjerg, Dragan Milićević, and Vladimir Katić. Comparative analysis of reliability for string and central inverter pv systems in accordance with the fmeca. In *2020 IEEE 11th*

International Symposium on Power Electronics for Distributed Generation Systems (PEDG), pages 591–596, 2020.

[34] Mohammad Jafari, Zahra Malekjamshidi, Glenn Platt, Jian Guo Zhu, and D. G. Dorrell. A multi-port converter based renewable energy system for residential consumers of smart grid. In *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, pages 005168–005173, 2015.

[35] Lu Zhou, Yihan Gao, Hao Ma, and Philip T Krein. A soft-switching four-port integrated converter topology based on residential pv energy storage and charging application. In *IECON 2023- 49th Annual Conference of the IEEE Industrial Electronics Society*, pages 1–6, 2023.

[36] Liran Zheng, Rajendra Prasad Kandula, and Deepak Divan. Multiport control with partial power processing in solid-state transformer for pv, storage, and fast-charging electric vehicle integration. *IEEE Transactions on Power Electronics*, 38(2):2606–2616, 2023.

[37] Guipeng Chen, Yuwei Liu, and Wenfeng Cui. Partial power processing multiport dc-dc converters. In *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, pages 1406–1411, 2020.

[38] Yong Dae Kwon, Francisco D. Freijedo, Thiwanka Wijekoon, and Marco Liserre. A multiport partial power converter for smart home applications. *IEEE Transactions on Power Electronics*, 39(7):8824–8833, 2024.

[39] Neelesh Yadav, Andrii Chub, and Lauri Kütt. Three-port current fed push/pull partial power converter for integration of pv/battery systems in dc microgrids. In *2024 19th Biennial Baltic Electronics Conference (BEC)*, pages 1–6, 2024.

[40] Jiangfeng Wang, Kai Sun, Cheng Xue, Tingting Liu, and Yunwei Li. Multiport dc-ac converter with differential power processing dc-dc converter and flexible power control for battery ess integrated pv systems. *IEEE Transactions on Industrial Electronics*, 69(5):4879–4889, 2022.

[41] Khalil Alluhaybi, Issa Batarseh, and Haibing Hu. Comprehensive review and comparison of single-phase grid-tied photovoltaic microinverters. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8(2):1310–1329, 2020.

[42] Matthias Kasper, Dominik Bortis, and Johann W. Kolar. Classification and comparative evaluation of pv panel-integrated dc–dc converter concepts. *IEEE Transactions on Power Electronics*, 29(5):2511–2526, 2014.

[43] Antoneta Iuliana Bratcu, Iulian Munteanu, Seddik Bacha, Damien Picault, and Bertrand Raison. Cascaded dc–dc converter photovoltaic systems: Power optimization issues. *IEEE Transactions on Industrial Electronics*, 58(2):403–411, 2011.

[44] Sally Sajadian and Reza Ahmadi. Distributed maximum power point tracking using model predictive control for photovoltaic energy harvesting architectures based on cascaded power optimizers. *IEEE Journal of Photovoltaics*, 7(3):849–857, 2017.

[45] Riad Kadri, Jean-Paul Gaubert, and Gerard Champenois. Nondissipative string current diverter for solving the cascaded dc–dc converter connection problem in photovoltaic power generation system. *IEEE Transactions on Power Electronics*, 27(3):1249–1258, 2012.

[46] Sara M. MacAlpine, Robert W. Erickson, and Michael J. Brandemuehl. Characterization of power optimizer potential to increase energy capture in photovoltaic systems operating under nonuniform conditions. *IEEE Transactions on Power Electronics*, 28(6):2936–2945, 2013.

[47] Tekai Eddine Khalil Zidane, Ali Saleh Aziz, Younes Zahraoui, Hossam Kotb, Kareem M. AboRas, Kitmo, and Yosef Berhan Jember. Grid-connected solar pv power plants optimization: A review. *IEEE Access*, 11:79588–79608, 2023.

[48] Daniel de B. Mesquita, João Lucas de S. Silva, Hugo S. Moreira, Michelle Kitayama, and Marcelo G. Villalva. A review and analysis of technologies applied in pv modules. In *2019 IEEE PES Innovative Smart Grid Technologies Conference - Latin America (ISGT Latin America)*, pages 1–6, 2019.

[49] Vaibhav R. Pannase and H. B. Nanavala. A review of pv technology power generation, pv material, performance and its applications. In *2017 International Conference on Inventive Systems and Control (ICISC)*, pages 1–5, 2017.

[50] Apolline Puaud, Anne-Sophie Ozanne, Laurie-Lou Senaud, Delfina Muñoz, and Charles Roux. Microcrystalline silicon tunnel junction for monolithic tandem solar cells using silicon heterojunction technology. *IEEE Journal of Photovoltaics*, 11(1):58–64, 2021.

[51] Sani Mohammed Lawal, Nazila Fough, Nazmi Sellami, and Firdaus Muhammad-Sukki. Modeling and simulation of heterojunction solar cell; determination of optimal values. In *2023 21st IEEE Interregional NEWCAS Conference (NEWCAS)*, pages 1–2, 2023.

[52] Yeongrack Son, Satyaki Mukherjee, Rahul Mallik, Branko Majmunovi'c, Soham Dutta, Brian Johnson, Dragan Maksimović, and Gab-Su Seo. Levelized cost of energy-oriented modular string inverter design optimization for pv generation system using geometric programming. *IEEE Access*, 10:27561–27578, 2022.

[53] Automatic switching point between a grid-parallel self-generation plant and the public low-voltage grid. Technical report, VDE, 2013.

[54] TC 82. Iec 62116:2014: Utility-interconnected photovoltaic inverters - test procedure of islanding prevention measures. Technical report, IEC, 2014.

[55] TC 82. Iec 61727:2004: Photovoltaic (pv) systems - characteristics of the utility interface. Technical report, IEC, 2004.

[56] Ward Bower and Michael Ropp. Report iea pvps t5-09: Evaluation of islanding detection for photovoltaic utility-interactive power systems. Technical report, International Energy Agency, 2002.

[57] TC 82. Iec 62109-1:2010: Safety of power converters for use in photovoltaic power systems - part 1: General requirements. Technical report, IEC, 2010.

[58] Christoph Panhuber. Report iea pvps t5-04:2001: Pv system installation and grid-interconnection guidelines in selected iea countries. Technical report, International Energy Agency, 2001.

[59] Vde-ar-e 2100-712: Measures for the dc area of a photovoltaic system to ensure electrical safety in the event of firefighting or technical assistance. Technical report, VDE, 2018.

[60] Simon Ravyts, Mauricio Dalla Vecchia, Giel Van den Broeck, and Johan Driesen. Review on building-integrated photovoltaics electrical system requirements and module-integrated converter recommendations. *Energies*, 12(8), 2019.

[61] Paolo Corti, Luisa Capannolo, Pierluigi Bonomo, Pierluigi De Berardinis, and Francesco Frontini. Comparative analysis of bipv solutions to define energy and cost-effectiveness in a case study. *Energies*, 13(15), 2020.

[62] R. Opsomer, S. Ravyts, G. van den Broeck, and J. Driesen. Techno-economic analysis of building integrated photovoltaics electrical installations. In *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, volume 1, pages 2572–2577, 2019.

[63] Andrii Chub, Dmitri Vinnikov, Oleksandr Korkh, Mariusz Malinowski, and Samir Kouro. Ultrawide voltage gain range microconverter for integration of silicon and thin-film photovoltaic modules in dc microgrids. *IEEE Transactions on Power Electronics*, 36(12):13763–13778, 2021.

[64] Mojtaba Forouzesh, Yam P. Siwakoti, Saman A. Gorji, Frede Blaabjerg, and Brad Lehman. Step-up dc–dc converters: A comprehensive review of voltage-boosting techniques, topologies, and applications. *IEEE Transactions on Power Electronics*, 32(12):9143–9178, 2017.

[65] Yueshi Guan, Carlo Cecati, J. Marcos Alonso, and Zhe Zhang. Review of high-frequency high-voltage-conversion-ratio dc–dc converters. *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, 2(4):374–389, 2021.

[66] Márcio R. S. de Carvalho, Rafael C. Neto, Eduardo J. Barbosa, Leonardo R. Limongi, Fabrício Bradaschia, and Marcelo C. Cavalcanti. An overview of voltage boosting techniques and step-up dc-dc converters topologies for pv applications. *Energies*, 14(24), 2021.

[67] Mahmoud A. Gaafar, Mohamed Orabi, Ahmed Ibrahim, Ralph Kennel, and Mohamed Abdelrahem. Common-ground photovoltaic inverters for leakage current mitigation: Comparative review. *Applied Sciences*, 11(23), 2021.

[68] Manxin Chen, Changqing Yin, Poh Chiang Loh, and Adrian Ioinovici. Improved large dc gain converters with low voltage stress on switches based on coupled-inductor and voltage multiplier for renewable energy applications. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8(3):2824–2836, 2020.

[69] Jian Ai and Mingyao Lin. Ultralarge gain step-up coupled-inductor dc–dc converter with an asymmetric voltage multiplier network for a sustainable energy system. *IEEE Transactions on Power Electronics*, 32(9):6896–6903, 2017.

[70] Gang Wu, Xinbo Ruan, and Zhihong Ye. High step-up dc–dc converter based on switched capacitor and coupled inductor. *IEEE Transactions on Industrial Electronics*, 65(7):5572–5579, 2018.

[71] Yan Deng, Qiang Rong, Wuhua Li, Yi Zhao, Jianjiang Shi, and Xiangning He. Single-switch high step-up converters with built-in transformer voltage multiplier cell. *IEEE Transactions on Power Electronics*, 27(8):3557–3567, 2012.

[72] Waqas Hassan, Dylan Dah-Chuan Lu, and Weidong Xiao. Single-switch high step-up dc–dc converter with low and steady switch voltage stress. *IEEE Transactions on Industrial Electronics*, 66(12):9326–9338, 2019.

[73] Vafa Marzang, Seyed Hossein Hosseini, Naghi Rostami, Peyman Alavi, Parham Mohseni, and Seyed Majid Hashemzadeh. A high step-up nonisolated dc–dc converter with flexible voltage gain. *IEEE Transactions on Power Electronics*, 35(10):10489–10500, 2020.

[74] Sareh Daneshgar, Ebrahim Babaei, and Mohammad Bagher Bannae Sharifian. Quadratic high step-up interleaved z-source dc-dc converters based on asymmetric gamma cell. *IEEE Transactions on Power Electronics*, 40(12):17858–17868, 2025.

[75] António Manuel Santos Spencer Andrade, Luciano Schuch, and Mário Lúcio da Silva Martins. Analysis and design of high-efficiency hybrid high step-up dc–dc converter for distributed pv generation systems. *IEEE Transactions on Industrial Electronics*, 66(5):3860–3868, 2019.

[76] Yam P. Siwakoti and Frede Blaabjerg. Single switch nonisolated ultra-step-up dc–dc converter with an integrated coupled inductor for high boost applications. *IEEE Transactions on Power Electronics*, 32(11):8544–8558, 2017.

[77] Arshad Mahmood, Mohammad Zaid, Javed Ahmad, Mohd Anas Khan, Shahrukh Khan, Zaid Sifat, Chang-Hua Lin, Adil Sarwar, Mohd Tariq, and Basem Alamri. A non-inverting high gain dc-dc converter with continuous input current. *IEEE Access*, 9:54710–54721, 2021.

[78] Vemparala Seshagiri Rao, M. S. Bhaskar, Mahmoud F. Elmorshedy, and Dhafer Almakhles. Wide voltage gain range enhanced cubic boost converter with reduced components voltage stress. *IEEE Access*, 13:8032–8041, 2025.

[79] Yuanmao Ye, K. W. E. Cheng, and Sizhe Chen. A high step-up pwm dc-dc converter with coupled-inductor and resonant switched-capacitor. *IEEE Transactions on Power Electronics*, 32(10):7739–7749, 2017.

[80] Xiangjun Zhang, Lei Sun, Yueshi Guan, Shouheng Han, Hongye Cai, Yijie Wang, and Dianguo Xu. Novel high step-up soft-switching dc–dc converter based on switched capacitor and coupled inductor. *IEEE Transactions on Power Electronics*, 35(9):9471–9481, 2020.

[81] Peyman Alavi, Parham Mohseni, Ebrahim Babaei, and Vafa Marzang. An ultra-high step-up dc–dc converter with extendable voltage gain and soft-switching capability. *IEEE Transactions on Industrial Electronics*, 67(11):9238–9250, 2020.

[82] Sohrab Abbasian, Mohammad Farsijani, Haniyeh Katiraee, Hossein Hafezi, and Tomi Roinila. Fully soft-switched single-switch high gain dc–dc topology based on coupled inductor. *IEEE Access*, 12:108121–108133, 2024.

[83] D. V. Sudarsan Reddy, Mallikarjuna Golla, and S. Thangavel. A new soft-switching high gain dc-dc converter with reduced components realized by active clamp and coupled inductors. *IEEE Transactions on Consumer Electronics*, 71(2):2749–2761, 2025.

[84] Sara Hasanpour, Mojtaba Forouzesh, Yam P. Siwakoti, and Frede Blaabjerg. A new high-gain, high-efficiency sepic-based dc–dc converter for renewable energy applications. *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, 2(4):567–578, 2021.

[85] Manoharan Premkumar, Umashankar Subramaniam, Hassan Haes Alhelou, and Pierluigi Siano. Design and development of non-isolated modified sepic dc-dc converter topology for high-step-up applications: Investigation and hardware implementation. *Energies*, 13(15), 2020.

[86] Lenon Schmitz, Denizar C. Martins, and Roberto F. Coelho. High step-up nonisolated zvs/zcs dc–dc converter for photovoltaic thin-film module applications. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 7(1):565–575, 2019.

[87] Hongfei Wu, Tian Xia, Yan Xing, Peng Xu, Haibing Hu, and Zhuoran Zhang. Secondary-side phase-shift-controlled high step-up hybrid resonant converter with voltage multiplier for high efficiency pv applications. In *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 1428–1434, 2015.

[88] Christian P. Dick, Furkan K. Titiz, and Rik W. De Doncker. A high-efficient llcc series-parallel resonant converter. In *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 696–701, 2010.

[89] Thomas LaBella and Jih-Sheng Lai. A hybrid resonant converter utilizing a bidirectional gan ac switch for high-efficiency pv applications. *IEEE Transactions on Industry Applications*, 50(5):3468–3475, 2014.

[90] Dmitri Vinnikov, Andrii Chub, Elizaveta Liivik, and Indrek Roasto. High-performance quasi-z-source series resonant dc–dc converter for photovoltaic module-level power electronics applications. *IEEE Transactions on Power Electronics*, 32(5):3634–3650, 2017.

[91] Vadim Sidorov, Andrii Chub, and Dmitri Vinnikov. High-efficiency quad-mode parallel pv power optimizer for dc microgrids. *IEEE Transactions on Industry Applications*, 59(1):1002–1012, 2023.

[92] Wenjie Zhao, Qunfang Wu, Qin Wang, Lan Xiao, Xiaodong Yang, and Xinrong Cai. An ultrawide input range llc resonant converter with multi-mode switchable rectifier. In *2024 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 2752–2755, 2024.

[93] Xiaonan Zhao, Lanhua Zhang, Rachael Born, and Jih-Sheng Lai. A high-efficiency hybrid resonant converter with wide-input regulation for photovoltaic applications. *IEEE Transactions on Industrial Electronics*, 64(5):3684–3695, 2017.

[94] Fahad Alaql, Abdullah Alhatlani, and Issa Batarseh. Improved llc resonant converter with rectifier operating in three operation modes for wide voltage range applications. In *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 1945–1950, 2021.

[95] Fahad Alaql, Reza Rezaii, Abdullah Alhatlani, Sahin Gullu, Md Safayatullah, and Issa Batarseh. Multi-mode rectifier-based dual-input llc converter for wide voltage pv applications. In *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 1–5, 2022.

[96] Rasedul Hasan and Saad Mekhilef. A resonant double stage flyback microinverter for pv applications. In *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 2051–2056, 2017.

[97] Pengyu Jia and Yang Mei. Derivation and analysis of a secondary-side llc resonant converter for the high step-up applications. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 9(5):5865–5882, 2021.

[98] Nicolas Muller, Freddy Flores-Bahamonde, Daniel Pesantez, Hugues Renaudineau, Diana Lopez-Caiza, and Samir Kouro. Reconfigurable partial power converter for power optimizers in pv systems. In *IECON 2022 – 48th Annual Conference of the IEEE Industrial Electronics Society*, pages 1–6, 2022.

[99] Niraj Rana and Subrata Banerjee. Development of an improved input-parallel output-series buck-boost converter and its closed-loop control. *IEEE Transactions on Industrial Electronics*, 67(8):6428–6438, 2020.

[100] Víctor Ferreira Gruner, Lucas Fiamoncini, Lenon Schmitz, Denizar Cruz Martins, and Roberto Francisco Coelho. High step-up dc-dc converter with input current sharing based on the forward converter. In *2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC)*, pages 1–6, 2019.

[101] Shahin Honarmand, Amirhossein Rajaei, Mahdi Shahparasti, Alvaro Luna, and Edris Pouresmaeil. A modified partial power structure for quasi z-source converter to improve voltage gain and power rating. *Energies*, 12(11), 2019.

[102] Mojtaba Forouzesh, Yanfeng Shen, Keyvan Yari, Yam P. Siwakoti, and Frede Blaabjerg. High-efficiency high step-up dc–dc converter with dual coupled inductors for grid-connected photovoltaic systems. *IEEE Transactions on Power Electronics*, 33(7):5967–5982, 2018.

[103] Tongmin Liu, Mingyao Lin, and Jian Ai. High step-up interleaved dc–dc converter with asymmetric voltage multiplier cell and coupled inductor. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8(4):4209–4222, 2020.

[104] Xuefeng Hu, Xing Liu, Yujia Zhang, Zhixiang Yu, and Shunde Jiang. A hybrid cascaded high step-up dc–dc converter with ultralow voltage stress. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 9(2):1824–1836, 2021.

[105] Mamdouh L. Alghaythi, Robert M. O'Connell, Naz E. Islam, and Josep M. Guerrero. A non-isolated high step-up interleaved dc-dc converter with diode-capacitor multiplier cells and dual coupled inductors. In *2020 52nd North American Power Symposium (NAPS)*, pages 1–6, 2021.

[106] Qiao Zhang, Xuefeng Hu, Han Xu, and Zhenhai Yu. A novel input-parallel output-series high gain dc- dc boost converter with voltage-doubler cell. In *2022 IEEE 5th International Electrical and Energy Conference (CIEEC)*, pages 641–646, 2022.

[107] Mohammad Altimania, Mohamad Saleh Sanjari Nia, Mehdi Ferdowsi, and Pourya Shamsi. A new topology of a high-voltage-gain dc-dc converter based on modified greinacher voltage multiplier. In *2020 IEEE Kansas Power and Energy Conference (KPEC)*, pages 1–6, 2020.

[108] Wuhua Li, Weichen Li, Xiangning He, David Xu, and Bin Wu. General derivation law of nonisolated high-step-up interleaved converters with built-in transformer. *IEEE Transactions on Industrial Electronics*, 59(3):1650–1661, 2012.

[109] Jianfei Chen, Kewei Ding, Yulin Zhong, Fujin Deng, and Sayed Abulanwar. A double input-parallel-output-series hybrid switched-capacitor boost converter. *Chinese Journal of Electrical Engineering*, 6(4):15–27, 2020.

[110] Haodong Lei, Ruixiang Hao, Xiaojie You, and Fang Li. Nonisolated high step-up soft-switching dc–dc converter with interleaving and dickson switched-capacitor techniques. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 8(3):2007–2021, 2020.

[111] Mohammad Nilian, Reza Rezaii, Mohamed Tamasas Elrais, and Issa Batarseh. A gan-based dc–dc multistage hybrid converter for step-up applications. In *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 2512–2517, 2023.

[112] M. S. Bhaskar, Nikita Gupta, Sivakumar Selvam, Dhafer J. Almakhles, P. Sanjeevikumar, Jagabar Sathik Mohamed Ali, and S. Umashankar. A new hybrid zeta-boost converter with active quad switched inductor for high voltage gain. *IEEE Access*, 9:20022–20034, 2021.

[113] Shuai Jiang, Dong Cao, Yuan Li, and Fang Zheng Peng. Grid-connected boost-half-bridge photovoltaic microinverter system using repetitive current control and maximum power point tracking. *IEEE Transactions on Power Electronics*, 27(11):4711–4722, 2012.

[114] Ji-Ho Choi, Muhammad Mubeen Khan, Su-Hyeong Kim, Han-Ho Choi, and Minsung Kim. Highly efficient asymmetric boost half-bridge diode-clamped dc/dc converter under wide input voltage range. *IEEE Transactions on Industrial Electronics*, 71(7):6986–6999, 2024.

[115] Ben York, Wensong Yu, and Jih-Sheng Lai. An integrated boost resonant converter for photovoltaic applications. *IEEE Transactions on Power Electronics*, 28(3):1199–1207, 2013.

[116] Armin Miremad and Suzan Eren. Hybrid resonant and non-resonant coupled-inductor-based current-fed dc–dc converter. *IEEE Open Journal of Power Electronics*, 6:761–779, 2025.

[117] Preenu Paul, Babita R. Jose, Thottathikkulam K. Shahana, Chikku Abraham, and Jimson Mathew. High gain isolated quasi-switched boost converter

embedded with switched capacitor cell. *Electric Power Components and Systems*, 49(4-5):333–344, 2021.

[118] Young-Ho Kim, Soo-Cheol Shin, Jung-Hyo Lee, Yong-Chae Jung, and Chung-Yuen Won. Soft-switching current-fed push–pull converter for 250-w ac module applications. *IEEE Transactions on Power Electronics*, 29(2):863–872, 2014.

[119] Dongchun Wu, Yunya Wu, Jiarong Kan, Yu Tang, Jian Chen, and Lin Jiang. Full-bridge current-fed pv microinverter with dlfcr reduction ability. *IEEE Transactions on Power Electronics*, 35(9):9541–9552, 2020.

[120] Saeed Pourjafar, Parham Mohseni, Oleksandr Matiushkin, Oleksandr Husev, and Dmitri Vinnikov. Novel isolated high step-up dc-dc converter with wide input voltage regulation range. In *2023 IEEE 64th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON)*, pages 1–6, 2023.

[121] Parham Mohseni, Saeed Pourjafar, Oleksandr Matiushkin, Oleksandr Husev, and Dmitri Vinnikov. Isolated high step-up current-fed dc-dc converter with low input current ripple and wide full-soft-switching capability. *IEEE Transactions on Industry Applications*, 61(4):6499–6510, 2025.

[122] Salman Khan, Andrii Chub, Dmitri Vinnikov, Matthias Kasper, and Gerald Deboy. Comparative study of buck control methods for current-fed series resonant converters in wide voltage gain range applications. In *IECON 2025 – 51st Annual Conference of the IEEE Industrial Electronics Society*, pages 1–6, 2025.

[123] Runan Gu, Donglai Zhang, Jinpei Duan, and Anshou Li. An interleaved current-fed integrated llc resonant converter with input current ripple cancellation. *IEEE Transactions on Industrial Electronics*, 72(4):3587–3597, 2025.

[124] Matthias Kasper, Magdalena Ritz, Dominik Bortis, and Johann W. Kolar. Pv panel-integrated high step-up high efficiency isolated gan dc-dc boost converter. In *Intelec 2013; 35th International Telecommunications Energy Conference, SMART POWER AND EFFICIENCY*, pages 1–7, 2013.

[125] Kerui Li, Cho Kin Yeung, Siew Chong Tan, and Ron Shu Yuen Hui. Multimode llc resonant dc-dc converters for wide range input voltage. In *2019 IEEE 4th International Future Energy Electronics Conference (IFEEC)*, pages 1–5, 2019.

[126] Xikun Sang, Yijie Wang, Shanshan Gao, Yueshi Guan, and Dianguo Xu. Analysis and design of a partial power processing architecture for high step-up applications. *IEEE Transactions on Power Electronics*, 38(7):8654–8665, 2023.

[127] Runan Gu, Jinpei Duan, Donglai Zhang, and He Liu. Regulated series hybrid converter with dc transformer (dcx) for step-up power conversion. *IEEE Transactions on Industrial Electronics*, 69(9):8961–8971, 2022.

[128] Xikun Sang, Shanshan Gao, Yijie Wang, and Dianguo Xu. A high step-up partial power regulated dc–dc converter with zero input current ripple and wide input range. *IEEE Transactions on Industrial Electronics*, 71(11):14097–14110, 2024.

[129] Mingxiao Li, Ziwei Ouyang, Michael A. E. Andersen, and Gang Wang. An efficiency-oriented two-stage structure employing partial power regulation. In *2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)*, pages 2104–2109, 2020.

[130] Saeed Peyghami, Frede Blaabjerg, and Peter Palensky. Incorporating power electronic converters reliability into modern power system reliability analysis. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 9(2):1668–1681, 2021.

[131] Anastasios Golnas. Pv system reliability: An operator's perspective. *IEEE Journal of Photovoltaics*, 3(1):416–421, 2013.

[132] Geoffrey Klise, Olga Lavrova, and Renee Gooding. Pv system component fault and failure compilation and analysis. Technical report, Sandia National Laboratories, 2018.

[133] Saeed Peyghami, Zhongxu Wang, and Frede Blaabjerg. A guideline for reliability prediction in power electronic converters. *IEEE Transactions on Power Electronics*, 35(10):10958–10968, 2020.

[134] Saeed Peyghami, Zhongxu Wang, and Frede Blaabjerg. Reliability modeling of power electronic converters: A general approach. In *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pages 1–7, 2019.

[135] Rui Wu, Frede Blaabjerg, Huai Wang, Marco Liserre, and Francesco Iannuzzo. Catastrophic failure and fault-tolerant design of igbt power electronic converters - an overview. In *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, pages 507–513, 2013.

[136] USA Department of Defence. *MIL-HDBK-217F: Military Handbook Reliability Prediction of Electronic Equipment*. 1991.

[137] K. Priyadarshini and A. B. Raju. Reliability of dc-dc converters used as mppt in grid connected photovoltaic systems. In *2016 International Conference on Circuits, Controls, Communications and Computing (I4C)*, pages 1–6, 2016.

[138] M. Catelani, L. Ciani, A. Reatti, F. Corti, V. Sorrentino, Agasthya Ayachit, and Marian K. Kazimierczuk. Reliability analysis and electrical characterization of a class-e resonant inverter. In *2018 IEEE International Instrumentation and Measurement Technology Conference (I2MTC)*, pages 1–6, 2018.

[139] Salman Khan, Andrii Chub, Dmitri Vinnikov, Matthias Kasper, and Gerald Deboy. Reliability evaluation of the universal power electronic interface converter for pv applications. In *2024 IEEE 21st International Power Electronics and Motion Control Conference (PEMC)*, pages 1–8, 2024.

[140] Hui Huang and P. A. Mawby. A lifetime estimation technique for voltage source inverters. *IEEE Transactions on Power Electronics*, 28(8):4113–4119, 2013.

[141] Paula Diaz Reigosa, Huai Wang, Yongheng Yang, and Frede Blaabjerg. Prediction of bond wire fatigue of igbts in a pv inverter under a long-term operation. *IEEE Transactions on Power Electronics*, 31(10):7171–7182, 2016.

[142] Johannes Falck, Christian Felgemacher, Andreja Rojko, Marco Liserre, and Peter Zacharias. Reliability of power electronic systems: An industry perspective. *IEEE Industrial Electronics Magazine*, 12(2):24–35, 2018.

[143] Reinhold Bayerer, Tobias Herrmann, Thomas Licht, Josef Lutz, and Marco Feller. Model for power cycling lifetime of igbt modules - various factors influencing lifetime. In *5th International Conference on Integrated Power Electronics Systems*, pages 1–6, 2008.

[144] Mahera Musallam, Chunyan Yin, Chris Bailey, and C. Mark Johnson. Application of coupled electro-thermal and physics-of-failure-based analysis to the design of accelerated life tests for power modules. *Microelectronics Reliability*, 54(1):172–181, 2014.

[145] Mahera Musallam, Chunyan Yin, Christopher Bailey, and Mark Johnson. Mission profile-based reliability design and real-time life consumption estimation in power electronics. *IEEE Transactions on Power Electronics*, 30(5):2601–2613, 2015.

[146] Alexander Otto and Sven Rzepka. Lifetime modelling of discrete power electronic devices for automotive applications. In *AmE 2019 - Automotive meets Electronics; 10th GMM-Symposium*, pages 1–6, 2019.

[147] Alessandro Vaccaro, Andrea Zilio, and Paolo Magnone. Lifetime prediction in power semiconductor devices: A comparative study between analytical modeling and artificial neural network. In *2023 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 1172–1176, 2023.

[148] Serkan Dusmez, Hamit Duran, and Bilal Akin. Remaining useful lifetime estimation for thermally stressed power mosfets based on on-state resistance variation. *IEEE Transactions on Industry Applications*, 52(3):2554–2563, 2016.

[149] Kumar Sachin, Vivek Prakash Yadav, Aashiwal Nirmal Mukesh, Praveen Kumar Sharma, and L Solanki. Design and development of pwm based solar hybrid charge controller. In *2021 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT)*, pages 1–6, 2021.

[150] Amar Brar, Robert Sanborn, Amr Radwan, and Xichen Jiang. A mobile photovoltaic-battery system for off-grid applications. In *2020 International Conference on Electrical, Communication, and Computer Engineering (ICECCE)*, pages 1–5, 2020.

[151] Ting-Lien Wu and Jia-Sheng Hu. Dual-input dc-dc power converter for solar battery charger. In *2016 IEEE 11th Conference on Industrial Electronics and Applications (ICIEA)*, pages 1201–1206, 2016.

[152] Debashish Mohapatra, Subhransu Padhee, and Jhansirani Jena. Design of solar powered battery charger: An experimental verification. In *2018 IEEE International Students' Conference on Electrical, Electronics and Computer Science (SCEECS)*, pages 1–5, 2018.

[153] Aldrin Claytus Vaz, C Gurudas Nayak, and Dayananda Nayak. Pulse width modulation based solar charge controller. In *2019 3rd International conference on Electronics, Communication and Aerospace Technology (ICECA)*, pages 1067–1071, 2019.

[154] S. J. Chiang, Hsin-Jang Shieh, and Ming-Chieh Chen. Modeling and control of pv charger system with sepic converter. *IEEE Transactions on Industrial Electronics*, 56(11):4344–4353, 2009.

[155] Cheng-Wei Chen, Kun-Hung Chen, and Yaow-Ming Chen. A semi-isolated multi-input converter for hybrid pv/wind power charger system. In *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, pages 3592–3597, 2014.

[156] Ying-Chun Chuang and Yu-Lung Ke. A novel high-efficiency battery charger with a buck zero-voltage-switching resonant converter. *IEEE Transactions on Energy Conversion*, 22(4):848–854, 2007.

[157] A. S. Werulkar and P. S. Kulkarni. Design of a constant current solar charge controller with microcontroller based soft switching buck converter for solar home lighting system. In *2012 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, pages 1–6, 2012.

[158] Yu-Lung Ke, Ying-Chun Chuang, Mei-Sung Kang, Yuan-Kang Wu, Ching-Ming Lai, and Chien-Chih Yu. Solar power battery charger with a parallel-load resonant converter. In *2011 IEEE Industry Applications Society Annual Meeting*, pages 1–8, 2011.

[159] Rakhi K., Ilango K., Manjunath H.V, and Manjula G Nair. Simulation analysis of half bridge series parallel resonant converter based battery charger for photovoltaic system. In *2014 POWER AND ENERGY SYSTEMS: TOWARDS SUSTAINABLE ENERGY*, pages 1–5, 2014.

[160] Mohammad Mousavi, Younes Sangsefidi, Ali Mehrizi-Sani, and Reza Beiranvand. Generalized step-down switched-capacitor converter under zcs for photovoltaic applications. *IEEE Transactions on Energy Conversion*, 33(3):1321–1329, 2018.

[161] Jon Anzola, Iosu Aizpuru, Asier Arruti Romero, Argiñe Alacano Loiti, Ramon Lopez-Erauskin, Jesús Sergio Artal-Sevil, and Carlos Bernal. Review of architectures based on partial power processing for dc-dc applications. *IEEE Access*, 8:103405–103418, 2020.

[162] Kiwoo Park and Zhe Chen. A double uneven power converter-based dc–dc converter for high-power dc grid systems. *IEEE Transactions on Industrial Electronics*, 62(12):7599–7608, 2015.

[163] Stefano Cerutti, Mario Giuseppe Pavone, Francesco Gennaro, Natale Aiello, Francesco Musolino, and Paolo Stefano Crovetti. Design of a multi-mode input-parallel-output-series power optimizer for wide-voltage range photovoltaic applications. In *2024 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 444–451, 2024.

[164] Yifeng Wang, Zhongjie Wang, Bo Chen, and Hao Wang. Accurate modeling and efficiency optimization of high frequency bcm mode boost converter based on gan devices. *CSEE Journal of Power and Energy Systems*, pages 1–11, 2023.

[165] Mehdi Abbasi, Reza Emamalipour, Kajanan Kanathipan, Muhammad Ali Masood Cheema, and John Lam. A step-up reconfigurable multimode llc converter module with extended high-efficiency range for wide voltage gain application in medium voltage dc grid systems. *IEEE Transactions on Power Electronics*, 37(7):8118–8132, 2022.

[166] Yuqi Wei, Dereje Woldegiorgis, and Alan Mantooth. Control strategies overview for llc resonant converter with fixed frequency operation. In *2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pages 63–68, 2020.

[167] Jee hoon Jung and Joong gi Kwon. Theoretical analysis and optimal design of llc resonant converter. In *2007 European Conference on Power Electronics and Applications*, pages 1–10, 2007.

[168] Eung-Ho Kim and Bong-Hwan Kwon. Zero-voltage- and zero-current-switching full-bridge converter with secondary resonance. *IEEE Transactions on Industrial Electronics*, 57(3):1017–1025, 2010.

[169] Vadim Sidorov, Andrii Chub, and Dmitri Vinnikov. Feasibility study of universal power electronics interface operation in 350 v and 700 v residential dc microgrids. In *2023 IEEE 17th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*, pages 1–7, 2023.

[170] Utsab Kundu, Kalyan Yenduri, and Parthasarathi Sensarma. Accurate zvs analysis for magnetic design and efficiency improvement of full-bridge llc resonant converter. *IEEE Transactions on Power Electronics*, 32(3):1703–1706, 2017.

[171] M. Bartoli, N. Noferi, A. Reatti, and M.K. Kazimierczuk. Modeling litz-wire winding losses in high-frequency power inductors. In *PESC Record. 27th Annual IEEE Power Electronics Specialists Conference*, volume 2, pages 1690–1696 vol.2, 1996.

[172] Vesa Väisänen, Jani Hiltunen, Janne Nerg, and Pertti Silventoinen. Ac resistance calculation methods and practical design considerations when using litz wire. In *IECON 2013 - 39th Annual Conference of the IEEE Industrial Electronics Society*, pages 368–375, 2013.

[173] Rafal P. Wojda and Marian K. Kazimierczuk. Winding resistance and power loss of inductors with litz and solid-round wires. *IEEE Transactions on Industry Applications*, 54(4):3548–3557, 2018.

[174] A. Reatti and M.K. Kazimierczuk. Comparison of various methods for calculating the ac resistance of inductors. *IEEE Transactions on Magnetics*, 38(3):1512–1518, 2002.

[175] John Schonberger. A single phase multi-string pv inverter with minimal bus capacitance. In *2009 13th European Conference on Power Electronics and Applications*, pages 1–10, 2009.

[176] S.B. Kjaer, J.K. Pedersen, and F. Blaabjerg. A review of single-phase grid-connected inverters for photovoltaic modules. *IEEE Transactions on Industry Applications*, 41(5):1292–1306, 2005.

[177] Shiqi Kan, Xinbo Ruan, Hao Dang, Li Zhang, and Xinze Huang. Second harmonic current reduction in front-end dc−dc converter for two-stage single-phase photovoltaic grid-connected inverter. *IEEE Transactions on Power Electronics*, 34(7):6399–6410, 2019.

[178] Subhendu Bikash Santra, Debashis Chatterjee, Kundan Kumar, Manuele Bertoluzzo, Ariya Sangwongwanich, and Frede Blaabjerg. Capacitor selection method in pv interfaced converter suitable for maximum power point tracking. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 9(2):2136–2146, 2021.

[179] Amjad Ali, Khalid Almutairi, Sanjeevikumar Padmanaban, Vineet Tirth, Salem Algarni, Kashif Irshad, Saiful Islam, Md. Hasan Zahir, Md. Shafiullah, and Muhammad Zeeshan Malik. Investigation of mppt techniques under uniform and non-uniform solar irradiation condition–a retrospection. *IEEE Access*, 8:127368–127392, 2020.

[180] Saeed H. Hanzaei, Saman A. Gorji, and Mehran Ektesabi. A scheme-based review of mppt techniques with respect to input variables including solar irradiance and pv arrays' temperature. *IEEE Access*, 8:182229–182239, 2020.

[181] Dongdong Yang, Changsong Chen, Shanxu Duan, Jiuqing Cai, and Liangle Xiao. A variable duty cycle soft startup strategy for llc series resonant converter based on optimal current-limiting curve. *IEEE Transactions on Power Electronics*, 31(11):7996–8006, 2016.

[182] Vadim Sidorov, Andrii Chub, and Dmitri Vinnikov. Topology morphing control with soft transients for multimode series resonant dc-dc converter. In *2021 IEEE 22nd International Conference of Young Professionals in Electron Devices and Materials (EDM)*, pages 331–336, 2021.

[183] Charles Proteus Steinmetz. On the law of hysteresis (part ii.) and other phenomena of the magnetic circuit. *Transactions of the American Institute of Electrical Engineers*, IX(1):619–758, 1892.

[184] J. Reinert, A. Brockmeyer, and R.W.A.A. De Doncker. Calculation of losses in ferro- and ferrimagnetic materials based on the modified steinmetz equation. *IEEE Transactions on Industry Applications*, 37(4):1055–1061, 2001.

[185] Shuaichao Yue, Yongjian Li, Qingxin Yang, Xinran Yu, and Changgeng Zhang. Comparative analysis of core loss calculation methods for magnetic materials under nonsinusoidal excitations. *IEEE Transactions on Magnetics*, 54(11):1–5, 2018.

[186] Marco Torrisi, Sebastiano Messina, and Mario Cacciato. Hysteresis current control for a high efficiency totem pole pfc in zero voltage switching. In *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, pages P.1–P.10, 2021.

[187] Vivek Sankaranarayanan, Yucheng Gao, Robert W. Erickson, and Dragan Maksimovic. Online efficiency optimization of a closed-loop controlled sic-based bidirectional boost converter. *IEEE Transactions on Power Electronics*, 37(4):4008–4021, 2022.

[188] J. Biela, D. Hassler, Johann Minibock, and Johann Kolar. Optimal design of a 5kw/dm3 / 98.3 pages 1709 – 1716, 07 2010.

[189] Mehrdad Biglarbegian, Namwon Kim, and Babak Parkhideh. Boundary conduction mode control of a boost converter with active switch current-mirroring sensing. *IEEE Transactions on Power Electronics*, 33(1):32–36, 2018.

[190] Chuhan Peng, Mingde Zhou, Qishan Pan, Hengzhao Yang, and Haoyu Wang. A zvs realization method for bidirectional buck/boost converter based on current zero-crossing prediction. In *2023 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 421–426, 2023.

[191] Jinghui Yan, Xiaonan Zhao, Cheng-wei Chen, and Jil-Sheng Lai. Comparison of secondary topology of the llc converter for photovoltaic application. In *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 4750–4755, 2018.

[192] F. Tourkhani and P. Viarouge. Accurate analytical model of winding losses in round litz wire windings. *IEEE Transactions on Magnetics*, 37(1):538–543, 2001.

[193] Stefano Cerutti, Francesco Iannuzzo, Ariya Sangwongwanich, Tamas Kerekes, Mario Giuseppe Pavone, Francesco Gennaro, Natale Aiello, Francesco Musolino, and Paolo Stefano Crovetti. Reliability-constrained design of a high-gain power optimizer based on a real mission profile. In *2025 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 738–745, 2025.

[194] Susana Estefany De León-Aldaco, Hugo Calleja, and Jesús Aguayo Alquicira. Metaheuristic optimization methods applied to power converters: A review. *IEEE Transactions on Power Electronics*, 30(12):6791–6803, 2015.

[195] Stéphane Vighetti, Jean-Paul Ferrieux, and Yves Lembeye. Optimization and design of a cascaded dc/dc converter devoted to grid-connected photovoltaic systems. *IEEE Transactions on Power Electronics*, 27(4):2018–2027, 2012.

[196] Mehran Mirjafari and Robert S. Balog. Multi-objective optimization of the energy capture and boost inductor mass in a module-integrated converter (mic) photovoltaic energy system. In *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 2002–2007, 2012.

[197] Michael D'Antonio, Chuan Shi, Bin Wu, and Alireza Khaligh. Design and optimization of a solar power conversion system for space applications. *IEEE Transactions on Industry Applications*, 55(3):2310–2319, 2019.

[198] Edemar O. Prado, Pedro C. Bolsi, Luan Aleixo, Hamiltom C. Sartori, and José R. Pinheiro. Optimized design of non-isolated dc-dc converters for pv system applications. In *2023 15th Seminar on Power Electronics and Control (SEPOC)*, pages 1–6, 2023.

[199] Lenon Schmitz, Gustavo C. Knabben, Denizar C. Martins, Roberto F. Coelho, Odair J. Custodio, Renato Z. de Medeiros, and Alexandre L. Ferreira. Design optimization of a high step-up dc-dc converter for photovoltaic microinverters. In *2017 IEEE International Telecommunications Energy Conference (INTELEC)*, pages 432–437, 2017.

[200] Wilmar Martinez, Camilo Cortes, Ahmad Bilal, and Jorma Kyyra. Finite element methods for multi-objective optimization of a high step-up interleaved boost converter. In *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, pages 2193–2198, 2018.

[201] Saeed Peyghami, Huai Wang, Pooya Davari, and Frede Blaabjerg. Mission profile based power converter reliability analysis in a dc power electronic based power system. In *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 4122–4128, 2018.

[202] Yanfeng Shen, Andrii Chub, Huai Wang, Dmitri Vinnikov, Elizaveta Liivik, and Frede Blaabjerg. Wear-out failure analysis of an impedance-source pv microinverter based on system-level electrothermal modeling. *IEEE Transactions on Industrial Electronics*, 66(5):3914–3927, 2019.

[203] Abualkasim Bakeer, Andrii Chub, and Yanfeng Shen. Reliability evaluation of isolated buck-boost dc-dc series resonant converter. *IEEE Open Journal of Power Electronics*, 3:131–141, 2022.

[204] Giovanna Adinolfi, Giorgio Graditi, Pierluigi Siano, and Antonio Piccolo. Multiobjective optimal design of photovoltaic synchronous boost converters assessing efficiency, reliability, and cost savings. *IEEE Transactions on Industrial Informatics*, 11(5):1038–1048, 2015.

[205] G. Marsala and A. Ragusa. Reliability and efficiency optimization assisted by genetic algorithm to design a quadratic boost dc/dc converter. In *2018 IEEE International Conference on Industrial Engineering and Engineering Management (IEEM)*, pages 1687–1692, 2018.

[206] Mehran Mirjafari, Souhib Harb, and Robert S. Balog. Multiobjective optimization and topology selection for a module-integrated inverter. *IEEE Transactions on Power Electronics*, 30(8):4219–4231, 2015.

[207] Tomislav Dragičević, Patrick Wheeler, and Frede Blaabjerg. Artificial intelligence aided automated design for reliability of power electronic systems. *IEEE Transactions on Power Electronics*, 34(8):7161–7171, 2019.

[208] Marco Rosa-Clot and Giuseppe Marco Tina. *Floating PV Plants*. Academic Press, 2020.

[209] Francesco Iannuzzo. *Modern Power Electronic Devices: Physics, applications, and reliability*. Institution of Engineering and Technology Engineering Series, 2020.

[210] Andrew Hopkins, Neville McNeill, Philip Anthony, and Phil Mellor. Figure of merit for selecting super-junction mosfets in high efficiency voltage source converters. In *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 3788–3793, 2015.

[211] Section 4 – power transformer design. Technical report, Texas Instrument, 2001.

[212] Colonel W. T. McLyman. *Transformer and Inductor Design Handbook*. Taylor & Francis Inc, 2011.

[213] W.-J. Gu and R. Liu. A study of volume and weight vs. frequency for high-frequency transformers. In *Proceedings of IEEE Power Electronics Specialist Conference - PESC '93*, pages 1123–1129, 1993.

[214] Ralph M. Burkart. *Advanced Modeling and Multi-Objective Optimization of Power Electronic Converter Systems*. PhD thesis, ETH Zurich, 2016.

[215] Mohammad A. Hossain, Timothy J. Peshek, Yifan Xu, Yang Hu, Liang Ji, Alexis R. Abramson, and Roger H. French. Predictive linear regression model for microinverter internal temperature. In *2014 IEEE 40th Photovoltaic Specialist Conference (PVSC)*, pages 0992–0996, 2014.

[216] Bangbing Shi, Shiwei Feng, Lei Shi, Dong Shi, Yamin Zhang, and Hui Zhu. Junction temperature measurement method for power mosfets using turn-on delay of impulse signal. *IEEE Transactions on Power Electronics*, 33(6):5274–5282, 2018.

[217] S. Cerutti. Analysis and design of a high efficiency pv-fed battery charger with soft-switching tracking and mppt control. Master's thesis, Politecnico di Torino, 2022.

[218] Stefano Cerutti, Francesco Musolino, and Paolo S. Crovetti. A novel quasi-resonant battery charger for photovoltaic applications. In *IEEE EUROCON 2023 - 20th International Conference on Smart Technologies*, pages 740–745, 2023.

[219] Stefano Cerutti, Francesco Musolino, and Paolo S. Crovetti. Modeling and design of a zero-voltage switching battery charger for photovoltaic applications. *IEEE Access*, 12:88251–88263, 2024.

[220] N.K. Poon, B.M.H. Pong, and C.K. Tse. A constant-power battery charger with inherent soft switching and power factor correction. *IEEE Transactions on Power Electronics*, 18(6):1262–1269, 2003.

[221] Flex-03n 110-130w cigs. https://www.enfsolar.com/pv/panel-datasheet/crystalline/59250. Accessed: May 2024.

[222] Bluesun bsm-flex-130n flexible solar cell 75w 85w 95w 100w 130w cigs thin film solar panel product. https://www.bluesunpv.com/bluesun-bsm-flex-130n-75-85-95-100-130_p445.html. Accessed: May 2024.

[223] Basim najim Al-din Abed, Bayda Z. Kamil, Muhanad A. Hameed, and Jenan N. Abdullah. Using cardano's method for solving cubic equation in the cryptosystem to protect data security against cyber attack. In *2020 2nd Annual International Conference on Information and Sciences (AiCIS)*, pages 127–131, 2020.

[224] S. Gerner and T. Ruhlmann. Effect of ac ripple on vrla battery performance. Technical report, Emerson Network Power, 2010.

Appendix A

Full schematics of the PCB prototypes

This appendix contains the pictures of the full schematic sheets of the three converter prototypes that were designed and characterized in this work. More in details, Appendix A.1 includes the schematic of the multi-mode IPOS converter, Appendix A.2 includes the schematic of the optimized IPOS converter, while Appendix A.3 includes the schematic of the quasi-resonant battery charger.

A.1 Schematic sheets of the multi-mode wide-range IPOS converter

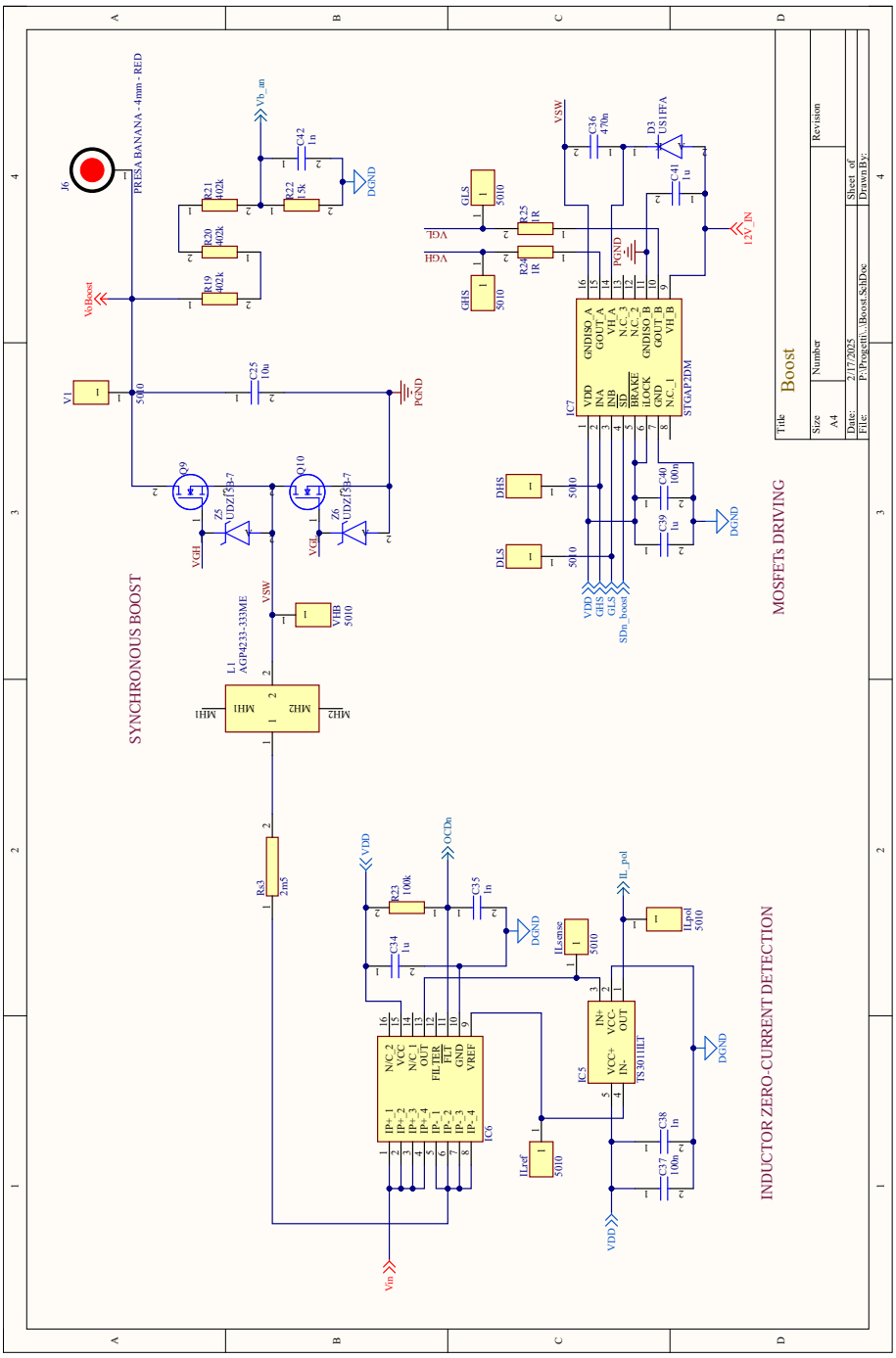


Fig. A.1 Sheet 1 of the *Altium Designer* schematic view (*Boost*).

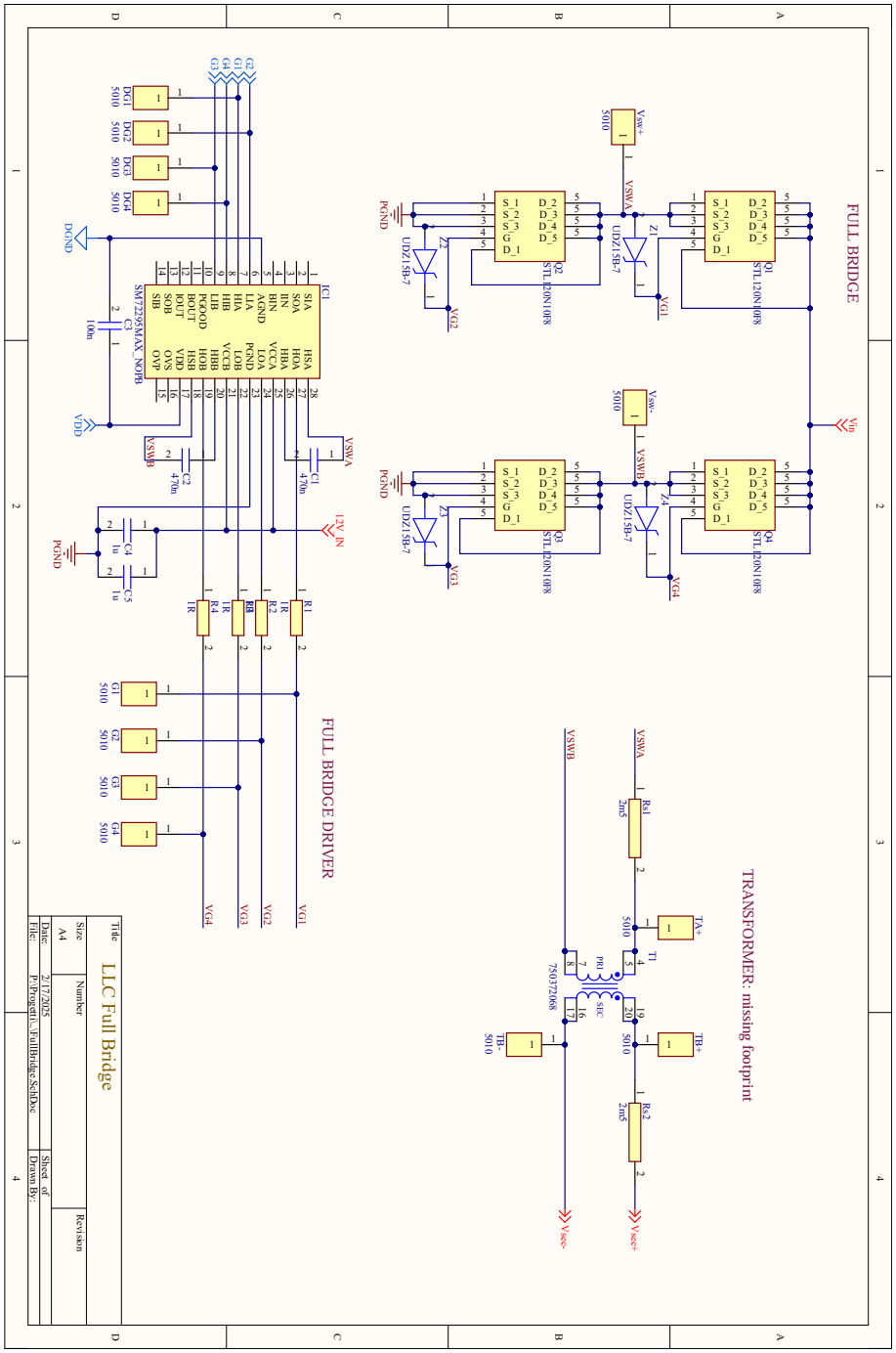


Fig. A.2 Sheet 2 of the *Altium Designer* schematic view (*SRC Full Bridge*).

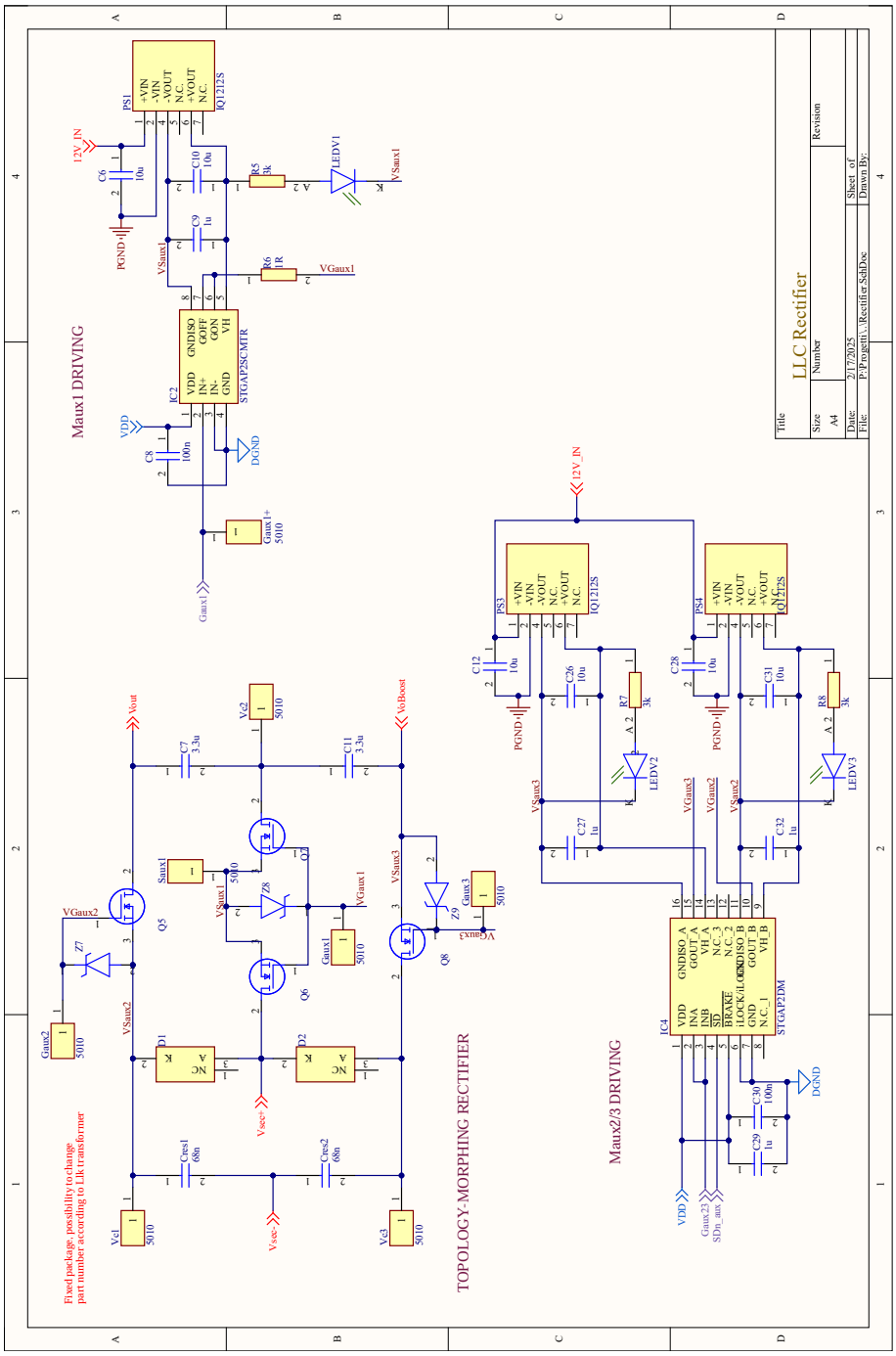


Fig. A.3 Sheet 3 of the *Altium Designer* schematic view (*SRC Rectifier*).

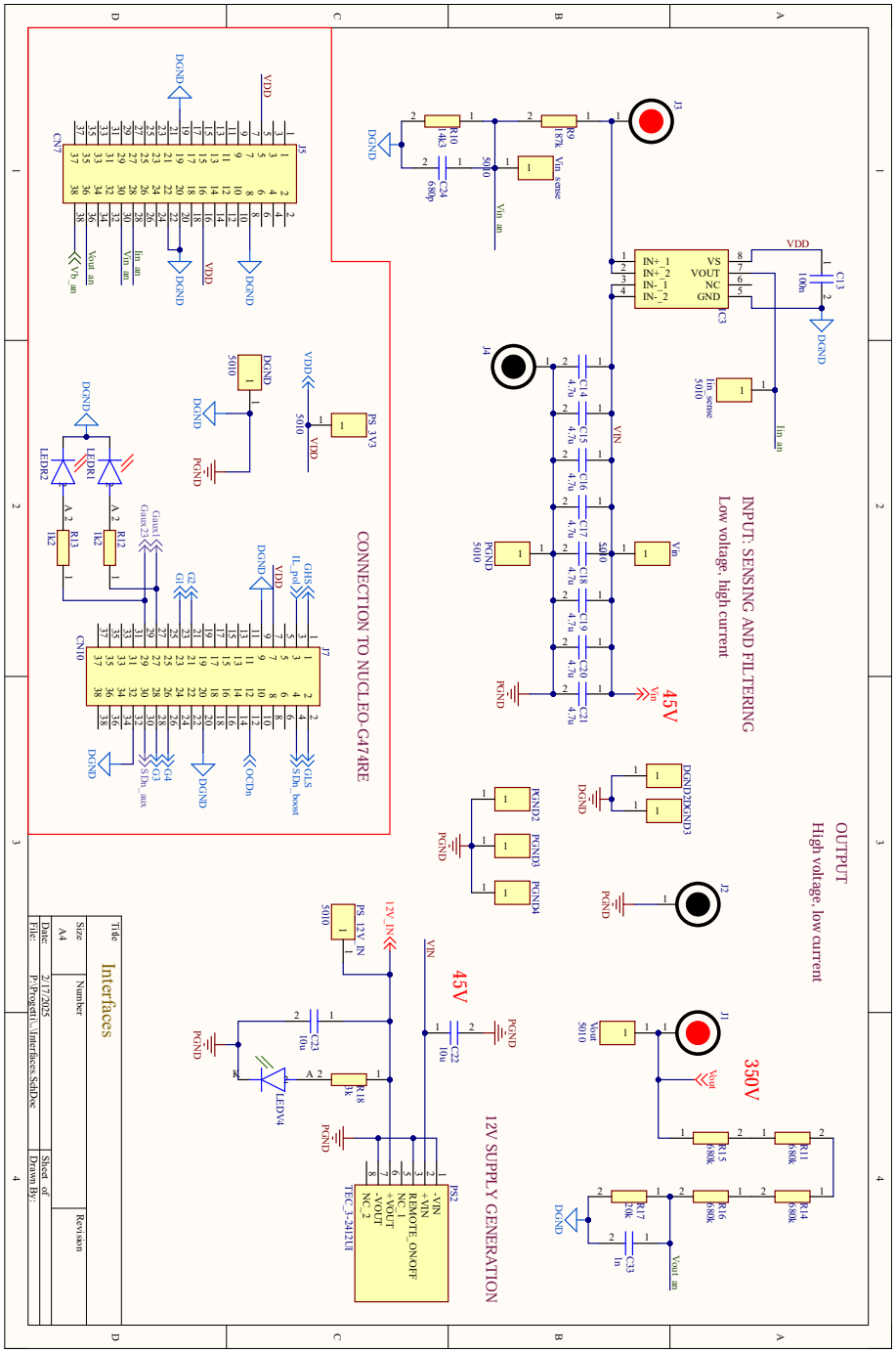


Fig. A.4 Sheet 4 of the *Altium Designer* schematic view (*Interfaces*).

A.2 Schematic sheets of the optimal IPOS converter

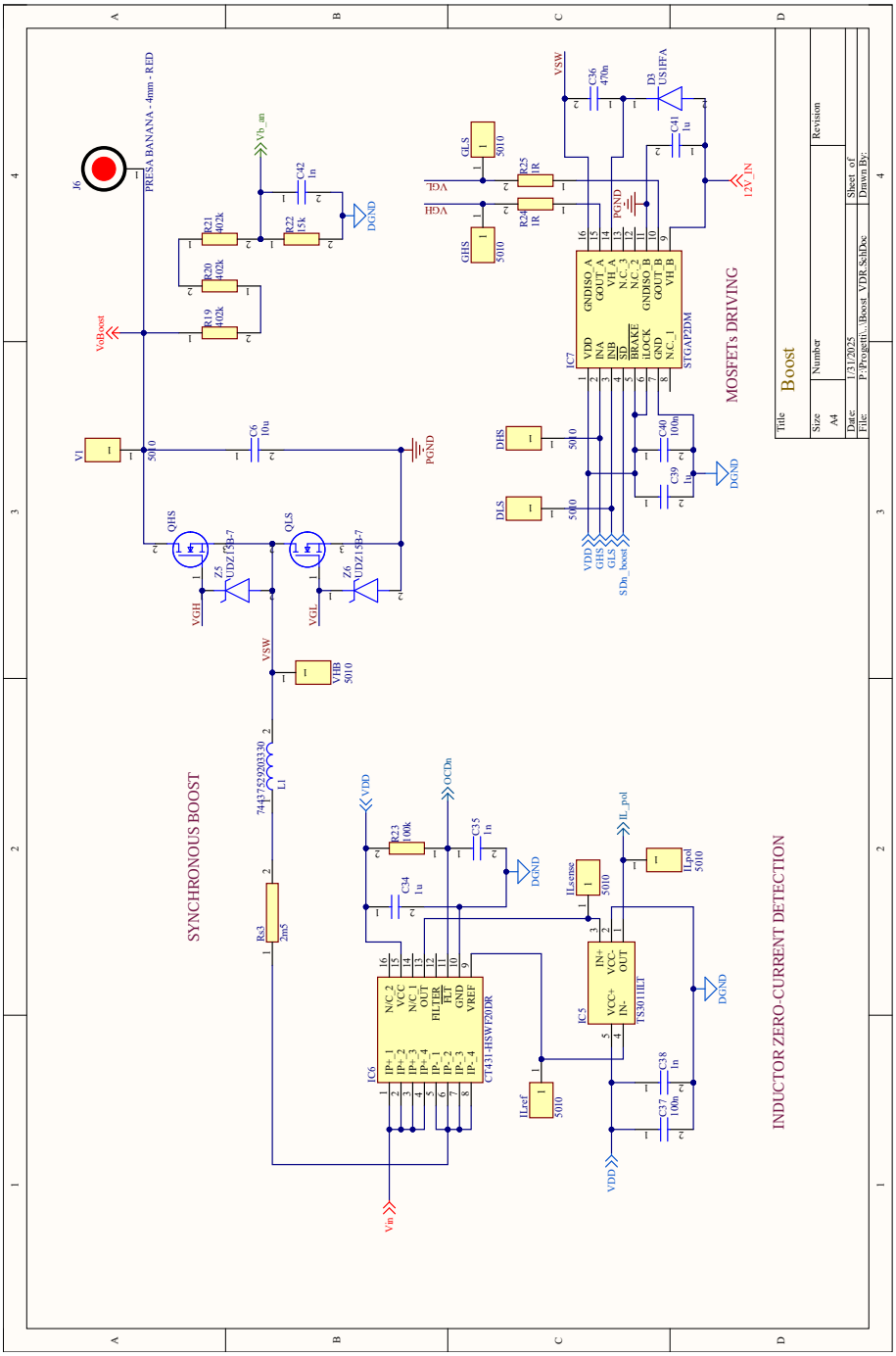


Fig. A.5 Sheet 1 of the *Altium Designer* schematic view (*Boost*).

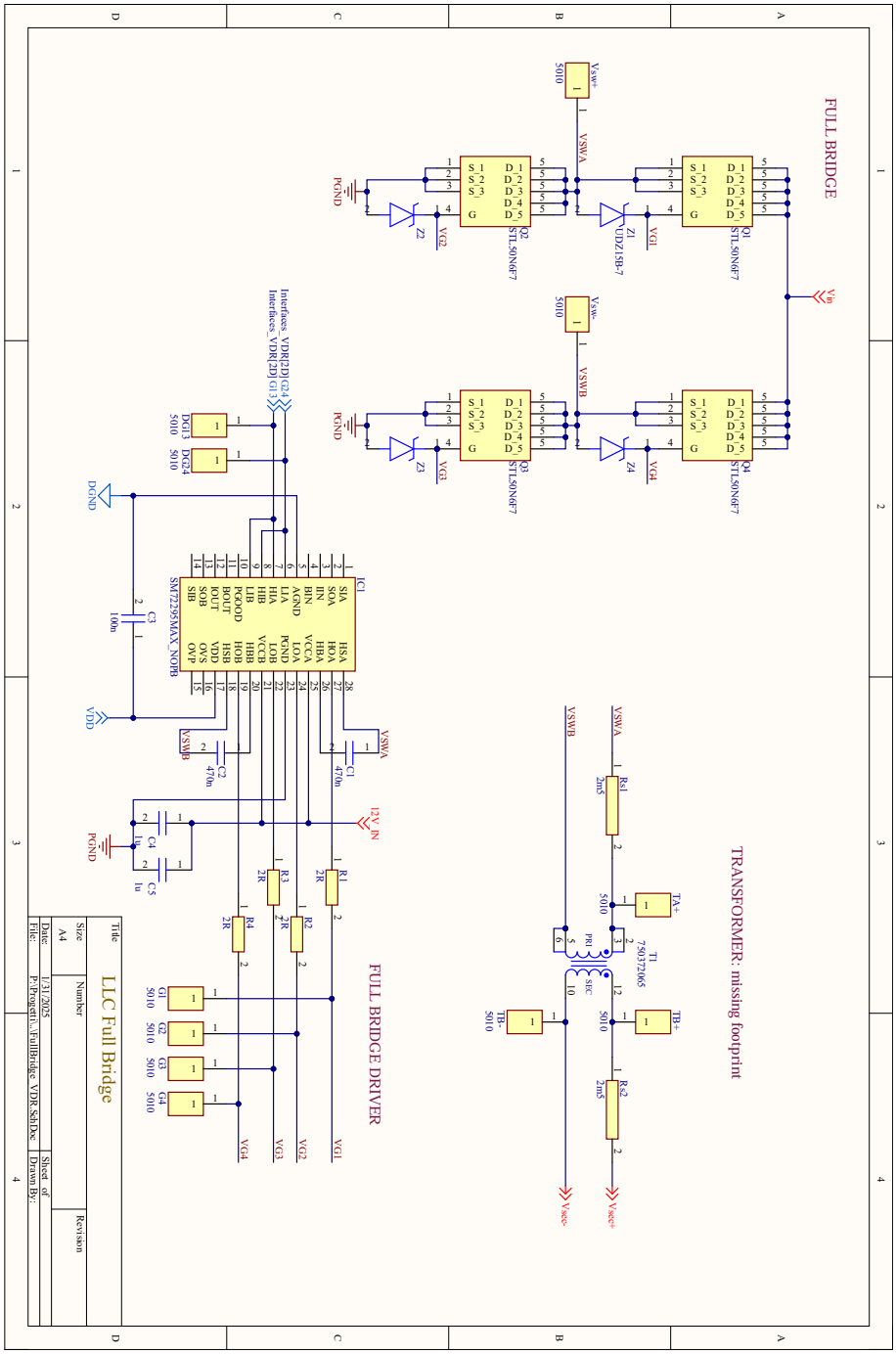


Fig. A.6 Sheet 2 of the *Altium Designer* schematic view (*SRC Full Bridge*).

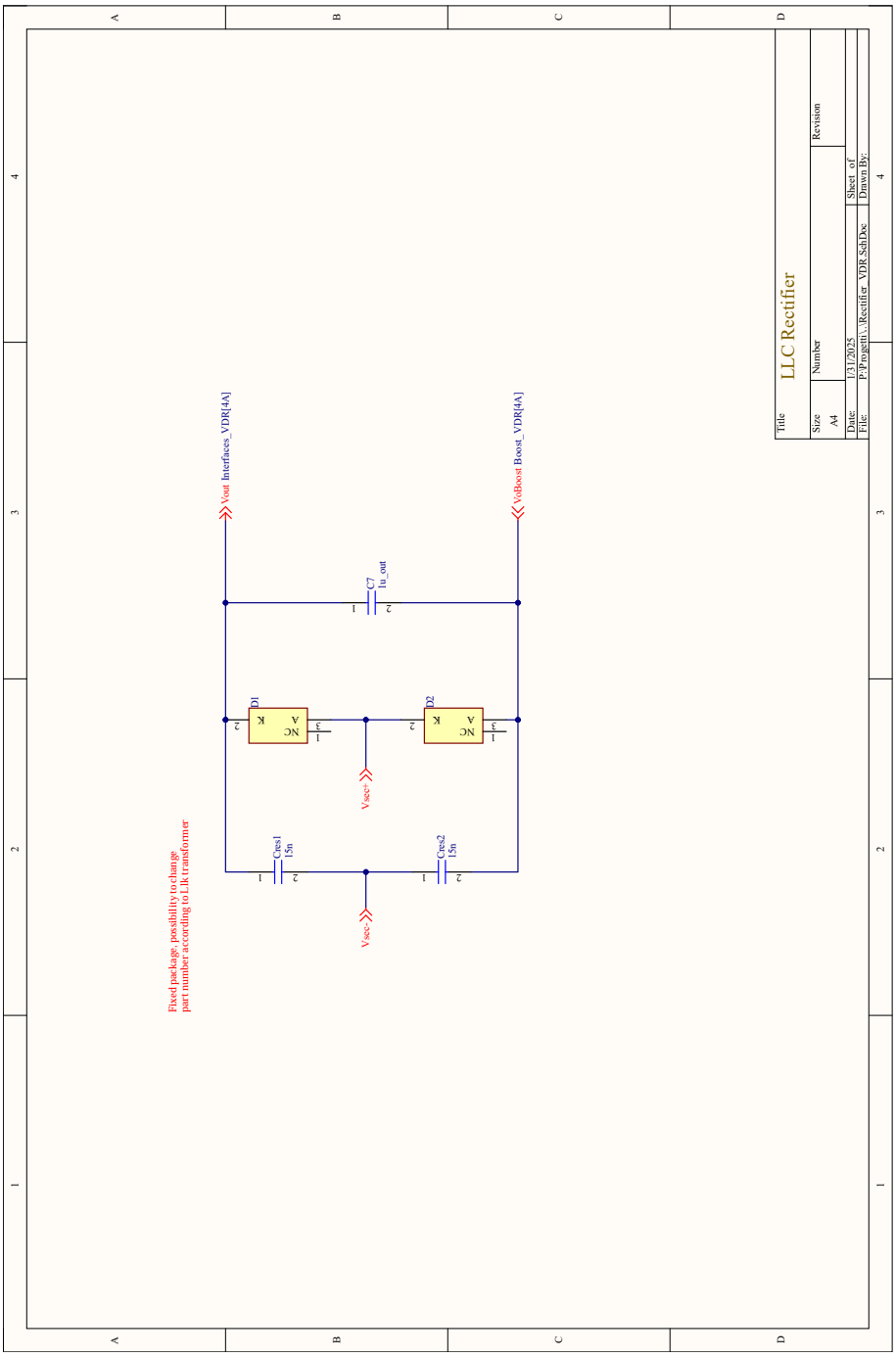


Fig. A.7 Sheet 3 of the *Altium Designer* schematic view (*SRC Rectifier*).

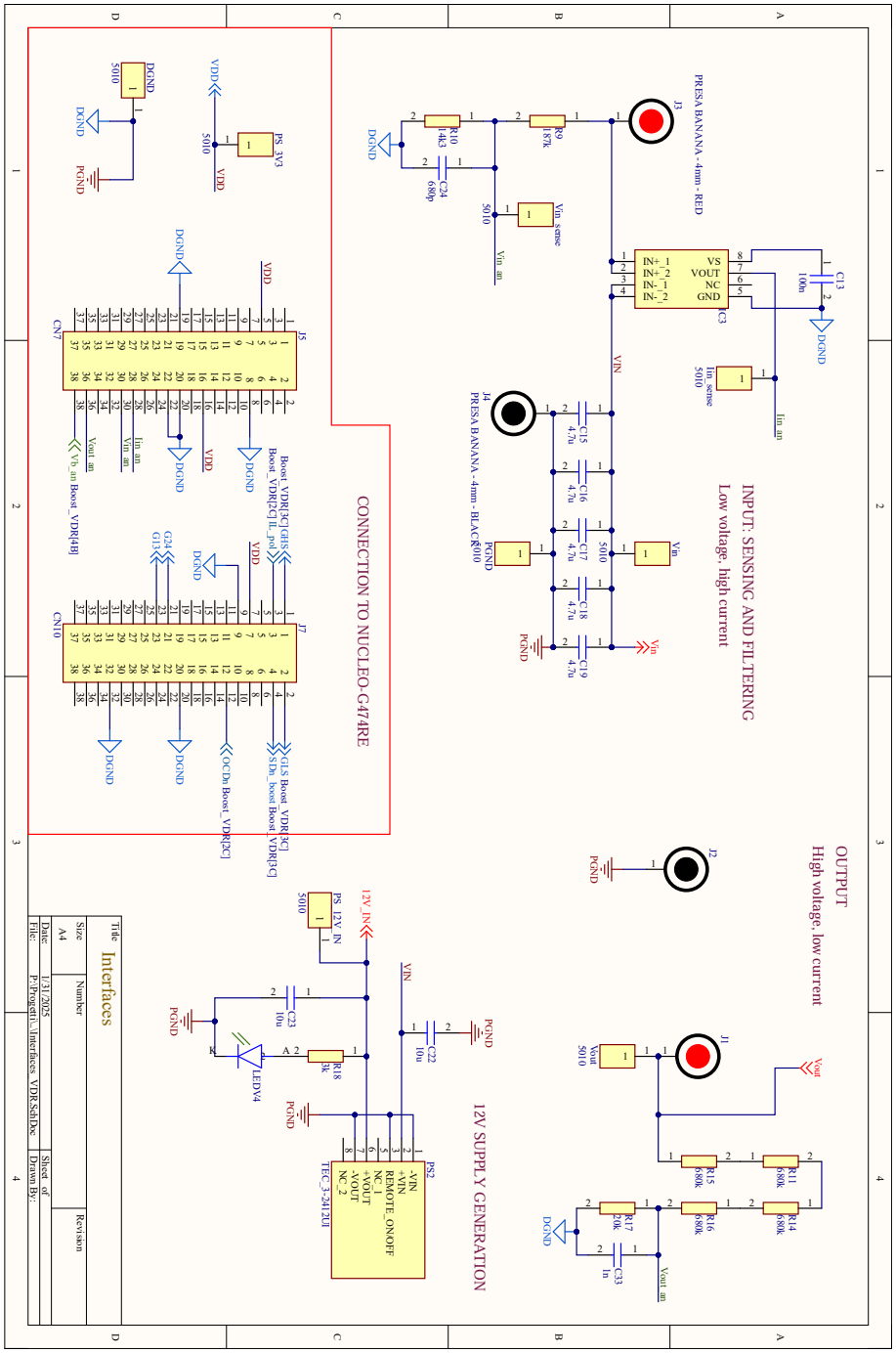


Fig. A.8 Sheet 4 of the *Altium Designer* schematic view (*Interfaces*).

A.3 Schematic sheets of the quasi-resonant PV-fed battery charger

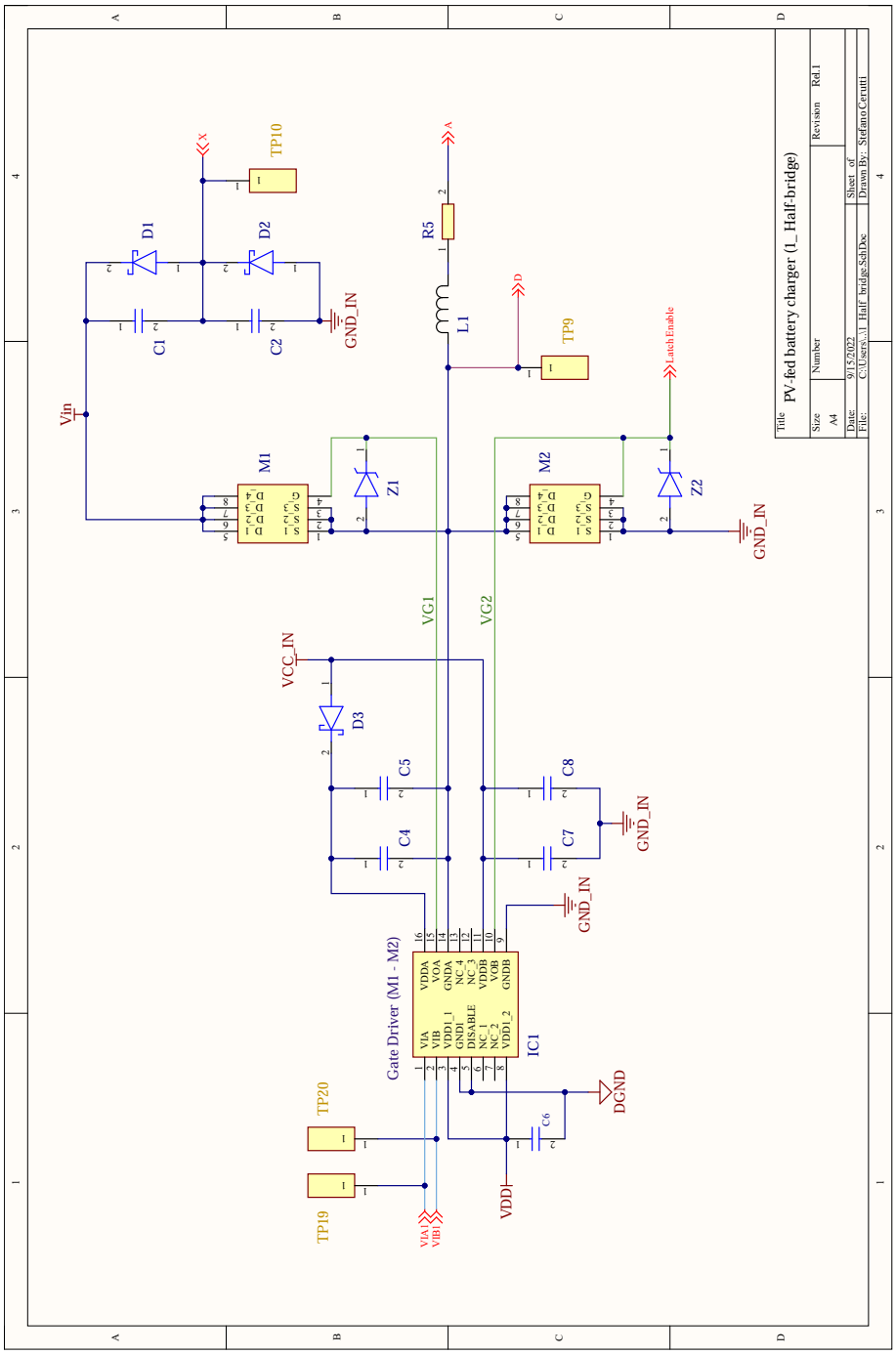


Fig. A.9 Sheet 1 of the *Altium Designer* schematic view (*Half-bridge*).

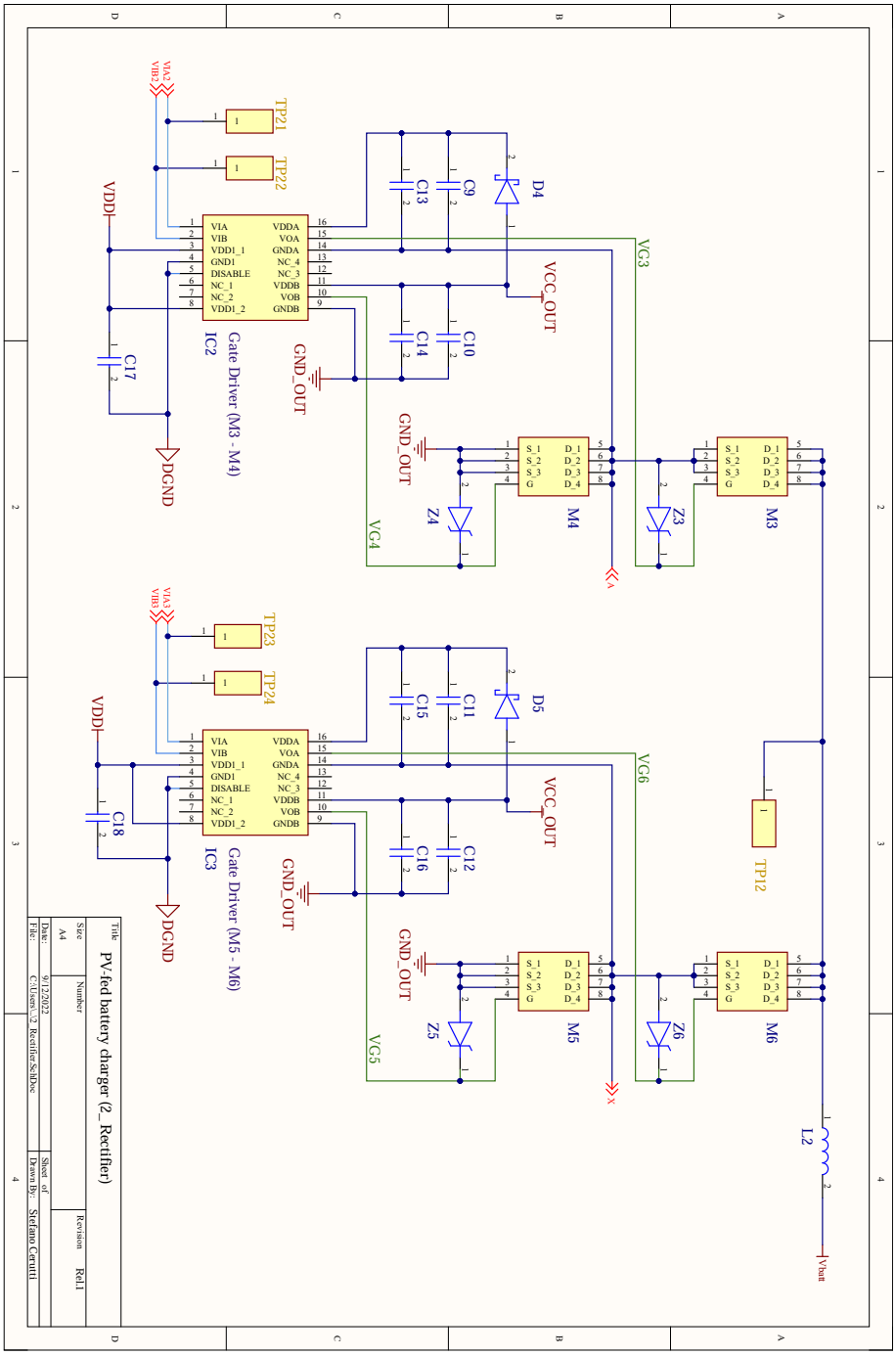


Fig. A.10 Sheet 2 of the *Altium Designer* schematic view (*Rectifier*).

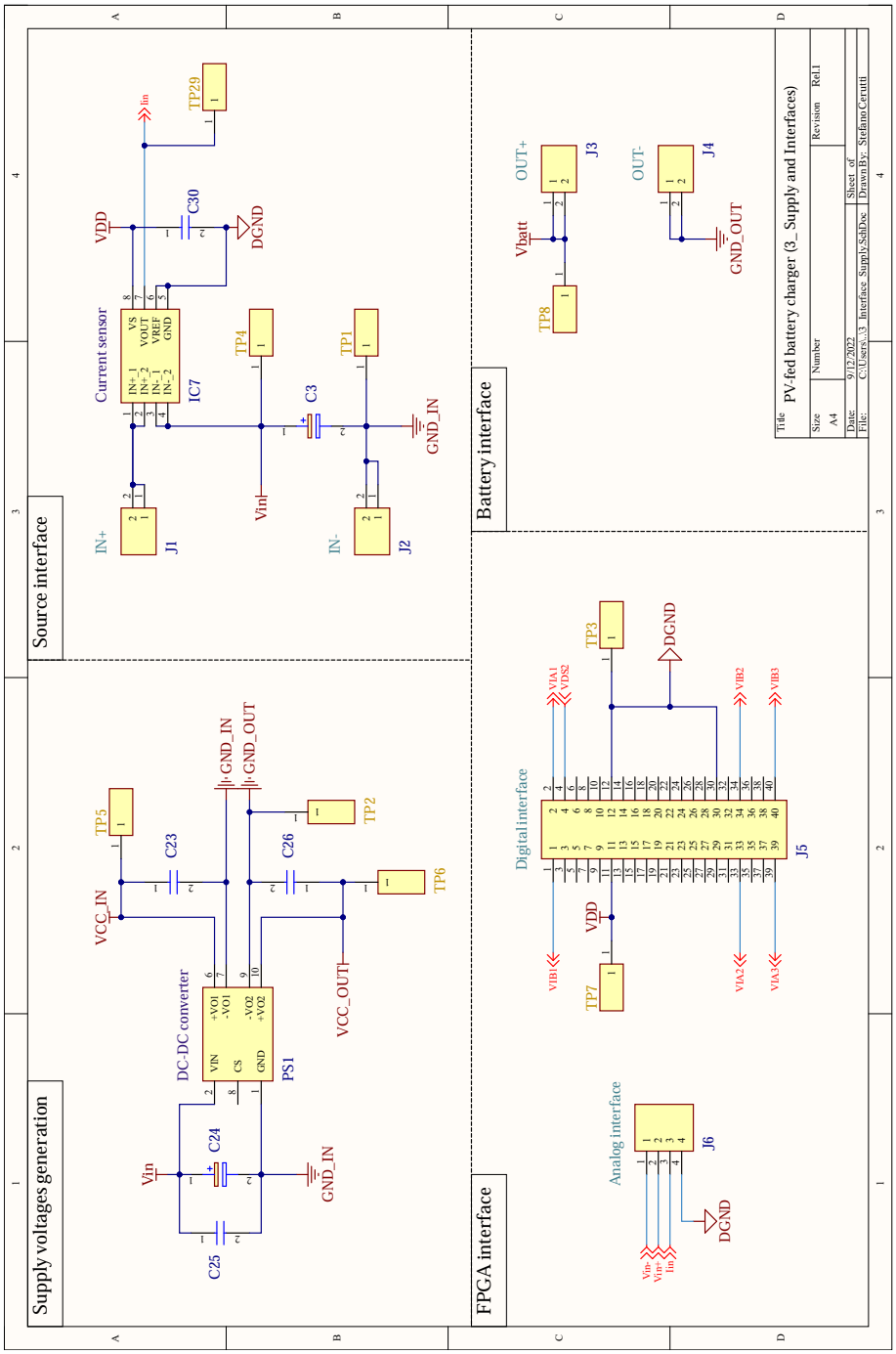


Fig. A.11 Sheet 3 of the *Altium Designer* schematic view (*Supply and interfaces*).

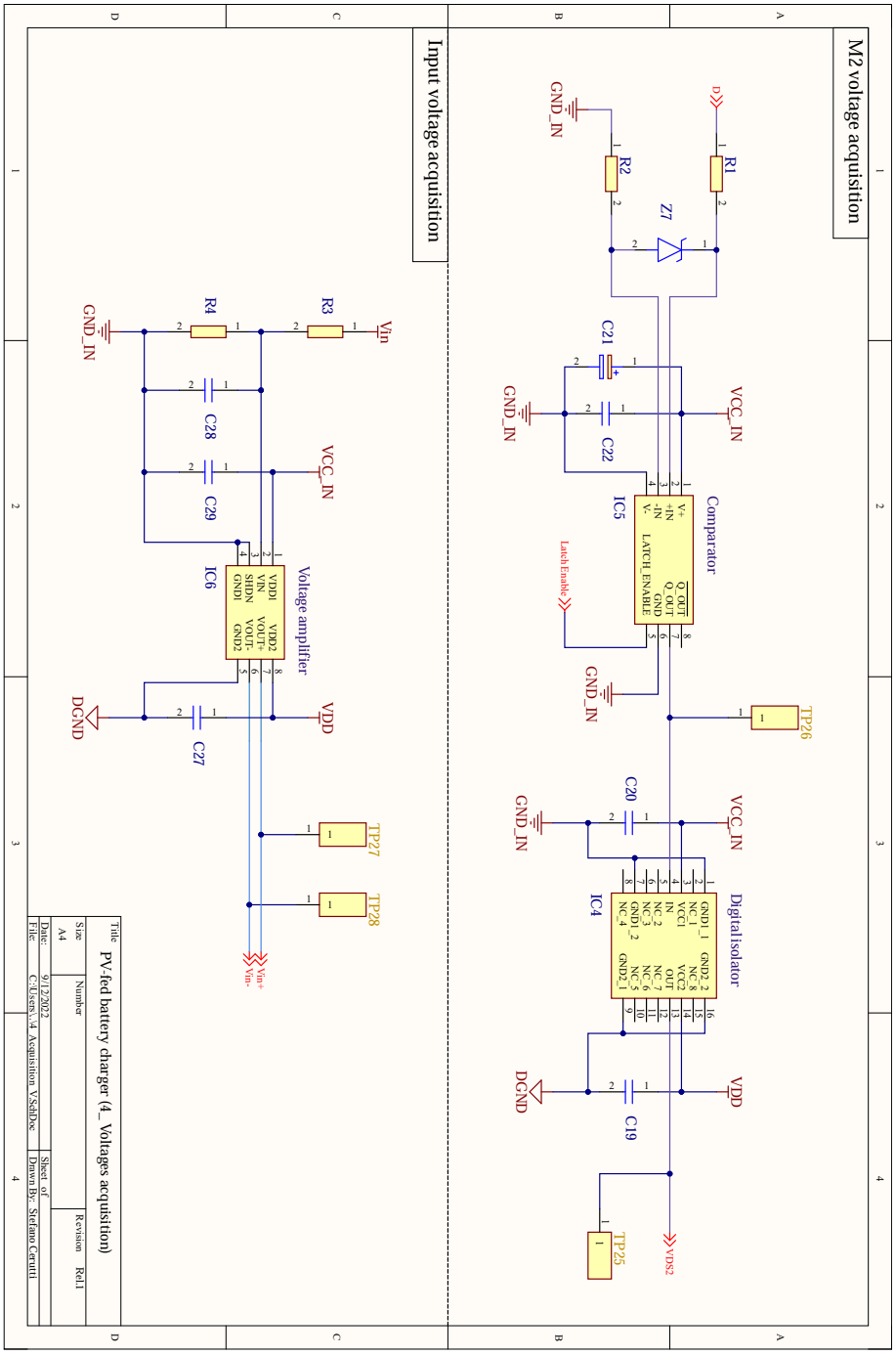


Fig. A.12 Sheet 4 of the *Altium Designer* schematic view (*Voltages acquisition*).

Appendix B

Matlab implementation of PSO-based reliability-constrained optimization

As relevant part of the innovative potential of this work, this appendix contains the Matlab code implementing the reliability-constrained optimization of the proposed PV-fed IPOS converter. The code can be adjusted and updated according to the needs of a potential future user. The hierarchical structure of the code is the following:

- *PSO_MATLAB.m* constitutes the top-level code, including the definition and initialization of parameters, functions and constants, and the implementation of the PSO algorithm;
- *transformer_design.m* contains the subroutine that optimizes, for every set of trial design variables of the search algorithm, the transformer design on the basis of cost and losses;
- *MonteCarlo_LLC_LS_HS.m* is a specific part of the code that implements Monte Carlo simulations of the converter transistors lifetime.

B.1 Main code of the algorithm: *PSO_MATLAB.m*

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Main code of the algorithm
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%% Part 1: User-defined parameters
```

```
6
7  sheet_index = 2;        % 1: Aalborg; 2: Turin; 3: Arizona
8  core_sel = 2;      % 1: EE, 2: ETD
9
10 % PSO coefficients and convergence criterion
11 omega_PSO = 0.8;
12 c1_PSO = 0.2;
13 c2_PSO = 0.2;
14 N_population = 25;
15 N_generation = 1;       % Initialization
16 epsilon = 0.001;     % Convergence factor [1-epsilon; 1+epsilon]
17 N_generations_convergence = 10;      % After how many converging steps the
       algorithm can stop
18 Obj_function_index = 2;     % legend: 1 = min LCOE; 2 = min cost/eta_EURO
19
20 % Circuit constants
21 Vout = 350;
22 L = 33e-6;          % Boost inductance
23 Gboost_min = 1;     % Constraints for the boost
24 Gboost_max = 5;
25
26 % PV panel constants
27 PMPP_BSTC = 470;
28 IMPP_BSTC = 12.89;
29 VMPP_BSTC = PMPP_BSTC/IMPP_BSTC;
30 gamma_PMPP = -0.0024;
31 alpha_IMPP = 0.00044;
32
33 PMPPmin = 20;           % Minimum power under which no power is harvested
34 Degradation_panel = [1, 0.99-(1:1:24)*0.0025];
35
36 % Details for the computation of EURO efficiency
37 Vrated = 36;
38 Trated = 25;
39 P_EURO = PMPP_BSTC*[0.05, 0.1, 0.2, 0.3, 0.5, 1];
40 weights_EURO = [0.03; 0.06; 0.13; 0.1; 0.48; 0.2];
41
42
43 %% Part 2: Preliminary functions: Cost, Losses, Reliability
44
45 % PV model (assuming the BSTC parameteres of the panel reported in datasheet)
46 PMPP = @(G, Tpanel) PMPP_BSTC*G/1000.*(1+gamma_PMPP*(Tpanel-25));
47 IMPP = @(G, Tpanel) IMPP_BSTC*G/1000.*(1+alpha_IMPP*(Tpanel-25));
48
49 % Core materials parameters: [N27, N87, N97]
50 % Legend: Pcore \propto rho_SE * fsw^alpha_SE * DeltaB^beta_SE
51 rho_SE = [153.1, 51.96, 51.97];     % [kW/m^3]
52 alpha_SE = [1.969, 1.936, 1.858];
53 beta_SE = [2.737, 2.593, 2.363];
54
55 % Transformer constants
56 mu0 = 4*pi*1e-7;
57 Bsat = 0.32;
```

```
Kcore = 1.8;          % Ratio of the effective core losses (datasheet) and the
    theoretical ones
Kf = 4;               % Waveform factor for square-wave voltage excitation
Ku = 0.3;             % Typical window utilization factor when using Litz wire
J = 420e4;            % Nominal current density assumed in the transformer
    design (typical value) [A/m^2]
rhoCu = 1.72e-8;      % Copper resistivity [ohm*m]
delta_Cu = 8.93e3;    % Copper density (kg/m3)
Vmaxsat = 45;

% Fitting parameters of the geometry (Curve Fitting Tool)
AP_Ae = 0.9677;
AP_Aw = 1.043;
AP_Ve = 7.445;
AP_MTL = 5.846;

% Derived functions (geometry) -> AP in cm4!
Ae = @(AP) AP_Ae*1e-4*AP.^0.5;
Ve = @(AP) AP_Ve*1e-6*AP.^0.75;
MTL = @(AP) AP_MTL*1e-2*AP.^0.25;
Aw = @(AP) AP_Aw*1e-4*AP.^0.5;
le = @(AP) Ve(AP)./Ae(AP);

% Coefficients for the Al-mueff linear function: [EE, ETD]
% Legend: AL = mueff*(q+m*Ae)
m = [1.077 0.6614];
q = [0.5232 0.921];


% Derived functions:

% Transformer
DB_100mWcm3 = @(core_index, fsw) 0.2*(4/pi*100/rho_SE(core_index)*(100e3/fsw)^
    alpha_SE(core_index))^(1/beta_SE(core_index));
Volume_Litz = @(AP, N1, IRMSMAX) 2*MTL(AP)*IRMSMAX/J.*N1;    % [m3]
delta_skin = @(fsw) 6.52./sqrt(fsw);        % [cm]!
diameter_Litz = @(fsw) delta_skin(fsw)/3;       % [cm]! Assumption: the Litz
    wire diameter is always selected as 1/3 of the skin depth
Nstrands_prim = @(fsw, IRMSMAX) 4*IRMSMAX./(pi*J*1e-4.*diameter_Litz(fsw).^2);
         % Assumption: the diameter is selected as 1/3 of the skin depth
Nstrands_sec = @(fsw, IRMSMAX, n) Nstrands_prim(fsw, IRMSMAX)./n;
FR_prim = @(fsw, IRMSMAX) 1+3.056e-4*Nstrands_prim(fsw, IRMSMAX);        %
    Ratio between AC and DC resistance of Litz wire including proximity effect
FR_sec = @(fsw, IRMSMAX, n) 1+3.056e-4*Nstrands_sec(fsw, IRMSMAX, n);

% 60V FETs [1: MOS, 2: GaN]
alpha_60V = [181.1e-12, 40.71e-12];      % [C*Ohm]
QG_60V = @(M60V_index, RDSON60V) alpha_60V(M60V_index)./RDSON60V;   % [C]
COSS_60V = @(M60V_index, RDSON60V) 2*(14.24e-3*QG_60V(M60V_index, RDSON60V)*(
    M60V_index==1)+62.52e-3*QG_60V(M60V_index, RDSON60V)*(M60V_index==2));  %
    [F] (datasheet parameter, NOT charge-equivalent capacitance -> the
    additional factor 2 takes considers a worst-case overestimation)
QSW_60V = @(M60V_index, RDSON60V) 0.229*QG_60V(M60V_index, RDSON60V)*(
    M60V_index==1)+0.1685*QG_60V(M60V_index, RDSON60V)*(M60V_index==2);  % [C]
```

```
102 RthJAmb_60V = @(M60V_index, RDSON60V) 60*(M60V_index==1)+(457.6*(RDSON60V)
        .^(0.04798)-297.3)*(M60V_index==2);   % For MOSFETs, consider PowerFLAT
        package, for GaNFET only the die
103 Tjmax_60V = @(M60V_index) 175*(M60V_index==1)+150*(M60V_index==2);
104 beta_60V = 4.9e-3;          % Coefficient of the linear term to solve the Tj-P
         equation
105 gamma_60V = 1.2e-5;         % Coefficient of the quadratic term to solve the
        Tj-P equation
106
107 % 250V MOSFETs
108 alpha_250V = 1918e-12;      % [C*Ohm]
109 QG_250V = @(RDSON250V) alpha_250V./RDSON250V;
110 COSS_250V = @(RDSON250V) 7.563e-12./RDSON250V;  % [F]
111 QSW_250V = @(RDSON250V) 396.2e-12./RDSON250V;  % [C]
112 Rthjamb_250V = 42;      % D2PAK
113 Tjmax_250V = 175;
114 beta_250V = 7.17e-3;          % Coefficient of the linear term to solve the Tj
        -P equation
115 gamma_250V = 3.57e-5;         % Coefficient of the quadratic term to solve the
         Tj-P equation
116
117 % Cin
118 ESR_CIN = @(C) 12.47e-9./C;         % C in Farad, result in Ohm
119
120 % Cboost
121 ESR_CBOOST = @(Cb) 1.88e-3+34.57e-9./Cb;     % Cb in Farad, result in Ohm
122
123 % Boost derived functions
124 Gboost = @(Vin, n) Vout./Vin-2*n;
125 Dboost = @(Vin, n) min(1, max(0.01, 1-1./Gboost(Vin, n)));     % Saturated
        between 0 and 1
126
127 % Components and total costs functions
128 Cost_bias = 85;
129 b1 = [23.84, 39.36];
130 e1 = [-2467, -821.2];
131 b2 = [3.236, 2.346];
132 e2 = [-91.01, -13.04];
133 Price_MOS_60V = @(M60V_index, RDSON60V) b1(M60V_index)*exp(e1(M60V_index)*
        RDSON60V)+b2(M60V_index)*exp(e2(M60V_index)*RDSON60V); % [euro per item]
134 Price_MOS_250V = @(RDSON250V) 7.62*exp(-39.29*RDSON250V)+2.791*exp(-3.032*
        RDSON250V);   % [euro]
135 Price_CIN = @(C) 2.128+0.328e6*C;   % C in Farad
136 Price_CBOOST = @(Cb) 2.017+0.1938e6*Cb;      % Cb in Farad
137 Price_core = @(AP) 0.7042+2.83*AP.^0.5;      % Core cost (market analysis)
138 Price_Litz = @(fsw, AP, N1, IRMSMAX) 0.5+(19.04+1323*exp(-886.4*diameter_Litz(
        fsw)))*delta_Cu*Volume_Litz(AP, N1, IRMSMAX);     % Litz wire cost (
        Burkart PhD thesis)
139 Price_T = @(fsw, AP, N1, IRMSMAX) Price_core(AP)+Price_Litz(fsw, AP, N1,
        IRMSMAX);     % Including core and bobbin (AP in cm^4)
140
141 PRICE = @(M60V_index, RDSON60V, RDSON250V, C, Cb, fsw, AP, N1, IRMSMAX)
        Cost_bias+4*Price_MOS_60V(M60V_index, RDSON60V)+...
142                         2*Price_MOS_250V(RDSON250V)+...
```

```
143                         Price_CIN(C)+Price_CBOOST(Cb)+Price_T(fsw, AP, N1,
                                IRMSMAX);
144
145
146
147
148 % Lifetime model for reliability analysis (MOSFETs TO-2xx packages)
149 % Lifetime model parameters
150 A_LT = 4.9283e13;
151 alpha_LT = -5.2776;
152 Ea_LT = 812;
153 Nfi = @(DeltaT, Tjmin) A_LT*exp(Ea_LT./(Tjmin+0.5*DeltaT+273.15)).*((DeltaT).^
        alpha_LT);
154 nMC = 10000;
155 Minutes_year = 60*24*365;
156
157 % Monte-carlo simulations parameters
158 tolerance = 0.1;
159 sigma_A = tolerance/3*A_LT;
160 A_MC = normrnd(A_LT, sigma_A, [nMC,1]);
161 sigma_alpha = tolerance/3*abs(alpha_LT);
162 alpha_MC = normrnd(alpha_LT, sigma_alpha, [nMC,1]);
163 sigma_Ea = tolerance/3*Ea_LT;
164 Ea_MC = normrnd(Ea_LT, sigma_Ea, [nMC,1]);
165 Tjav_eq = 20;       % Assumption: the equivalent average junction temperature
        is fixed, while the equivalent DeltaT is derived from the computed
        accumulated damage
166 Tjav_MC = normrnd(Tjav_eq, 2*tolerance/3*Tjav_eq, [nMC,1]);
167 t = linspace(0, 1e4, 1e4+1);
168
169
170 %% Part 3: Mission profile-dependent stresses
171
172 % Worst-case power and voltage conditions
173
174 filename = "MissionProfiles.mat";
175 load(filename);
176
177 SheetName = ["Aalborg", "Turin", "Arizona"];
178
179 if sheet_index == 1
180     G = MP.Aalborg(:,1);
181     Tamb = MP.Aalborg(:,2);
182     Tpanel = MP.Aalborg(:,3);
183     Tsample = 1;
184 elseif sheet_index == 2
185     G = MP.Turin(:,1);
186     Tamb = MP.Turin(:,2);
187     Tpanel = MP.Turin(:,3);
188     Tsample = 15;
189 elseif sheet_index == 3
190     G = MP.Arizona(:,1);
191     Tamb = MP.Arizona(:,2);
192     Tpanel = MP.Arizona(:,3);
```

```
193     Tsample = 1;
194 else
195     fprintf('Mission profile not found')
196 end
197
198 Ncycles_eq = 0.5*Minutes_year/Tsample;
199 G(G<0.5) = 0.5;
200 [G_max, Gmax_index] = max(G);
201 Tamb_max = max(Tamb);
202 [Tpanel_max, Tpanelmax_index] = max(Tpanel);
203 PMPP_max = PMPP(G_max, Tpanel(Gmax_index));
204 VMPP_min = PMPP(G(Tpanelmax_index), Tpanel_max)/IMPP(G(Tpanelmax_index),
        Tpanel_max);
205 VMPP_max = PMPP(100, 0)/IMPP(100, 0);
206
207 % High-level constants and functions (outside the loop)
208
209 tOFF60V = @(RDSON_60V, Tech60V_index) 46.64e-12/RDSON_60V*(Tech60V_index==1)
        +15.6e-12/RDSON_60V*(Tech60V_index==2);
210 tdead_250V = 300e-9;
211 tOFF250V = @(RDSON_250V) 344.7e-12/RDSON_250V;
212
213 % Input / output currents
214 Iout = @(P) P/Vout;
215 Iin = @(P, Vin) P./Vin;
216
217 % Boost variables: alpha and beta are adimenional variables related to the
218 % ZVS control of the BCM boost.
219 % alpha corresponds to the "extra" negative current that the boost inductor
        must carry to provide the ZVS of the
220 % low-side MOSFET
221 % beta is defined for more compact expressions of the electrical stresses
222 alpha_ZVS = @(P, Vin, neff, IR) min(1-IR./(Iout(P).*Gboost(Vin, neff)), 5);
223 beta_ZVS = @(P, Vin, neff, IR) 0.5*sqrt(3+alpha_ZVS(P, Vin, neff, IR).^2);
224 fswmax = 200e3;
225 fswBoost = @(P, Vin, neff, IR) min(fswmax, Gboost(Vin, neff).*Vout.*Dboost(Vin
        , neff).*(1-Dboost(Vin, neff)).^2./(2*L*Iin(P, Vin).*alpha_ZVS(P, Vin,
        neff, IR)));
226
227 % Peak inductor current
228 ILpeak = @(P, Vin, neff, IR) (fswBoost(P, Vin, neff, IR)<fswmax).*(Gboost(Vin,
         neff).*Iout(P).*(1+alpha_ZVS(P, Vin, neff, IR)))+...
229     (fswBoost(P, Vin, neff, IR)==fswmax).*(Gboost(Vin, neff).*Iout(P)+0.5*Vin
            .*Dboost(Vin, neff)/(L*fswmax));     % According to fsw, variable-
            frequency or fixed-frequency BCM
230
231 % RMS inductor current
232 ILRMS = @(P, Vin, neff, IR) (fswBoost(P, Vin, neff, IR)<fswmax).*(ILpeak(P,
        Vin, neff, IR).*beta_ZVS(P, Vin, neff, IR)/sqrt(3))+...
233     (fswBoost(P, Vin, neff, IR)==fswmax).*(sqrt((Gboost(Vin, neff).*Iout(P))
            .^2+(Vin.*Dboost(Vin, neff)/(2*sqrt(3)*L*fswmax)).^2));     %
            According to fsw, variable-frequency or fixed-frequency BCM
234
235 % Inductor losses (Curve Fitting Tool applied to the commercial Coilcraft
```

```
% inductor AGP4233-333)
RAC_L = @(P, Vin, neff, IR) 3*6.033e-7*(1222+fswBoost(P, Vin, neff, IR));
          % Inductor AC resistance
P_L = @(P, Vin, neff, IR) RAC_L(P, Vin, neff, IR).*ILRMS(P, Vin, neff, IR);


% Boost capacitor
P_Cb = @(P, Vin, neff, Cboost, IR) ESR_CBOOST(Cboost).*Iout(P).^2.*(4/3*
    beta_ZVS(P, Vin, neff, IR).^2.*Gboost(Vin, neff)-1);

% High-side switch
Psw_HS = @(P, Vin, neff, IR, RDSON_250V) abs(0.5*tOFF250V(RDSON_250V)*fswBoost
    (P, Vin, neff, IR).*Gboost(Vin, neff).*Vin.*(IR*(fswBoost(P, Vin, neff, IR
    )<fswmax)+(Gboost(Vin, neff).*Iout(P)-0.5*Vin.*Dboost(Vin, neff)/(L*fswmax
    )).*(fswBoost(P, Vin, neff, IR)==fswmax)));
IRMS_HS = @(P, Vin, neff, IR) sqrt((1-Dboost(Vin, neff))).*ILRMS(P, Vin, neff,
     IR);
Pcond_HS = @(P, Vin, neff, IR, Tj, RDSON_250V) RDSON_250V.*(1+beta_250V*(Tj
    -25)+gamma_250V*(Tj-25).^2).*IRMS_HS(P, Vin, neff, IR).^2;
Ptot_HS = @(P, Vin, neff, IR, Tj, RDSON_250V) Psw_HS(P, Vin, neff, IR,
    RDSON_250V)+Pcond_HS(P, Vin, neff, IR, Tj, RDSON_250V);

% Low-side switch
Psw_LS = @(P, Vin, neff, IR, RDSON_250V) 0.5*tOFF250V(RDSON_250V)*fswBoost(P,
    Vin, neff, IR).*Gboost(Vin, neff).*Vin.*ILpeak(P, Vin, neff, IR);
IRMS_LS = @(P, Vin, neff, IR) sqrt(Dboost(Vin, neff)).*ILRMS(P, Vin, neff, IR)
    ;
Pcond_LS = @(P, Vin, neff, IR, Tj, RDSON_250V) RDSON_250V*(1+beta_250V*(Tj-25)
    +gamma_250V*(Tj-25).^2).*IRMS_LS(P, Vin, neff, IR).^2;
Ptot_LS = @(P, Vin, neff, IR, Tj, RDSON_250V) Psw_LS(P, Vin, neff, IR,
    RDSON_250V)+Pcond_LS(P, Vin, neff, IR, Tj, RDSON_250V);

% Diodes
Pdiodes = @(P) 2*(0.9*Iout(P)+0.01*(pi/2*Iout(P)).^2);       % STTH30R04

% Output capacitors
P_caps = @(P) 5e-3*((pi^2/8-1)+pi^2/4)*Iout(P).^2;

% Transformer currents
Imagn = @(Vin, Lmagn, fsw) Vin./(4*sqrt(3)*Lmagn.*fsw);
Iprim = @(P, neff, Vin, Lmagn, fsw) sqrt((pi*neff/sqrt(2)*Iout(P)).^2+Imagn(
    Vin, Lmagn, fsw).^2);
Isec = @(P) pi/sqrt(2)*Iout(P);

% LLC switches
Psw_LLC = @(Vin, RDSON_60V, Tech60V_index, Lmagn) tOFF60V(RDSON_60V,
    Tech60V_index)/(8*Lmagn)*Vin.^2;
IRMS_LLC = @(P, neff, Vin, Lmagn, fsw) Iprim(P, neff, Vin, Lmagn, fsw)/sqrt(2)
    ;
Pcond_LLC = @(P, neff, Vin, Tj, Lmagn, fsw, RDSON_60V) RDSON_60V*(1+beta_60V*(
    Tj-25)+gamma_60V*(Tj-25).^2).*IRMS_LLC(P, neff, Vin, Lmagn, fsw).^2;
Pswitches_tot = @(P, neff, Vin, Tj, Lmagn, fsw, RDSON_60V, Tech60V_index) 4*(
    Pcond_LLC(P, neff, Vin, Tj, Lmagn, fsw, RDSON_60V)+Psw_LLC(Vin, RDSON_60V,
     Tech60V_index, Lmagn));
```

```
272
273 % Input capacitor
274 Pcin = @(P, Vin, Cin, Lmagn, fsw, neff, IR) ESR_CIN(Cin)*(Imagn(Vin, Lmagn,
        fsw).^2+Iout(P).^2.*(4*(pi^2/8-1)*neff^2+(4/3*beta_ZVS(P, Vin, neff, IR)
        .^2-1).*Gboost(Vin, neff).^2));
275
276 % Switching gate voltage
277 Vcc = 10;
278
279
280 %% Part 4: PSO
281
282 % Definition of the constraints of the solution space
283 fsw_min = 50e3;
284 fsw_max = 600e3;
285 n_min  = 0.5*(Vout/VMPP_min-Gboost_max);
286 n_max = 0.5*(Vout/VMPP_max-Gboost_min);
287 core_min = 1;
288 core_max = 3;
289 RDSON60V_min = 1e-3;
290 RDSON60V_max = 10e-3;
291 RDSON250V_min = 10e-3;
292 RDSON250V_max = 70e-3;
293
294 % Legend: [fsw, n, core_material, RDSON LLC, tech_LLC, RDSON Boost]
295 Limits = [fsw_min, n_min, core_min, RDSON60V_min, 1, RDSON250V_min;
296           fsw_max, n_max, core_max, RDSON60V_max, 2, RDSON250V_max];
297
298 % Initialization of the population vector
299 % Legend: Population_X = [fsw, neff, core, RDS60V, tech, RDS250V, obj_function
        ]
300 Population_current = zeros(N_population, 7);
301 Population_next = zeros(N_population, 7);
302 Xbest = zeros(N_population, 7);        % Matrix of the best solutions of each
        individual across all the generations
303 Gbest = zeros(1,7);                    % Vector of the global best across all
        the generations
304
305 % PSO loop
306
307 % Initialization before the loop
308 Consecutive_converging_solution = 1;   % Counter for the consecutive
        iterations for which the objective function converges
309 individual = 1;
310 Obj_function_best_previous = 0;
311 LCOE = 0;
312 Cost_efficiency = 0;
313 V_next = zeros(N_population, 6);        % Initialization of speed vector
314
315 % External loop: it goes on until the converence is reached
316 while Consecutive_converging_solution<=N_generations_convergence
317
318     % Internal loop: it goes on until all the individuals of the population
319     % have moved inside the solution space and been tested
```

```
320     while individual<=N_population
321
322         if N_generation==1
323
324             % Are we exploring the first generation? Then create an individual
                    with totally random position inside the
325             % solution space
326             fsw = round((fsw_max-fsw_min)*rand(1)+fsw_min, -3);
327             n = (n_max-n_min)*rand(1)+n_min;
328             core_index = randi([1 3], 1);
329             RDSON_60V = round((RDSON60V_max-RDSON60V_min)*rand(1)+RDSON60V_min
                    , 4);
330             Tech60V_index = randi([1 2], 1);
331             RDSON_250V = round((RDSON250V_max-RDSON250V_min)*rand(1)+
                    RDSON250V_min, 3);
332
333         else
334
335             % Are we exploring the next generations? Then create an individual
                    from the previous
336             % position and the velocity vector
337             Population_next(individual,1:6) = min(Limits(2,1:6), max(Limits
                    (1,1:6), Population_current(individual,1:6)+V_next(individual
                    ,1:6)));
338
339             fsw = round(Population_next(individual, 1),-3);
340             n = Population_next(individual, 2);
341             core_index = round(Population_next(individual, 3));
342             RDSON_60V = round(Population_next(individual, 4),4);
343             Tech60V_index = round(Population_next(individual, 5));
344             RDSON_250V = round(Population_next(individual, 6),3);
345
346         end
347
348
349
350         % Derived variables for the LLC switches
351         Rthjamb_60V = RthJAmb_60V(Tech60V_index, RDSON_60V);
352         Tmax_60V = Tjmax_60V(Tech60V_index);
353         tdead_60V = 0.01/fsw;       % Assumption: the deadtime is always
                selected as 1% of the switching period
354
355         % Derived variables for the boost switches
356         Ceq = 8*COSS_250V(RDSON_250V);          % Equivalent output
                capacitances of the boost switches: the 8 takes into account the 2
                 parallel Coss and the additional factor "4" to move from the
                datasheet value to the energy-equivalent capacitance (
                overestimation)
357         wres = 1/sqrt(Ceq*L);
358         Z0 = sqrt(L/Ceq);
359
360
361         %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
362         % Optimization of transformer (updated with magnetizing inductance
```

```
363         % constraint)
364         Lmagn = tdead_60V/(8*COSS_60V(Tech60V_index, RDSON_60V)*fsw);
365         IRMSmax =pi/sqrt(2)*n*PMPP_max/Vout;
366         Acond_prim = IRMSmax/J;          % [m^2]
367         N = 500;
368         transformer_design;
369         %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
370
371         % Transformer winding and core losses
372         Pwind = @(P, Vin) Rprim*Iprim(P, neff, Vin, Lmagn, fsw).^2+Rsec*Isec(P
                ).^2;
373         Pcore = @(Vin) pi/4*Kcore*Ve(APopt)*rho*(fsw/100e3)^alpha*(Vin/(0.1*4*
                Ae(APopt)*N1*fsw)).^beta;
374         P_Transf = @(P, Vin) Pwind(P, Vin)+Pcore(Vin);
375
376
377         % Derived design variables dependent on the transformer
378         IR = min(-(VMPP_min+(Gboost(VMPP_min, neff)-1)*VMPP_min*cos(wres*
                tdead_250V))/(Z0*sin(wres*tdead_250V)), 0);    % IR is the
                negative current value ensuring ZVS of the low-side MOSFET
379         Cboost = L*PMPP_max^2/(0.01*Vout*2*VMPP_min*Vout^2)*(2*Gboost(VMPP_min
                , neff)-1)^2/(Gboost(VMPP_min, neff)-1);
380         Cin = 1/(0.05*VMPP_min)*(1/(2*pi*fsw)*sqrt((4*neff*PMPP_max/(3*Vout))
                ^2+(VMPP_min/(2*pi*fsw*Lmagn))^2)+L*Gboost(VMPP_min, neff)^2*
                PMPP_max^2/(2*Dboost(VMPP_min, neff)*VMPP_min*Vout^2));
381
382
383         % Switching gate losses
384         Pgate = @(P, Vin) 4*fsw*Vcc*QG_60V(Tech60V_index, RDSON_60V)+2*
                fswBoost(P, Vin, neff, IR)*Vcc*QG_250V(RDSON_250V);
385
386
387         % Estimated converter temperature profiles according to Hossain et
388         % al., 2014
389         Tconv = @(Tamb, Tpanel, G, Ppv) -0.232+0.676*Tamb+0.365*Tpanel+0.002*G
                -0.0095*Ppv;
390
391         % Junction tempperature profiles functions
392         Tj_HS = @(P, Vin, Tconv) 25+1./(2*gamma_250V*RDSON_250V*IRMS_HS(P, Vin
                , neff, IR).^2).*(1/Rthjamb_250V-beta_250V*RDSON_250V*IRMS_HS(P,
                Vin, neff, IR).^2-...
393             abs(sqrt((1/Rthjamb_250V-beta_250V*RDSON_250V*IRMS_HS(P, Vin, neff
                    , IR).^2).^2-4*gamma_250V*RDSON_250V*IRMS_HS(P, Vin, neff, IR)
                    .^2.*(RDSON_250V*IRMS_HS(P, Vin, neff, IR).^2+Psw_HS(P, Vin,
                    neff, IR, RDSON_250V)+(Tconv-25)/Rthjamb_250V))));
394
395         Tj_LS = @(P, Vin, Tconv) 25+1./(2*gamma_250V*RDSON_250V*IRMS_LS(P, Vin
                , neff, IR).^2).*(1/Rthjamb_250V-beta_250V*RDSON_250V*IRMS_LS(P,
                Vin, neff, IR).^2-...
396             abs(sqrt((1/Rthjamb_250V-beta_250V*RDSON_250V*IRMS_LS(P, Vin, neff
                    , IR).^2).^2-4*gamma_250V*RDSON_250V*IRMS_LS(P, Vin, neff, IR)
                    .^2.*(RDSON_250V*IRMS_LS(P, Vin, neff, IR).^2+Psw_LS(P, Vin,
                    neff, IR, RDSON_250V)+(Tconv-25)/Rthjamb_250V))));
397
```

```
398         Tj_LLC = @(P, Vin, Tconv) 25+1./(2*gamma_60V*RDSON_60V*IRMS_LLC(P,
                neff, Vin, Lmagn, fsw).^2).*(1/Rthjamb_60V-beta_60V*RDSON_60V*
                IRMS_LLC(P, neff, Vin, Lmagn, fsw).^2-...
399             abs(sqrt((1/Rthjamb_60V-beta_60V*RDSON_60V*IRMS_LLC(P, neff, Vin,
                    Lmagn, fsw).^2).^2-4*gamma_60V*RDSON_60V*IRMS_LLC(P, neff, Vin
                    , Lmagn, fsw).^2.*(RDSON_60V*IRMS_LLC(P, neff, Vin, Lmagn, fsw
                    ).^2+Psw_LLC(Vin, RDSON_60V, Tech60V_index, Lmagn)+(Tconv-25)/
                    Rthjamb_60V))));
400
401
402         %%%%%%%%%% Total losses (reduced-orded function)
403         Ploss_TOTAL = @(P, Vin, TjLLC, TjLS, TjHS) Pcin(P, Vin, Cin, Lmagn,
                fsw, neff, IR) + Pswitches_tot(P, neff, Vin, TjLLC, Lmagn, fsw,
                RDSON_60V, Tech60V_index) + P_caps(P) + P_Transf(P, Vin) + Pdiodes
                (P) +...
404             Ptot_LS(P, Vin, neff, IR, TjLS, RDSON_250V) + Ptot_HS(P, Vin, neff
                    , IR, TjHS, RDSON_250V) + P_Cb(P, Vin, neff, Cboost, IR) + P_L
                    (P, Vin, neff, IR) + Pgate(P, Vin);
405
406
407         % Inclusion of degradation of the panel in the total energy
                computation
408         Energy_year = zeros(1, 25);
409
410         % Reliability analysis performed on the first year
411         Ppv = Degradation_panel(1)*PMPP(G, Tpanel);
412         Ipv = Degradation_panel(1)*IMPP(G, Tpanel);
413         Vpv = Ppv./Ipv;
414
415
416
417         %  Compute the temperature profiles at first year to be used as
                constraints
418         Tj_LLC_1 = Tj_LLC(Ppv, Vpv, Tconv(Tamb, Tpanel, G, Ppv));
419         Tj_LS_1 = Tj_LS(Ppv, Vpv, Tconv(Tamb, Tpanel, G, Ppv));
420         Tj_HS_1 = Tj_HS(Ppv, Vpv, Tconv(Tamb, Tpanel, G, Ppv));
421
422         % Number of times the junction temperatures exceed Tjmax
423         Failures_LLC = size(find(Tj_LLC_1>Tjmax_60V(Tech60V_index)),1);
424         Failures_LS = size(find(Tj_LS_1>Tjmax_250V),1);
425         Failures_HS = size(find(Tj_HS_1>Tjmax_250V),1);
426         Max_allowed_failures = 5;  % Due to potential localized errors in the
                irradiance measurement, relax the max temperature constraint
427
428
429         % Proceed with the reliability analysis and computation of the
                objective
430         % function only in case the maximum temperatures are not exceeded
431         if Failures_LLC<Max_allowed_failures && Failures_LS<
                Max_allowed_failures && Failures_HS<Max_allowed_failures &&
                TrDesign==1
432
433             % Monte-Carlo simulations to extract B1
434             MonteCarlo_LLC_LS_HS;
```

```
435             [B1_value, B1_index] = min(abs(Unrel_converter-0.01));
436             B1 = t(B1_index);
437
438
439             % Reliability constraint on B1 (>25 years): if satisfied,
440             % proceed with the computation of the losses, cost and
441             % objective function
442 %             if Damage_TOT_LLC<0.04 && Damage_TOT_Boost_LS<0.04 &&
    Damage_TOT_Boost_HS<0.04
443             if B1>25
444
445                 % Computation of converter cost
446                 Cost_conv = PRICE(Tech60V_index, RDSON_60V, RDSON_250V, Cin,
                        Cboost, fsw, APopt, N1, IRMSmax);
447
448                 if Obj_function_index==1        % min LCOE
449
450                     % Computation of first year energy
451                     Pout = (Ppv-real(Ploss_TOTAL(Ppv, Vpv, Tj_LLC(Ppv, Vpv,
                            Tconv(Tamb, Tpanel, G, Ppv)), Tj_LS(Ppv, Vpv, Tconv(
                            Tamb, Tpanel, G, Ppv)), Tj_HS(Ppv, Vpv, Tconv(Tamb,
                            Tpanel, G, Ppv))))).*(Ppv>20);
452                     Energy_year(1) = sum(Pout)*Tsample/(60e6);
453
454                     % Inside the loop, compute the collected energy on
455                     % 25 years operation
456                     for year_index=2:25
457                         Ppv = Degradation_panel(year_index)*PMPP(G, Tpanel);
458                         Ipv = Degradation_panel(year_index)*IMPP(G, Tpanel);
459                         Vpv = Ppv./Ipv;
460
461                         Pout = (Ppv-real(Ploss_TOTAL(Ppv, Vpv, Tj_LLC(Ppv, Vpv
                                , Tconv(Tamb, Tpanel, G, Ppv)), Tj_LS(Ppv, Vpv,
                                Tconv(Tamb, Tpanel, G, Ppv)), Tj_HS(Ppv, Vpv,
                                Tconv(Tamb, Tpanel, G, Ppv))))).*(Ppv>20);
462                         Energy_year(year_index) = sum(Pout)*Tsample/(60e6);
463                     end
464                     Energy_TOT = sum(Energy_year);
465
466                     % Computation of LCOE
467                     LCOE = Cost_conv/Energy_TOT;
468
469                 else      % min cost/efficiency
470
471                     % Computation of EURO efficiency
472                     eta_EURO = 100*((P_EURO-Ploss_TOTAL(P_EURO, Vrated, Tj_LLC
                            (P_EURO, Vrated, Trated), Tj_LS(P_EURO, Vrated, Trated
                            ), Tj_HS(P_EURO, Vrated, Trated)))./P_EURO)*
                            weights_EURO;
473
474                     % Computation of Cost / eta_EURO
475                     Cost_efficiency = Cost_conv/eta_EURO;
476
477                 end
```

```
478
479
480                 % Both the objective functions are computed and save in a
481                 % vector: a selector will then filter on the one of
482                 % interest
483                 Obj_function = [LCOE, Cost_efficiency];
484
485
486                 % This variable set leads to an acceptable solution: save
487                 % it
488                 Population_next(individual, :) = [fsw, neff, core_index,
                        RDSON_60V, Tech60V_index, RDSON_250V, Obj_function(
                        Obj_function_index)];
489
490                 % If we are at next generations and the objective function
491                 % for the k individual is lower, update it
492                 if N_generation>1 && Obj_function(Obj_function_index)<Xbest(
                        individual,7)
493                     Xbest(individual,:) = Population_next(individual, :);
494                 end
495
496                 individual = individual +1;
497
498
499             else
500                 % This trial individual did not survive the B1 constraint:
                        save
501                 % the current individual instead
502                 Population_next(individual, :) = Population_current(individual
                        , :);
503                 if N_generation>1
504                     individual=individual+1;
505                 end
506
507             end     % Close the computation of the objective function for B1
                    >25
508
509
510         else
511                 % This trial individual did not survive the Tjmax constraint:
                        save
512                 % the current individual instead
513                 Population_next(individual, :) = Population_current(individual
                        , :);
514                 if N_generation>1
515                     individual=individual+1;
516                 end
517
518         end     % Close the if for the computation of B1
519
520     end         % Close the "while" loop inside the generation: all the
                individuals have been created or have moved
521
522     % Update the current population, by filtering only the survivors (check=1)
```

```
523     Population_current = Population_next;
524
525     % Save the current generation in the output structure
526     Generation_structure(N_generation).Population = Population_current;
527
528
529
530     % Update the best solutions and the speed vector
531     if N_generation==1
532
533         % If we are at the first generation, the current generation is
534         % automatically the best generation, and the speed vector is
535         % randomly generated
536         Xbest = Population_current;
537
538         for k=1:N_population
539             V_next(k,:) = [-5e4+10e4*round(rand(1)),...       % +-50kHz
540                            -0.2+0.4*round(rand(1)),...        % +-0.2
541                            -1+2*round(rand(1)),...            % +-1
542                            -3e-3+6e-3*round(rand(1)),...      % +-3mOhm
543                            -1+2*round(rand(1)),...            % +-1
544                            -3e-2+6e-2*round(rand(1))];        % +-30mOhm
545         end
546
547     else
548
549         % If we are at next generations, the speed vector is generated from
550         % the current positions and speeds
551         V_next = omega_PSO*V_next+...        % Inertia term
552              c1_PSO*rand(N_population,6).*(Xbest(:,1:6)-Population_current
                     (:,1:6))+...        % Cognitive term
553              c2_PSO*rand(N_population,6).*(ones(N_population,1)*Gbest(1:6)-
                     Population_current(:,1:6));      % Social term
554     end
555
556     % Identify the global best among the individuals' best
557     [Obj_min, index_Objmin] = min(Xbest(:,7));
558     Gbest = Xbest(index_Objmin,:);
559
560     % Compare the current minimum with the previous one: if it is in the
561     % boundaries defined for the convergence, update the number of
562     % consecutive convergent generations; otherwise, re-initialize that
563     % flag
564     Obj_function_best_current = min(Population_current(:,7));
565
566     if Obj_function_best_current>=(1-epsilon)*Obj_function_best_previous &&
            Obj_function_best_current<=(1+epsilon)*Obj_function_best_previous
567         Consecutive_converging_solution = Consecutive_converging_solution+1;
568     else
569         Consecutive_converging_solution = 1;
570     end
571
572     % Update the value of the best objective function in the current
573     % generation
```

```
574     Obj_function_best_previous = Obj_function_best_current;
575
576     % Re-initialize the individuals' index
577     individual = 1;
578
579     % Update the number of generation
580     N_generation = N_generation+1
581
582
583 end     % Close the "while" loop on the generations: the algorithm has found a
          convergent solution
584
585
586
587 %% Part 5: Optimal design
588
589 % Derive the best transformer and capacitors design
590 fsw = Gbest(1);
591 n = Gbest(2);
592 core_index = Gbest(3);
593 RDSON_60V = Gbest(4);
594 Tech60V_index = Gbest(5);
595 RDSON_250V = Gbest(6);
596
597 % Preliminary functions
598 tdead_60V = 0.01/fsw;       % Assumption: the deadtime is always selected as
        1% of the switching period
599 Lmagn = tdead_60V/(8*COSS_60V(Tech60V_index, RDSON_60V)*fsw);
600 IRMSmax =pi/sqrt(2)*n*PMPP_max/Vout;
601 Acond_prim = IRMSmax/J;         % [m^2]
602
603 % Computation of transformer design and capacitors
604 transformer_design;
605 Cboost = L*PMPP_max^2/(0.01*Vout*2*VMPP_min*Vout^2)*(2*Gboost(VMPP_min, neff)
        -1)^2/(Gboost(VMPP_min, neff)-1);
606 Cin = 1/(0.05*VMPP_min)*(1/(2*pi*fsw)*sqrt((4*neff*PMPP_max/(3*Vout))^2+(
        VMPP_min/(2*pi*fsw*Lmagn))^2)+L*Gboost(VMPP_min, neff)^2*PMPP_max^2/(2*
        Dboost(VMPP_min, neff)*VMPP_min*Vout^2));
607
608 OptTransfC.N1 = N1;
609 OptTransfC.N2 = N2;
610 OptTransfC.AP = APopt;
611 OptTransfC.neff = neff;
612 OptTransfC.mueff = mueff;
613 OptTransfC.Lmagn = Lmagn;
614 OptTransfC.Rprim = Rprim;
615 OptTransfC.Rsec = Rsec;
616 OptTransfC.Cboost = Cboost;
617 OptTransfC.Cin = Cin;
618
619 OptSolution = Gbest;
620 save("Populations_PSO.mat", "Generation_structure")
621 save("OptInputs.mat", "OptSolution")
622
```

```
623
624
625 % Reliability analysis performed on the first year
626 Ppv = Degradation_panel(1)*PMPP(G, Tpanel);
627 Ipv = Degradation_panel(1)*IMPP(G, Tpanel);
628 Vpv = Ppv./Ipv;
629
630 %  Compute the temperature profiles at first year to be used as constraints
631 Tj_LLC_1 = Tj_LLC(Ppv, Vpv, Tconv(Tamb, Tpanel, G, Ppv));
632 Tj_LS_1 = Tj_LS(Ppv, Vpv, Tconv(Tamb, Tpanel, G, Ppv));
633 Tj_HS_1 = Tj_HS(Ppv, Vpv, Tconv(Tamb, Tpanel, G, Ppv));
634
635 MonteCarlo_LLC_LS_HS;
636 Damage_TOT_LLC;
637 Damage_TOT_Boost_LS;
638 Damage_TOT_Boost_HS;
639 [B1_value, B1_index] = min(abs(Unrel_converter-0.01));
640 B1 = t(B1_index)
```

B.2 Transformer design subroutine: *transformer_design.m*

```
1  % 75%-rated power case, at which minimizing the losses or the Cost-power ratio
       (more frequent working point than the rated one)
2  Pinput_75 = 0.75*PMPP_BSTC*2*n*VMPP_BSTC/Vout;
3  Iprim_75 = pi/(2*sqrt(2))*Pinput_75/VMPP_BSTC;
4
5  % Litz wire parameters (based on the max current): diameter and increase in
       resistance due to proximity effect
6  ds = diameter_Litz(fsw);      % [cm]
7  Fp = FR_prim(fsw, IRMSmax);
8  Fs = FR_sec(fsw, IRMSmax, n);
9
10 % Material-specific parameters
11 rho = 1e3*rho_SE(core_index);
12 alpha = alpha_SE(core_index);
13 beta = beta_SE(core_index);
14
15 % Constraint on the minimum Area Product
16 B100mW = 0.1*(4*100/(pi*rho*1e-3)*(100e3/fsw)^alpha).^(1/beta);
17 APmin = 2*VMPP_min*IRMSmax*1e8/(J*B100mW*fsw*Kf*Ku);      % Area product
       approach
18 AP = linspace(APmin, 10*APmin, N);
19
20 % Computation of worst-case magnetizing current that may lead to saturation
21 % Assumption: the minimum acceptable magnetizing inductance is set to 80% of
       the target one, to avoid oversizing the air gap (fringing flux losses)
22 Lmagn_min = 0.8*Lmagn;
23 Imagn_max = Vmaxsat/(4*fsw*Lmagn_min);
24
25
```

```
% Initialization of Losses and Cost-to-Power Ratio (rows: constant N1; columns: constant AP)
P = zeros(10, N);
Cost_Power = zeros(10, N);


% Losses function at the 75% rated power condition
Ptransf = @(AP, Np) Kcore*pi/4*Ve(AP)*rho*(fsw/100e3)^alpha.*(VMPP_min./(4*fsw*0.1*Ae(AP).*Np)).^beta+...
    rhoCu*Np.*MTL(AP)/Acond_prim*Iprim_75^2*(Fp+Fs);


% Transformer CPR function at 75% rated power
Cost_core = @(AP) Price_core(AP);
Cost_Litz = @(AP, Np) Price_Litz(fsw, AP, Np, IRMSmax);
Cost_T = @(AP,Np) Cost_core(AP)+Cost_Litz(AP, Np);
CPR_T = @(AP, Np) Cost_T(AP, Np)./(Pinput_75-Ptransf(AP, Np));


% For each N1, compute the power losses and only consider the domain
% obtained by intersecting the constraints on AP (Delta B, window area, Lmagn_min)
options = optimoptions('fsolve','Display','none');
Nrows = 10;
for N1_step=1:1:Nrows

    % At the current N1 step, identify the constrain on the minimum AP
    APmin_Ae = (1e4/AP_Ae*VMPP_max/(4*B100mW*fsw*N1_step))^2;       % Delta B (flux density) constraint
    APmin_Aw = (1e4/AP_Aw*2*Acond_prim*N1_step/Ku)^2;              % Window area (space) constraint
    APmin_Lmagn = fsolve(@(x) N1_step-Lmagn_min*mu0*sqrt(2)*Imagn_max*1e9./(0.6*Bsat*le(x).*(q(core_sel)+m(core_sel)*Ae(x)*1e4)), 10, options);
            % Lmagn constraint: q and m are geometry-related coefficients for the linear function AL = f(Ae, mu_eff)

    % Compute the two objective functions at the current N1 step and in the available AP domain. For the points outside the domain, assign an arbitrary high value (these points will be non-optimal)
    P(N1_step, :)=Ptransf(AP, N1_step).*(AP>=max(APmin_Ae, max(APmin_Aw, APmin_Lmagn)))+100*(AP<max(APmin_Ae, max(APmin_Aw, APmin_Lmagn)));
    Cost_Power(N1_step, :)=CPR_T(AP, N1_step).*(AP>=max(APmin_Ae, max(APmin_Aw, APmin_Lmagn)))+100*(AP<max(APmin_Ae, max(APmin_Aw, APmin_Lmagn)));
end

% According to the desired objective function, comment the other one: this command extracts the value and coordinate of the minimum value of obj. function
[tot_min, min_index] = min(P, [], 'all');
%[tot_min, min_index] = min(Cost_Power, [], 'all');


% Extract the row and column coordinates from the matrix coordinate
column_index_opt = ceil(min_index/Nrows);
```

```
row_index_opt = min_index-Nrows*floor(min_index/Nrows)+Nrows*(min_index-Nrows*
    floor(min_index/Nrows)==0);


%%%% Optimal design and related derived parameters
N1 = row_index_opt;
APopt = AP(column_index_opt);
N2 = ceil(n*N1);        % Round excess to take into account leakage inductance
neff = N2/N1;
Rprim = rhoCu*N1*MTL(APopt)/Acond_prim*Fp;
Rsec = rhoCu*N1*MTL(APopt)/Acond_prim*neff^2*Fs;

% Lmagn and mueff are interconnected: one is a choice, the other follows
Lmagn = Lmagn_min;      % Free choice (minimum value to be sure to achieve ZVS
    )
mueff = 1e9*Lmagn/((q(core_sel)+m(core_sel)*Ae(APopt)*1e4)*N1^2);

% Satisfying temperature and Bmax constraint?
Tamb_max = 40;
Tcore_max = Tamb_max+Ptransf(APopt, N1)*53/(Ve(APopt)*1e6)^0.54;
Bmax = Vmaxsat/(4*fsw*Ae(APopt)*N1);

% If at least one of the two constraints (max temp or Bmax) is not met, the
% identified transformer solution must be discarded
if Tcore_max<100 && Bmax<Bsat
    TrDesign = 1;
else
    TrDesign = 0;
    row_index_opt
    column_index_opt
    fprintf('No available solution for the transformer\n')
end
```

B.3 Monte-Carlo simulations: *MonteCarlo_LLC_LS_HS.m*

```
% Monte-Carlo analysis for the LLC switches
TableLLC = rainflow(Tj_LLC(Ppv, Vpv, Tamb));
Cycles_1min_1day_index = find((TableLLC(:,5)-TableLLC(:,4))*Tsample>=1 & (
    TableLLC(:,5)-TableLLC(:,4))*Tsample<=24*60);
CountsLLC = TableLLC(Cycles_1min_1day_index,1);
RangeLLC = TableLLC(Cycles_1min_1day_index,2);
Tj_minLLC = TableLLC(Cycles_1min_1day_index,3)-0.5*RangeLLC;
Damage_LLC = CountsLLC./Nfi(RangeLLC, Tj_minLLC);
Damage_TOT_LLC = sum(Damage_LLC);
DeltaTeq_LLC = (Ncycles_eq./(Damage_TOT_LLC*A_LT*exp(Ea_LT/(Tjav_eq+273.15))))
    .^(1/alpha_LT);
DTLLC_MC = normrnd(DeltaTeq_LLC, 2*tolerance/3*DeltaTeq_LLC, [nMC,1]);
Nfi_LLC_MC = A_MC.*exp(Ea_MC./(Tjav_MC+273.15)).*DeltaTeq_LLC.^alpha_MC;
Life_LLC_MC = Nfi_LLC_MC/Ncycles_eq;
GammaParams = gamfit(Life_LLC_MC);
```

```
alpha_LLC = GammaParams(1);
beta_LLC = GammaParams(2);


% Monte-Carlo analysis for the low-side boost switch
TableBoost = rainflow(Tj_LS(Ppv, Vpv, Tamb));
Cycles_1min_1day_index = find((TableBoost(:,5)-TableBoost(:,4))*Tsample>=1 & (TableBoost(:,5)-TableBoost(:,4))*Tsample<=24*60);
CountsBoost = TableBoost(Cycles_1min_1day_index,1);
RangeBoost = TableBoost(Cycles_1min_1day_index,2);
Tj_minBoost = TableBoost(Cycles_1min_1day_index,3)-0.5*RangeBoost;
Damage_Boost = CountsBoost./Nfi(RangeBoost, Tj_minBoost);
Damage_TOT_Boost_LS = sum(Damage_Boost);
DeltaTeq_b = (Ncycles_eq./(Damage_TOT_Boost_LS*A_LT*exp(Ea_LT/(Tjav_eq+273.15)))).^(1/alpha_LT);
DTb_MC = normrnd(DeltaTeq_b, 2*tolerance/3*DeltaTeq_b, [nMC,1]);
Nfi_b_MC = A_MC.*exp(Ea_MC./(Tjav_MC+273.15)).*DTb_MC.^alpha_MC;
Life_b_MC = Nfi_b_MC/Ncycles_eq;
GammaParams = gamfit(Life_b_MC);
alpha_bLS = GammaParams(1);
beta_bLS = GammaParams(2);


% Monte-Carlo analysis for the high-side boost switch
TableBoost = rainflow(Tj_HS(Ppv, Vpv, Tamb));
Cycles_1min_1day_index = find((TableBoost(:,5)-TableBoost(:,4))*Tsample>=1 & (TableBoost(:,5)-TableBoost(:,4))*Tsample<=24*60);
CountsBoost = TableBoost(Cycles_1min_1day_index,1);
RangeBoost = TableBoost(Cycles_1min_1day_index,2);
Tj_minBoost = TableBoost(Cycles_1min_1day_index,3)-0.5*RangeBoost;
Damage_Boost = CountsBoost./Nfi(RangeBoost, Tj_minBoost);
Damage_TOT_Boost_HS = sum(Damage_Boost);
DeltaTeq_b = (Ncycles_eq./(Damage_TOT_Boost_HS*A_LT*exp(Ea_LT/(Tjav_eq+273.15)))).^(1/alpha_LT);
DTb_MC = normrnd(DeltaTeq_b, 2*tolerance/3*DeltaTeq_b, [nMC,1]);
Nfi_b_MC = A_MC.*exp(Ea_MC./(Tjav_MC+273.15)).*DTb_MC.^alpha_MC;
Life_b_MC = Nfi_b_MC/Ncycles_eq;
GammaParams = gamfit(Life_b_MC);
alpha_bHS = GammaParams(1);
beta_bHS = GammaParams(2);


% Unreliability functions
Unrel_M14 = gamcdf(t, alpha_LLC, beta_LLC);
Unrel_MLS = gamcdf(t, alpha_bLS, beta_bLS);
Unrel_MHS = gamcdf(t, alpha_bHS, beta_bHS);
Unrel_converter = 1-(1-Unrel_M14).^4.*(1-Unrel_MLS).*(1-Unrel_MHS);
```