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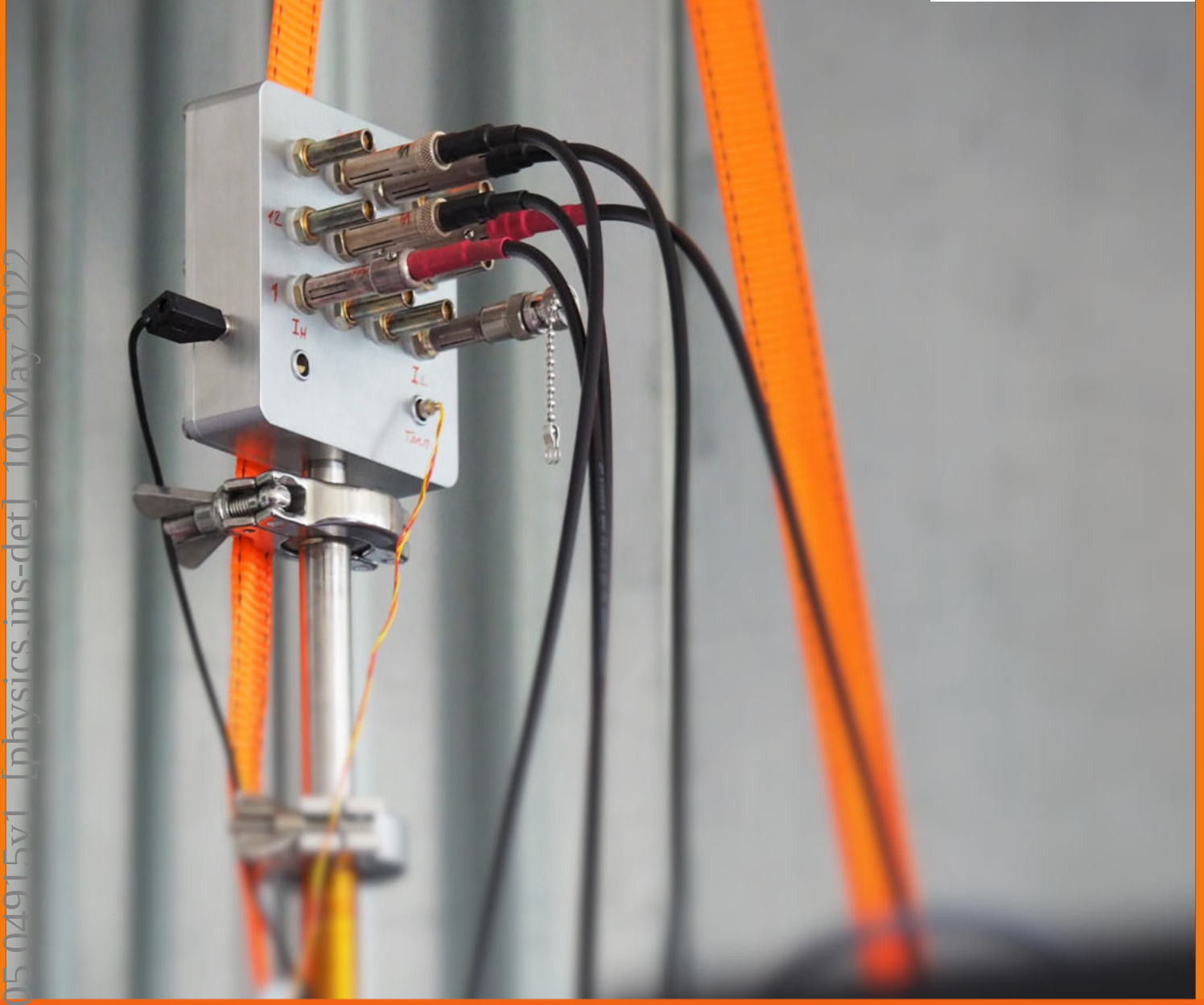
Graphene Impedance Quantum Standard



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Good Practice Guide

Graphene-based AC-QHE realization of the farad

EMPIR
EURAMET
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Good practice guide on the graphene-based AC-QHE realization of the farad

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Guide information

What is this about?
This guide provides information for the realization of the farad from the quantum Hall resistance in graphene devices by using digital impedance bridges.

Who is it for?
This guide is for researchers active in electrical metrology (national metrology institutes, calibration centers, metrology laboratories in the academy) who need to perform impedance measurements traceable to the International System of Units.

What is its purpose?
This guide provides a detailed description of how to set up a laboratory to perform measurements of artifact capacitance standards in terms of the quantized Hall resistance in graphene devices. The fabrication and characterization of graphene quantum Hall effect devices, the cryogenic environment required to achieve the quantization conditions, the digital impedance bridges and calibration procedures are reported.

What is the prerequired knowledge?
This guide is for users in research and industry who have experience with and access to the advanced techniques described herein. It is targeted at researchers having experience in electrical metrology.

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Introduction

GIQS - Graphene Impedance Quantum Standard [ ] is a three-year Joint Research Project (code 18SIB07) of the European Metrology Programme for Innovation and Research (EMPIR).

The aim of GIQS is to enable an economically efficient traceability of measurements of impedance quantities (resistance, capacitance, inductance) to the defining constants (the Planck constant and the elementary charge) of the revised International System of Units (SI). New and easier to operate measurement bridges, convenient and easier to use graphene quantum standards, cryogenic systems, and methods to combine them will be developed.

The overall objective of GIQS is to combine novel digital impedance measurement bridges with graphene-based ac quantized Hall resistance standards in a simplified cryogenic environment, and disseminate the technology to national metrology institutes, calibration centers, research institutions and industry. Specific objectives are:

- To optimize graphene devices for their use in the ac regime under relaxed experimental conditions (temperature of 4 K or higher, magnetic field less than 6 T);
- To advance digital and Josephson impedance bridges working in a wide range of impedance and frequency;
- To combine the graphene devices with the bridges developed, and realize a quantum capacitance standard with accuracy in the 0.1 to 0.01 ppm range;
- To develop a cryocooler system hosting both Josephson and quantum Hall devices as the core element of an integrated quantum resistance and impedance standard;
- To facilitate the take up of the technology and measurement infrastructure developed in the project by the measurement supply chain: graphene manufacturers, standards developing organisations and end users.

1 The SI and the quantum Hall effect

The International System of Units (SI) in its present form was approved by the 26th General Conference of Weights and Measures in November 2018 [ ] and implemented on 20 May 2019. It is described in the *SI Brochure*, 9th edition [ ]. The electrical units are defined by the values of the elementary charge $e = 1.602\,176\,634 \times 10^{-19}$ C and the Planck constant $h = 6.626\,070\,15 \times 10^{-34}$ J s, fixed as exact in the definition of the ampere and the kilogram.

1.1 Units of electrical impedance

In the SI, the units of electrical impedance are the ohm (Ω), the farad (F) and the henry (H). They are related by

$$1\,\Omega = 1\,\mathrm{H\,s^{-1}} = 1\,\mathrm{F^{-1}s}. \tag{1.1}$$

A realization of one of the units can thus form the basis for the realisation of the other two, provided that a realization of the second or the hertz is also available.

1.2 The quantum Hall effect

Edwin Hall discovered the Hall effect in 1879 [ ]: if a conducting slab carries an electric current I, and a static magnetic field B is applied orthogonally to the slab surface, a voltage V develops across the slab, perpendicularly to both the current direction and the magnetic field. The ratio $R_\mathrm{H} = V/I$ is called the *Hall resistance*, and in the normal Hall effect its value is proportional to B and dependent on slab material, thickness and temperature.

In 1980, Klaus von Klizing discovered the *quantum Hall effect* [ ]: in samples where a two-dimensional layer of conduction is present, for high B and low temperature T, the Hall resistance becomes *quantized*. Its value is no longer dependent on the device material or the temperature: it is a fraction R_K/i (where i is a small integer, typically $i = 2$) of a fundamental constant, the *von Klitzing constant*, or *quantum of resistance*, $R_\mathrm{K} = h/e^2$.

The samples investigated by von Klitzing were silicon devices. In the 1990s gallium arsenide (GaAs) heterostructures were developed [ ], displaying a robust effect at a magnetic field in the order of 10 T and at measurement currents ($> 50\,\mu$A) suited for the calibration of artifact standard resistors. The temperature required by either Si or GaAs devices are typically of the order of 1.5 K or less.

1.3 Realization of impedance units

According to 9th SI Brochure, Appendix 2 [ ],

> **The ohm** Ω can be realized as follows [. . .] by using the quantum Hall effect in a manner consistent with the CCEM Guidelines and the following value of the von Klitzing constant
>
> $$R_\mathrm{K} = 25\,812.807\,459\,304\,5\,\Omega. \tag{1.2}$$

[. . .]

The farad F can be realized [. . .] by comparing the impedance of a known resistance obtained using the quantum Hall effect and the value of the von Klitzing constant given in Eq. , including a quantized Hall resistance itself, to the impedance of an unknown capacitance using, for example, a quadrature bridge [. . .]

The henry H can be realized [. . .] by comparing the impedance of an unknown inductance to the impedance of a known capacitance with the aid of known resistances using, for example, a Maxwell-Wien bridge, where the known capacitance and resistances have been determined, for example, from the quantum Hall effect and the value of R_K given in Eq. [. . .]

The impedance units can therefore be realized in terms of the quantum Hall effect, using impedance bridges. The focus of this guide is on the realization of the capacitance unit by exploiting the quantum Hall effect in graphene devices, and digital impedance bridges.

2 Graphene

2.1 The quantum Hall effect in graphene

The discovery of graphene (2004) [ ] initiated research to exploit the quantum Hall effect in this new material. It was demonstrated [,] that, with respect to GaAs devices, graphene QHE devices can operate at lower magnetic field (5 T or less), higher measurement current (up to hundreds of µA) and higher temperature (5 K). These conditions allow to implement tabletop quantized Hall resistance standards using small, inexpensive dry cryocoolers [,], suitable to be continuously operated in a calibration laboratory. Research is now focusing on achieving better reproducibility of fabrication and long-term stability of devices.

2.2 Fabrication of graphene samples

Here the steps for the production of graphene QHR devices are described. Section is about the growth of graphene films including all involved preparation steps, Section involves the lithographic processes to realize a QHR device in form of a graphene Hall bar. The described processes and measurements apply to the devices produced and investigated in the cleanroom facility and laboratories of PTB; other fabrication techniques that achieve high-quality QHR devices have been considered [, ,].

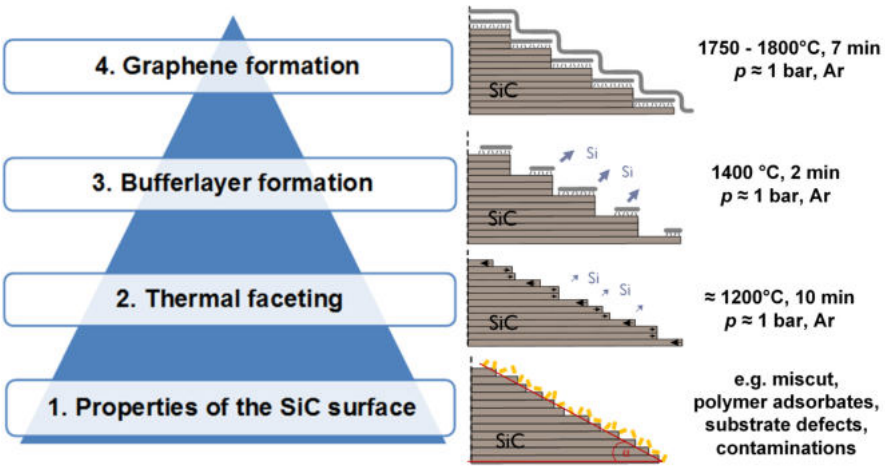


Figure 2.1: Process steps involved in the growth of graphene on SiC substrates - from the bottom to the top.

2.2.1 Graphene growth

The processes shown in Figure describe, from bottom to top, the four major steps to consider for the growth of high quality monolayer graphene films.

Realizing the appropriate starting properties of the SiC before the thermal annealing is initiated in the growth chamber is a very crucial step. Suggested substrates are prime-grade (low defect density) 4H and 6H-SiC wafers with a CMP prepared Si-face with a miscut angle $\leq$ 0.15°. Semi-insulating or n-type wafers may be used since both types of wafers are insulating at temperatures around 4 K. The substrate should be free of metal or organic contaminations which can originate from the processes involved during the dicing procedure of the wafer. Dicing tapes may be used to protect the Si-face of the wafer, but intensive cleaning must be applied before processing is continued. Usually, a batch of diced substrate pieces is kept in a beaker with acetone for at least 12 h. On the day the diced substrate pieces are introduced into the growth chamber, they are cleaned in ULSI grade acetone and ULSI isopropanol for 10 min and 15 min, respectively, and spin-dried afterward. The substrates then follow a polymer treatment for Polymer-Assisted Sublimation Growth (PASG) by spin-on deposition at 6000 rpm. The suitable volume ratio of the polymer solution is 2.3 µl concentrated AZ5214E photoresist solved in 1 µl isopropanol.

The so prepared substrates are then introduced into the growth chamber to initiate the growth process following the evacuation of the growth chamber. The base pressure to be reached before the annealing process is initiated is 10^{-6} mbar, after which the chamber and samples are heated in vacuum for 30 min at 900 ℃. The thermal faceting of the substrate is initiated at 1200 ℃ for 10 min. Then the temperature is raised to 1400 ℃, where Si sublimation of the substrate starts and the deposited amorphous

[1] This step is for additional cleaning and decomposition of the polymer adsorbate into amorphous carbon.

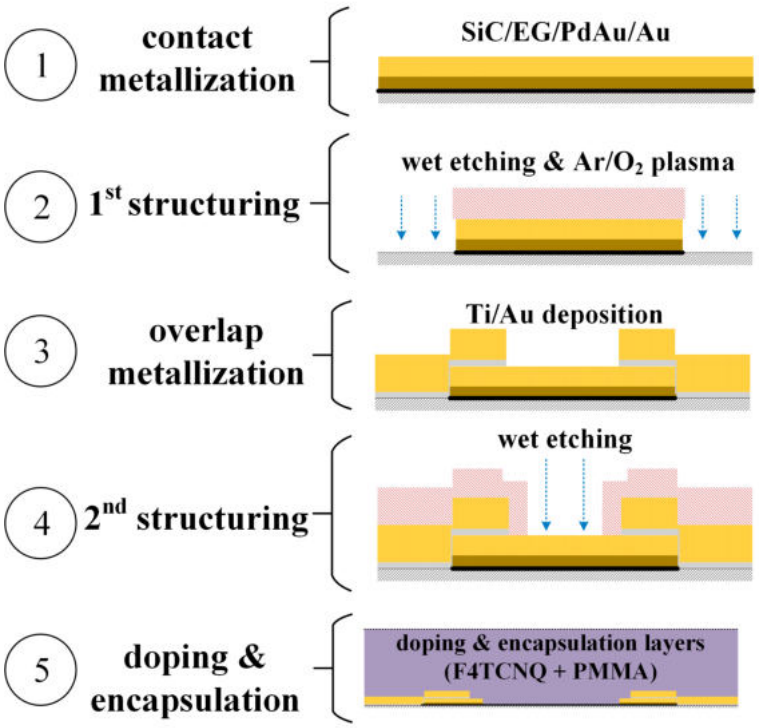


Figure 2.2: Photolitography steps for the fabrication of graphene Hall bars.

carbon converts into a high density of buffer layer domains. The high density of buffer layer islands prevents the formation of high step edges, so-called giant steps, during the subsequent graphene growth at a temperature of 1750 ℃ and 1800 ℃ for 7 min in total.

2.2.2 Device fabrication

For device fabrication, a UV-photolithography process is used, which compared to e-beam lithography has the advantage of being much faster. The process principle originated at NIST [ ], and was further improved at PTB with respect to different wet- and dry-etching processes, metal compositions, and photoresists during the GIQS project.

In the first step, the graphene layer, indicated by the thick black line in Figure , is covered by a PdAu/Au layer which is then structured by wet-etching using potassium iodide solution and O_2 plasma in the second step. In step 3, the structured Hall bar, which is at this point still covered by PdAu/Au, is partially overlapped by Ti/Au pads in the regions that later become the electrical contacts. In step 4, the metal covering the Hall bar is selectively removed by wet etching using a photomask. Microscope images from steps 2, 3, 4, and graphene/metal contacts are given in Figure . For chemical adjustment of the charge carrier density, the device is covered by doping and encapsulation layers using F4TCNQ molecules as dopant and PMMA resist for encapsulation [,]. Subsequently, the devices are wire bonded onto a chip carrier.

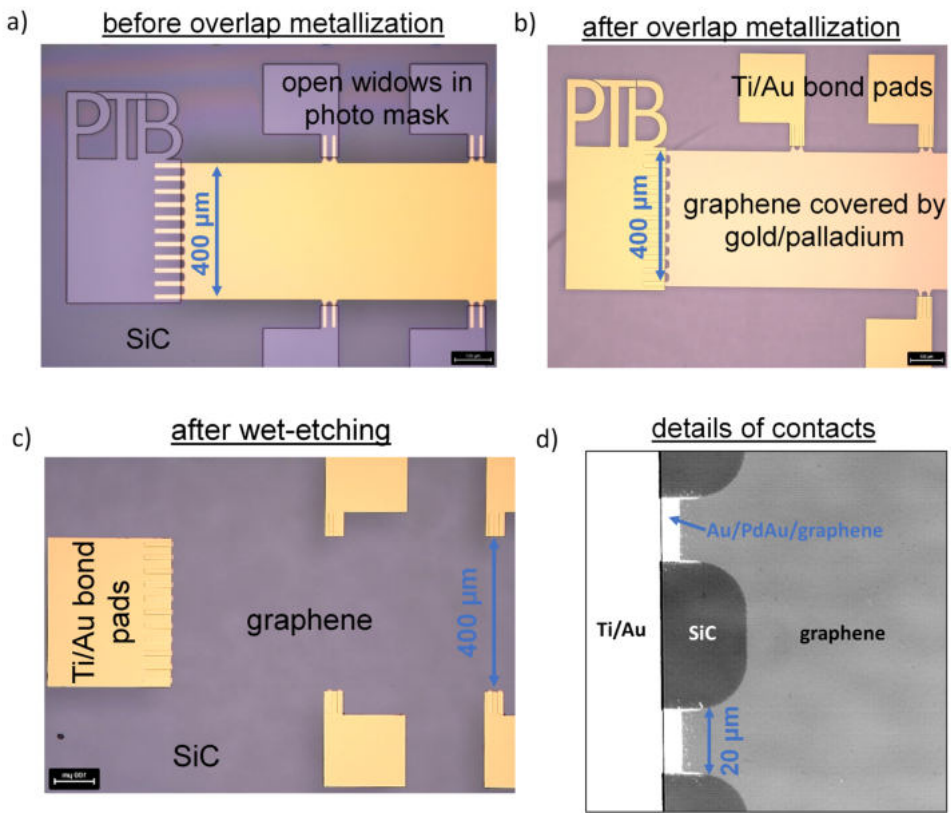


Figure 2.3: Microscope images of graphene QHR Hall bars at different steps of the device processing. (a) Structured Hall bar and the developed photo mask befrore the deposition of Ti/Au. (b) after Ti/Au deposition,with the graphene still being covered and protected by the Au/PdAu layer. (c) After selective removal of the metal cover of the graphene film by wet-etching. (d) Detail image of the split-contact design, showing$\approx$ 20 µm **wide graphene fingers that are separated from each other by**$\approx$ 40 µm**.**

The Hall bar geometry for devices used for standard dc measurements (Figure) has eight contacts of which six are Hall contacts, and two are the source and drain contacts. For the purpose of ac operation, the number of Hall contacts was reduced to the minimum number of six contacts that are required for the triple-series connection [ ]. Both the distance between two neighboring contacts and the width of the graphene channel are 400 µm. Electrical contacting is realized by split-contacts with eleven individual fingers in case of the source/drain contacts and two fingers in the Hall contacts as it can be understood from (a). The split contact helps to minimize the contact resistance of the device, and typical values of the order of a few mΩ or even on the µΩ level can be realized [ ].

2.3 Characterization

The electrical characterization of graphene devices follows several steps, from pre-characterization to high accuracy measurements. The framework for precision quantum Hall measurements are the existing guidelines of quantum Hall resistance metrology for

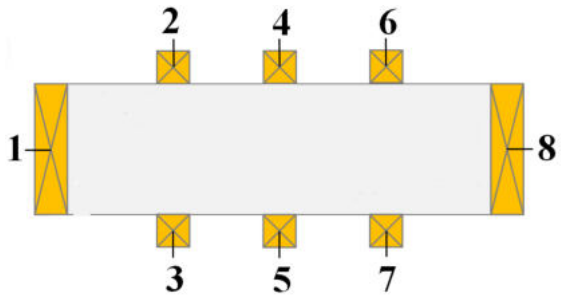


Figure 2.4: Device schematic of the electrical contact labels and equi-potentials in the quantum Hall regime.

T	cooldown	$R_{2.4}$	$R_{4,6}$	$R_{3,5}$	$R_{5,7}$	$R_{1,8}$	$R_{2,3}$	$R_{4,5}$	$R_{6,7}$
K	min	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ	kΩ
294	0	6.2	5.8	6.2	5.9	25.5	-0.14	-0.13	-0.03
4.2	30	3.9	3.8	4.0	3.9	16.5	-0.28	-0.24	-0.15

Table 2.1: Typical four-terminal resistances of graphene QHE devices measured at RT and at 4.2 K **and** $B = 0$ T **with fixed current terminals using pin 1 and 8.**

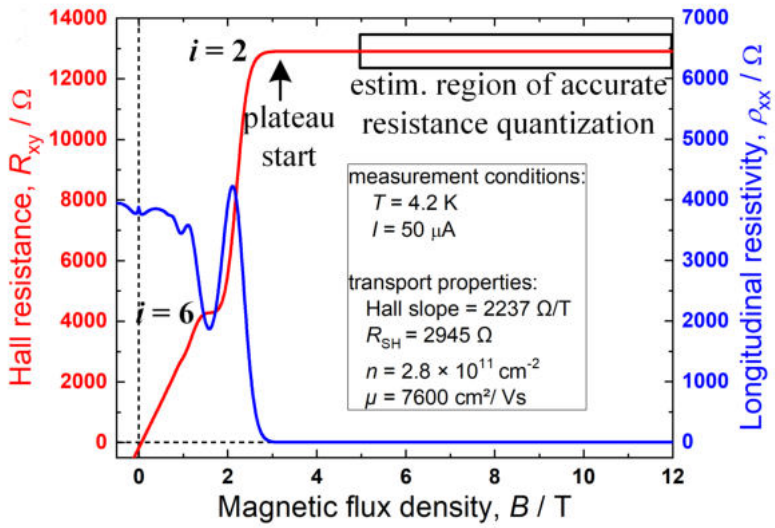
GaAs QHE devices [ ]. However, since the handling and behaviour of graphene QHE devices are different from those of GaAs devices, the steps involved in the electrical characterization including the precision measurements require specific adjustments of the measurement protocol.

The following measurement protocol for graphene QHR devices starts with introducing the measurement methods that are important to characterize the device quality prior to high accuracy quantum Hall measurements. These preliminary investigations comprise, e.g., measurements of the sheet resistance(s), the overall shape of the Hall curve over a wide range of magnetic flux densities and the contact resistances. In Sections , , . In Sections , , a dc resistance bridge is used to evaluate the so-called *s*-parameter and to validate the relevant device characteristics with the highest possible precision.

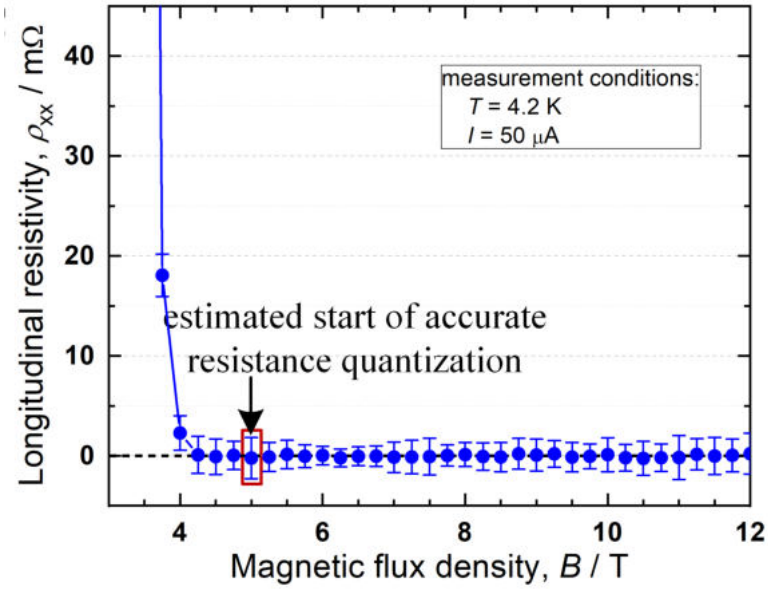
The measurement protocol is explained with the help of a practical example. The schematic in Figure shows the labeling of the electrical contacts and the typical configuration of the electrical potentials in the quantum Hall regime.

2.3.1 Room-temperature resistances and cooldown procedure

Before the device (mounted on the chip carrier) is cooled down in the cryostat, it is attached to the probe stick at room temperature for simple room temperature characterization to identify open contacts or inhomogeneities in its electrical properties.



(a)



(b)

Figure 2.5: Typical magnetotransport measurements of a graphene-based QHE device. ( ) The start of the resistance plateau (black arrow) and the expectable range of B-field values where accurate resistance quantization with $R_{xy} = R_K/2$ is achieved (black square box) are marked accordingly. The electrical transport properties in the inset are typical for devices with accurate resistance quantization starting around $B = 5$ T at the given conditions. ( ) Longitudinal resistances determined by the current-reversal measurement technique at fixed B-field values using a precision current source and a nano-voltmeter. For separation of $\Delta B = 0.25$ T and the given measurement conditions, the 4th ρ_{xx} value that is zero within the measurement uncertainty typically gives the margins for accurate resistance quantization. The error bar indicates the type A uncertainty ($k = 1$).

contact/pin	current contacts	voltage contacts	resistance Ω
1	1 & 8	1 & 2	1.2
2	2 & 7	2 & 4	1.5
4	4 & 5	4 & 6	1.6
6	6 & 3	6 & 8	1.5
8	8 & 1	8 & 7	1.2
7	7 & 2	7 & 5	1.5
5	5 & 4	5 & 3	1.6
3	3 & 6	3 & 1	1.5

Table 2.2: Measurement procedure for three-terminal contact resistance measurements within the well-quantized resistance plateau. The resistance values represent a practical example performed at 4.2 K **and** $B = 6$ T **in a system with non-coaxial cables.**

Graphene quantum Hall devices with an electron charge carrier density on the order of $1 \times 10^{-11}\,\mathrm{cm}^{-2}$ to $2 \times 10^{-11}\,\mathrm{cm}^{-2}$ typically have a room temperature sheet resistance around 6 kΩ to 7 kΩ. Table shows electrical resistances measured at room temperature (RT) as well as after the cooldown at 4.2 K. All resistances $R_{i,j} = U_{i,j}/I_{1,8}$ are four-terminal measurements with fixed current ports at pin 1 and pin 8 while the voltage ports are changed as given by the indices i and j. During the cooldown procedure, which is typically performed within 30 min, all contacts are shorted to each other as well as to the cryostat. A device is considered *good* if the sheet resistances ($R_{2,4}, R_{4,6}, R_{3,5}, R_{5,7}$) are similar within a few hundred ohms, and if the zero-field Hall resistances ($R_{2,3}, R_{4,5}, R_{6,7}$) are below 500 Ω. Note, that these figures are no sharp limits, but they rather reflect the margins (typical variation) of the electrical property values of high-quality graphene devices. However, devices with anomalies in the Hall and sheet resistances at zero magnetic (B) field indicated the presence of defect contacts or pronounced material inhomogeneities and thus should not be used for calibration or other purposes requiring ultimate accuracy.

2.3.2 Magnetotransport properties, Hall measurements

For the characterization of the magnetotransport properties a sweep of the magnetic flux density is performed while measuring the longitudinal resistivity ρ_{xx} (= $R_{3,7}/2$) and the Hall resistance R_{xy} (= $R_{4,5}$).

Figure shows results of a typical magnetotransport measurement on a graphene-based QHE device for magnetic flux densities up to 12 T, performed with a precision dc current source and a dc nano-voltmeter (alternatively, a lock-in amplifier can be used).

Depending on the charge carrier density, the start of the $i = 2$ plateau with $R_{xy} = R_K/2$

is found at magnetic flux densities as low as a few T. While the device in Figure shows a quantum Hall plateau starting at around 3 T (depending on the measurement temperature), the first point of accurate resistance quantization on the level of 1 n$\Omega\,\Omega^{-1}$ is found at a B-field that is typically 1 T to 2 T higher than the beginning of the plateau, as marked by the black square box.

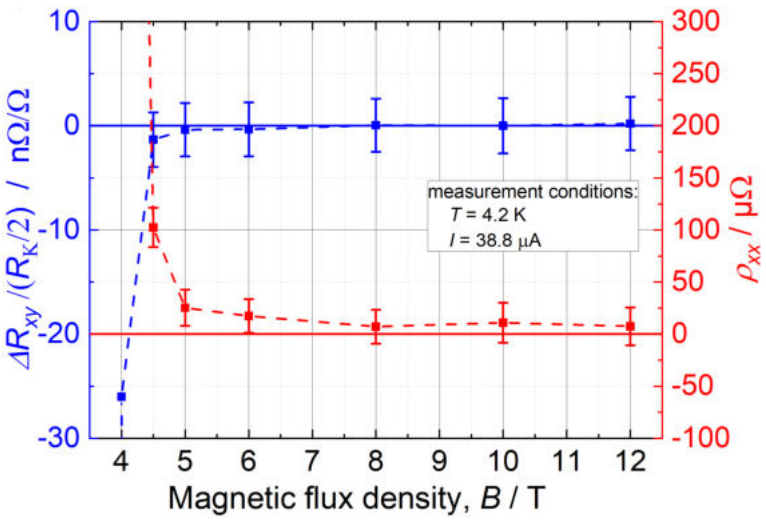
In addition to the shape and the onset of the resistance plateau, the Hall slope s_{Hall}, the sheet resistance R_{SH} as well as the charge carrier density $n = 1/(s_{\mathrm{Hall}} \cdot e)$ and the charge carrier mobility $\mu = 1/(n \cdot R_{\mathrm{SH}} \cdot e)$ are important properties that must be documented to judge the quality of the device in terms of QHR application. Typical electron densities of devices that start to be accurately quantized between 4 T and 6 T are $n = 1 \times 10^{11}\,\mathrm{cm}^{-2}$ to $n = 3 \times 10^{11}\,\mathrm{cm}^{-2}$ with electron mobilities $\mu \geq 5000\,\mathrm{cm}^2/(\mathrm{Vs})$.

A suitable way of pre-characterizing the start of the resistance plateau with higher precision is by measuring the longitudinal resistance with a precision current source and a nano-voltmeter at fixed *B*-field points. To suppress thermal voltages due to temperature gradients in cables and connectors the current reversal measurement technique is applied. Representative results that were obtained using such a relatively simple measurement setup (with a measurement uncertainty on the level $\leq 5\,\mathrm{m}\Omega$ are shown in Figure . In this way, the *B*-field range of "accurate resistance quantization" can be estimated and prominent anomalies in the longitudinal resistance can be identified.

With a $\Delta B = 0.25$ T between the individual ρ_{xx} measurements and with $I = 50\,\mu\mathrm{A}$ at $T = 4.2$ K, "accurate quantization" typically starts not before the 4th ρ_{xx} value drops to zero within the measurement uncertainty. However, even if no anomalies can be identified in the ρ_{xx} measurements, the estimation of the starting point of accurate quantization is just a preparation step to select an appropriate range of magnetic flux densities to be applied in the subsequent parts of the measurement protocol.

2.3.3 Contact resistance measurements

For detailed contact resistance investigations, the same measurement equipment as in is used in combination with in the current reversal measurement technique in a three-terminal configuration. The measurements are performed at a fixed *B*-field values within the margins of the resistance plateau where the longitudinal resistance is zero within the measurement (see Figure). The measurements in Table represent typical values that are obtained in a cryostat with cable resistances being of the order of 1 Ω. Since the three-terminal measurements also include cable resistances and any other resistances along the current-carrying line that is part of the voltage signal path, the true contact resistances are always lower than the measured values. After considering the included resistances of cables and connectors, the remaining contact resistance of a typical device fabricated by the techniques described in Section is below 1 Ω. However, also higher contact resistances below 10 Ω are acceptable [ ].



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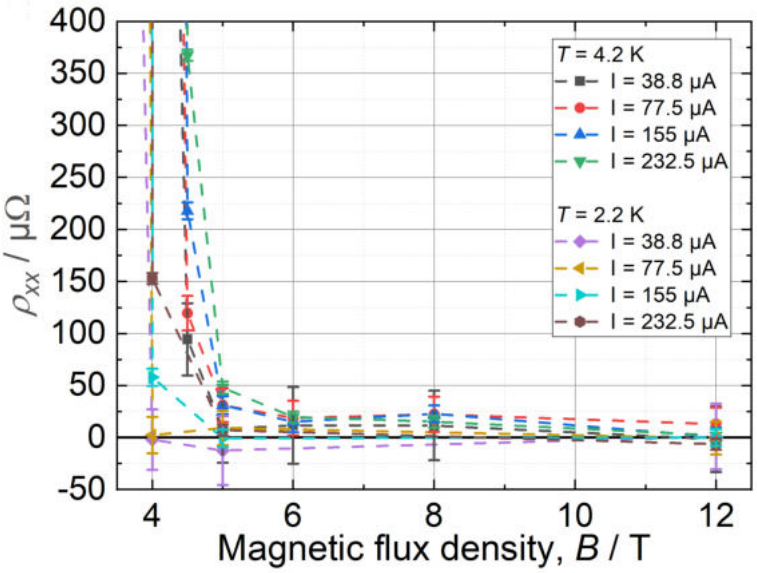


(b)

Figure 2.6: Precision measurements of the Hall and the longitudinal resistance. ( ) In the regions with the longitudinal resistivity being below $\rho_{xx} < 50\,\mu\Omega$, the deviation of the Hall resistance from $R_K/2$ is consistent with zero within the measurement uncertainty. ( ) Measurements at higher currents and different temperatures demonstrate the robustness of the QHR devices. As a result of the robustness, temperature and current variations are of limited use for the determination of the s-parameter within the resistance plateau. All uncertainty figures correspond to combined expanded uncertainties ($k = 2$).

B	ρ_{xx}	ΔR_{xy}	s-parameter
T	µΩ	µΩ	
3.5	$168\,499 \pm 306$	$-51\,608 \pm 445$	-0.310 ± 0.003
4.0	1602.3 ± 17.5	-335.8 ± 33.7	-0.21 ± 0.02
4.5	102.5 ± 18.8	-17.1 ± 33.8	-0.17 ± 0.30
5.0	25.3 ± 17.3	-4.8 ± 33.1	-0.19 ± 1.31
6.0	17.4 ± 16.1	-4.4 ± 33.3	-0.25 ± 1.90

Table 2.3: *s*-parameter values determined at the edge of the quantum Hall plateau. *s*-parameter values that were determined at the outer edge of the plateau may be used as an estimate for s-parameter values within the plateau. Inside the resistance plateau with ρ_{xx} values below 100 µΩ (in this example at B = 5 T), the uncertainty of the *s*-parameter becomes too large. Uncertainties figures are combined expanded uncertainties (k = 2).

2.3.4 Precision dc quantum Hall measurements

While any of the previous steps apply relatively simple measurement equipment, a device must finally be checked with high accuracy before it is used for calibration purposes. Suitable measurement systems are CCC (Cryogenic Current Comparator) or DCC (Direct Current Comparator) resistance bridges that allow determining the $R_K/2$ value with a type A uncertainty of less than 20 µΩ at a current of 50 µA. These systems can also be used to determine the longitudinal resistivity ρ_{xx} from the difference of two Hall resistances measured at orthogonally and diagonally aligned contact pairs.

2.3.5 Evaluation of the longitudinal resistivity and the *s*-parameter

The main quantization criterium is the vanishing of the longitudinal resistivity ρ_{xx} such that the admixing of the longitudinal contribution becomes negligible. Since in practice the longitudinal resistivity is often low, but non-zero, ρ_{xx} values below 50 µΩ are still acceptable if the *s*-parameter can be evaluated and if it is sufficiently small.

The *s*-parameter $s = \Delta R_{xy}/\rho_{xx}$ describes the dependency between R_{xy} and ρ_{xx}, where $\Delta R_{xy} = R_{xy} - (R_K/2))$ is the deviation of the measured Hall resistance.

In the case that $s \leq \pm 0.5$ or even $s \leq \pm 1$, the acceptable upper limit for ρ_{xx} is $\rho_{xx} \leq 25.8$ µΩ or $\rho_{xx} \leq 12.9$ µΩ respectively. Typically, graphene QHR devices can be operated under conditions where s and ρ_{xx} are within these limits. If a device is operated outside these limits, there is still the possibility to correct for the longitudinal contribution in a calculative way. Ideally, s is characterized at the same B-field value at which the device is operated later. This can be done by varying the temperature or current until a significant increase in the longitudinal resistivity and related changes in ΔR_{xy} are observed. However, due to the robustness of the QHE in graphene devices as well as due to parameter limits of individual cryostats and measurement systems, the *s*-parameter may alternatively be determined at the outer edge of the accurately

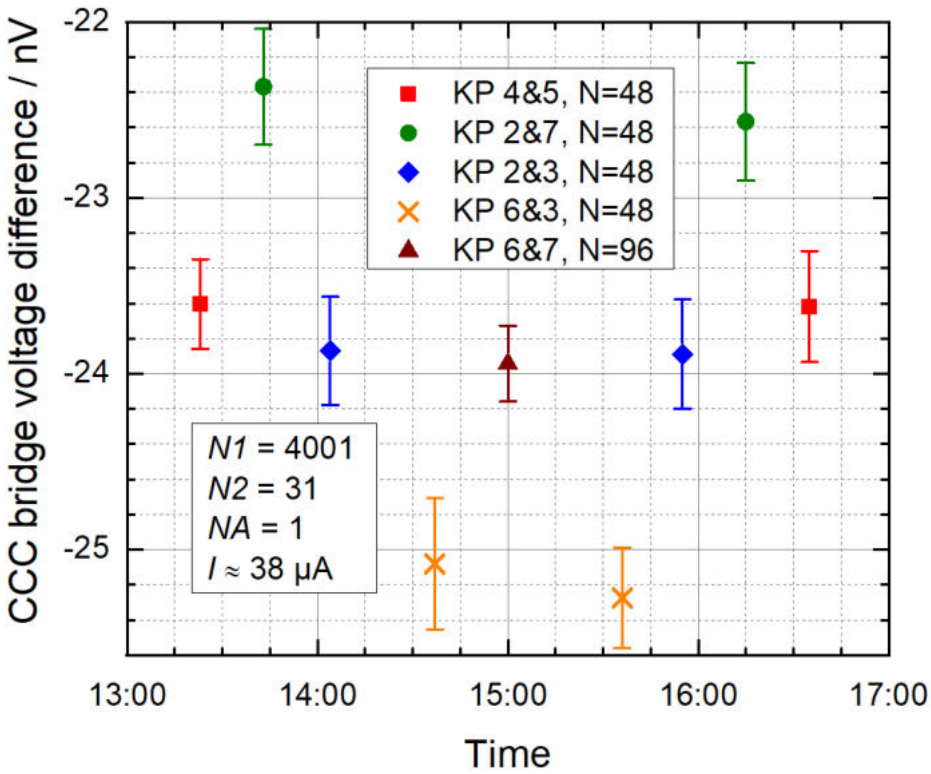


Figure 2.7: An example of the final precision device validation prior to calibration at a fixed $B = 6\,\mathrm{T}$ where the deviation from $R_K/2$ is expected to be below $1\,\mathrm{n\Omega\,\Omega^{-1}}$. In this final characterization step of the device, a series of CCC measurements is performed that involves all Hall contacts with the primary purpose to identify instabilities over time as well as inhomogeneities in the device properties. The quantity N describes the number of measurement cycles in the CCC measurement. The uncertainty figures are type A expanded measurement uncertainties ($k = 2$).

quantized resistance plateau where ρ_{xx} increases to a few 100 µΩ. When operating the device in this regime, one can determine the s-parameter with relatively low uncertainty figures by measuring ΔR_{xy} and ρ_{xx} while varying the temperature, current or magnetic field. An example of systems that allow temperature variations in only small margins are compact table-top cryostats that are being adopted by many NMI's [,]. In Table , the s-parameter and the related quantities ΔR_{xy}, ρ_{xx}, were determined by varying the magnetic field. Since within the resistance plateau with ρ_{xx} values below 100 µΩ the uncertainty of the s-parameter becomes too large, reliable s-parameter values are only obtained at the edge of the plateau. In the practical example, all evaluated s values are smaller than $s = \pm 0.5$. As a result, the upper limit for an acceptable longitudinal resistivity is $\rho_{xx} = 25.8\,\mu\Omega$ allow for precision resistance quantization with a deviation from $R_K/2$ below or equal to $1\,\mathrm{n\Omega\,\Omega^{-1}}$. As a result of the measured ρ_{xx} values in Figure , the lowest magnetic flux density point where the device can be expected to be sufficiently well-quantized is around $B = 6\,\mathrm{T}$.

2.3.6 Final precision device validation

Figure represents the final check before the device can be used for calibrations. This systematic series of CCC measurements involves all Hall contacts of the device. It is performed at the same fixed B-field that is intended to be later used for the calibration procedure in which the QHR will be the reference. The suitable B-field was selected where the deviation from $R_K/2$ is expected to be on the level of 1 n$\Omega\,\Omega^{-1}$, as described in Section . The main purpose of this measurement is to identify instabilities over time as well as inhomogeneities in the device properties for different combinations of contacts.

Before high accuracy measurements are performed, a pre-measurement is started for at least 1.5 h to ensure that the reference resistor reaches a stable temperature. Then a series of eight time-symmetrically arranged Hall measurements at five pairs of Hall contacts (see contact labels in Figure) are applied in the following order: 1. $\rightarrow$ 4&5, 2. $\rightarrow$ 2&7, 3. $\rightarrow$ 2&3, 4. $\rightarrow$ 6&3, 5. $\rightarrow$ 6&7, 7. $\rightarrow$ 2&7, 8. $\rightarrow$ 4&5.

While the contact pairs 2&7 and 6&3 are each diagonally aligned and are thus expected to display a significant longitudinal resistance component, the remaining contact pairs 4&5, 2&3 and 6&7 are orthogonally aligned Hall contacts. Therefore, in the case of a device where all areas of the device are equally quantized, the Hall resistances and corresponding bridge voltages at the Hall contact pairs 4&5, 2&3, and 6&7 should be the same within the expanded uncertainties. Since the remaining contact pairs 2&7 and 6&3 have a longitudinal component across the full accessible length of the device, they should deviate from the previous three pairs according to their longitudinal resistance component. The results of the practical example, plotted in Figure , represent a typical pattern of such a measurement series. For a known reference resistor value, winding ratio, and compensation network configuration, the value of the second resistor (device under test) can be determined from the bridge voltage difference [ ].

In the case of instabilities in the QHR device properties or in the reference resistor, the measurement results can be asymmetrically distributed, have different noise figures and may not be reproducible over time within the expanded uncertainties. To be able to identify instabilities caused by the reference resistor, it is recommended to continuously record the ambient pressure and resistor temperature during the measurement, primarily if dependencies are known or suspected. The final dc calibration procedure in which the QHR is used as a reference is typically realized by using the center Hall contact pair 4&5 after the device passes the complete characterization procedure discussed in this document.

3 Cryogenic environment

3.1 Temperature and field requirements

Two of the major advantages of graphene based QHE devices is that the requirements concerning temperature and magnetic field can be reduced compared to devices based on GaAs. The latter need typical magnetic field strengths of approx. 8 T to 10 T. In contrast to this, graphene-based devices can be tuned to have good quantisation starting at a magnetic field strength of about 3 T. Even though lower fields are possible there is no big advantage to further reduce this operating range. On the one hand this is achieved with lowering the carrier density of the device into regions where quantization starts to get unstable. On the other hand, superconducting magnets will not change significantly in price and handling under a field of 7 T. The temperature requirements are also relaxed if a graphene based QHE devices is used. There is no urgent need to operate the device at temperature below 4.2 K (boiling point of Helium). Although a GaAs based QHE device can be operated at 4.2 K [ ], the range of the magnetic field where the device shows a quantized Hall resistance is significantly reduced. Lowering the temperature below 4.2 K will cause some more effort (Lambda cooler, 1 K pot, VTI,. . .) but will reduce the thermal noise (Johnson noise) of the QHR.

3.2 Shielding and coaxiality

In the DC regime the quantum Hall resistance is defined as a four-terminal (4T) resistance [, Sec. 2.1]. If the 4T definition is applied (no current is drawn from the voltage terminals by the measurement setup) the cable errors are due to the wiring parasitic conductances, which can be made negligible with adequate isolation.

In the AC regime a proper *impedance definition* becomes essential. Most accurate impedance definition rely on the *coaxial terminal-pair* concept [, Sec. 2.2.1]. The QHE device must be shielded, each terminal becomes a coaxial connection to the outside, and the measurement circuit must take care of the coaxiality condition (that is, in each coaxial pair the electrical currents in the inner and outer conductor are equal and opposite).

The coaxiality condition requires that all coaxial lines must be completely isolated from the cryostat, and be terminated by isolated coaxial connectors. The shields (outer connector) of all coaxial lines connecting the QHR, should be joint at a single point at or close to the sample holder. Such configuration is not standard (typical commercially-available coaxial lines are unisolated RF ones) and may pose thermalization problems in dry cryostats.

3.3 Cryo probes and cabling

In order to have high flexibility, QHE devices are typically installed into so called cryo probes or dip sticks. They are set up by a sample holder or carrier which is connected to a thin walled stainless steel tube with a connector box on top. The tube can be moved

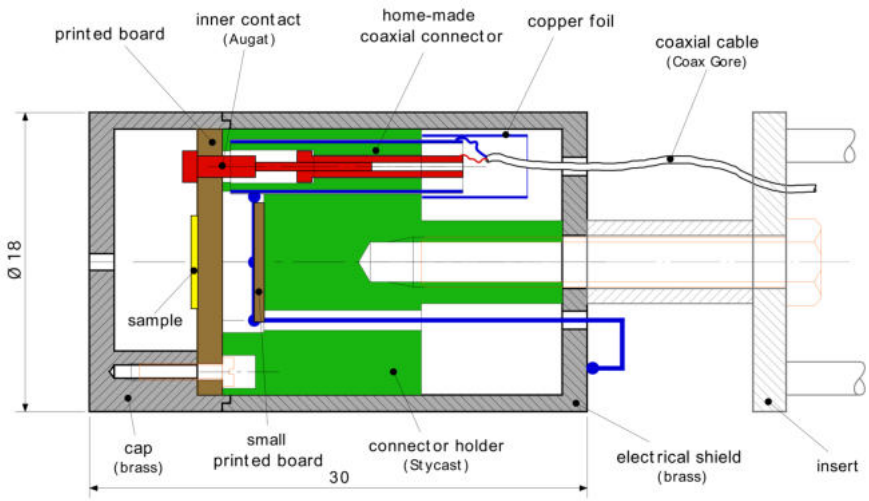


Figure 3.1: Schematic diagram of the EUROMET sample holder.

into the cryostat through a sliding seal. By this the loss of helium is minimized. To minimize the heat load to the cryogenic system the material used needs to have good mechanical properties and low thermal conductance as for example stainless steel or fiberglass reinforced plastics.

Using materials with low thermal conductivity for the needed coaxial cables contradicts the need of low electrical resistance. Since at least six coaxial lines are needed to connect one quantum Hall device, the heat load to the cryo system can be quite large when using standard coaxial cables. The introduced heat is already reduced when (sub) miniature coaxial cables are used. This is a possible solution e.g. for operation in a liquid helium Dewar in combination with a recovery system. Using such a coaxial cable with an characteristic impedance of 75 Ω will result in a cabling with low resistance and capacitance. Some care has to be taken to the material of the inner and outer conductor since pure copper can get brittle at cryogenic temperatures. This can be avoided using copper alloys or copper / steel compounds.

For systems operated below liquid helium temperature (lambda cooler, 1 K pot, ^3He systems, ...) or closed loop cryo cooler, the amount of heat introduced to the system needs to be further reduced. This is done by using e.g. brass, steel or stainless steel for the outer conductor and in some cases also for the inner conductor. This results in coaxial cables with low thermal conductance but increases the electric resistance in the range of a few $\Omega\,\mathrm{m}^{-1}$.

3.4 Sample holder

AC measurements ask for a definition of the quantum Hall device as a terminal-pair impedance standard. In order to achieve this, the normal QHR wiring exploited in dc (one conductor per contact) must be replaced by coaxial wiring. The sample holder must be designed to carry on the coaxial structure of the wiring as close as possible to

Figure 3.2: The EUROMET holder printed circuit board where the QHE sample is bonded.

the device. With the aforementioned connection point for all outer conductors.

3.4.1 EUROMET holder

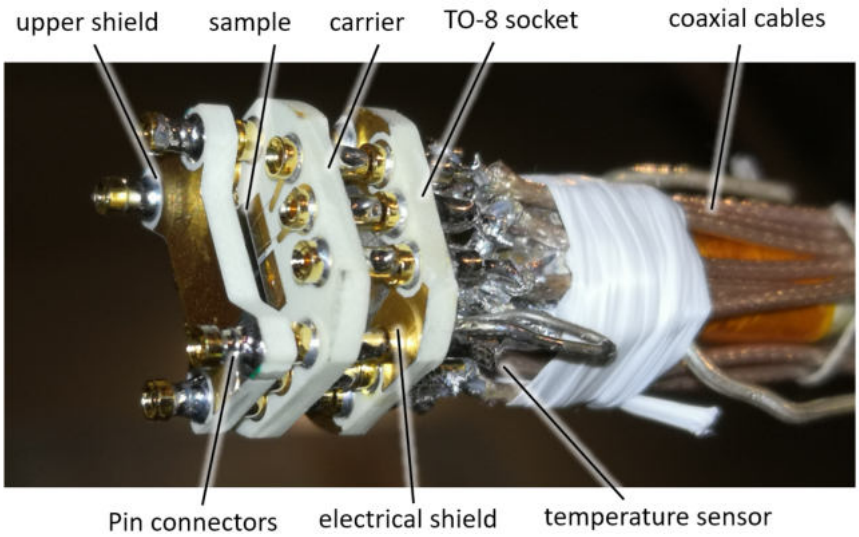
The EUROMET holder was developed by the Swiss Federal Office of Metrology and Accreditation (METAS) in the framework of an EUROMET project [ ]. A schematic diagram of the holder is shown in Figure , and a picture of the socket is shown in Figure .

3.4.2 TO-8 shielded holder

The TO-8 holder is adapted from the 12-pin version of the standardized TO-8 (*transistor outline*) metal semiconductor package. It was developed by PTB and CMI [ ] and implements the double-shielding technique of [ ] .

[2] A standard PCB material such FR4 was used. The introduction of modern materials, dedicated for high frequency applications and space technology, enable metrologists to design the holder with lower thermal expansion, conductivity, dissipation factor and lower dielectric constant, leading to lowering of several parasitic effects.

(a)



(b)

Figure 3.3: TO-8 holder, consisting of two PCBs with splitted shields. ( ) disassembled. ( ) with the QHR device mounted.

4 Digital impedance bridges

The comparison of two impedance standards can be performed with an *impedance bridge*, an instrument based on a measuring method invented by Christie [ ] and made popular by Wheatstone [ ]. Figure shows the principle schematic diagram of a generic impedance bridge. The two impedance standards Z_1 and Z_2 under comparison are connected in series. When a current I flows through the impedances, two voltages $E_1 = Z_1 I$ and $E_2 = Z_2 I$ develop across Z_1 and Z_2. At equilibrium ($V_D = 0, I_D = 0$) The impedance ratio is related to the voltage ratio by the equation

$$\frac{Z_1}{Z_2} = -\frac{E_1}{E_2}. \tag{4.1}$$

In the Wheatstone bridge voltages E_1 and E_2 are provided by a single source, using a resistive divider.

In transformer bridges [,] the voltages E_1 and E_2 are generated by an inductive voltage divider; the nominal E_1/E_2 ratio is determined (and very close numerically) to the turns ratio, and can be calibrated to a very high accuracy. Transformer bridges allow extremely accurate ratio measurements, reaching uncertainties of parts in 10^9 [ ], but are large and complex electrical networks, can measure only impedance ratios very close to the limited set of nominal ratios fixed by construction, and their frequency bandwidth is limited.

4.1 Digital bridges

Digital bridges are impedance bridges that make extensive use of mixed-signal electronic devices, either analog-to-digital converters (ADC) or digital-to-analog converters (DAC) and have digital representations of the voltage and current waveforms in the bridge mesh.

The concept of digital bridges dates back to decades ago [, ,], but only more recently the performances of ADCs and DACs improved to underpin the implementation

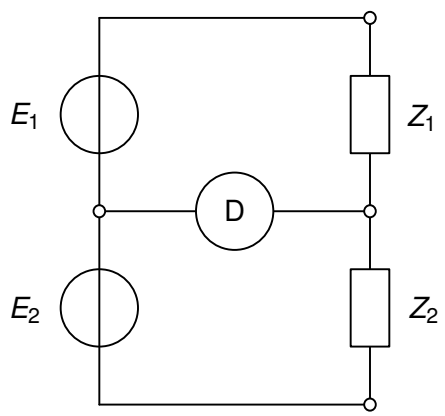


Figure 4.1: Principle schematics of an impedance bridge.

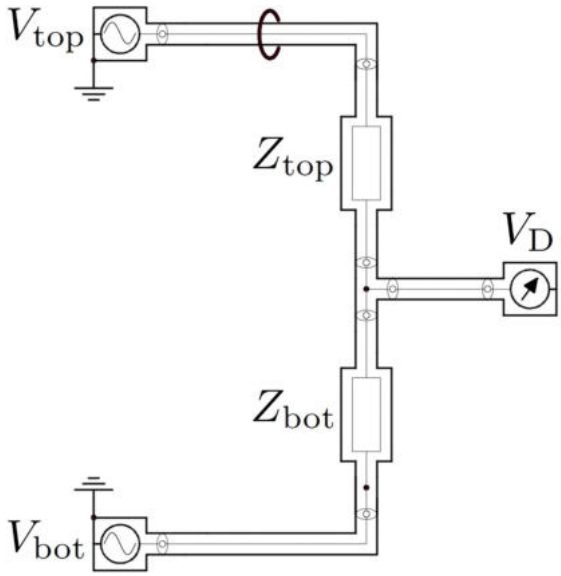


Figure 4.2: Simple schematic of a two terminal-pair electronic source bridge. The amplitudes and phases of the sources V_{top} and V_{bot} are adjusted to obtain $V_{\mathrm{D}} = 0$ (the main balance), then $Z_{\mathrm{bot}}/Z_{\mathrm{top}} = -V_{\mathrm{bot}}/V_{\mathrm{top}}$.

of primary impedance bridges. With respect to transformer impedance bridges, digital bridges have simpler electrical networks, are less expensive and easier to automate.

4.2 Digitally-assisted bridges

Digitally-assisted bridges [, , ,] are digital bridges that employ electromagnetic components, transformers and inductive voltage dividers, as ratio standards. The bridge is energized by a large-amplitude signal; a number of auxiliary signals (voltages and currents) of smaller amplitude are employed to achieve the main equilibrium (that gives the bridge reading) and the auxiliary equilibria necessary to set the impedance standards in the proper defining conditions. The main and auxiliary signals are generated by digital synthesis with DACs.

The accuracy of digitally-assisted bridges is guaranteed by the electromagnetic ratio standard, hence the bridge performances - and the corresponding limitations (fixed set of ratios and frequencies available) are similar to those of the traditional transformer bridges. The digital source employed must guarantee a limited harmonic content and noise, but the requirements on the accuracy and stability are moderate (in the 10^{-4} range).

An implementation with digitally-assisted bridges of capacitance realisation from the dc quantum Hall effect is presently operating [ ].

4.3 Electronic fully-digital bridges

Electronic fully-digital bridges [,] are voltage ratio bidges where the bridge volt-

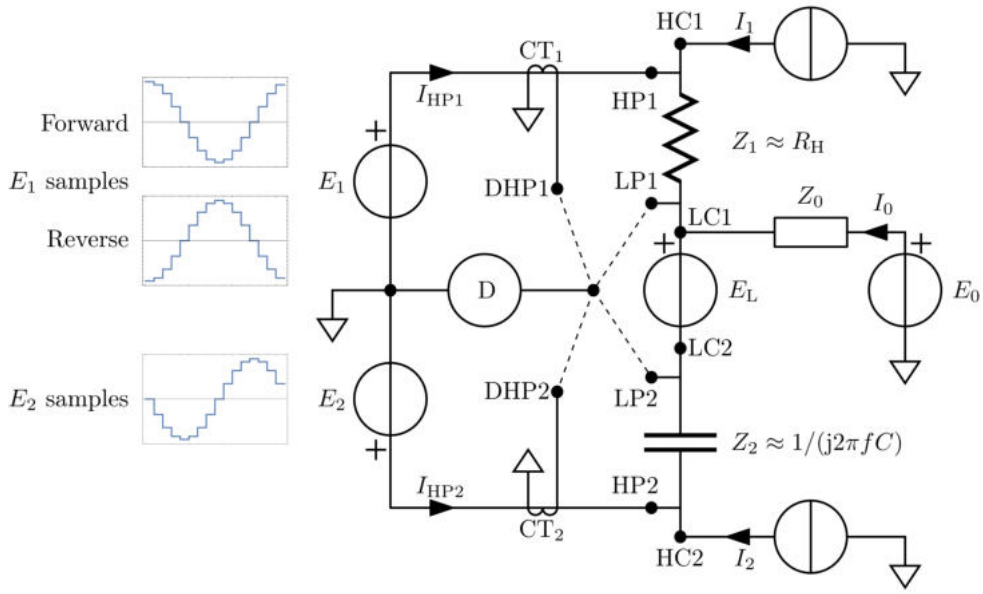


Figure 4.3: Simplified principle schematic of a fully-digital electronic bridge suitable for a direct $R - C$ comparison between standards defined as four terminal-pair impedances. $Z_1 = R_H$ and $Z_2 = 1/(j\omega C)$ are the impedances under comparison; ω is the bridge operating frequency, chosen so that $\omega RC = 1$; E_1 and E_2 are the main bridge voltages; I_1 and I_2 are the current sources balancing I_{HP1} and I_{HP2}; E_L is the voltage source balancing the difference $V_{LP1} - V_{LP2}$; CT1 and CT2 are current transformers measuring the currents I_{HP1} and I_{HP2}, respectively; the voltage source E_0 and the impedance Z_0 constitute an auxiliary injection arm to fine-tune the bridge balance; and D is a synchronous detector that can be connected, in turn, to the detection terminals LP1, LP2, DHP1 and DHP2. The diagrams on the left represent example waveform samples: the samples of E_1 are changed in sign between the forward and reverse configurations; the samples of E_2 are instead kept fixed. After Ref. [ ], courtesy of the authors.

age ratio standard is based on the linearity properties of DACs (or ADCs). The digital source employed must therefore comply with strict requirements of accuracy and stability. Since sampling and digital processing allow to generate (or measure) arbitrary voltage ratios, frequencies and phase differences, and frequencies, fully-digital bridges overcome the intrinsic limitations of transformer bridges, either traditional or digitally-assisted.

A simple implementation of a two terminal-pair digital bridge [ ] is shown in Figure . Two digital voltage sources supply the measuring current to the two impedances standards, which are connected in series. The amplitude and phase of one of the sources is adjusted [ ] until the voltage measured at the node between the two impedances is set to zero ($V_D = 0$). The impedance ratio determination is completely relying on the the agreement between the settings of the generators and the actual voltages applied to the impedances.

It is possible to perform two different measurements by reversing the top and bottom

standards. Averaging the readings obtained in the two configurations allows for a significant reduction of the error related to a possible asymmetry between the two channels of the source [,]. The remaining uncertainty components are related to the nonlinearities[ ], gain and phase stability [,] and loading effect of the parasitic stray admittances [ ].

Some published implementations of digital bridges still rely on inductive voltage dividers for the voltage ratio adjustment [, ,], but they can be anyway used to perform comparisons of any kind of impedances, like *R*-*C* comparisons [,] or *L*-*C* comparisons [ ]. Four terminal-pair versions of digital bridges have also been successfully developed [, , ,].

The operating frequency range of these bridges starts from a few tens of Hz [ ] or even lower [ ] to 10 kHz [ ]. The uncertainty on the generated voltage ratio ranges from a few parts in 10^5 [ ] down to less than 1 part in 10^6 [,].

Specialized fully-digital bridges suitable for a direct realisation of the farad in terms of the quantized Hall resistance can be conceived. On example of such a bridge is given in [ ]; Figure shows its working principle. The restriction of the operational parameters to the condition $\omega RC = 1$ minimizes the contribution of DAC nonlinearty to the bridge uncertainty.

4.4 Josephson bridges

The accuracy limitation of electronic DACs employed in a fully-digital bridge can be overcome by employing Josephson DACs. These are composed of integrated circuits including thousands of Josephson junctions in series, called Josephson arrays, driven by room-temperature electronics.

The two main types of Josephson DACs available give rise to two different waveform synthesis methods:

Programmable Josephson Voltage Generators (PJVS) work like binary-weighed DACs: the array is divided into segments composed of a binary sequence (1, 2, 4, 8, . . .) of junctions in series. The segment can generate, when driven by a proper dc bias current, a positive, zero or negative quantized voltage. The voltage is proportional to the number of junctions in each segment.

In static bias conditions of bias the output of a binary array is a quantized voltage

$$V = b\frac{f}{K_J},$$

where b is an integer dependent on the code selected to drive the binary segments, f is the frequency of the biasing microwave, and K_J is the Josephson constant.

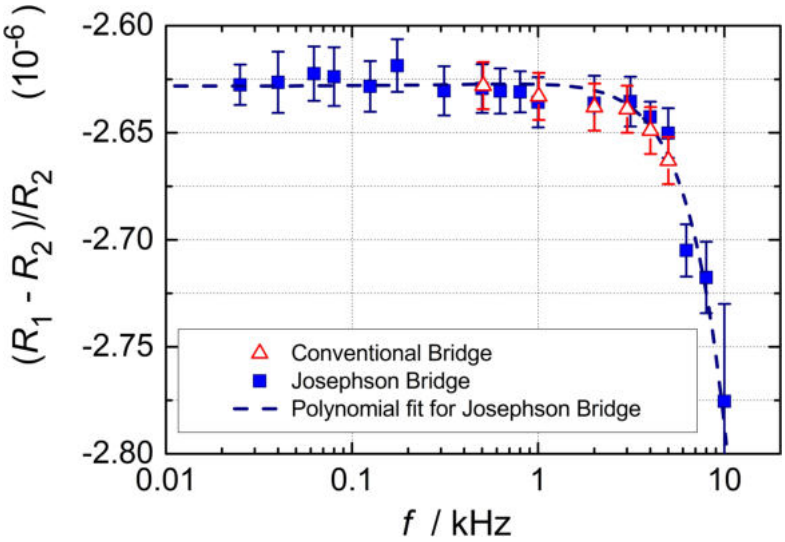


Figure 4.4: Measurement of the relative difference between two 10 kΩ **resistors versus frequency, performed using traditional transformer based bridge and the 2TP PJVS based bridge (after [ ], courtesy J. Lee).**

The limitations of binary Josepshon array DACs are the resolution in bits, typically 10 to 16, and thus which in turn is dependent by the number of integrated Josephson junctions, and the settling time. The latter limits the maximum operating frequency to achieve quantum performance to the kHz at most. Josephson voltage ratio bridges with relative accuracies in the 10^{-8} range have been published [ ].

Josephson array waveform synthesizers (JAWS) are based on arrays of N junctions in series, driven by a sequence of microwave pulses [ ]. The array transform each driving pulse in a corresponding voltage impulse of quantized amplitude $V\mathrm{d}t = NK_{\mathrm{J}}^{-1}$. The rf pulses are rejected by LP filters, and a voltage $V = pNK_{\mathrm{J}}^{-1}$ appears at the output, where p is the pulse rate. When operating the array with positive and negative pulses and a pulse sequence where the pulse rate varies in time, arbitrary wave forms can be generated.

Pulse-driven array DACs are typically drive by pulse pattern generators with generation rates in the GHz range, and allow to generate high-resolution sinewaves with frequencies up the MHz range. The major limitation is related to the maximum output voltage, although recently multi-chip generators with $>$ 1 V output range [ ] have been achieved.

4.4.1 Programmable Josephson Bridges

Programmable Josephson Voltage Standards (PJVS) generate stepwise approximated ac waveforms, that can be used to generate accurate voltage ratios. The first bridge based on PJVS synthesized voltages, a two terminal-pair bridge, was demonstrated in 2010 [ ]. The bridge was employed to compare two 10 kΩ resistances, reaching an accuracy comparable to that of traditional transformer-based bridges. Figure

shows that the agreement between the measurements performed with a traditional 2TP transformer bridge and the PJVS bridge is around a few parts in 10^8, well within the measurement uncertainties. One can appreciate that thePJVS bridge measurements were performed over a wider frequency range (from 25 Hz to 10 kHz). This 2TP bridge was also used to compare two 100 pF capacitance standards [ ] with a relative accuracy of 2×10^{-8} at 1 kHz.

The bridge was then employed, with a ratio of 10:1, to compare two capacitors (10 pF to 100 pF) in the frequency range 25 Hz and 20 kHz [ ]. The uncertainty was 3×10^{-7}, with full agreement with traditional methods for frequencies around 1 kHz. The bridge was equipped with 10 V arrays [ ], which reduced the signal to noise ratio. Unfortunately, at 10 V, the helium consumption increased to a level which is quoted as "prohibitive" in [ ].

The 2TP programmable Josephson bridge was then upgraded to a 4TP version, in order to compare low-valued impedances. The first set of measurements performed was the comparison of two 10 kΩ resistance standards over the frequency range 20 Hz to 10 kHz [ ]. The outcome of the measurement show a systematic offset of 6×10^{-8}, which is larger than the (type A) measurement uncertainty of a few parts in 10^9. Moreover, the frequency dependence shows the wrong curvature above 3 kHz. Such behavior was tracked back to the large harmonic content of the PJVS waveform, which is difficult to cope with in this type of bridge configuration. The 4TP bridge was further refined recently [ ], but the improvement was not considered satisfactory. Quoting [ ]: "These results clearly show that further ideas are needed to setup a 4TP Josephson impedance bridge based on PJVS".

The 2TP bridge performance was also tested in the measurement of two unlike impedances, a 12.9 kΩ resistor versus a 10 nF capacitor at the frequency of 1233 Hz [ ]. The type A uncertainty was 1.5×10^{-6}; a comparison with a traditional measurement agrees within such uncertainty. Again, the limitation of the system was due to the large harmonic content of the PJVS waveforms.

In summary, the Josephson impedance bridge based on a PJVS has certainly played an relevant role in impedance metrology research, by showing that Josephson arrays can be used in impedance bridges to achieve competitive uncertainties. However, the large harmonic content of the PJVS waveforms, intrinsic to the working principle of the PJVS, considerably limits the application area of this type of bridges. In this sense the Dual Josephson Impedance Bridge, based on JAWS, represents a much more promising approach.

4.4.2 Dual Josephson Impedance Bridge (DJIB)

Josephson arbitrary waveform synthesizers (JAWS) are digital-to-analog converters that generate quantum-accurate distortion-free voltage wave forms over frequencies in the Hz to MHz frequency range. By combining and synchronizing two such JAWS systems enables generation of quantum-accurate, calculable voltages with arbitrary ratios

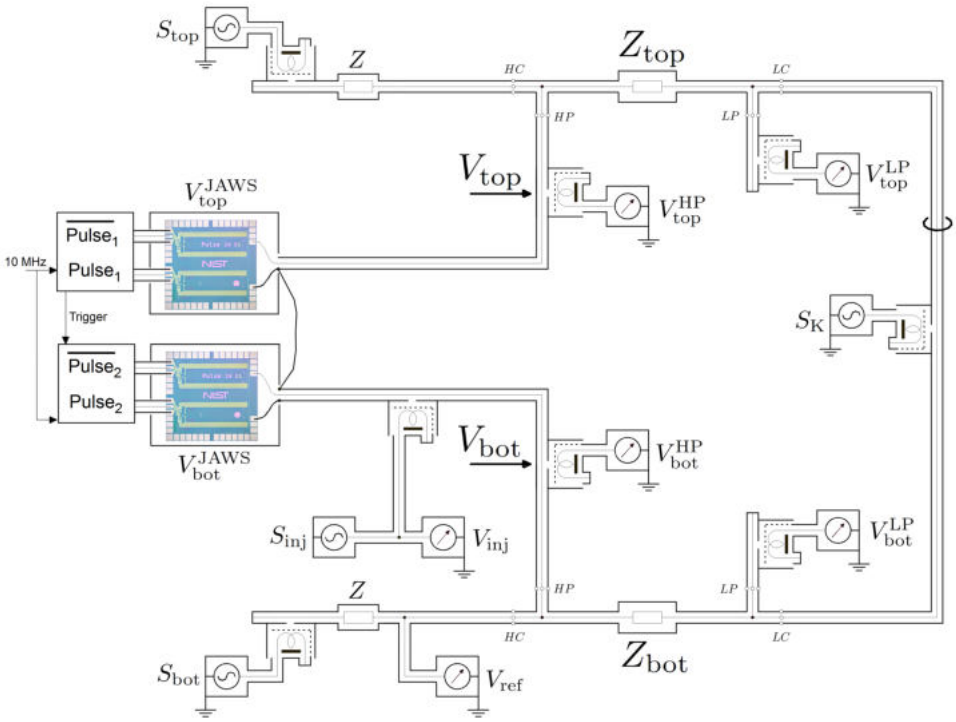


Figure 4.5: Simplified coaxial schematic of a four-terminal pair DJIB bridge circuit. The bridge by setting V_{top}^{HP}, V_{bot}^{HP}, V_{top}^{LP} and V_{bot}^{LP} to zero; this is achieved by adjusting the amplitude and the phase of the bottom JAWS source, as well as the voltages S_{top}, S_{bot}, and S_K, which give the four-terminal-pair definition of the two impedance standards. In this condition, the impedance ratio Z_{bot}/Z_{top} is equal to the voltage ratio $-V_{bot}/V_{top}$. The difference between the DJIB and the digital assisted bridge [ ] is that the accurate and stable voltage ratio is generated using two JAWS systems instead of a ratio transformer. The full description of the bridge can be found in [ ].

and arbitrary relative phase angles.

The two voltage sources required by a DJIB are provided by two independent pulse-driven JAWS systems operated in either a single or two separate dewars of liquid helium. The setup used at METAS each JAWS chip (NIST) include four arrays of 12800 double-stacked Josephson junctions (JJs) each, connected in series by on-chip superconducting traces to produce a voltage of 1 V. The PTB system, in a typical configurations, employs two independent JJ arrays having up to 12000 JJ. The clock signals of the JAWS system and of the other components of the DJIB are all locked to a 10 MHz reference frequency signal. The phase matching of the two JAWS is ensured because the two pulse generators share a single 14.4 GHz clock. More details for both systems are given in [,]. The performances of the DJIB relies on the stability, linearity, and tunability of the two JAWS systems.

Figure shows a simplified schematic of the DJIB, which was developed at METAS to perform high accuracy comparisons of the four terminal-pair impedances Z_{top} and Z_{bot}. The working principle of the DJIB is similar to that of the digitally assisted bridge (DAB) described in [ ] and is given in [ ]. The principal difference between the two bridges is that in the DJIB the accurate and stable voltage ratio is generated using two JAWS sources, whereas in the DAB it is achieved with a ratio transformer. Therefore, in the DJIB the amplitudes and the phases of $V_{\mathrm{top}}^{\mathrm{JAWS}}$ and $V_{\mathrm{bot}}^{\mathrm{JAWS}}$ can be independently set to any desired value, hence making the comparison of arbitrary impedances possible.

A first test performed with the DJIB consisted in the measurement of the relative frequency dependence of two resistance standards, $Z_{12\mathrm{k}9}^{\mathrm{B}}$ and $Z_{12\mathrm{k}9}^{\mathrm{A}}$ (taken as a reference). The lower part of figure displays the outcome of the measurements, performed between 1 kHz and 20 kHz at the voltage 1 V rms. The points give the values measured using the DJIB, the solid line is a quadratic fit to the measurements performed with the DAB.

Figure , upper part, gives the difference between the values measured with the DJIB and those measured with the DAB are shown. The gray zone represents the combined (1-σ) uncertainty of the DAB [ ], while the bars correspond solely to the Type A uncertainties of the DJIB measurements. The DJIB measurements were repeated a number of times over a few days; corrections for the small drift in the dc resistance were applied. At these particular frequencies, the residual spread of the results is slightly larger than the Type A uncertainty. Such deviations indicates that some systematic effects remain to be investigated. Nevertheless, there is an agreement between the results obtained with the DJIB and the DAB better than 0.1 $\mu\Omega/\Omega$, confirming the potential of the JAWS sources when implemented in an impedance bridge.

In addition, consistency check to compare different stable unknown impedance standards were performed. Figure shows the residuals $|\Delta|$, smaller than 0.5 $\mu\Omega\,\Omega^{-1}$, which is ten times better than the results obtained using the sampling bridge.

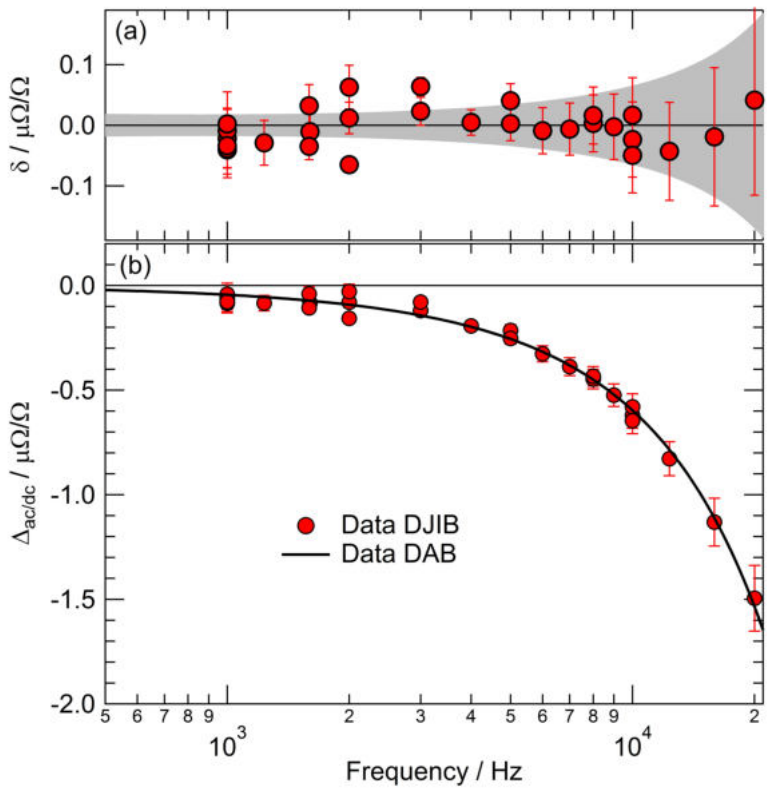


Figure 4.6: The bottom plot (b) shows the frequency dependence, $\Delta_{ac/dc}$, of the resistance Z^{B}_{12k9} measured with the DJIB (symbols) and with the DAB (solid line). The top plot (a) shows the difference δ between the DJIB and DAB results. The errors bars correspond to the Type A uncertainty of the DJIB measurement. The gray zone represents the combined (k=1) uncertainties for the measurements made with the DAB [ ].

Another four terminal-pair Josephson impedance brige, developed at PTB, is shown in Figure and described in full details in [ ]. The two impedances to be compared are biased by the voltages U_1 and U_2 provided by two JJA. Both arrays are driven by a pulse pattern generator with has two independent but synchronized memories sharing the same rf clock. The phase angle between U_1 and U_2 can be varied by changing the delay between both memories with a maximum resolution of 250 fs. To balance the bridge, one of the voltage amplitudes and the phase angle between both voltages are adjusted until detector D is minimized. For a quadrature bridge with a resistance R and a capacitance C, the real part of the bridge equation becomes $\omega RC = U_1/U_2$ with a 90 degree phase angle between U_1 and U_2.

In Figure , the DJIB is set up with a QHR and a 10 nF capacitance standard, resulting in a nominal signal frequency of 1233 HzṪo eliminate the influence of the contact and the lead resistance, the QHR is connected to the bridge using a triple series connection [ ].

The quantum based voltage generated by each JJA is affected by the output cable

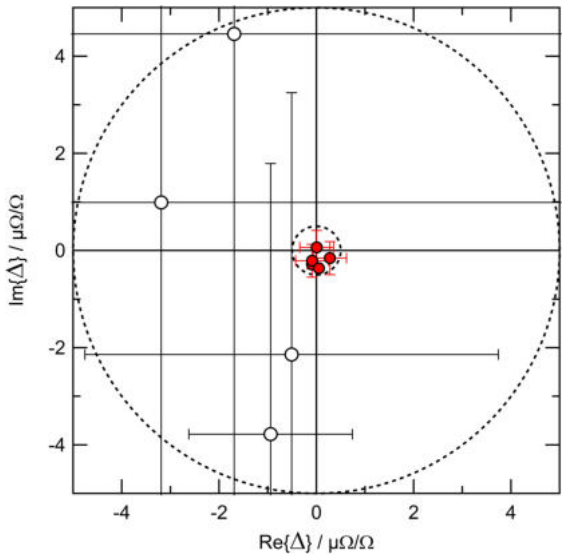


Figure 4.7: Residuals, $|\Delta|$, of the consistency checks for the sampling bridge [ ] (open circles) and the DJIB [ ] (solid circles). Dashed line circles correspond to $|\Delta| < 5\ \mu\Omega/\Omega$ and $|\Delta| < 0.5\ \mu\Omega/\Omega$.

impedances [,] which are matched to mitigate their influence. This influence is further reduced by interchanging the position of the measured impedances inside the bridge setup at the level of the current detection D_1 and D_2 (see Figure).

With this universal impedance bridge a large variety of like and unlike impedacnes ca be compared with low uncertaintes and a measurement noise which is as lo as expected by theory.

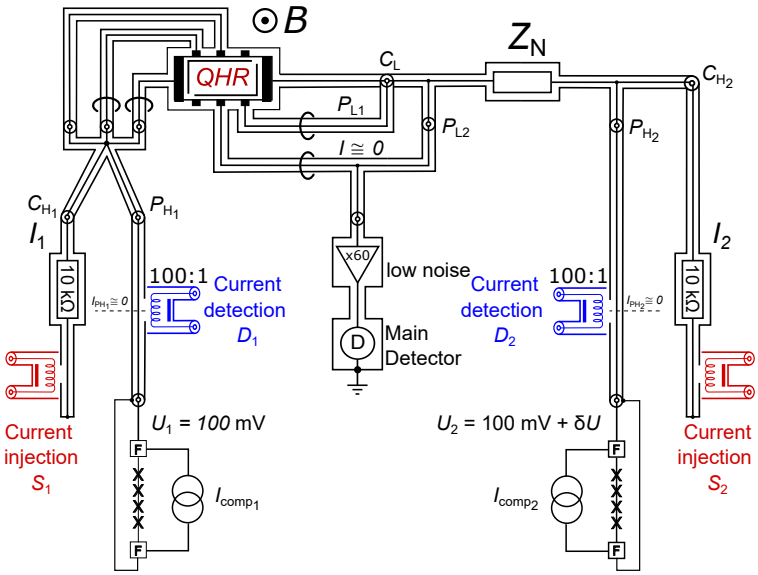


Figure 4.8: Schematic overview of the measurement setup for the quadrature measurements with a 10 nF capacitance standard and a QHR (after [ ], courtesy S. Bauer).

5 Maintaining a capacitance scale with the AC QHE in graphene

5.1 Calibration and traceability

The concepts of calibration and traceability are defined in the *International Vocabulary of Metrology* [ ], here quoted:

2.39 Calibration operation that, under specified conditions, in a first step, establishes a relation between the quantity values with measurement uncertainties provided by measurement standards and corresponding indications with associated measurement uncertainties and, in a second step, uses this information to establish a relation for obtaining a measurement result from an indication.

2.41 Metrological traceability property of a measurement result whereby the result can be related to a reference through a documented unbroken chain of calibrations, each contributing to the measurement uncertainty.

(NOTE 2) Metrological traceability requires an established calibration hierarchy.

(NOTE 3) Specification of the reference must include the time at which this reference was used in establishing the calibration hierarchy, along with any other relevant metrological information about the reference, such as when the first calibration in the calibration hierarchy was performed.

5.2 Traceability chains

In primary electrical impedance metrology a traceability chain starts with the realisation of the ohm from the quantum Hall effect.

The chain then logically proceeds by comparisons performed with dedicated measurement setups, until the calibration of a set of impedances (maintained standard) of very high stability is achieved.

The typical target of a capacitance traceability chain is the calibration of capacitors of 10 pF or 100 pF nominal values, since these are the most stable available and hence the capacitance unit can be maintained between successive calibration at the highest accuracy level.

5.3 Traditional traceability chain

An example of a traditional traceability chain from the (dc) quantum Hall effect to 10 pF capacitance is shown in Figure . Others can be found in [, ,].

In Figure the DC quantum Hall resistance is employed to calibrate in dc, using a cryogenic current comparator (CCC), an ac-dc resistor of appropriate value (in this case

[3] The ordering in time of the comparisons can be different from the logical ordering implied in the traceability chain.

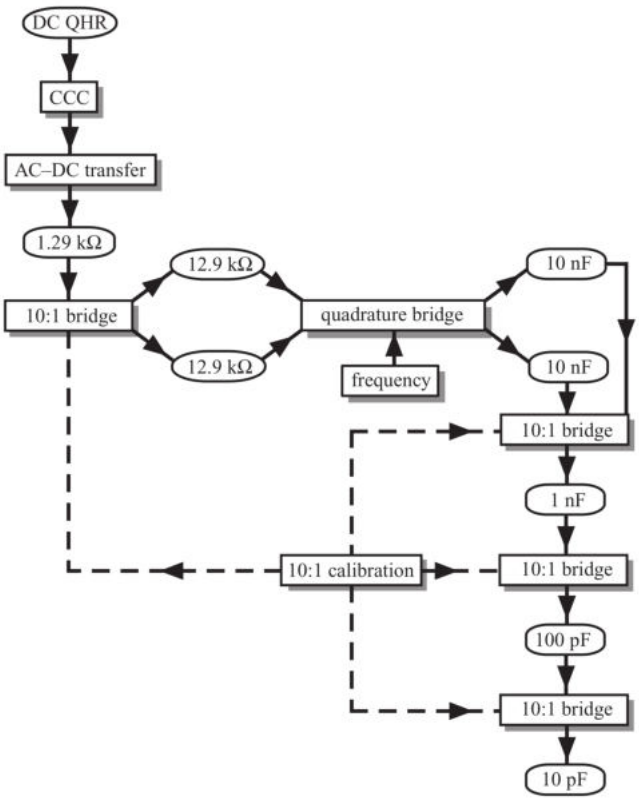


Figure 5.1: Traceability chain for the realisation of capacitance (at 10 pF – 100 pF **level) from the dc quantum Hall effect. After Ref. [Sec. 6.37][ ]**

1.29 kΩ of calculable frequency performance [, ,]. A resistance transformer ratio bridge is employed to scale up in the ac regime the resistance, calibrating two resistance standards R_1 and R_2 (in this case of 12.9 kΩ. A quadrature bridge can calibrate the product of two capacitors C_1 and C_2 under the condition $\omega^2 R_1 R_2 C_1 C_2 = 1$; in this example, two 10 nF capacitors at the frequency of about 1233 Hz. Further scaling with a capacitance transformer ratio bridge allows to realise a capacitance scale down to 10 pF.

5.3.1 GIQS traceability chains

The GIQS project results allow to consideraby simplify the traditional traceability chain of Figure via three routes:

ACQHE The direct exploitation of the quantum Hall resistance in the AC regime (AC-QHR) allows to avoid completely the need of a calculable resistor to perform the AC-DC resistance transfer [, ,]. The calculable resistors and the associated DC measurements can be avoided;

$R - C$ **transfer** The most complex step of the traditional traceability chain is the $R - C$ comparison, which asks for four standards. As described in Section the $R - C$

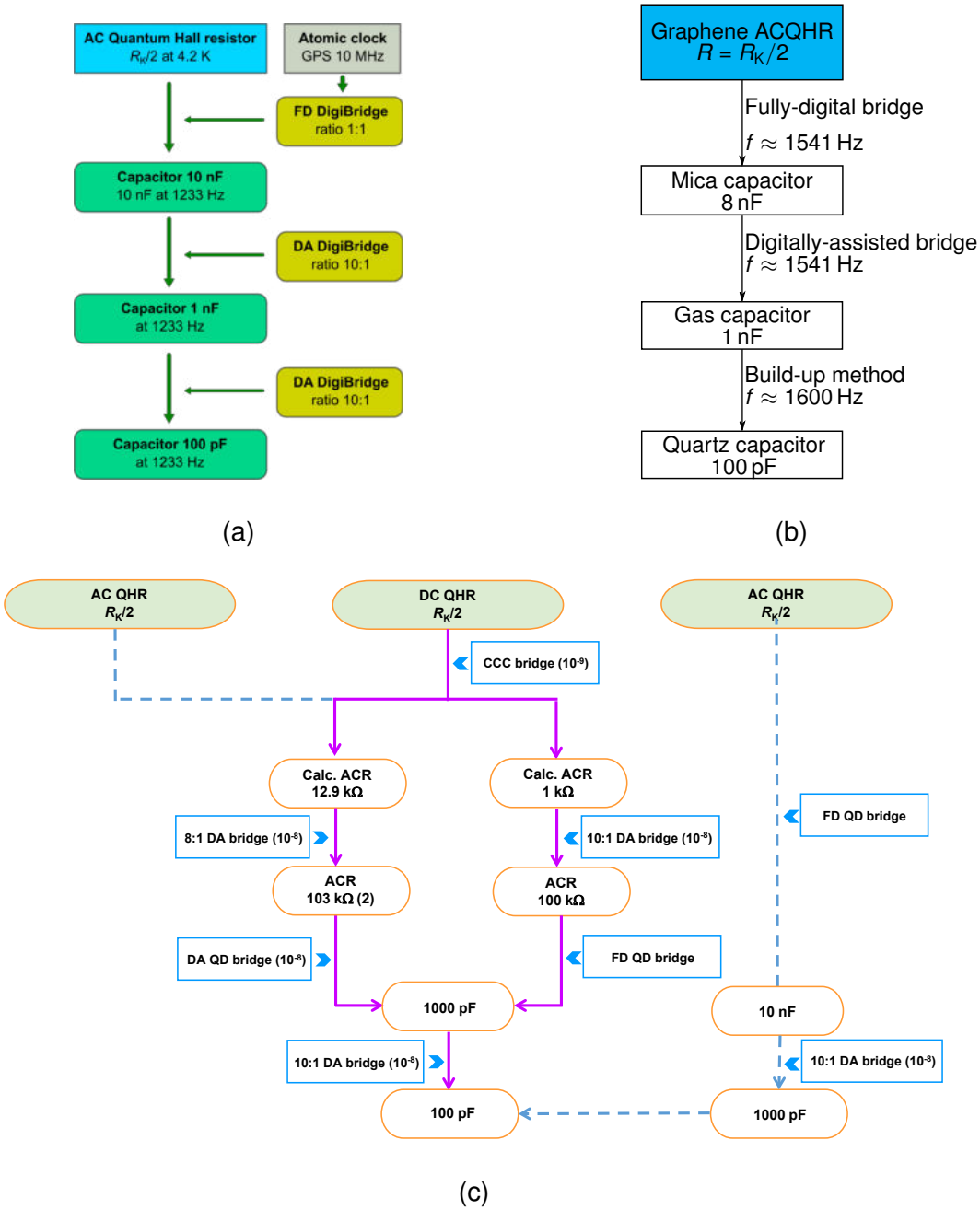


Figure 5.2: Traceability chains under development at (a) CMI, (b) INRIM and (c) KRISS within the framework of the project 18SIB07 GIQS, from a graphene AC QHR standard to a 100 pF **standard capacitor.**

transfer with digital bridges can be performed between two standards, a resistor and a capacitor

C **scaling** Josephson bridges (Section) allow to perform ratio measurement for capacitance scaling without the need of a ratio standard calibration, as occurs for the inductive voltage divider of traditional transformer bridges. Electronic digitally-assisted bridges can also considerably simplify the task of ratio measurements, although they still require a ratio calibration.

As examples, we briefly summarize three traceability chains developed within GIQS:

CMI The CMI traceability chain, figure (a), starts with the calibration at 1233 Hz of a 10 nF capacitance standard against a graphene ACQHR standard by means of an electronic fully-digital quadrature bridge, working at 1 : 1 impedance magnitude ratio. Then, the 10 nF value is scaled down to a 1 nF capacitance standard by means of a 10 : 1 digitally-assisted bridge operating again at 1233 Hz. Finally, the 1 nF value is scaled down to a 100 pF capacitance standard with the same digitally-assisted bridge.

INRIM The INRIM traceability chain, figure (b), starts with the calibration at 1541 Hz of an 8 nF solid-dielectric capacitance standard against a graphene ACQHR standard by means of an electronic quadrature fully-digital bridge [ ], working at 1 : 1 impedance magnitude ratio. Then, the 8 nF value is scaled down to a 1 nF gas capacitance standard by means of an 8 : 1 digitally-assisted bridge [ ] operating again at 1541 Hz. Finally, the 1 nF value is scaled down to a 100 pF quartz capacitance standard by means of a capacitance build-up method [ ].

KRISS is evaluating different possible traceability chains as shown in figure (c). The leftmost one is the current traceability chain starting with a DCQHR standard and which was described in [ ]. The rightmost chain starts with an ACQHR standard and is the same CMI chain described above. The center chain starts with a DC-QHR standard which is used to calibrate a 1 kΩ calculable AC/DC Haddad resistance standard by means of a cryogenic current comparator. The 1 kΩ standard is then used to calibrate a 100 kΩ AC resistance standard by means of a 10 : 1 digitally-assisted bridge, in two successive steps. The 100 kΩ resistor value is transferred to a 1 nF capacitance standard by means of an electronic quadrature fully-digital bridge. Finally, the 1 nF value is scaled down to a 100 pF capacitance standard with the 10 : 1 digitally-assisted bridge.

5.4 Capacitance artifact standards

National metrology institutes maintain a local capacitance scale, typically composed of one or more standard for each decadal value. Each standard is thoroughly characterized for the influence of the environmental parameters (typically temperature, sometimes humidity and temperature also) and calibrated periodically; its value is monitored over the long term to determine the drift over time, so a prediction of the capacitance

value and the corresponding in-use uncertainty at any time after the last calibration can be obtained. The range covered by commercial capacitance standards starts from 1 pF and goes up to 100 µF. Higher values, up to 1 F, are synthesized by passive transformer standards [,] or with the aid of electronic amplifiers.

5.4.1 Fused-silica capacitors

The most stable capacitance standards, used for long-term maintenance of the farad unit in national metrology institutes, are given by monolithic fused-silica or fused-quartz standards, available in the 1 pF to 100 pF range. The present construction is due to Cutkosky [ ]: active and shield silver film electrodes are directly fired over a dielectric "hockey puck" and the element contacted by springs in a supporting cell.

The frequency dependence of fused-silica capacitors is small (of the order of 1×10^{-6} in the audio frequency range [ ]) and the temperature coefficient is around $12 \times 10^{-6}\,\mathrm{K}^{-1}$ [ ]. The time drift can be below 10^{-7} per year. A commercial model with a thermostated enclosure is available (Andeen-Hagerling AH1100) is available and has been employed in international intercomparisons [ ].

5.4.2 Gas-dielectric capacitors

The range from 1 pF to 10 nF can be also covered by sealed gas-dielectric capacitors [,]. Gas-dielectric capacitors can have a low (less than $2 \times 10^{-6}\,\mathrm{K}^{-1}$ [ ]) temperature coefficient, and a very low (in the 10^{-6} range) loss. The very small frequency dependence in the audio frequency range,can be evaluated from radio-frequency measurements [,].

5.4.3 Solid-dielectric capacitors

Standards from 1 nF to 100 µF are available as dielectric (mica, polymer) capacitors. The temperature dependence (several $10^{-5}\,\mathrm{K}^{-1}$), the frequency dependence and loss (in the 10^{-5}-10^{-4} range) is much larger than silica or gas-dielectric standards, and the time stability is typically worse. Standards made from electronic components in a thermostated enclosure have been realized [, ,]

5.5 Calibration of commercial meters

5.5.1 Capacitance meters

At the present time the highest-accuracy capacitance meters available on the market are the Andeen-Hagerling AH2500A, AH2550A (fixed frequency, 1 kHz and AH2700A (variable frequency, 20 Hz to 20 kHz). The measurement range is up to 1 µF. The bridges rely on internal fused-silica capacitance standards; an artifact calibration mode is available, performed by measurement of a capacitor in the 10 pF to 1600 pF range.

5.5.2 Impedance meters

In commercially available impedance meters (also called *LCR* or *RCL* meters/bridges, or impedance analyzers) the ratio standard necessary for the measurement action is provided by an electronic circuit, either analog or digital. The impedance being measured is compared with a internal reference impedance (chosen within a set). The base accuracy is typically limited to parts in 10^4.

The calibration of impedance meters is performed with a set of impedance standards of different kind (resistors, capacitors and inductors) and different nominal values. Each standard has to be manually connected to the meter. The difference between the reading value and the reference value (the latter coming from a calibration certificate) is the meter reading error, for that particular nominal impedance value and measurement frequency. Often, electronic impedance bridges allow to perform the so-called *artifact calibration*, which is a *de facto* adjustment procedure: for each impedance standard measured, the corresponding reference numerical value is entered (typically with a keyboard) in the bridge memory. A firmware calculates a set of adjustment numerical coefficients and store them in the bridge permanent memory. The coefficients are then employed during normal measurements, to convert raw data into readings.

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