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Doctoral Dissertation
Doctoral Program in Electrical Electronics and Communications Engineering
(35^{th}cycle)

Design of the Readout Chip with Multi-Energy Bins for Spectroscopic X-ray Imaging

By

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Politecnico di Torino
2024

Declaration

I hereby declare that, the contents and organization of this dissertation constitute my own original work and does not compromise in any way the rights of third parties, including those relating to the security of personal data.

Jiale Cai
2024

* This dissertation is presented in partial fulfillment of the requirements for **Ph.D. degree** in the Graduate School of Politecnico di Torino (ScuDo).

I would like to dedicate this thesis to my loving family

Acknowledgements

I would like to acknowledge my supervisors, colleagues, friends, and family for their care and help in completing my doctoral work at the Politecnico di Torino. I am thankful to the great city of Turin and to the INFN Turin section, where I had a very happy and memorable time.

Angelo Rivetti is an outstanding and respected tutor, and this PhD work was completed under his careful guidance. Manuel Dionisio Da Rocha Rolo is my co-supervisor, who gives me the chance to come to Turin, and provided me with a great deal of help both in life and work, especially during the pandemic. He supports me a lot with most of the issues in Politecnico and INFN. Here I express my gratitude to him. Thanks to Giovanni Mazza, who provided a lot of help and guidance when I used the design resources of the INFN Turin section. I would like to thank Andrea Paternò and Andrea Di Salvo, as both Andreas taught me a lot about digital circuit design. I am grateful to Giulio Dellacasa for his help in the digital circuit in this work. I appreciate Edoardo Bianco, as he completed the analog circuit part of this work. I am grateful to other colleagues at the VLSI group, including Silvia, Fabio, Raffaele, Lorenzo, Stefano, Alejandro, Simona, Weishuai, and Ramshan. I really enjoy working with them and having lunch with them every day.

I also would like to thank my colleagues at the Institute of High Energy Physics. Xiaohui Li provided me with a lot of guidance in this work and also helped me a lot in life. I am grateful to Prof. Long Wei, Prof. Cunfeng Wei, Prof. Zhiming Zhang, and Prof. Shuai Lei for their support in my work.

At last, thank my beloved family, my beloved parents, my beautiful wife, and my lovely son. Without their support, I would not have been able to complete my PhD work. I miss them every day in Italy.

Abstract

Spectroscopic X-ray imaging is an important development direction in the field of medical CT in recent years. Spectroscopic CT can detect X-rays in multiple energy ranges simultaneously, and assign different weight factors to X-rays of different energies, effectively improving the contrast of X-ray imaging. In addition, it can identify substances based on the differences in their abilities to absorb X-rays. X-ray detection can be divided into energy integration and photon counting according to the detection method. Photon counting detection can eliminate the influence of electronic noise compared to the former and has better energy resolution. In this thesis, a readout chip for a hybrid pixel detector was designed, using 110nm CMOS technology, with 8×112 pixels, each pixel size is $110 \times 110 \mu m^2$. Each pixel contains four digitally programmable thresholds that can simultaneously count photons in four energy ranges, and the counter depth for each energy range is 12 bits. When incident photons interact with the detector on the edge of the pixel or when the pixel size is relatively small compared to the detector thickness, the charge generated by the incident particle will diffuse to adjacent pixels, i.e. the charge sharing effect, which will affect the energy resolution of the pixel and may also cause imaging artifacts due to incorrect photon counting. To eliminate the charge sharing effect, a correction circuit was designed in the digital circuit section of this chip, which can reconstruct all the charge generated by the incident particle and find the pixel actually hit by comparing the ToT signals of adjacent pixels, and then assign all the collected charge to that pixel. The chip adopts a two-stage amplifier structure in the analog circuit section, which can complete the amplification shaping and charge summation of the signal. The signal amplified and shaped generates ToT signals after the discriminator, and then completes digitization through the ToT counter. Finally, the event is distributed to the corresponding energy counter by comparing with four preset energy thresholds in the threshold comparator module of the digital circuit. Currently, mainstream pixel sizes range from $50 \mu m$ to $150 \mu m$,

and implementing charge sharing correction and multiple energy thresholds within such a small circuit area is a huge challenge for chip design. This chip innovatively provides a digital threshold scheme based on ToT technology, implementing four digitally programmable thresholds in each pixel instead of discriminators that are commonly used in photon counting detector systems. In this thesis, the post layout simulation verification was carried out for the charge sharing correction logic of the analog and digital circuits, the digital threshold comparator, and the energy counter.

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Chapter 1

Introduction

X-rays was discovered by the German physicist Wilhelm Conrad Röntgen in 1895. He found that this mysterious radiation could penetrate through solid objects, including the human body, and create an image of their internal structure on photographic film [1]. The discovery of X-rays has revolutionized medical diagnosis and imaging, as well as other fields. It also sparked a new era of research into the nature of radiation and the properties of matter. Computed tomography (CT) is a medical imaging technique that uses X-rays and advanced computer algorithms to create detailed 3D images of the inside of the body. The first CT scanner was developed by British engineer Godfrey Hounsfield and his team in the early 1970s [2–4]. The invention of CT was a major breakthrough in medical imaging, providing doctors with a new tool for visualizing the brain, detecting tumors, and diagnosing a wide range of medical conditions.

Since the first CT scanner was developed, there have been many advancements in CT technology, including improvements in scanner design, detector technology, and image processing algorithm. Photon-counting detectors (PCD) based CT is an emerging technology in recent years, which has the potential to dramatically change the clinical applications of CT [5–8]. PCD records the number of incoming photons and measure each photon energy.The identification of different materials can be achieved by measuring the unique k-edges of various elements. (discussed in section 1.2). Two energy thresholds are required for k-edge detection, one below and one above the binding energy of the k-shell electrons for the element of interest. When implements multiple energy thresholds in the PCD, the incoming photons are divided

into different energy bins and counted separately. Implementation of multi-thresholds gives PCD energy resolving capability, one could measure more than one X-ray spectrum simultaneously, which means more than one element can be identified simultaneously as well. This is referred to spectroscopic X-ray imaging [9–11]. A CT embodying this capability is called spectral CT, which can differentiate between different materials based on their X-ray energy different absorption coefficients. Spectral CT uses energy-sensitive detectors that can measure the attenuation of X-rays at multiple energy levels. Spectral CT acquires data at different energy levels, allowing radiologists to perform material decomposition. Material decomposition is a process of separating the detected X-ray signals into different components based on their energy-dependent attenuation properties. Different tissues and materials attenuate X-rays differently at various energy levels. Spectral CT can provide quantitative information about tissue composition, allowing radiologists to measure parameters such as iodine concentration, fat content, and calcium content in tissues. This quantitative analysis can be valuable for diagnosing specific conditions or monitoring treatment responses. This is the motivation for this thesis to develop a readout chip with multi-energy thresholds for spectroscopic X-ray imaging.

1.1 Interaction between photons and matter

When X-ray photons interact with matter, there are four main processes that can occur [12–14]:

- Photoelectric effect: an X-ray photon is absorbed by an atom, and an electron is ejected from the atom.
- Compton scattering: an X-ray photon interacts with an electron in an atom and transfers some of its energy to the electron.
- Pair production: an X-ray photon interacts with the nucleus of an atom and produces an electron-positron pair.
- Coherent scattering (Rayleigh scattering): an X-ray photon interacts with an atom and changes direction without losing energy.

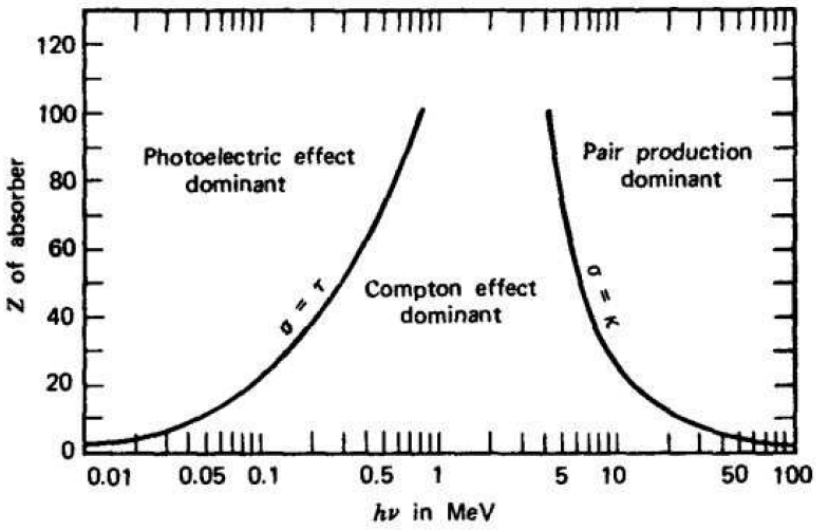

Fig. 1.1 The relative importance of various processes of electromagnetic radiation interaction with matter. [15]

The probabilities for each of processes mentioned above depends on a complex interplay between the energy of the photon, the properties of the material, and the angle and polarization of the incident photon (Figure 1.1). Each process has a threshold energy below which it cannot occur. The photoelectric effect requires a minimum energy to overcome the binding energy of an electron in an atom, while pair production requires a minimum energy to create a pair of particles. On the other hand, the probability of the photoelectric effect and pair production depend on the atomic number of the material, which determines the strength of the electromagnetic interaction between the photon and the material. The angle between the incident photon and the electron or atom it interacts with and its polarization influences the probability of Compton scattering and Coherent scattering.

1.1.1 Photoelectric effect

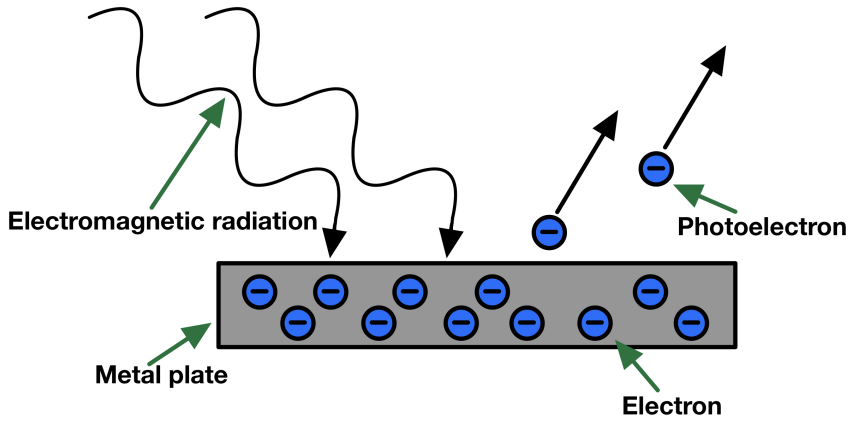

Fig. 1.2 Photoelectric effect.

The photoelectric effect (Figure 1.2) is a phenomenon in which electrons are emitted from a material when it is exposed to electromagnetic radiation, such as X-rays. When a photon with enough energy above the binding energy of the electron in the material is absorbed, the electron can be ejected from its orbit around the nucleus and becomes a free electron with a kinetic energy:

$$E = h\nu - E_b \tag{1.1}$$

where $h\nu$ (h is the Planck constant and ν is the photon's frequency) is the energy of incoming photon, and E_b is the binding energy for an electron.

After an electron ejects from inner shell of the ionized atom, the vacancy created in the inner shell can be filled by an electron from outer shell while releasing energy in the form of a photon. The emitted photon is called a characteristic fluorescence photon, its energy is equal to the difference of binding energies in the two corresponding shells. The characteristic fluorescence photon has a specific energy that is related to the element that emitted it. By measuring the energy of fluorescence photon, it is possible to determine the identity and concentration of the elements present in the sample.

In some cases, instead of emitting a photon, the excess energy is transferred to another electron in the atom, which is then ejected from the atom. The ejected electron is called an Auger electron. The energy of the Auger electron is equal to

the difference in energy between the two the two electron shells involved in the transition, minus the binding energy of the ejected electron. An Auger electron could be ejected from the L-shell with an energy of $E_K - 2E_L$, or from the M-shell, with an energy of $E_K - E_L - E_M$.

Cross section in physics is a measurement of the probability of a specific interaction occurring between particles. The cross section of the photoelectric effect is generally larger for lower energy photons and decreases with increasing photon energy. When the incident photon has sufficient energy to liberate an electron from the inner shell, the cross section increases abruptly. These sharp increases are called edges in the cross section function. The edge energy are unique to each element, therefore it can be used for element-specific imaging and analysis. The details about k-edge imaging will be discussed in section 1.2.2.

1.1.2 Compton scattering

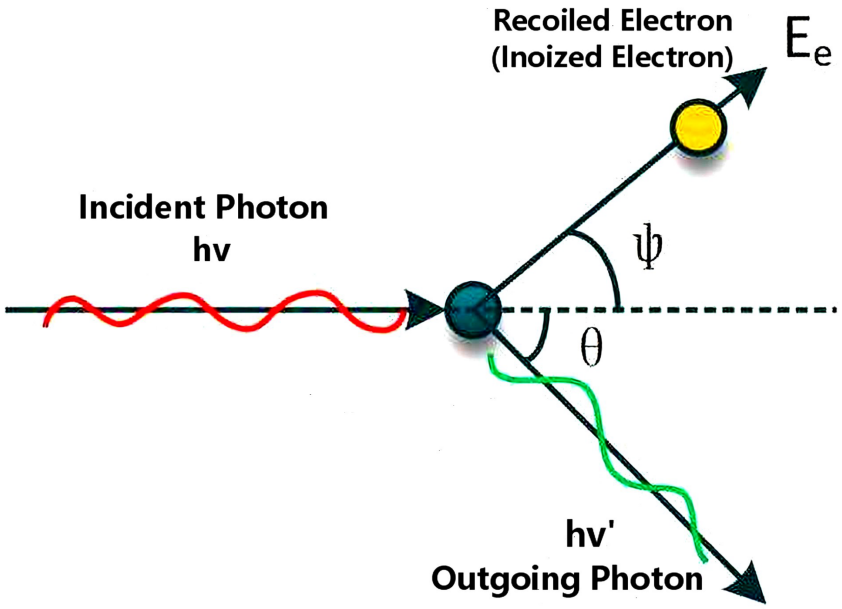

Fig. 1.3 Compton scattering.

Compton scattering is process in which a photon collides with an electron, transferring some of its energy and changing its direction (Figure 1.3). The energy of the scattered photon is determined by the angle between the incident photon and the

electron it interacts with, as well as the initial energy of the incident photon, it can be calculated by the following equation,

$$h\nu' = \frac{h\nu}{1 + \frac{h\nu}{m_0 c^2}(1 - \cos\theta)} \tag{1.2}$$

where $h\nu$ is the energy of the incident photon, $h\nu'$ is the energy of the scattered photon. In Compton scattering the incident photon has much larger energy than the binding energy of an electron, therefore the electron can be treated as a free electron, and its binding energy can be ignored. The electron is assumed to be at rest before the scattering occurs with zero kinetic energy and only its rest energy $m_0 c^2$.

The Compton scattering cross-section can be calculated using the Klein-Nishina formula, which describes the differential cross-section of Compton scattering, $d\sigma/d\Omega$, i.e., the probability density of photon scattering within a fixed solid angle. The Klein-Nishina formula is,

$$\frac{d\sigma}{d\Omega} = \frac{r_e^2}{2}\left(\frac{E'}{E}\right)^2\left[\frac{E}{E'} + \frac{E'}{E} - \sin^2\theta\right] \tag{1.3}$$

where r_e is the classical electron radius, E is the initial photon energy, E' is the scattered photon energy, θ is the scattering angle.

1.1.3 Pair production

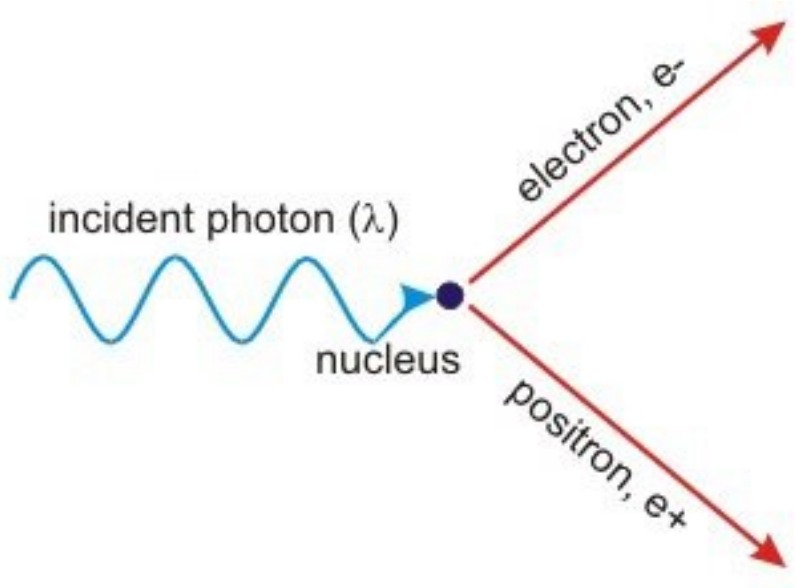

Fig. 1.4 Pair production.

Pair production is a process where a high-energy photon interacts with the electric field of an atomic nucleus, resulting in the creation of an electron-positron pair (Figure 1.4), as shown in following equation,

$$\gamma \rightarrow e^{-} + e^{+} \tag{1.4}$$

where γ represents a high-energy photon, and e^{-} and e^{+} represent an electron and its antiparticle, a positron.

The energy of the photon must be at least equal to the rest mass of the electron and positron combined, which is approximately 1.02 MeV. The created positron has a short life-time and will be annihilated with the formation of two photons of 511 keV that have opposite directions.

1.1.4 Coherent scattering

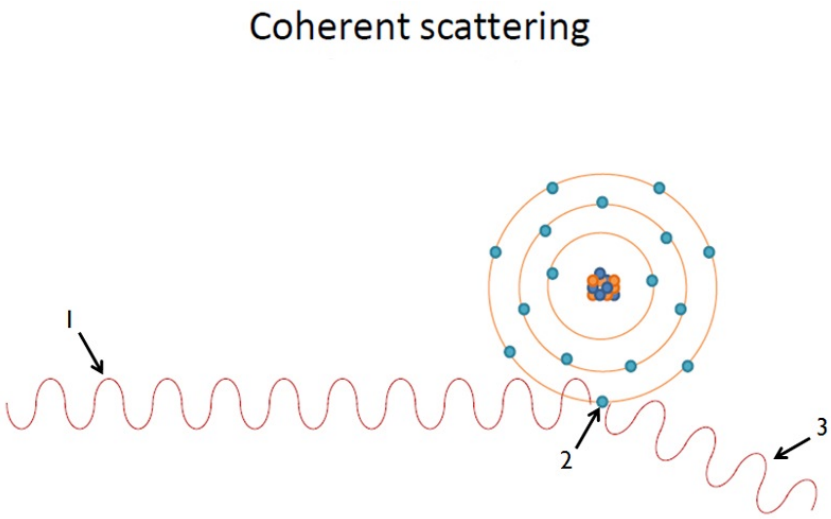

Fig. 1.5 Coherent scattering.

Coherent scattering is also known as Rayleigh scattering, it is a type of photon interaction that occurs when the energy of an X-ray or gamma photon is small compared to the ionization energy of an atom (Figure 1.5). As a result, the photon does not have enough energy to ionize the atom and instead undergoes elastic scattering, where it changes direction but retains its original energy. The scattered photon has the same energy and wavelength as the incident photon. The coherent scattering cross section depends on the atomic number and electron density of the material, as well as the energy of the incident photon. It is proportional to $(Z/h\nu)^2$, where Z is the atomic number of the target atom.

1.2 Spectroscopic X-ray imaging

Spectroscopic X-ray imaging is an advanced medical imaging technique that allows acquiring more than one X-ray spectrum simultaneously by means of multiple energy thresholds implementation in PCD [9–11]. Spectroscopic X-ray imaging can produce multiple images that display different properties of the body's internal structure, including bone, soft tissue, and contrast-enhanced structures. In traditional X-ray imaging, the image is created by measuring the intensity of X-ray that pass

through the body. However, spectroscopic X-ray measures the X-ray beam's energy distribution, enabling differentiation between different tissue types based on their X-ray attenuation properties. One significant advantage of spectroscopic x-ray imaging is its ability to provide contrast agents with a high degree of definition, enabling clear images of soft-tissue organs or pathologies [16–21]. Spectroscopic imaging can distinguish the absorption of different materials due to their atomic number or composition, and this information can be used to differentiate between tissues that are difficult to distinguish in conventional X-ray imaging. In recent years, spectroscopic X-ray imaging has been increasingly applied in various fields, including medical imaging, materials science, and security scanning.

1.2.1 X-ray linear attenuation coefficient

When an X-ray beam passes through a material, its intensity is reduced due to the absorption and scattering of photons by the atoms in the material. The amount of reduction in X-ray intensity is related to the linear attenuation coefficient of the material, which depends on its composition and density. Different materials have different linear attenuation coefficients at different X-ray energies [22]. By measuring the linear attenuation coefficients of a material at different energies, it is possible to develop a spectral profile that can be used to distinguish it from other materials. For example, bone has a higher attenuation coefficient than soft tissue at lower X-ray energies, while at higher energies, the attenuation coefficient of bone decreases faster than soft tissues. Spectroscopic X-ray imaging techniques utilize this principle to distinguish between different materials in an object.

In X-ray imaging, the photoelectric effect and Compton scattering are two dominant processes of photon interaction with matter. The photoelectric coefficient strongly depends on the atomic number of a material, and therefore it can be used as an indicator of the composition of an object. The utilization of X-ray linear attenuation coefficient information in the domain of medical applications holds profound significance.

As a function of energy the attenuation coefficient $\mu(E)$ can be represented by a linear combination of a number of basis functions as given by [23],

$$\mu(E) = a_1 f_1(E) + a_2 f_2(E) + \ldots + a_n f_n(E) \tag{1.5}$$

Finding the optimal basis functions is ultimately based on empirical data. A suitable set of functions must be identified to fit experimental data with errors that are smaller than the ones introduced by the proposed measurement system. Here is an achieved success in fitting experimental data using functions that take on the following form [23],

$$\mu(E) = a_1 f_1(E) + a_2 f_2(E) + \ldots + a_n f_n(E)\mu(E) = a_1 \frac{1}{E^3} + a_2 f_{\mathrm{KN}}(E) \tag{1.6}$$

where $f_{\mathrm{KN}}(E)$ is the Klein-Nishina function,

$$f_{KN}(\alpha) = \frac{1+\alpha}{\alpha^2}\left[\frac{2(1+\alpha)}{1+2\alpha} - \frac{1}{\alpha}\ln(1+2\alpha)\right] + \frac{1}{2\alpha}\ln(1+2\alpha) - \frac{1+3\alpha}{(1+2\alpha)^2} \tag{1.7}$$

and $\alpha = E/510.975$ keV. This basis set is particularly convenient as the two functions have physical significance. The function $\frac{1}{E^3}$ approximates the energy dependence of the photoelectric interaction, while $f_{KN}(E)$ represents the energy dependence of the total cross-section for Compton scattering. Below are the expressions for the dependence of α_1 and α_2 on physical parameters,

$$\alpha_1 \approx K_1 \frac{\rho}{A} Z^n, n \approx 4 \tag{1.8}$$

$$\alpha_2 \approx K_2 \frac{\rho}{A} Z \tag{1.9}$$

where K_1 and K_2 are constants, ρ is mass density, A is atomic weight and Z is atomic number.

1.2.2 K-edge imaging and material decomposition

When an X-ray photon of sufficient energy passes through a material, it can be absorbed by an inner-shell electron, causing it to be ejected from the atom, leaving behind a hole in the inner shell. The minimum energy required to remove the electron, also known as the binding energy, is specific to each element and it is related to

the atomic number of the material. An abrupt increase in X-ray attenuation curve (as shown in Figure 1.6) occurs when the incident X-rays have energy just above the k-shell's binding energy in the atom. This is the so called k-edge [24, 25]. The X-ray mass attenuation for the element iodine is shown in Figure 1.6, the drop of the mass attenuation coefficient appears at 33.2 keV for iodine. In most of the X-ray regime used in materials characterization (up to 150 keV), the photo-electric effect is the main process that causes X-ray attenuation. When the photo-electric process is dominant, the values for μ/ρ depends strongly on Z of the atom and on X-ray energy E. As can be seen in Figure 1.6, the attenuation drops very strongly with E approximately as E^3. μ also depends strongly with Z, though the sharp absorption edges make this more complicated.

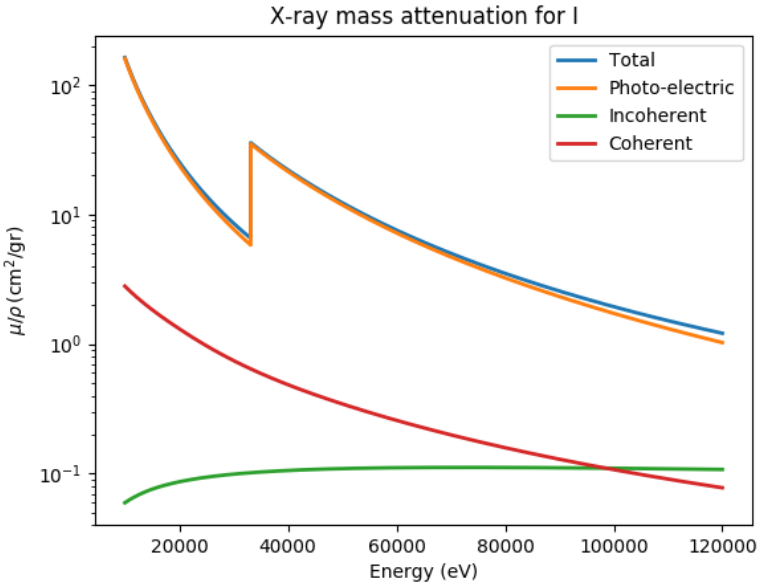

Fig. 1.6 X-ray mass attenuation for the element Iodine, data is from [26].

A conventional X-ray misses spectrally varying attenuation information due to the energy integration, while an energy-discriminative photon-counting detector can distinguish the energy levels of incoming photons, which helps acquiring additional information. Two X-ray energy bins are required in k-edge imaging, one below and one above the binding energy of the k-shell electrons for an element of interest [24, 25]. Different materials can be easily identified by measuring their unique k-edges. K-edge imaging offers a promising approach to improve the sensitivity and

specificity of X-ray imaging techniques, particularly in applications where accurate determination of tissue composition is critical.

K-edge imaging can be achieved through the use of multi-bin energy-discriminating counting detectors. This technique allows for material-specific imaging in CT, and when combined with contrast agents based on high-Z elements, it creates new possibilities for spectral CT. By utilizing energy-discriminating detectors, spectral CT can enhance contrast resolution, particularly when using contrast agents containing heavy elements, such as iodine or gadolinium. When heavier elements are used in contrast agents such as, e.g., gadolinium, iodine or bismuth, their K-absorption edges at 50.2 keV, 80.7 keV, and 90.5 keV, respectively, can be accessed for diagnostic x-ray imaging. These k-edge features can be distinguished from other contributions to x-ray attenuation by employing more than two spectrally distinct measurements, e.g. more than two energy bins. Spectral CT opens up possibilities for advanced imaging techniques, such as virtual non-contrast imaging and virtual monoenergetic imaging, which can improve diagnostic accuracy and reduce the need for additional imaging studies.

1.3 Photon counting detectors

Conventional CT scanners use an indirect conversion process to detect X-rays. In this process, a scintillator converts X-ray photons into light photons, which are then converted to electric charges by a photodiode and integrated. Since the amount of light is proportional to the X-ray energy, and signals are collected for many X-ray photons, these detectors are called energy-integrating detectors (EIDs). PCDs directly convert X-ray photons to charge carriers and are fast enough to count individual X-ray photons and sort them by energy. PCDs have the potential to enhance dose efficiency through higher geometric efficiency with respect to EIDs, reduced sensitivity to electronic noise, and optimized signal weighting. They also offer improved spatial resolution and better spectral imaging than conventional CT, enabling the quantification of two or more materials.

Table 1.1 Properties of some commonly used semiconductor material in medical imaging.

semiconductor	density[g/cm^3]	Z	E_{gap}[eV]	ε[eV]	X_0[cm]
Si	2.33	14	1.12	3.6	9.37
Ge	5.33	32	0.67	2.9	2.30
CdTe	5.85	48,52	1.44	4.43	1.52
CdZnTe	5.81	48,30,52	1.6	4.6	
HgI2	6.40	80,53	2.13	4.2	1.16
GaAs	5.32	31,33	1.42	4.3	2.29

E_{gap} : band gap energy
ε : an ionization potential
X_0 : radiation length

1.3.1 Semiconductor detectors

Semiconductor detectors are a class of materials widely used in high-energy physics and medical imaging (Table 1.1 shows the properties of some commonly used semiconductor material in medical imaging). The bandwidth of semiconductors is relatively small, and only a small amount of energy is needed to generate electron-hole pairs in the semiconductor. Therefore, semiconductor detectors can provide excellent energy resolution and are very suitable for X-ray detection [13, 27, 28]. Incident light will generate photoelectrons in the semiconductor material, which will interact with other electrons to excite them to the conduction band and leave a hole in the valence band. Under the action of an external electric field, both electron and hole currents will move in the direction of the electric field, while diffusion will occur due to differences in concentration caused by the distribution of carriers in space, which tends to move from high concentration to low concentration. The movement of carriers in the semiconductor material will produce a signal on the charge collection electrode.

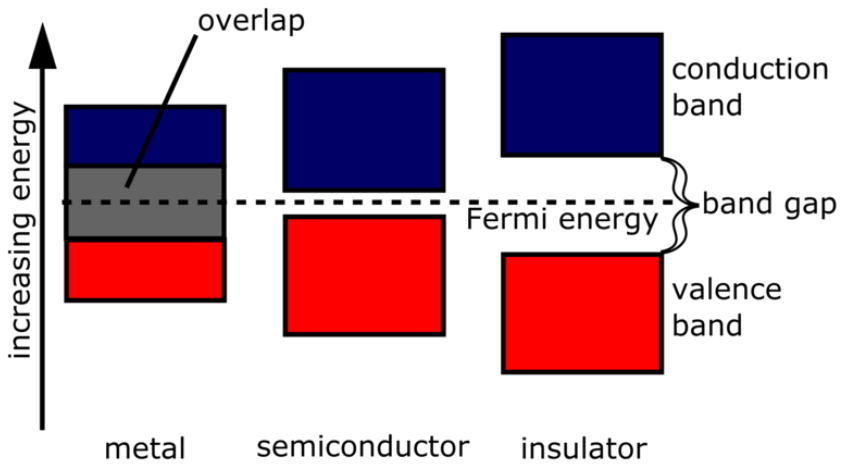

Fig. 1.7 Band gap structure for metal, semiconductor and insulator.

The periodic lattice structure of semiconductors is manifested in the form of energy band structures in semiconductor crystal materials (Figure 1.7), and the bandwidth values of the conduction and valence bands determine the electrical properties of the material. In the absence of thermal excitation, all electrons in the material will be confined to the valence band, with no electrons in the conduction band. With the increase of temperature, electrons in the valence band will gain thermal energy, and there is a certain probability that they will be excited to the conduction band, leaving behind a hole in the valence band. The surrounding electrons in the valence band will fill this hole while leaving new holes. Since the hole can be regarded as a positively charged particle, its motion can generate current in the material. Doping different elements of varying atomic numbers into semiconductors will change the concentration of carriers in the material. Taking silicon crystal as an example (Figure 1.8), there are four electrons in the outermost layer of a silicon atom, which combine with the outermost electrons of adjacent silicon atoms to form a stable structure. To increase the electron concentration in the conduction band, 5-valence elements such as phosphorus, arsenic, or antimony can be added to silicon materials. Impurity atoms have five valence electrons, four of which form covalent bonds with silicon atoms, while the remaining one is loosely bound around the impurity atom and easily excited to the conduction band. This greatly increases the electron concentration in the material, and we call this type of doped material an N-type semiconductor. Similarly, a P-type semiconductor refers

to doping with 3-valence elements such as boron, gallium, indium, or aluminum, which greatly increases the hole concentration in the material [29, 30].

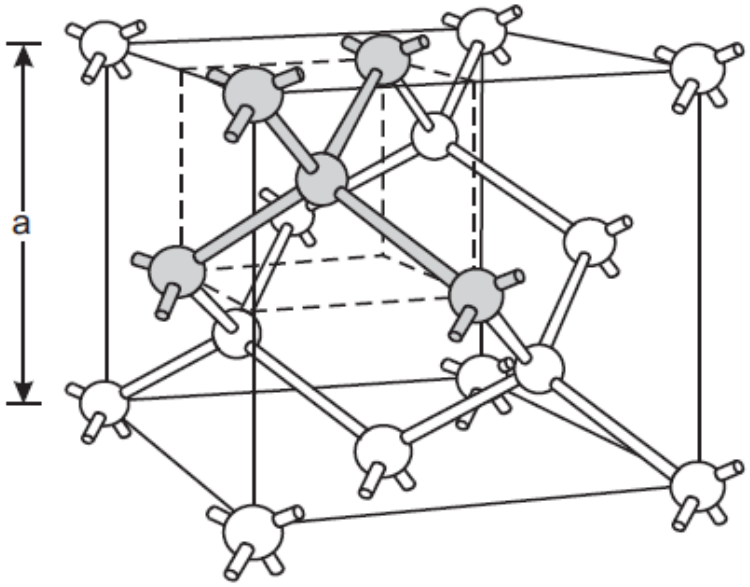

Fig. 1.8 Lattice structure of Si and Ge. [27]

When a P-type semiconductor and an N-type semiconductor are brought into contact, a PN junction is formed. The difference in carrier concentration gradient between the two different types of semiconductors causes the electrons in the N-type semiconductor to move towards the P-type semiconductor and recombine with the holes in it, while the holes in the P-type semiconductor move towards the N-type semiconductor and combine with the electrons there. The movement of electrons and holes will leave doping impurities with positive and negative charges respectively in the N-type and P-type semiconductors, creating an electric field between them. The electric field will counteract the movement of electrons and holes, eventually reaching a stable state. Finally, a region containing space charge called the depletion region will be formed in the PN junction, where there is no moving carrier. Any moving carriers in the depletion region will move towards both ends under the action of the electric field [29–31].

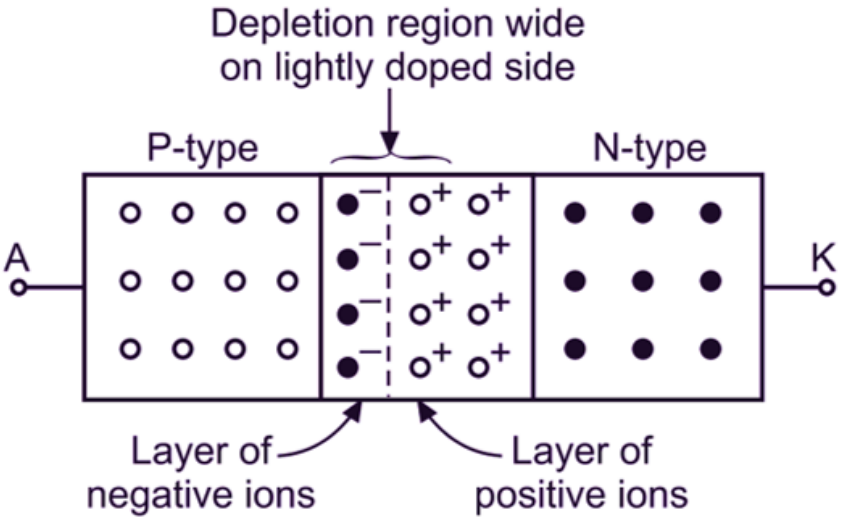

Fig. 1.9 A schematic diagram of PN junction.

The basic working principle of semiconductor detectors is based on the depletion region. Incident particles will generate freely moving charges in the depletion region, and these charges will move towards the collection electrode to produce an electrical signal under the action of an electric field (Figure 1.9). The density distribution of charges in the depletion region can be obtained by solving the following Poisson equation:

$$\frac{d^2\varphi}{dx^2} = -\frac{\rho(x)}{\varepsilon} \tag{1.10}$$

Where ε is the dielectric constant, $\rho(x)$ is the charge density, and the charge density varies in different regions defined by below equation,

$$\rho(x) = \begin{cases} eN_D, & 0 < x < x_n \\ -eN_A, & -x_p < x < 0 \end{cases} \tag{1.11}$$

Where N_D and N_A are the dopant concentrations of different types. The electric field intensity can be defined as $E(x) = -grad(\varphi(x))$, combining equation (1-4) and equation (1-5), and taking into account the boundary conditions,

$$-E(x) = \frac{d\varphi}{dx} = \begin{cases} -\frac{eN_D}{\varepsilon}(x - x_n), & 0 < x < x_n \\ \frac{eN_A}{\varepsilon}(x + x_p), & -x_p < x < 0 \end{cases} \tag{1.12}$$

integrating the electric field strength yields,

$$\varphi(x) = \begin{cases} -\frac{eN_D}{\varepsilon}(x-x_n)^2 + V, & 0 < x < x_n \\ -\frac{eN_A}{\varepsilon}(x+x_p)^2, & -x_p < x < 0 \end{cases} \tag{1.13}$$

The extension length of the depletion region in N-type and P-type semiconductors can also be obtained,

$$x_n = \sqrt{\frac{2\varepsilon V}{eN_D(1+N_D/N_A)}} \tag{1.14}$$

$$x_p = \sqrt{\frac{2\varepsilon V}{eN_A(1+N_A/N_D)}} \tag{1.15}$$

Generally, the doping concentration of two different types of materials are not the same. The depletion region length in material with lower doping concentration will be larger. If NA » ND, the length of the depletion region can be approximately determined as:

$$x_n = \sqrt{\frac{2\varepsilon V_0}{eN_D}} \tag{1.16}$$

The depletion region can be regarded as a charged capacitor (Figure 1.7), and the capacitance value per unit area is,

$$C = \frac{\varepsilon}{d} = \sqrt{\frac{e\varepsilon N}{2V}} \tag{1.17}$$

The noise of a semiconductor detector increases with increasing capacitance. From Formula (1.17), it can be seen that increasing the bias voltage can effectively decrease the capacitance of the detector, thereby reducing noise and improving system resolution.

1.3.2 Pixel detector

Pixel detector is a type of radiation detector that consists of an array of small, individual detector elements, known as pixels. Each pixel is capable of detecting incoming particles or photons, obtaining their energy and timing information. Pixel detectors were first introduced in the 1980s for use in particle physics experiments. The development of pixel detectors for particle detection was driven by the need for high-resolution imaging and precise tracking of charged particles in high-energy physics experiments. The first pixel detectors were developed at CERN, the European organization for nuclear research, in the early 1980s [32]. These early detectors were based on semiconductor technologies such as silicon and gallium arsenide, and consisted of arrays of small sensors, each capable of detecting individual charged particles. Over the years, pixel detectors have been used in a variety of particle physics experiments, including the DELPHI experiment at the Large Electron-Positron Collider (LEP) [33], the ATLAS and CMS experiments at the Large Hadron Collider (LHC), and the LHCb experiment, which studies the properties of B mesons [34, 35]. In the late 1990s, advances in semiconductor technology led to the development of monolithic pixel detectors, which combine a semiconductor sensor with readout electronics integrated onto the same piece of silicon. These detectors offer improved performance and reduced material budget compared to earlier pixel detectors. More recently, there has been interest in developing pixel detectors for medical applications, such as X-ray imaging [10, 36, 37].

Pixel detectors can be classified into two types, hybrid pixel detector (HPD) and monolithic pixel detector, according to their structures.

- A hybrid pixel detector typically consists of two main components: a sensor layer and a readout chip (Figure 1.10). They can be optimised separately. The sensor layer is made up of an array of individual pixels, each of which is capable of detecting photons or charged particles. The readout chip is responsible for collecting the generated charge and processing the induced signal. The sensor layer is typically made from a semiconductor material, which is doped with impurities to create depletion regions. When a charged particle or photon enters the depletion region, it creates a large number of electron-hole pairs, which move towards the positive and negative regions respectively under an electric field that is created by the applied bias voltage, creating a small electrical signal on the electrodes. The readout chip contains a circuit for each

pixel in the sensor layer, which collects, amplifies and digitizes the electrical signals generated by the sensor. The readout chip is connected directly onto the sensor layer using bump-bonding technology, which allows for a high-density array of pixels and minimizes the distance between the sensor and readout electronics, thereby reducing noise and increasing sensitivity.

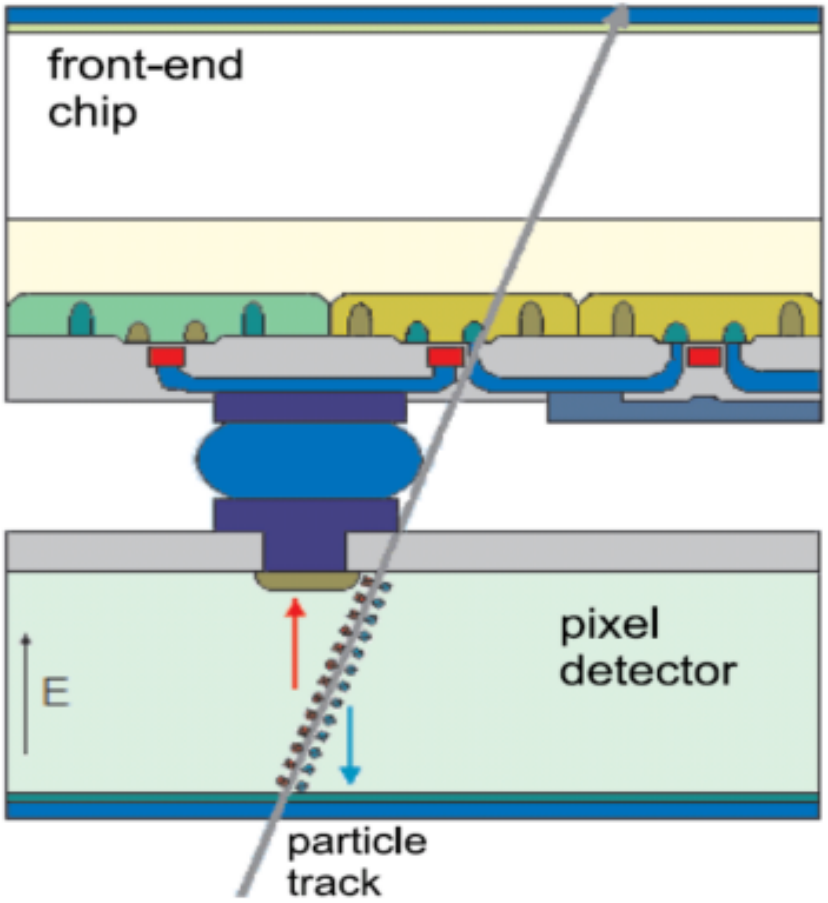

Fig. 1.10 Cross section of a hybrid pixel detector. [38]

- Unlike hybrid pixel detectors, monolithic pixel detectors have both the sensor and readout circuitry integrated onto a single piece of semiconductor material (Figure 1.11). Monolithic active pixel sensors (MAPS) is a type of monolithic pixel detector that is widely used in particle physics experiments. MAPS uses complementary metal-oxide-semiconductor (CMOS) technology to fabricate the sensor and readout circuitry on a single piece of semiconductor material. On the other hand, MAPS has lower power consumption and lower production

cost compares to HPD while offers high spatial resolution, low noise, and fast readout speed [39–42].

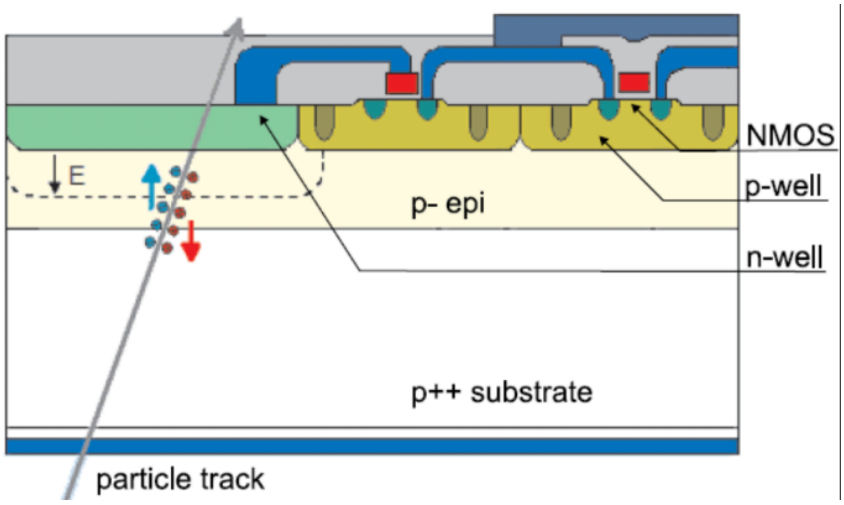

Fig. 1.11 Cross section of a monolithic active pixel sensor. [38]

Chapter 2

Hybrid pixel detector readout ASICs

As described in the previous chapter, a hybrid pixel detector consists of two components, the sensor layer and the readout electronics. The sensor contain an array of small sensitive elements called pixels, each of which is connected to its own readout channel. The most common materials used for hybrid pixel detector are Si, Ge, GaAs, CdTe or CdZnTe. The readout electronic is usually made of an application specific integrated circuit (ASIC), and it is attached to the back of the sensor with bump bonding. When X-ray photons pass through the semiconductor material, electron-hole pairs are generated by the interaction. Under the influence of applied electric field, the generated charge carriers separate and move toward the electrodes on both sides. These movements induce a current signal on the front-end of the readout ASIC. The amount of charge generated by the ionizing radiation is proportional to the energy deposited in the detector, allowing semiconductor detectors to be used for radiation detection and measurement applications, e.g., medical imaging, nuclear power plants, and particle physics experiments. In this chapter the architecture of the readout AISCs and the signal processing will be described, the status of the current research on the readout ASICs will be introduced as well.

2.1 Basic architectures of the readout electronics

The construction of a pixel detector faces the challenge of designing appropriate readout chips with numerous electronic channels, typically tens of thousands. The size of the pixel unit cells on the chip must be small enough to ensure high spatial

resolution. Despite consuming less power, each pixel circuit must offer low noise amplification of the sensor charge, hit discrimination, and readout architecture suitable for the application.The counting rate for spectral CT is generally expected to be above $10^8/mm^2/s$. Thus, an adequate speed for the analog chain and digital section, and a well-defined threshold are essential requirements for photon counting based CT[43–45]. Radiation hardness is necessary in some situations with high radiation levels.

2.1.1 Generic pixel readout chip

The vast number of channels in pixel detector systems necessitates the use of custom-designed electronics circuits that are highly integrated. Various readout chips have been designed for hybrid pixel detectors, featuring different pixel sizes, distinct analog circuitry, and unique readout approaches tailored to specific applications. However, several fundamental building blocks are common to the main components of generic readout chips [43]. As illustrated in Figure 2.1, these readout chips typically consist of two main parts: an area comprising a matrix of nearly identical rectangular, square, or hexagonal pixels, and a chip periphery that controls the pixel matrix, buffers data, and houses global configuration functions for all pixels. To enable three-sided abutment on a module, wire bond pads are located exclusively on one side of the chip, as depicted in Figure 2.1. Currently, ongoing research aims to develop systems that can be tiled on all four sides by utilizing Through Silicon Via (TSV) interconnections, enabling the formation of very large detector modules [46–50].

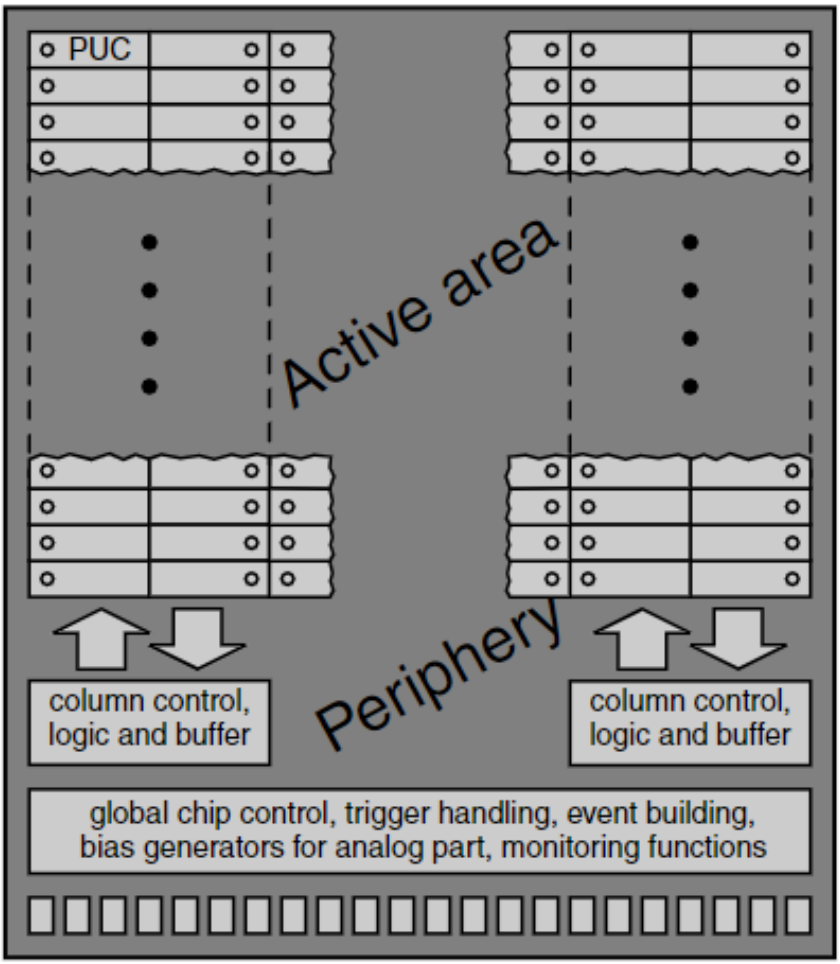

Fig. 2.1 Origanization of a generic pixel chip. [43]

The pixel unit cells (PUCs) are typically organized in columns, with power, bias, control signals and output data routed vertically, while few signals run horizontally. This column-based approach is advantageous for rectangular pixels due to some circuitry resource can be shared by two neighboring columns. As a result, less space is occupied in the PUC with bus signals, especially when only a few metal layers are available for routing. To reduce crosstalk between digital and analog sections and share circuitry between pixels, two columns are often grouped to form a "column pair". The column-based layout allows all signals to originate from the bottom of the chip, eliminating the need for circuitry on the side or above the active area. Therefore, there are no circuits between the top side of the pixel matrix and the top edge of the chip, and the distance between them can be made as small as possible. This spacing

depends on the manufacturing process used and the design rules dictated by process requirements.

The bottom part of a chip is typically separated into recurrent blocks that serve as an interface to the columns, a global control and bias division, and the wire bond pads. An analog test pulse generator is frequently incorporated on the chip to introduce predetermined charges into the pixels. The column interfaces distribute bias signals to the analog portions in the PUCs, also providing buffered digital control signals. They may also feature receivers and buffer memory for the data transmitted from the pixels. The process of buffering data until receiving a trigger signal can be quite intricate and space-consuming. The global control unit, at bottom part of Figure 2.1, is accountable for external communication. To save wire bond pads, it is common to use a serial protocol to download configuration data to the chip and transfer hit information from the chip to the data acquisition system (DAQ).

2.1.2 Simplified pixel detector model

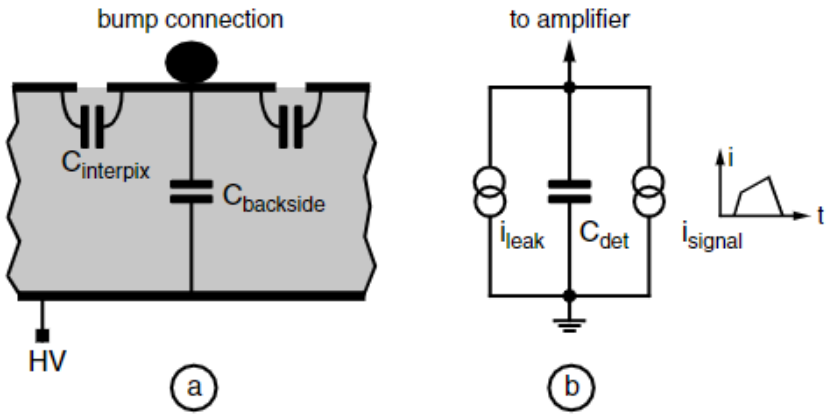

Fig. 2.2 A simplified semiconductor detector model. [43]

A pixellated semiconductor detector is represented by capacitances to the backside ($C_{backside}$) and its neighboring pixels ($C_{interpix}$), as illustrated in Figure 2.2(a). Although not entirely accurate, assuming the neighbor pixels are held at a constant potential by connected amplifiers allows for the summation of these two capacitances, leading to the effective detector capacitance C_{det} [13, 27, 28, 43, 51].

$$C_{det} = C_{backside} + C_{interpix} \tag{2.1}$$

An essential quantity for circuit analysis, C_{det} is the central element of the simple sensor circuit model presented in Figure 2.2(b). The model includes a constant current source to account for the fraction of the sensor leakage current flowing into the central pixel. As electron-hole pairs form in the detector volume, they drift to the electrodes under the influence of the electric field generated by the bias voltage. A time-dependent current source models the signal induced on the pixel and its neighbors during the charge motion.

2.1.3 Architecture of a generic pixel unit

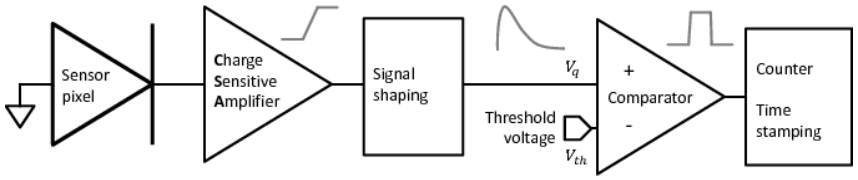

Fig. 2.3 Components of a generic pixel unit circuit.

The diagram presented in Figure 2.3 displays an architectural representation of a typical pixel unit. There are various circuit components that generally exist in the basic units of the active portion of the chip, e.g., charge-sensitive amplifier, shaper, discriminator and so on [51–54]. Initially, the signal that arises from the pixel's input pad is captured and amplified through a charge-sensitive preamplifier. Following this step, a band-pass filter is employed to improve the signal-to-noise ratio. As this filter alters the time response, it is known as a pulse shaper. The output from the shaper are evaluated against one or more thresholds with comparators. Afterward, the comparator output signals are delivered to the digital processing section within the pixel. Herein, the processed data is temporarily held before being communicated to the readout electronics located off the chip.

2.1.4 Analog front-end

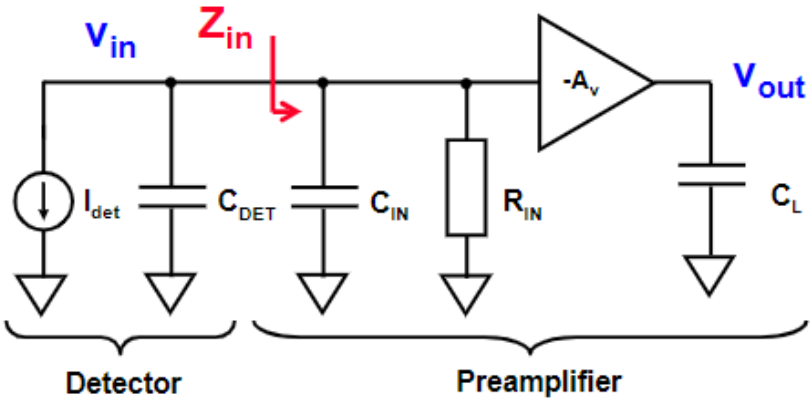

Fig. 2.4 A block digram of a generic preamplifier's structure.

The Charge Sensitive Amplifier (CSA) operates based on a fundamental principle, as illustrated in Figure 2.4 [55–58]. The detector is represented by a current source I_{det} running parallel to the detector capacitance, C_{DET}. Meanwhile, the preamplifier is characterized by a voltage amplifier that features a feedback capacitor C_F as shown in Figure 2.5. The feedback circuit removes signal charges from the input node or C_F after a response of the amplifier. It is essential to have a sufficiently slow discharge if additional filtering is utilized to prevent pulse degradation caused by the falling edge of the preamplifier output signal. Conversely, it is critical to discharge fast enough to avoid saturation or nonlinearities at the maximum allowable hit rate. It is possible to express the output of the preamplifier as a function of input voltage in this circuit,

$$V_{out} = -A_V V_{in} \tag{2.2}$$

then the voltage for the feedback capacitor can be represented by:

$$V_C = V_{in} - V_{out} = V_{in}(1 + A_V) \tag{2.3}$$

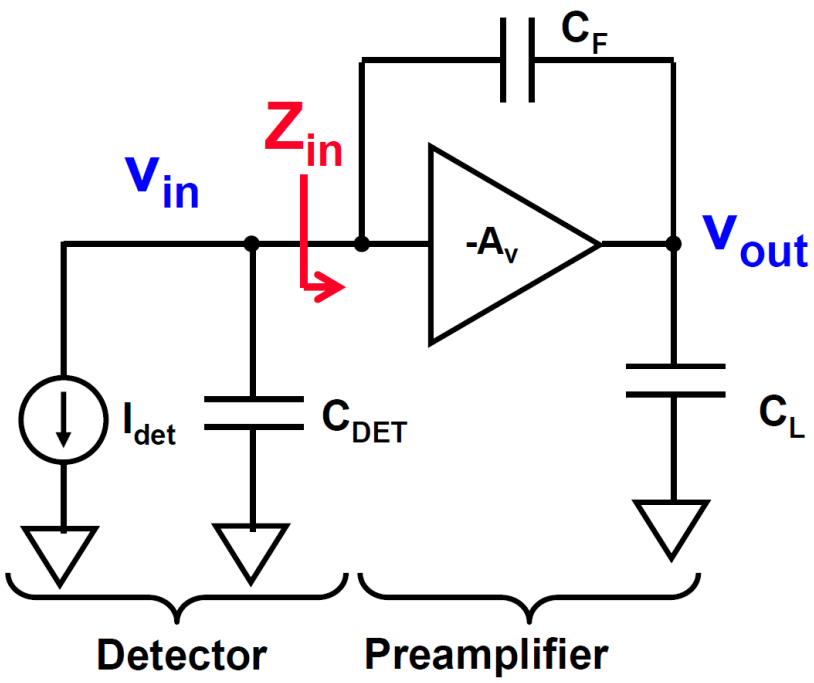

Fig. 2.5 Principle of the charge sensitive amplifier.

The charge collected by the feedback capacitor C_F from the input node is equivalent to $C_F(1+A_V)V_{in}$, thus resulting in a circuit that has an equivalent input capacitance of $C_F(1+A_V)$. Figure 2.5 shows the simplified model derived from this concept, where $C_{in} = C_F(1+A_V)$ and R_{in} represents the input impedance of the voltage amplifier circuit. Assuming these conditions, the voltage can be calculated at the input node due to a pulse in the current I_{det}:

$$V_{\text{in}} = \frac{Q}{C_{\text{total}}} = \frac{\int I_{\text{det}}(t)dt}{C_{DET} + (1+A_V)C_F} \tag{2.4}$$

and the output voltage is:

$$V_{\text{out}} = -A_V v_{\text{in}} = \frac{A_V \int I_{\text{det}}(t)dt}{(1+A_V)C_F} \cong \frac{\int I_{\text{det}}(t)dt}{C_F} = \frac{Q}{C_F} \tag{2.5}$$

The main conclusion of these equations is that the gain of the CSA depends solely on its feedback capacitance, given the high gain in the CSA amplifier to meet the condition $(1+A_V)C_F > C_{DET}$. As a result, the system becomes insensitive to technological and external parameters like temperature fluctuations.

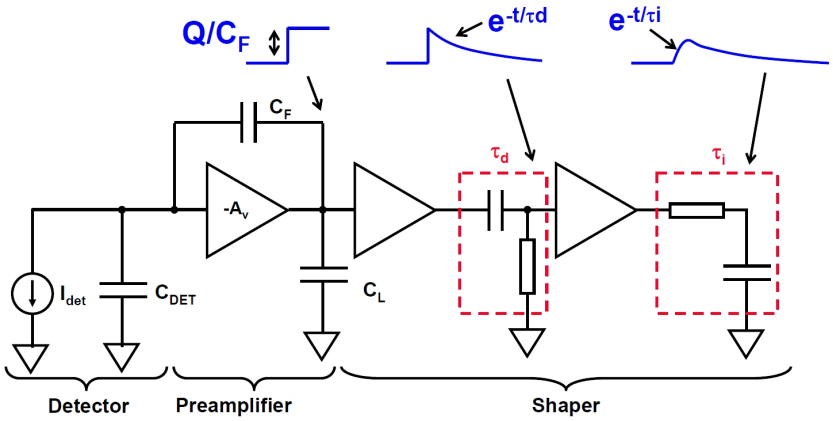

Fig. 2.6 Typical detector front-end circuit with a first order semi-gaussian shaper.

The preamplifier is responsible for providing input to a circuit that serves to customize the frequency response. This customization aims to optimize the overall system's response to suit a specific application. To achieve this, the output step of the preamplifier undergoes differentiation and is subsequently integrated n times. The purpose of this process is to enhance the signal-to-noise ratio and also to limit the pulse duration. By doing so, the system can efficiently process a new hit. The order of the shaper is defined by the number of signal integrations performed. In the circuit depicted in Figure 2.6, only one integration is carried out on the signal. This type of circuit is known as a first-order semi-Gaussian shaper, and its transfer function is given below,

$$H_{Shaper}(s) = \frac{s\tau_d}{1+s\tau_d}\frac{1}{1+s\tau_i} \tag{2.6}$$

where $\tau_i = R_i C_i$ is the time constant of the integrator and $\tau_d = R_d C_d$ is the time constant of the differentiator. The optimal value for maximizing the signal-to-noise ratio at the shaper's output is represented by,

$$\tau = \tau_d = \tau_i \tag{2.7}$$

2.1.5 Signal digitization

Time-over-threshold (ToT) is a measure of the duration of an electrical signal whose amplitude is above a certain threshold level, and it is commonly used in particle detectors to quantify the energy deposited by particles in the detector [59–61]. As described in the previous chapter, in most photon counting ASICs, *n* discriminators are used to compare the energy-proportional signal with *n* thresholds (Figure 2.7). Photons will be sorted into different counters based on their energy levels, thus obtaining the number of incoming photons in different energy ranges. In order to compensate for the intrinsic channel-to-channel offset mismatch and to set different threshold levels, each comparator is associated with a local on-pixel Digital-to-Analog (DAC) converter. ToT-based digitization technique is the most common used in PCD system.

In some pixel detector system Analog-to-Digital (ADC) converters have also been used for the digitization of the analog signal [62, 63]. Usually a peak-detect-and-hold circuit is incorporated into the channel processing chain is required. Or in some other cases an off-chip ADC was used to digitize the analog output. However, due to limitations in circuit area and power consumption, it is difficult for ADCs to achieve high resolution and high sampling rates. The microelectronics industry has shown a growing interest in successive approximation ADCs due to the need for low power consumption. The use of this ADC architecture could provide benefits for fine pixel pitch photon counting ASICs due to its low power consumption and small area.

2.1.6 Digital circuits

The digital signals produced by the discriminator undergoes further processing through circuitry located in both the pixel and the chip periphery. In certain medical applications, the determination of the number of particles absorbed in each pixel during a given time interval is necessary. As depicted in Figure 2.7., hit signals are counted in every pixel and read out after the measurement interval. Sometimes more than two discriminators and counters are implemented for spectral X-ray imaging. Additionally, some peripheral digital circuits are required for configuring the pixel matrix, reading data from the pixels' counters, and transmitting data out of the chip.

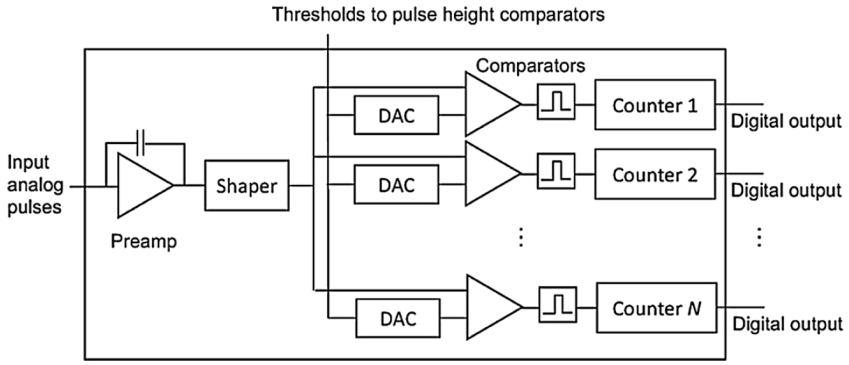

Fig. 2.7 Schematic block diagram of a general digital circuits in photon counting chips

2.2 Examples of PCD readout ASICs

Various research and design groups have developed diverse readout ASICs for HPC detectors, although these ASICs share the same fundamental operating principles, they vary in their specific design aspects, as they are tailored to different applications. this section introduces some example widely used ASICs alongside their distinctive features. For a more comprehensive overview, [10] provides additional information.

2.2.1 Medipix3

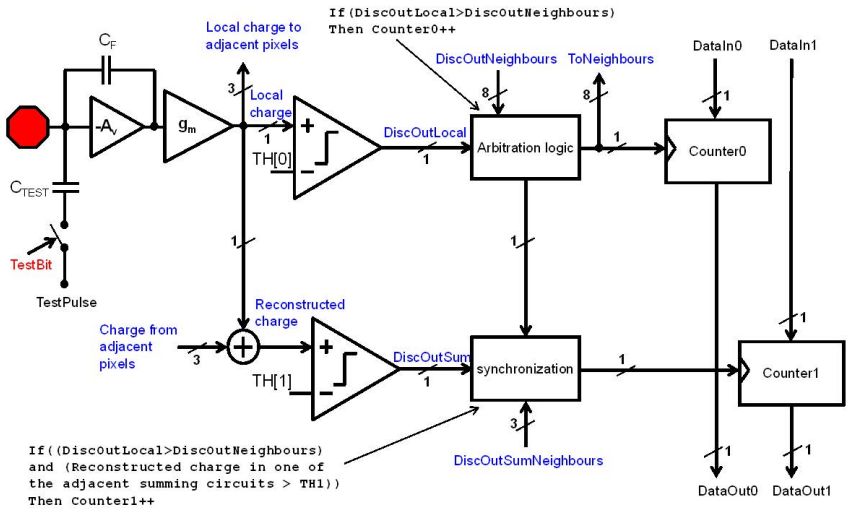

Fig. 2.8 Schematic block diagram of the Medipix3RX chip. [64]

Medipix3 is the third generation of the Medipix family of ASICs, which is developed by the european organization for nuclear research (CERN) in collaboration with several universities and research institutions [64–67]. The Medipix3 chip was fabricated with a commercial 0.13 μm CMOS technology. Its active area consists of an array of 256×256 pixels, each pixel has a size of $55 \times 55 \mu m^2$. One highlight of Medipix3 is the implementation of the charge sharing correction algorithm in each pixel. The charge deposited on each pixel is compared with the charges from its neighboring pixels using a network of arbitration circuits Figure 2.8. This network allocates the signal to the pixel that has the greatest charge deposit. Concurrently, summing circuits located at the corners between pixels reconstruct the charge in clusters consisting of four pixels (2×2 array). If a pixel displays the highest charge deposition among its neighboring pixels and if the charge in any of the adjacent summing circuits exceeds the predetermined threshold, a counter within that pixel is incremented. Medipix3 can also work with Spectroscopic Mode, in which a cluster of four pixel are grouped together as one single detector element with the size of $110 \times 110 \mu m^2$. In Spectroscopic Mode, eight thresholds are available when each unit works independently, four thresholds are available if charge reconstruction algorithm is active.

2.2.2 XPAD3

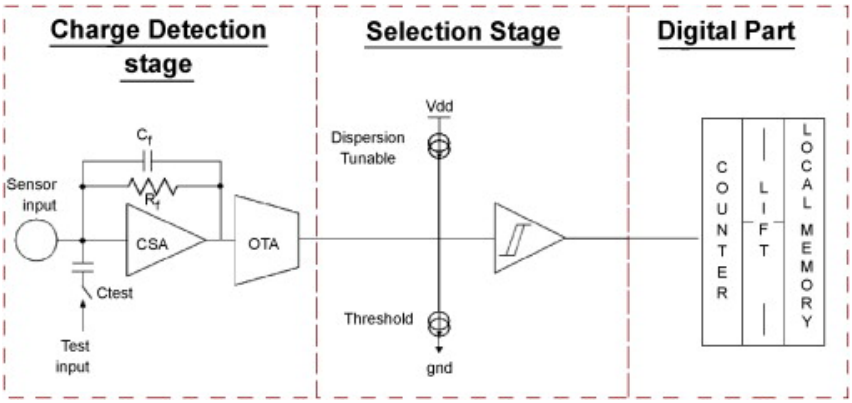

Fig. 2.9 Block diagram of the pixel front-end chain of XPAD chip. [68]

The XPAD series chip was developed by the electronics team of DELPHI experiment at CERN [68–71]. The third generation of photon counting chip XPAD3 was designed in IBM 0.25 CMOS μm technology, its active area contains 9,600 squared

pixels ($130\mu m \times 130\mu m$) divided into 80 columns. Its characteristics have been enhanced to deliver a high counting rate of over $10^9/mm^2/s$, a high dynamic range exceeding 60 keV, an exceptionally low detection noise level of 100 e^- rms, energy window selection capability, and quick image readout speed of less than 2 *ms* per frame. Two chip versions were developed to meet various experimental constraints. The S (as in silicon) version accepts holes as input and has a single threshold for energy selection, providing an energy range up to 35 keV. On the other hand, the C (as in CdTe) version accepts electrons, offering an energy range up to 60 keV through two thresholds for windowed energy selection. The windowed energy selection allows for effective filtering out of unwanted signals while retaining the desired ones. The digital component of the pixel comprises a 12-bit counter with overflow indication, a 9-bit configuration register, and a collection of registers that enable read and write operations to the pixel (Figure 2.9).

2.2.3 EIGER

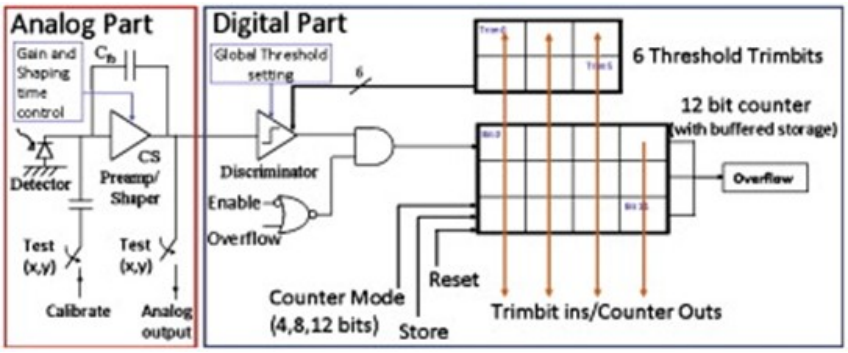

Fig. 2.10 Schematic representation of EIGER chip's architecture. [72]

EIGER is an upgrade version of PILATUS ASICs [73, 74] with improvements in several respects [72, 75, 76]. They were all designed by Paul Scherrer Institute (PSI) in Switzerland. EIGER was fabricated in UMC 0.25 μm cmos process, an array of 256×256 pixels was implemented. This device implements a pixel size of $75 \times 75\mu m^2$ with frame rates of up to 24 kHz. Each pixel is equipped with a 12-bit counter and a corresponding buffer, which allows for the storage and readout of a frame while new data is being acquired (Figure 2.10). Consequently, there is only a 3 μs dead time between two frames. These features make it ideal for use in diffraction experiments conducted at synchrotron sources. Furthermore, its high

frame rate enables successful performance of X-ray photon correlation spectroscopy on a sub-millisecond timescale.

2.2.4 miniVIPIC

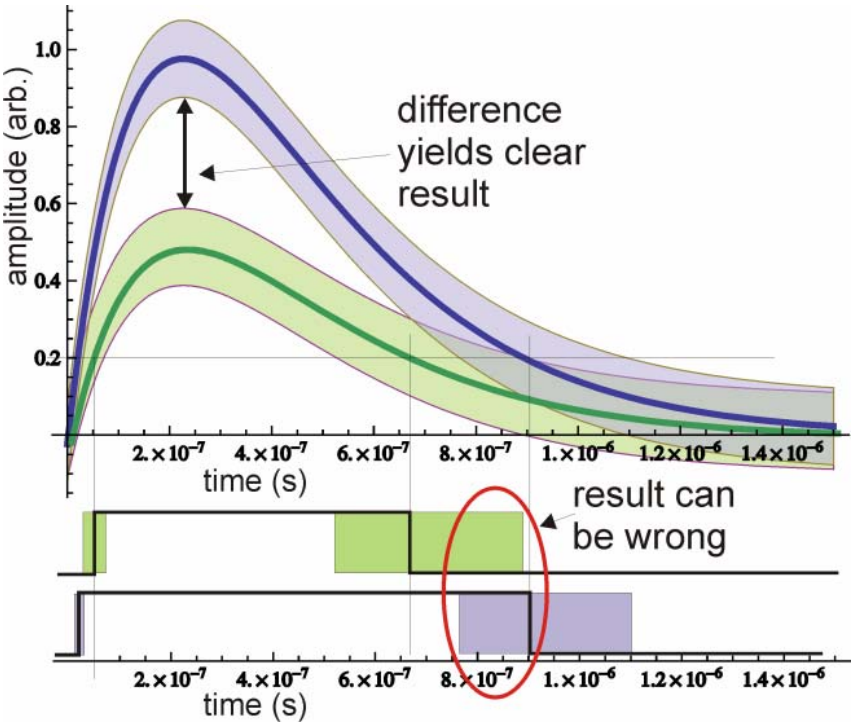

Fig. 2.11 Noise causes an overlap range in ToT signals. [77]

The miniVIPIC chip was designed by AGH University of Science and Technology and Fermi National Accelerator Laboratory [77, 78]. This chip was fabricated in a Low Power version of a 130 nm CMOS process, its active area consists of an array of 32×32 pixels, each pixel has a size of $100 \times 100 \mu m^2$. Two 10-bit counters are used for photon counting and energy selection.

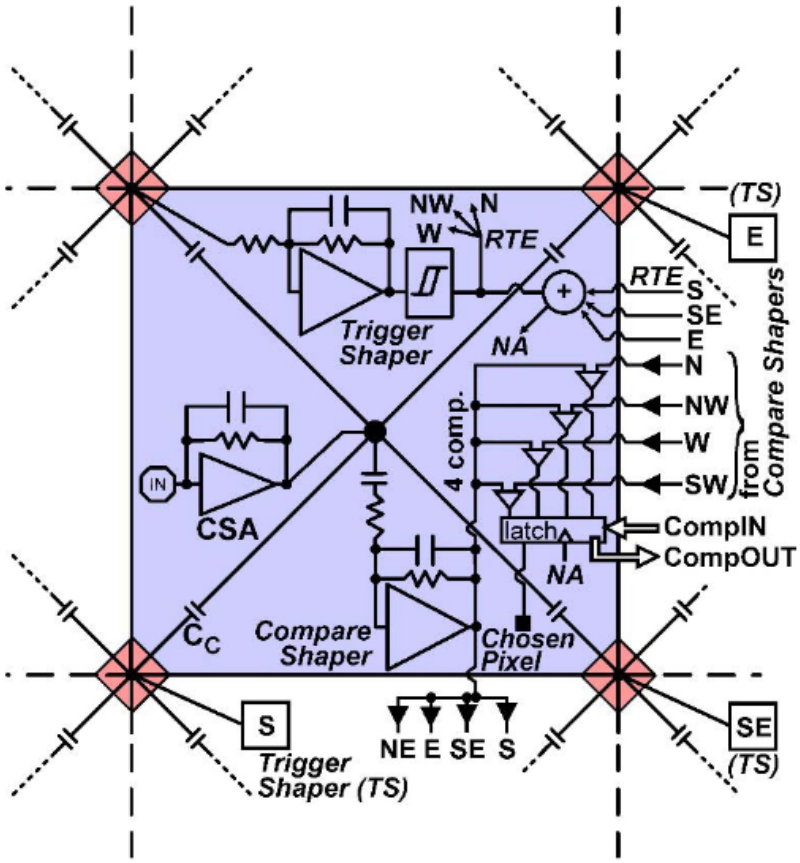

Fig. 2.12 Simplified block diagram of miniVIPIC's one pixel unit. [77]

As an example described in [77], noise could introduce an overlap range in ToT signals, the smaller signal can be misidentified as the the larger signal (Figure 2.11). An innovate algorithm called C8P1 [77–81] being a shorthand of "compare eight if one virtual pixel is above threshold" was implemented in miniVIPIC chip (Figure 2.12). It allows simultaneously for ToA measurements and handles charge sharing.

Chapter 3

Concept and architecture of METPC chip

The aim of this thesis is to design a photon counting chip that is capable of spectroscopic X-ray imaging with multiple energy thresholds and charge sharing correction. Conventional photon counting detectors experience two main limitations, namely the charge sharing effect and implementing multiple thresholds in a limited pixel area (usually is smaller than 150 μm). A Multi-Energy Thresholds Photon Counting (METPC) chip was developed under the INFN ARCADIA project framework to address these challenges. The primary objective of the METPC chip is to calibrate the charge-sharing effects on small pixelated sensors while simultaneously allowing 4 digital programmable thresholds to be achieved, complete with corresponding 12-bit counters, all within a very compact $110\mu m \times 110\mu m$ pixel area. This chapter will provide an overview of the reasons for developing the METPC chip, along with its architecture and implementation details for the pixel matrix as well as one pixel's circuit.

3.1 ARCADIA project

The design of the photon counting readout chip presented in this thesis was accomplished under the framework of Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays Research (ARCADIA) project [82–85]. ARCADIA is an INFN project aims at developing a new CMOS sensor platform that

operates in full depletion mode, making charge collection only by drift, which provides faster collection time than currently available MAPS based on charge diffusion, such as ALPIDE. ARCADIA builds upon the legacy of the prior INFN project SEED, with the goal of creating solutions for sensor thicknesses within the range of 50-500 μm that feature small charge collecting electrodes to optimize the signal-to-noise ratio. One of the main advantages of ARCADIA over state-of-the-art technologies is its reduced power consumption, being lowered to 10 mW/cm^2 [83]. The project utilizes a standard 110 nm CMOS technology (quad-well PMOS and NMOS) with a customized process for a patterned backside, developed in partnership with LFoundry. ARCADIA prioritizes scalability as the primary development criterion and is among the key projects in Europe working towards improving next-generation monolithic CMOS devices.

3.1.1 Arcadia monolithic sensors concept

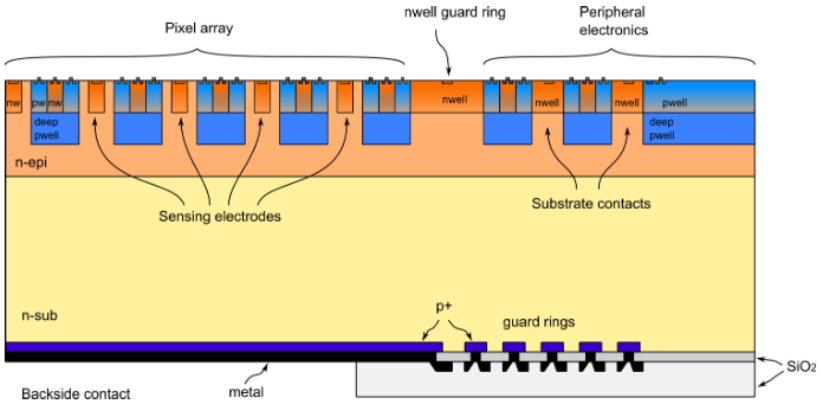

Fig. 3.1 The cross section diagram of the ARCADIA monolithic sensor. [82]

The ARCADIA project is working on developing fully depleted monolithic active pixel sensors (FD-MAPSs) featuring an innovative sensor design that utilizes backside bias to improve charge collection efficiency and timing under a wide range of operational and environmental conditions[82]. The sensor's design is based on a modified 110 nm CMOS process which integrates a low-doped n-type silicon active volume with a p^+ region positioned at the bottom as shown in Figure 3.1. There are two alternative methods for fabricating this structure, depending on the thickness of the active volume. Thick sensors, with a depth exceeding 100 μm, will be pro-

duced utilizing high-resistivity n-type substrates. Conversely, thin sensors less than 100 μm wide will be developed using low-doped $n-on-p^+$ epitaxial substrates. After completing the processing of the front-side, the backside layers underwent double-sided lithography. The substrate was initially thinned and polished, and a backside p^+ region was implanted and activated using laser annealing. This process created a very shallow junction with a depth around 100 nm on the backside surface. This feature is advantageous for visible light imaging in the blue spectral region and X-ray detection. To prevent early breakdown at the borders of the p^+/n^- substrate junction, termination structures with floating guard rings were incorporated. The $p-n$ junction sits on the underside of the sensor, resulting in the depletion region commencing at the reverse surface with an increase in bias voltage. Because of these FD-MAPS, it is possible to achieve low front-side supply voltages for standard analog and digital circuits and a fully depleted silicon bulk, allowing the electrode on top of the sensor to quickly detect drifting electrons.

3.1.2 Main demonstrator of ARCADIA

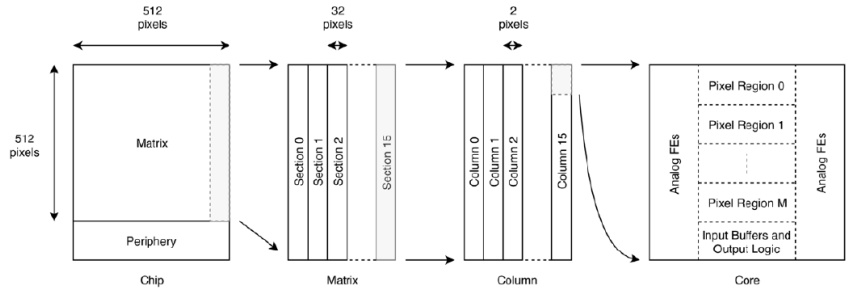

Fig. 3.2 Block diagram of the MD1 chip. [86]

The first main demonstrator (MD1) chip for the ARCADIA project was designed and fabricated in November 2020 [86]. The pixel matrix of the MD1 chip is comprised of 512×512 pixels, with each pixel measuring $25\mu m \times 25\mu m$. The pixel matrix is divided into 32 sections, with 16 columns grouped together to form a section. Each column's width equals two times the width of a single pixel (Figure 3.2). The cores of each column are sub-divided into 2×4 pixel regions, which are optimized to save area by sharing some resources (such as addressing, data muxing, bus arbitration logic, etc.). Every two neighboring pixels in the horizontal direction share the same digital circuit. The analog parts are symmetrically distributed at the two opposite

sides of the digital part. The MD1 chip can be "side-abutted" to accommodate a 1024×512 silicon active area, which measures $2.56 \times 1.28 cm^2$. The triggerless binary data readout mode allows an event rate of up to $10 - 100 MHz/cm^2$. The layout of MD1 chip is depicted in Figure 3.3, and the blue squares represent the sensor charge collection diodes that take up approximately 20% of the total active area.

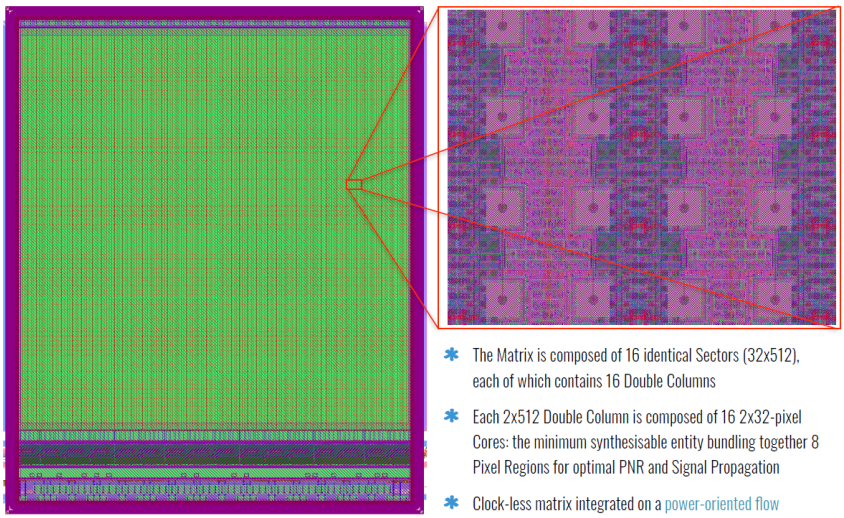

Fig. 3.3 Chip layout of MD1. [86]

The remaining area is shared equally by both front-end analog circuits and digital logic circuits. Data is propagated through the column to the periphery region of the chip while bypassing the inactive pixels. Each section (16 columns) is readout independently by following a dedicated serialiser and SLVS data link. The readout data is packed in the section output unit (SOU) (shown in the Figure 3.4), in which a 320 MHz DDR serialiser is implemented with 8b10b encoding. The MD1 chip has two working modes, High-rate and Low-Power modes. In the Low-Power mode, data from all SOUs are buffered in a central FIFO. The clocks to all SOUs but the SOU_0 are switched off, and all c-LVDS TXs but that of SOU_0 are closed. Only SOU_0 is used for sending out the data from the central FIFO.

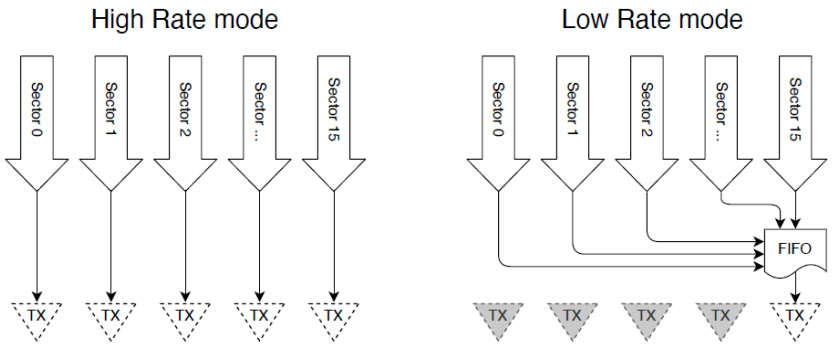

Fig. 3.4 Peripheral dataflow of MD1. [86]

3.2 Motivation for the METPC chip

The design of METPC chip is based on the ARCADIA project's technology. As explained in the previous section, the primary objective of the ARCADIA project is to develop monolithic pixel detectors with different thicknesses. METPC chip along with other chips from the ARCADIA project, shares the same wafer. METPC chip only requires modifications to the topmost layer in the modified Lfoundry 110 nm CMOS technology, which is used to create electrodes for charge collection (these electrodes can be used for bump bonding as well). This adaptation transforms METPC into a readout chip for hybrid pixel detectors. The sensor material can be silicon and CdZnTe.

METPC was specifically designed for application in spectroscopic X-ray imaging, aiming to capture extensive X-ray energy spectrum data simultaneously. The readout chip for spectroscopic X-ray imaging is required to have a minimum of 2 or more energy thresholds. Presently, mainstream readout chips typically feature pixel sizes ranging from 50 μm to 150 μm. This thesis' goal is to achieve multiple energy thresholds with a relatively compact pixel size. Taking various factors into consideration, e.g., the chosen CMOS manufacturing process (Lfoundry 110 nm CMOS technology), the required count rate for spectroscopic X-ray imaging (over $\times 10^8/mm^2/s$), achieving a spatial resolution of below 150 μm , having two or more energy thresholds with suitable counting depth, etc. METPC has chosen a pixel size of 110 μm and incorporated 4 energy thresholds with 12-bit conting depth.

The counting rate design specification for METPC is $3 \times 10^8 / mm^2 / s$, this counting rate is sufficient for conventional spectroscopic X-ray imaging applications. Translating to a counting rate of around 3.7×10^6 counts for each pixel per second. METPC operates with a readout frame rate of 1000 FPS, thus the corresponding counting rate for each threshold is approximately 3,700 counts per second. Consequently, each threshold requires a counting depth of at least 12 bits.

Another challenge that METPC needs to address is the charge-sharing effect. After photons interact with the detector, a large amount of charge is generated. Due to the difference in charge density and electrostatic repulsion between same charges, the charges will diffuse in space from the location where interactions occurred. During the drift towards the collection electrode under the influence of the electric field, the generated charge may move to neighboring pixels and be collected by adjacent pixels' electrodes, a phenomenon known as charge sharing effect. Charge sharing effect causes distortion in the energy spectrum and degradation in the spatial resolution [87–91].

3.2.1 Charge sharing effect in pixel detectors

The number of electron-hole pairs (n) generated by an interaction between an incident photon and a sensor is proportional to the deposited energy of the photon (E_{ph}) and depends on the detector material. Specifically, $n = E_{ph}/\varepsilon$, where ε is the average energy required to create an electron-hole pair by moving an electron from the valence band to the conduction band, leaving behind a hole (or vacancy) in the valence band. The value of ε is greater than the energy band gap of the semiconductor because some energy is lost through other processes, such as lattice excitations.

During the process of charge moving under the influence of the electric field, the distance between charges increases due to charge diffusion caused by differences in charge density, as well as electrostatic repulsion between charges of the same type. Considering only the effect of charge diffusion, the spatial extension (σ) of the charge cloud can be viewed as the standard deviation of a Gaussian distribution [13],

$$\sigma = d\sqrt{\frac{2k_BT}{qV_B}} \tag{3.1}$$

Table 3.1 Fluorescence photons' energies and mean free path for some commonly used semiconductor material.

Element	Z	K-edge [keV]	α_1 [keV]	α_2 [keV]	$d_{\alpha 1}$ [μm]	$d_{\alpha 2}$ [μm]
Si	14	1.839	1.74	1.739	11.86	11.86
Ga	31	10.367	9.25	9.225	40.62	40.28
As	33	11.867	10.54	10.508	15.62	15.47
Cd	48	26.711	23.17	22.984	113.2	110.7
Te	52	31.814	27.44	27.202	59.32	57.85

α_1, α_2 : fluorescence photons' energies
$d_{\alpha 1}$, $d_{\alpha 2}$: mean free path of fluorescence photons

where d represents the distance traveled by a charge, T is the temperature, k_B is the Boltzmann constant, q is the elementary charge, and V_B is the bias voltage applied to the detector. According to Formula (3.1), as an example, when the charge moves a distance of 320 μm and the bias voltage is set at 100 V under standard temperature conditions, the size of the charge cloud is 7.3 μm. However, according to the [74], the actual measured value of σ is 11.3 μm. The reason for this discrepancy may be due to the fact that the electrostatic repulsion between charges was not taken into account.

Furthermore, the percentage of the charge that is collected within a given radius R can be obtained by,

$$P_{\text{loss}} = 1 - e^{-\frac{qR^2E}{4KTd}} \tag{3.2}$$

where R is the radius of the charge cloud, E is the electric field q is the elementary charge, K is the Boltzmann constant, T is the temperature and d is the distance traveled by the carriers [92–95]. For instance, in a 2 mm CdTe chip with an electric field of 250 V/mm, about 90% of the charge generated near the cathode will be deposited within a region delimited by a radius of 62 μm in the segmented anode. Similarly, when the electric field is 500 V/mm, 90% of the charge is deposited within a radius of 44 μm. To evaluate the effect of charge diffusion on pixels, one must consider the dimensions of pixels in the system.

On the other hand, Table 3.1 summarizes the energies and mean free path of fluorescence photons for commonly used semiconductor materials in X-ray imaging. From the Table 3.1 we can see the mean free path ranges from 10 μm to 110 μm,

which is relatively large compared to the pixel size that is usually from 50 μm to 150 μm. The fluorescence photons can move from origin to neighboring pixels. Therefore, the correction for charge sharing must account for fluorescence photons.

Here are some examples of charge sharing effect simulations. As reported in [96], a 300 μm thick segmented Silicon $p^{+}n$ diode, reverse-biased with 100V, was used with Medipix2 chip to investigate the impact of charge sharing. A simulation was also carried out using a monochromatic 20 keV X-ray beam of 1 mm^2 in this research, adding a 190 e^{-} rms front-end electronic noise to the simulation. The simulated spectrum of the 20 keV X-ray beam was obtained on the collection electrode of a single pixel, as demonstrated in Figure 3.5.

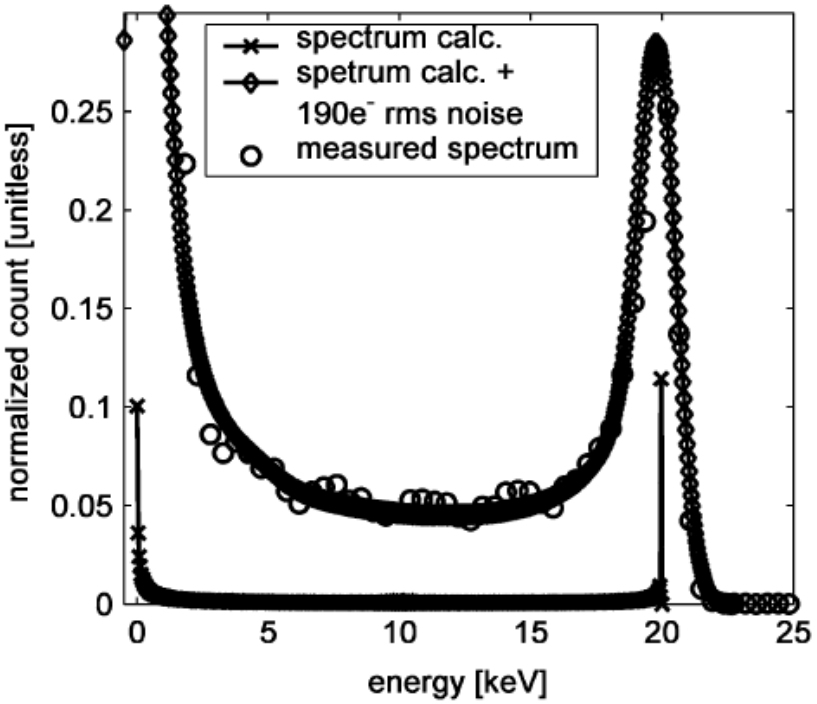

Fig. 3.5 A measured spectrum obtained with a monochromatic 20-keV photon beam of 1 mm, an additional charge sharing tail can be seen in the spectrum. [96]

The size of the charge cloud expansion depends on the depth of the interaction in the sensor. Only photons absorbed at the center of a pixel or extremely near to the collection electrode contribute to the full pulse height, while all other events are shared with neighboring pixels to different extents. Charge-shared events in the direct vicinity of the pixel resulted in the tail on the left of the energy spectrum. Reference [66] investigated a high-Z material, a 300 μm thick GaAs sensor. In high-Z materials,

even fluorescence photons can introduce distortion in the energy spectrum, resulting from depositing charges at some distance from the primary interaction. Figure 3.6 shows the simulation results of a 300 μm thick GaAs sensor segmented into 55 μm pixels. The simulation was carried out using a 20 keV monochromatic photon beam. The fluorescence photons of Ga (9.2 keV) and As (10.5 keV) present in the spectrum can be seen in the curve depicted by circles. Their mean free paths are comparable to the pixel pitch, being 42.62 μm for Ga and 15.62 μm for As (Table 3.1).

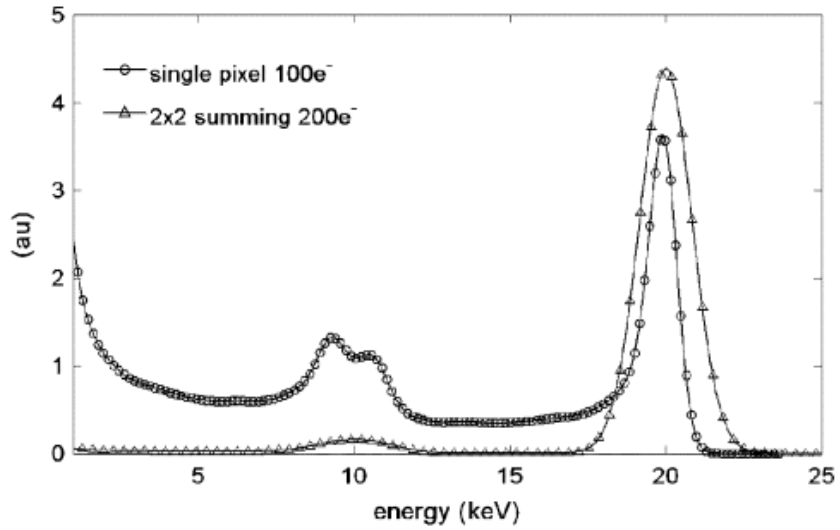

Fig. 3.6 A simulated 20keV spectrum obtained with a 300 μm thick GaAs sensor bump bonded to a 55 μm pixel pitch detector readout chip. [66]

In summary, the pixel size of METPC is 110 μm, when incident photons interact with the sensor material at the pixel edges or when the sensor thickness is more than 10 times of the pixel size, charge sharing occurs, which leads to a reduction in the sensor's energy resolution or erroneous counts. Therefore, it is necessary to consider charge sharing effect correction in the METPC chip. The next section will discuss in detail how to implement charge sharing effect functionality in each pixel circuit of METPC chip.

3.2.2 On-pixel charge sharing calibration in METPC chip

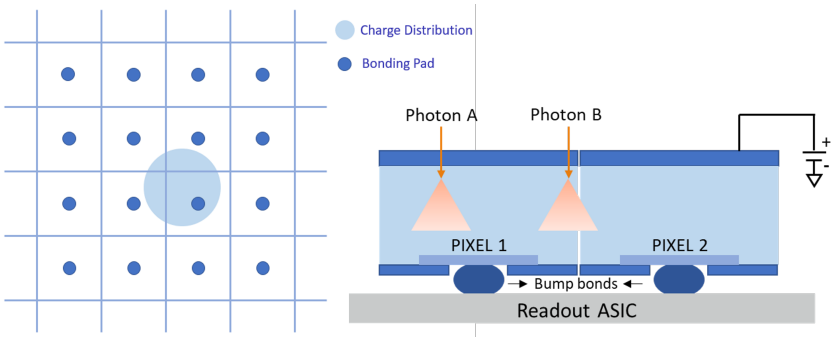

Fig. 3.7 Charge sharing happens within a range of four adjacent pixels at the condition of pixel size is 110 μm.

Based on the analysis of charge sharing effect in the previous section, and considering the pixel size designed for METPC chip is 110 μm. If a CdZnTe detector with thickness of 1mm will be connected to METPC, and 500 V/mm electric field is applied, the generated charge distributes within a circle that has a radius less than 50 μm. This means that we only need to consider charge sharing within four adjacent pixels. A charge collection node is implemented in every pixel in order to reconstruct the whole deposited energy in four adjacent pixels (as shown in Figure 3.8 left), which is currently the mainstream photon counting chip design.

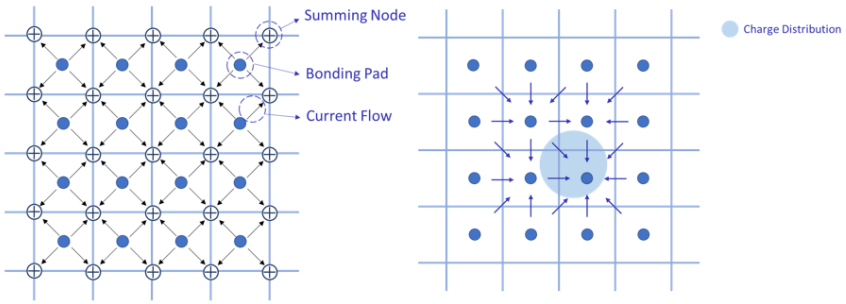

Fig. 3.8 Charge sharing correction is achieved by comparing ToT signals from a group of 9 pixels.

It is obvious that the pixel that collects the most charge is the one hit by the incoming photon. Charge sharing correction on each pixel is achieved by comparing ToT signals from different pixels. The charge collected by each pixel is amplified and shaped, then passed through a comparator to generate ToT signals, which are

sent to the adjacent pixels. Each pixel compares its ToT signal with the ToT signals of its surrounding eight neighboring pixels. The pixel with the maximum ToT signal is identified as the hit pixel. The charge generated by incident photons is fully collected and redistributed to the pixel was hit. However, the comparison logic is too complex, a ToT selection circuit is placed before the charge comparison to simplify the comparison logic and save more digital circuit resources, details are described in section 5.1 and in section 5.2.

Additionally, to reconstruct the entire deposited energy of an impinging photon, the analog circuit of each pixel adopts a two-stage amplifier structure (detals are discussed in Chapter 4). The output currents from the first-stage amplifier are transmitted to the summing nodes (second-stage amplifiers) of adjacent pixels. This process necessitates communication between analog current and digital signals (ToTs). A 6 μm wide routing channel has been allocated horizontally and vertically across each pixel to facilitate these interconnects. Figure 3.9 displays all incoming and outgoing inter-pixel connections.

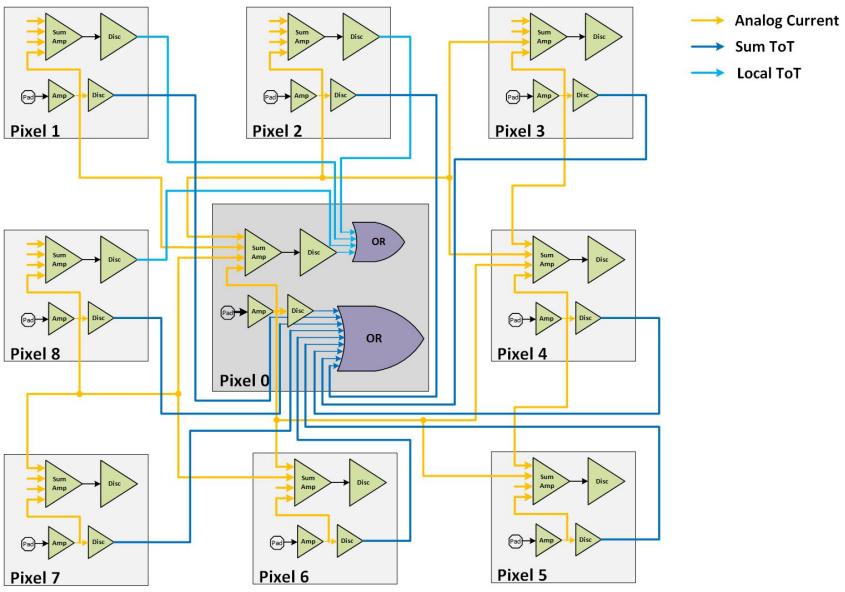

Fig. 3.9 An example of inter-pixel connections including both analog an digital signals

As shown in the Figure 3.9, pixel 0 has eight adjacent pixels from pixel1 to pixel 8, and each pixel contains a summing node (second-stage amplifier) to collect the charge collected by four surrounding pixels. The summing node of pixel 0 is used to collect signals generated by pixel 1, pixel 2, pixel 8, and pixel 0 itself, therefore the

analog current signals generated by the first-stage amplifiers of these four pixels will be transmitted to the summing node of pixel 0. The yellow lines in the Figure 3.9 represent the transmission pathways of the analog current signals.

There are four summing nodes around pixel 0 (including the summing node of pixel 0 itself). According to the working logic of charge sharing correction, any rising edge of the sum ToT signal outputted by any of these four summing nodes will trigger the charge sharing correction logical circuit to start working. Therefore, pixel 0 also needs to receive the sum ToT signal from other adjacent pixels, as shown in the Figure 3.9 by the dark blue line segment. The four sum ToT signals will pass through an OR-GATE unit (details about the OR-GATE uni are described in section 5.1) in pixel 0 to select the maximum signal to trigger the subsequent logical circuit.

The charge sharing correction implemented by the METPC chip is based on comparing the ToT signal of pixel 0 with that of the adjacent eight pixels, so the local ToT signal of the adjacent pixels needs to be inputted to pixel 0, as shown by the light blue lines in the Figure 3.9. The local ToT signals generated by pixel 0 and adjacent pixels are all inputted into an OR-GATE unit.

The output of the first-stage amplifier is split and transmitted to the summing nodes in adjacent pixels, as illustrated by the yellow wires in Figure 3.9. For this example, it is assumed that the current is sent to the summing nodes at the four corners of pixel 0, with summing node 0 belonging to this pixel. Since each pixel is compared with its neighboring pixels and the comparison relies on their ToTs, a ToT communication network is required for the charge sharing correction algorithm. The output of the local discriminator is conveyed to the eight surrounding pixels via light blue wires, as depicted in Figure 3.9.

However, there are some issues to address. For example, due to the convenience of design, the charge collection node will inevitably fall into the circuit of one pixel instead of designing the charge collection circuit after completing the pixel array layout. When the array size is large, this is almost an impossible task to accomplish. This will lead to different distances that the charge generated by each pixel travels to the summing node, resulting in differences in the arrival times of the charge at the summing node. This difference will cause a reduction in linearity of the amplifier output signal and result in errors. Ensuring that the charge transfer distance is as uniform as possible is a key research topic of this project. A digital-on-top design

method was adopted to address this problem. A set of signal path constraints were applied by the digital tools to ensure all signals will travel the same distance.

3.2.3 Digital multi-energy thresholds implementation

In spectral CT if the detectors have two or more energy thresholds or windows, it is possible to simultaneously image more than one contrast medium and distinguish between them. The incoming photons are sorted into appropriate energy bins according to their energies.

Figure 2.7 shows the basic architecture of multi-energy thresholds implementation. In each signal processing channel inside the readout chip, an amplifier collects and amplifies the generated charge from the corresponding pixelated anodes, the output of the amplifier is sent to a following shaper. The shaped signal is compared with N pulse height comparators. A count is registered in the counter associated with the given comparator if the pulse height exceeds the threshold value. Digital-to-analog-converters (DAC) allow for fine tuning of the threshold values for each channel as well as for compensating channel-to-channel offset variations through calibration procedures. Implementation of more than two energy thresholds is really a challenge for the chip design due to the CMOS technology and limited pixel area, the pixel size usually range from 55 μm to 150 μm [97]. It's really hard to place 4 or even more pulse height comparators in a analog way. The development of the METPC chip was also motivated by the desire to set multiple energy thresholds within a relatively small pixel area of 110 μm^2. In this thesis, a new approach based on ToT technique was developed. Instead of implementing the comparator in a analog way, four digital programmable comparators were designed.

In conventional photon counting detectors discriminators typically require analog methods, resulting in larger circuit areas and higher power consumption compared to digital circuits [98–101]. Implementing charge-sharing correction circuits and two or more energy thresholds within the limited pixel area of segmented pixel detectors presents a significant challenge for photon counting readout chip design. As mentioned in section 3.2, the charge comparison is often achieved through comparing digital ToT signals. This would avoid the use of comparators in the analog domain, saving circuit area and power consumption. METPC chip aims to further digitize ToT using a counter based method. The ToT signal is sampled with a

Table 3.2 Comparison of parameters between different photon counting chips.

	Medipix3	XPAD3	Pixie III	Pilatus3	METPC
Pixel size [$/mum^2$]	55	130	62	172	110
Energy thresholds NO.	2	2	2	1	4
Dynamic range	12 bit	12 bit	15 bit	20 bit	12 bit
Buttable sides	3	3	2	3	3
Technology node [nm]	130	250	160	250	110
Charge sharing correction [YES/NO]	YES	NO	YES	NO	YES

high-speed clock at each rising edge and converted into the number of clock cycles within the ToT duration. Based on the maximum event rate allowed for each pixel, the maximum length of the ToT signal is estimated to be below 320 ns. With a clock of 100 MHz, the counter depth only needs to be 5 bits. Then, by comparing the ToT count value (a 5-bit binary number) with four other digital threshold values (also 5 bits each), multi-threshold detection can be achieved. A 20-bit register are implemented in the digital domain to define these 4 digital thresholds, which can be easily programmed by sending new data to the threshold register when it is enabled to be written.

Integrating charge-sharing correction circuitry and 4 energy thresholds with 12-bit counting depth in 110 μm sized pixels is a capability not achieved by other photon counting readout chips. The details of the digital comparators is described in section 5.2. Table 3.2 lists various parameters of some widely used and mature photon counting readout chips. The rightmost column in the table represents specific parameters of the METPC chip. Although METPC does not have the smallest pixel size and falls in the intermediate range, it boasts the highest number of energy thresholds and charge-sharing correction capability. Additionally, the counting depth for each threshold in METPC has reached the mainstream 12-bit level, meeting the counting rate requirements for multi-spectrum X-ray imaging.

3.3 METPC chip architecture

METPC chip is divided into two main parts, core pixel matrix and peripheral circuits. All I/O padframes p are located at the bottom, and the I/O signals are connected to peripheral circuits. In this section the architectures of the full chip as well as one pixel unit are described.

3.3.1 Organization of the pixel matrix

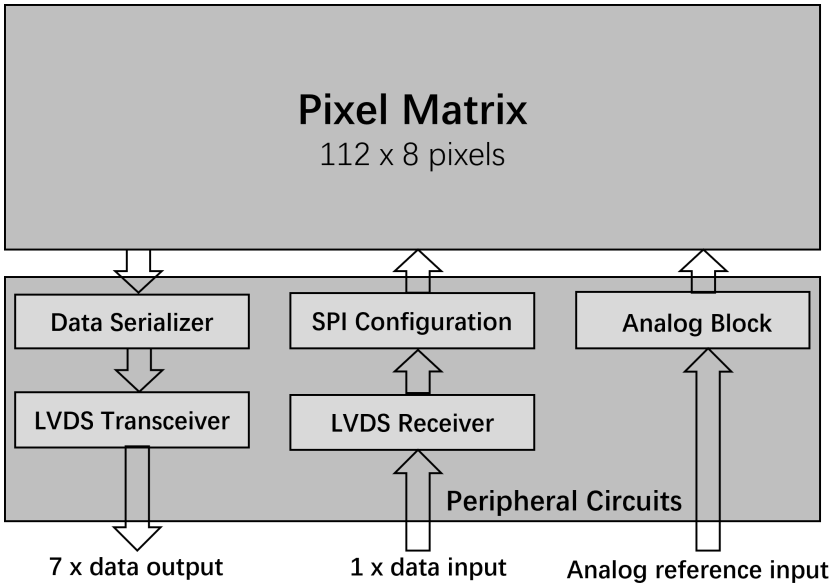

Fig. 3.10 Block diagram of the METPC chip.

The METPC chip's core is comprised of a matrix of 112×8 square-shaped pixels with a pitch of 110 μm (Figure 3.10). The peripheral circuit at the bottom of the chip contains a duplex serial peripheral interface block for pixel configuration and chip control, seven data serializers, seven I/O LVDS transceivers, one LVDS receiver, various analog blocks, and numerous power pads. The pixels are divided into seven super columns, each containing 16×8 pixels (with each super column having 16 sub-columns). Sub-columns in each group share the same data channel and are enabled for readout in a specific sequence. During the data readout phase, the energy bin counters in each sub-column form a shift register; the register content is loaded bit by bit to the peripheral circuits and shifted out via the LVDS transceivers. To ensure correct transmission of the data, an 8b10b encoding block and a 32-bit cyclic redundancy check code (CRC) block are implemented in each data channel. Analog block is used to provide bias voltages and other analog signals for each pixel's analog circuits.

3.3.2 Pixel unit architecture

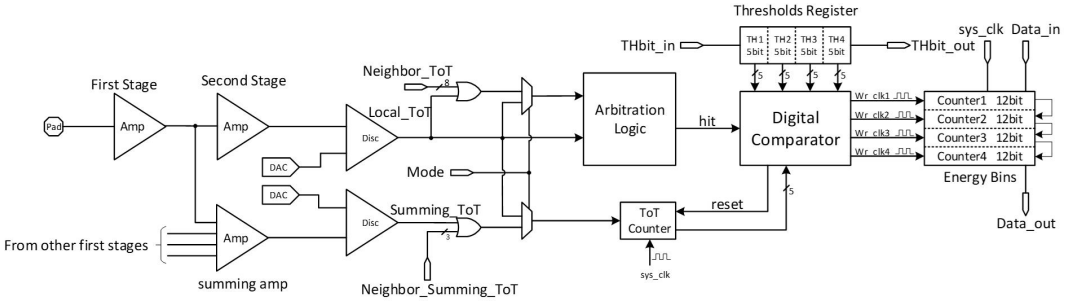

Fig. 3.11 Block diagram of a single signal processing channel architecture containing both analog and digital parts.

Figure 3.11 shows a diagram of the architecture of a single processing channel. The signal processing channel has two parts: the analog and digital domains.

In the analog domain, the charge collected by the electrode is processed by two stages of amplifiers, and the output of the second stage amplifier is discriminated. The output signal from the first stage amplifier is split into five paths, with one fed to the local discriminator, another to the local summing amplifier and summing discriminator, and the remaining three transmitted to the summing amplifiers belonging to adjacent pixels. The summing amplifier integrates the currents from the four surrounding pixels located at the center of a cluster of four pixels. Its purpose is to reconstruct the complete generated charge that is proportional to the energy deposited by the incident photon. The analog circuit includes two comparators, one generating the local ToT signal and the other generating the sum ToT signal. By comparing the local ToT of different pixels, the hit pixel is identified. The sum ToT is further converted into period counts and compared with digital thresholds.

In the digital domain, the arbitration logic module implements charge-sharing correction logic. It compares the ToT signals and identifies from which pixel the maximum ToT signal originates, confirming whether the local pixel is hit. The Digital Comparator module realizes 4 digital energy thresholds for spectral measurements. Each threshold can be reconfigured through a 5-bit configuration register, offering high flexibility. There is a corresponding 12-bit counter for each energy threshold, recording the number of incident photons within that energy range. Each counter utilizes a Linear Feedback Shift Register (LFSR) structure, enabling simultaneous

counting and readout without altering the counter structure, conserving significant circuit resources.

3.3.3 Working logic of the pixel circuit

Figure 3.12 presents a simplified timing diagram that illustrates how the digital logic operates. The rising and falling edges of the Shutter signal mark the start and end of a single photon counting process, respectively. When the Shutter signal is at a high level, the chip operates in photon counting mode. Conversely, when the Shutter signal is at a low level, photon counting ceases, and the chip enters the readout mode. During the readout phase, data recorded by each pixel's energy counters is sequentially read out. The ToT counter records the number of rising edges of the ToT clock in a specific time window equal to the duration of the ToT signal. The counting process ends with the falling edge of the ToT signal, and the state machine enters the comparison state in which the local ToT is compared with adjacent ToTs. Following the comparison, the ToT reset signal clears the contents of the ToT counter in the reset state. If the comparison yields a positive result, a hit signal is sent to the digital comparator unit. Here, the digitized energy is compared with four digital thresholds, and the event is assigned to an appropriate energy bin.

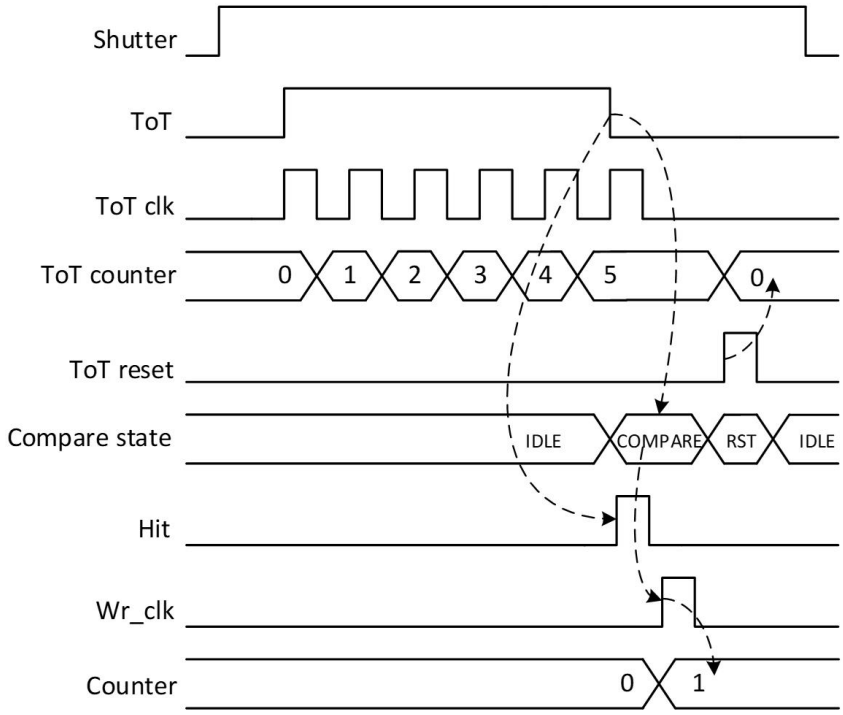

Fig. 3.12 Timing diagram for the working logic of METPC chip.

3.3.4 Layout of METPC chip

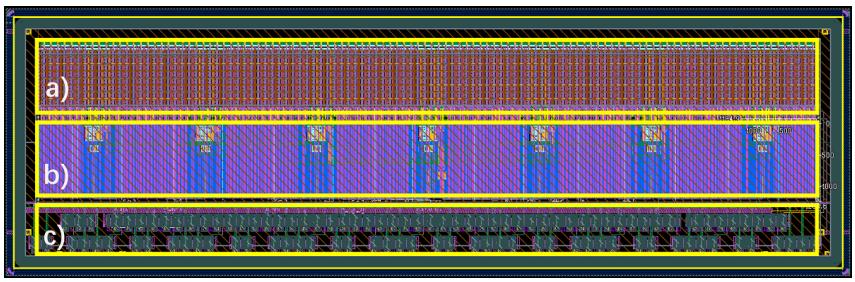

Fig. 3.13 Layout of the full chip. a) is the pixel matrix that contains 112 columns and each column has 8 pixels. b) is the peripheral circuits by which the SPI configuration, data transmission and receiving and analog bias blocks are implemented. c) is the double-rows padframes that are used for power supplies, analog bias input and digital I/Os.

The chip's layout has been submitted to the foundry for fabrication, the full chip layout that includes active circuits and padframes is shown in Figure 3.13, a) is the pixel array, b) is the peripheral readout and configuration circuitry, and c) is the

chip's padframes. The METPC chip uses a digital-on-top design method, where the analog circuit module is placed and routed as a part of the full chip layout by digital circuit design tools. The METPC chip design uses a 6-layer metal process in Lfoundry's 110 nm CMOS technology, which is available for wiring, clock networks, power, and ground networks for both analog and digital circuits. Metal layer 6, which is the highest metal layer, is oriented vertically and is used for analog bias voltage, analog and digital circuit power supply. Metal layers 5 and 4 are used to distribute the clock tree of the digital circuit. Metal layer 1 is mainly used for the supply of digital circuit transistors, while the other metal layers are used for signal routing. The clock tree of the METPC chip starts with the clock divider module output, and is distributed through the clock network to the peripheral circuits and pixel columns, while ensuring that the clock skew is minimized as much as possible.

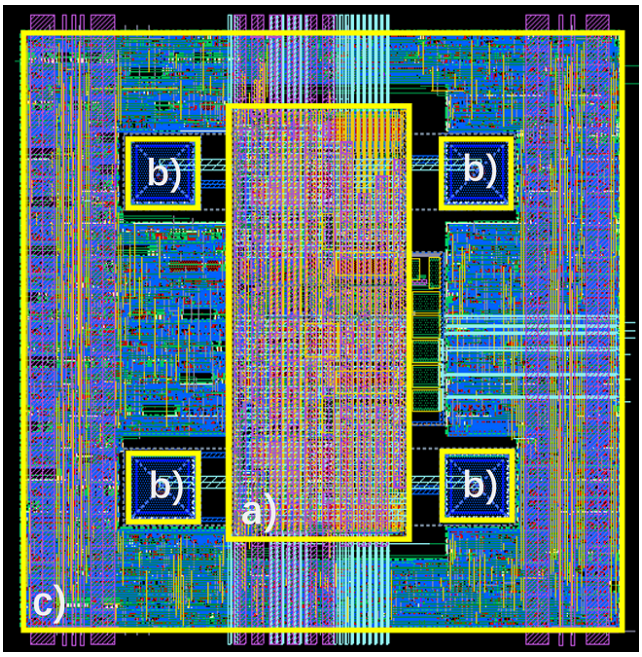

Fig. 3.14 Layout of a single pixel with a size of 110 μm $\times$ 110 μm. a) is the analog circuits placed at the center. b) are the 4 electrodes that are adopted for bump bonding connection to the sensor and for charge collection. The left area that excludes analog part and electrodes in c) is occupied by digital circuits. Gaps with width of 6 μm, black part outside the active area c), are reserved for inter-pixel communications.

Figure 3.14 presents the layout of a single pixel. The analog island is centrally located to optimize charge collection efficiency, while four square electrodes with the area of $20 \times 20 \mu m^2$ are situated at the corners of the analog section. Two versions of

the pixel exist: one with only electrodes, and another featuring a pad for external sensor connection. Since the charge sharing correction algorithm necessitates inter-pixel communications, gaps between pixels were intentionally reserved as routing channels for inter-pixel wire connections. To optimize connection resistance between the electrodes, digital electronics were inserted between them, resulting in analog islands between the digital electronics. To address cross noise between analog and digital electronics, several precautions were taken, including careful component placement, the implementation of guard rings to isolate analog electronics, separate power grids, and close attention paid to sensitive bias line placement. During this phase, the digital tool was used to automate the creation of the matrix and inter-pixel links required for the charge sharing algorithm. Special attention was also given to the placement of the three analog signals exiting the first-stage of each pixel and the three analog signals entering the global second stage.

Chapter 4

Analog Front-end circuits of METPC

When X-rays interacts with the detector material, it deposits energy in the form of electron-hole pairs within the material. The number of charge carriers created is proportional to the energy of the incident X-rays. Electric fields within the detector cause the free charge carriers to move towards the electrodes. The motion of charge carriers cause induced charge signals on the electrodes. The induced charge in each pixel is integrated over a certain period of time to create a measurable electrical signal. The digital electronics in METPC implement a charge sharing algorithm. Proper operation of this algorithm requires both locally collected charge (local-ToT) and the sum of three neighboring and local pixels (sum-ToT). To achieve these objectives, an architecture of two-stage amplifiers is adopted for the analog circuit. This chapter provides a detailed discussion of the analog circuit section of the METPC chip.

4.1 The first-stage amplifier

4.1.1 Architecture of the first-stage amplifier

Figure 3.11 shows that the first stage must generate five output signals to allow the second stage to produce the two signals required for accurate evaluation of total charge. To facilitate signal summing in the second stage, a decision was made to use current signals instead of voltage signals. Incorporating current signal operation mode rather than voltage signal operation mode is advantageous for signal summation, facilitating the second-stage amplifier to function as a signal integrator.

Thus, the output of the first stage is required to be in current mode. The block diagram of the first-stage amplifier is shown in Figure 4.1.

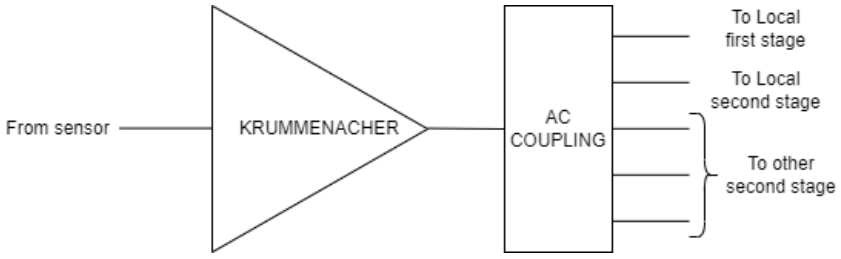

Fig. 4.1 Block diagram of the first-stage amplifier.

Figure 4.2 shows the schematic of the first-stage amplifier in transistor level. Since the Krummenacher stage transforms the current input into a voltage output signal [102, 103], five AC couplers were added, each based on one capacitance (6 fF) and one source follower, up to 600 mV can be transformed into current signals through the AC coupling circuits. This configuration generates the five current signals required. Additionally, in order to ensure that the digital circuits and the charger sharing correction logic work correctly, the global signal acts as a trigger and must always be greater than the local-ToT. To ensure compliance with this constraint, the system with AC couplers modifies the capacitance sizes so that the global ToT signals are always greater than the local-ToT signals. This design approach affects the linear relationship between local-ToT and sum-ToT, but it does not impact the linear relationship between the output and input signals of local-ToT and sum-ToT themselves. Local-ToT is utilized for comparison to determine which pixel is hit, while sum-ToT is used for energy measurement. Maintaining the relationship between the output and input signals for each ToT is crucial as they individually affect charge-sharing correction logic and energy resolution.

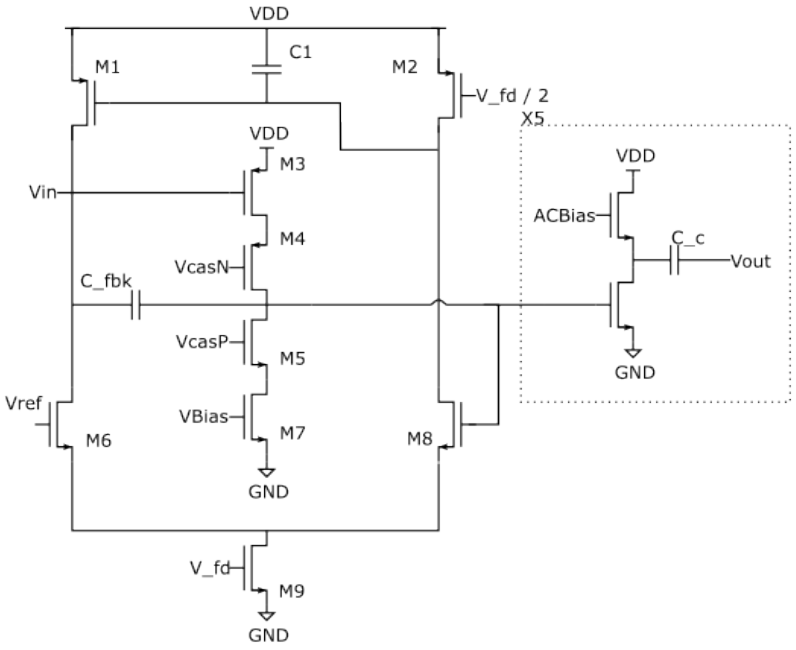

Fig. 4.2 Schematic diagram of the first-stage amplifier in transistor level.

To achieve better linearity of the analog front end's ToT signals, the first stage consists of a cascode core amplifier with Krummenacher-type feedback. The gain of this stage is 265 mV/fC, while power consumption is around 0.005 mW.

4.1.2 First-stage amplifier simulation

Before simulations, it is essential to understand the process by which signals are formed on the collection electrode to inject a simulation signal that closely resembles the real detector signal.

An electric field applied to the material causes free charge carriers to drift towards the collection electrodes, inducing charge signal on them. The variation in this induced charge over time, as the charge carriers move towards the electrodes, results in an electrical current. The induced current in the detector electrodes is calculated with the Shockley-Ramo theorem:

$$i(t) = q\overrightarrow{v} \cdot \overrightarrow{E_w} \tag{4.1}$$

where q is the charge of the carrier, v is its drift velocity and E_w is the weighting field. The weighting field is defined as the potential that would exist in the detector when the electrode under study is biased at unit potential, while all other electrodes are at zero potential. This weighting field determines how a moving charge electrostatically couples to a specific terminal. The induced charge is:

$$Q = -q\Delta V_w = -q[V_w(x_f) - V_w(x_i)] \tag{4.2}$$

Where ΔV_w is the difference in the weighting potential from the end of the path (the point in space where the carrier is collected) minus the origin (the point where the carrier is originated). In [97] the calculation of the induced charge in pixelated detector was carried out. Figure 4.3 illustrates the distribution of the weighting field. It is evident from Figure 4.3 that the weighting field significantly increases near the electrode, approaching zero elsewhere. Therefore, induced charges on the electrode only occur when the charge approaches the vicinity of the electrode. The generated signal closely resembles a step function

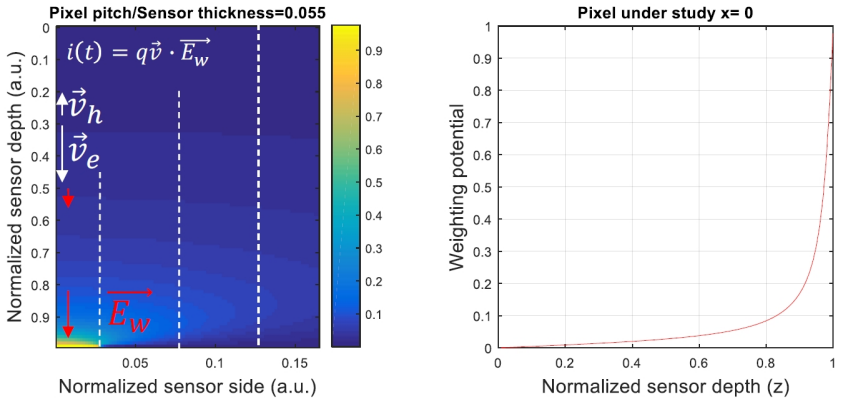

Fig. 4.3 Calculation of the weighting potential for a pixelated detector [97].

To simulate the analog circuits, an ideal capacitance of 20 fF was connected in parallel with an ideal current generator. A trapezoidal waveform that close to a step function was then transmitted to the first-stage amplifier for incoming particle event simulation. The charge released by incoming particles can be simulated by integrating the output current from the ideal current generator over time. Figure 4.4 displays the input current applied to the first-stage amplifier with a total charge of $1fC$.

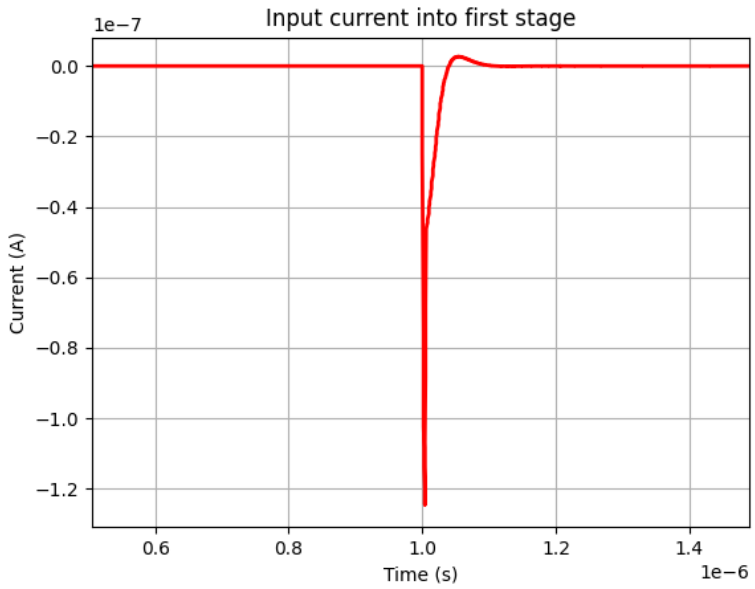

Fig. 4.4 A total charge of 1 fC was fed to first-stage amplifier for the simulation.

The first-stage amplifier's response to a 1 fC input charge is depicted in Figure 4.5. As previously described, the output from the first-stage Krummenacher amplifier is AC-coupled, as illustrated in Figure 4.1. This output is replicated for five separate paths that are transmitted to neighboring pixels for charge summing and sharing correction as shown in Figure 3.9 and Figure 3.11 . The first-stage gain is 265 mV/fC).

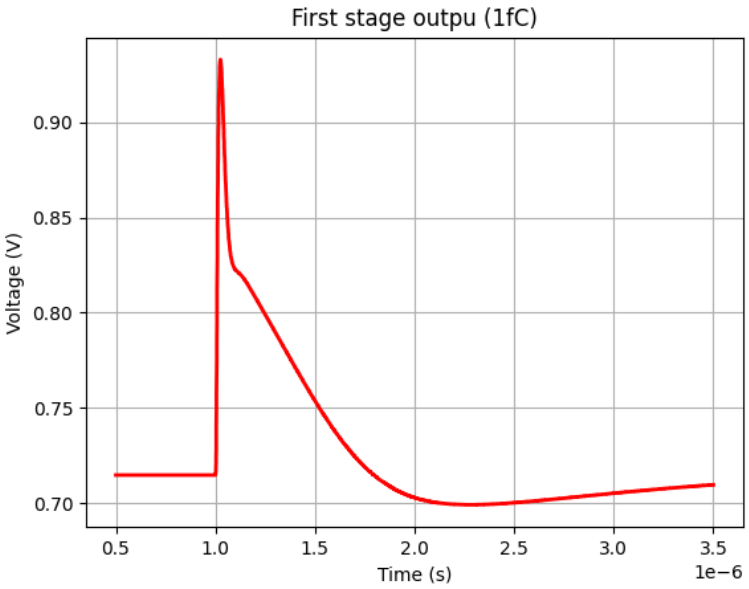

Fig. 4.5 Simulated output of the first-stage amplifier.

4.2 The second-stage amplifier

4.2.1 Architecture of the second-stage amplifier

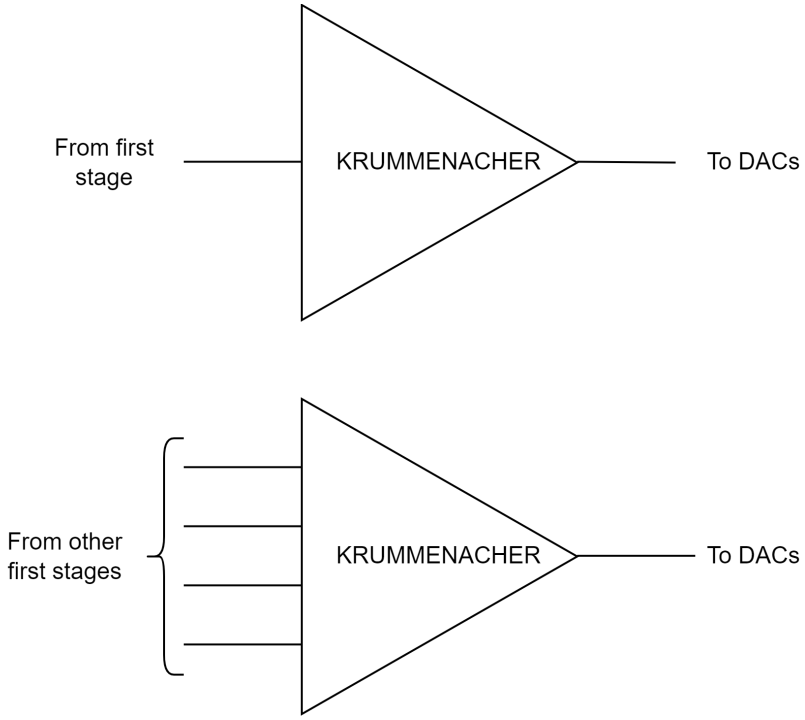

Fig. 4.6 Schematic diagram of the second amplifier.

The second stage (shown in Figure 4.6) consists of two separate amplifiers, as previously mentioned. Figure 4.7 illustrates the transistor-level schematic of the second stage's amplifiers. One amplifier generates the local ToT signal, while the other works as a summing node that receives current from first-stage amplifiers in the local pixel and three adjacent pixels. Both amplifiers feature large input current signals and two output voltage signals. They are connected to two discriminators for sampling and ToT signal generation. Given that the entire system uses ToT technique, the second stage amplifier shapes the signal, ensuring a linear discharge. Additionally, the charge sharing correction logic only operates when the sum ToT signal is in a valid state, and the charge sharing correction logic is working with comparing the local ToT with the ToT signals of surrounding pixels. If the sum ToT signal becomes invalid before the charge-sharing correction is completed, the judgment logic may produce incorrect results. Therefore, it is essential to ensure

that the sum ToT is greater than any local ToT signal. Although proportionality between local ToT and sum ToT signals is not essential, the second stage amplifier requires variable discharge time to guarantee that the sum ToT is always greater than the local ToT. This requirement necessitates that the sum signal discharges with a time constant greater than the local one. Therefore, a cascoded core amplifier with Krummenacher feedback was selected as it satisfies all the specified criteria with good linear discharge.

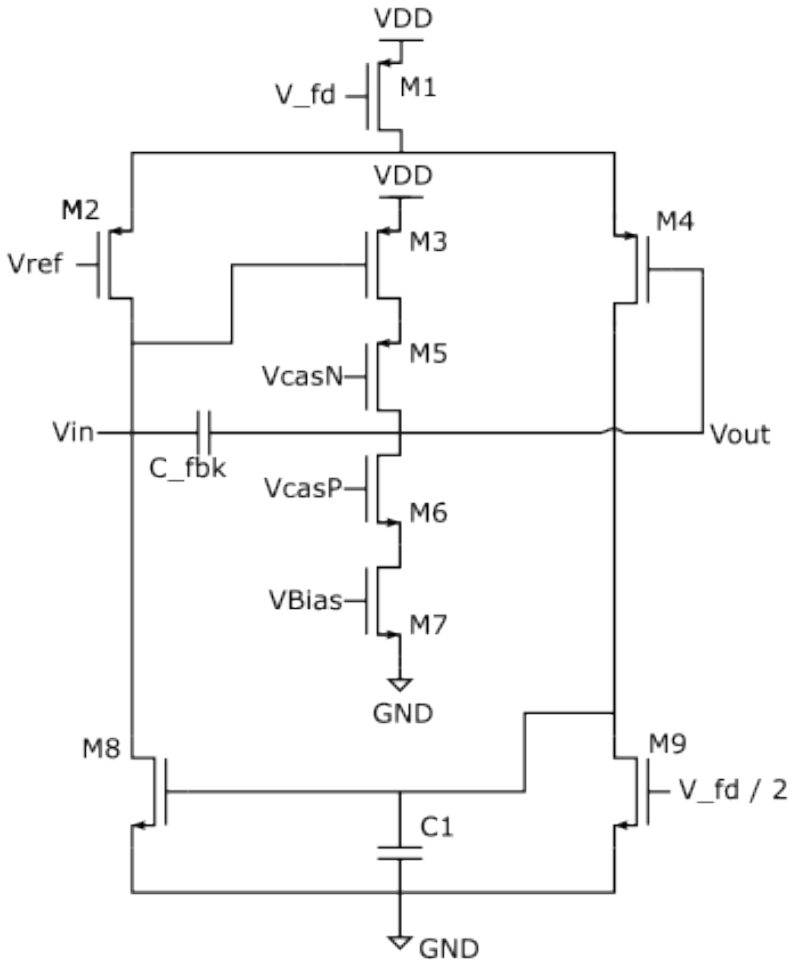

Fig. 4.7 Schematic diagram of the second amplifier in transistor level.

4.2.2 Simulation for the second-stage amplifier

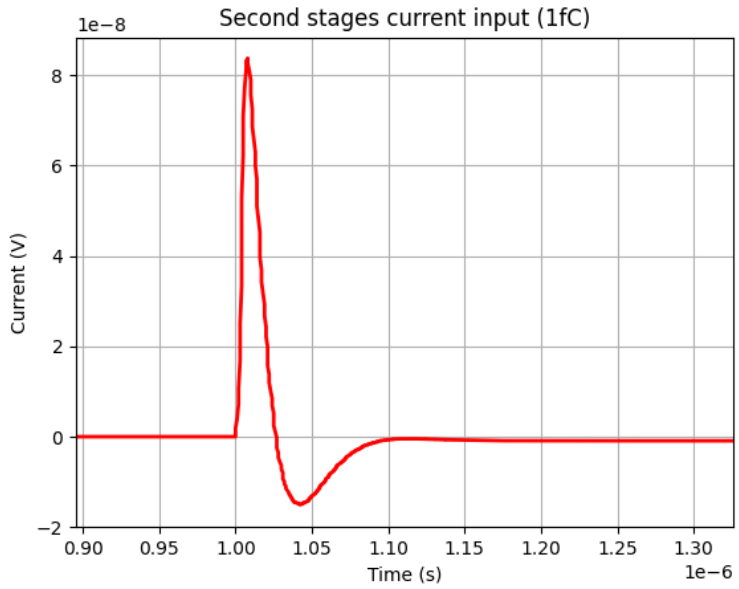

Fig. 4.8 Schematic diagram of the second amplifier in transistor level.

When charge is distributed among several pixels, the global amplifier (summing node) receives more charge than the local amplifier. Consequently, in such cases, sum ToT always exceeds local ToT. However, if no charge sharing occurs, local and global amplifiers theoretically receive the same input charge, which represents the most challenging scenario for this constraint. Figure 4.9 displays simulation outcomes for second-stage amplifiers with a 1 fC input charge at the start with assuming that all generated charge is collected by one pixel. The gain of the second-stage amplifier is 495 mV/fC.

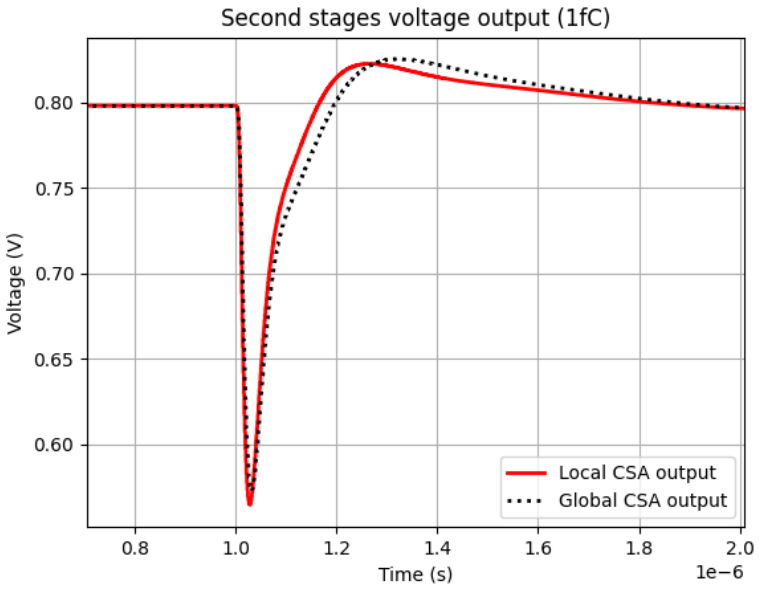

Fig. 4.9 Simulated output of the second amplifier.

4.3 Discriminator and DACs

Two asynchronous discriminators were implemented to digitize the output of the second-stage amplifiers, optimized for speed and low power consumption. In multichannel applications, transistor mismatches caused by production fluctuations in doping concentrations, oxide thickness, geometrical size, etc., can cause the threshold for a discriminator to vary from channel to channel. Baseline drift is a common problem that arises from countless factors that are difficult to control during the design phase. We addressed this issue by inserting two DACs (one for each discriminator) to generate the threshold voltage and eliminate variations. To enhance effectiveness, the DACs are programmable individually by digital electronics, allowing the threshold level to be set flexibly in accordance with different discharge configurations of the second stage. Krummenacher feedback is optimized to provide constant current discharge of the feedback capacitor to enable linear ToT measurement within the signal range of interest. After the second stages, two asynchronous discriminators are deployed to generate digital pulses for the pixel's digital part. The analog front-end can manage a rate of 350 kHz per pixel (it meets the requirements of the target

application discussed in section 3.2) with a power consumption of approximately 0.021 mW and an area of 2600 μm^2.

4.3.1 Simulation for discriminators

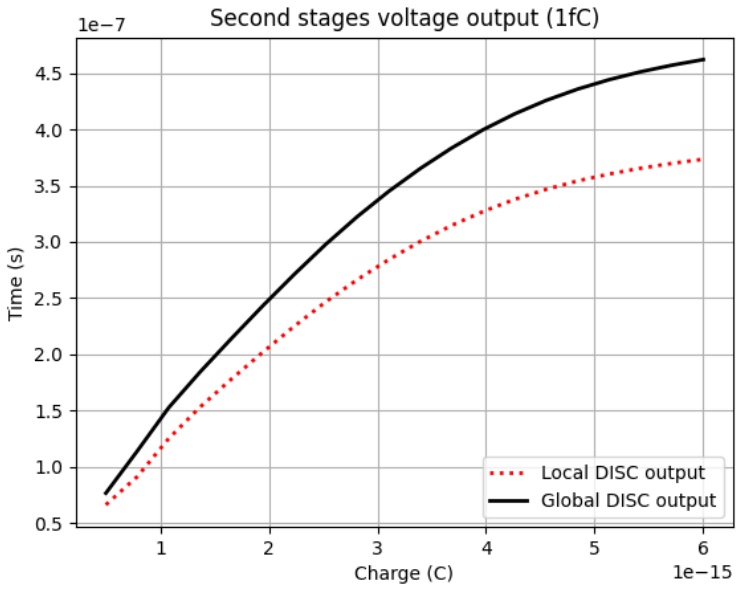

Fig. 4.10 Linearity simulation results of the discriminators.

Following the two stages of amplification, signals are transmitted to two asynchronous discriminators where they undergo ToT digitization. The duration time of generated ToT signals is determined by the discharge rates of the two amplifiers and the thresholds of the two discriminators. Outside the chip, a bias current can be employed to regulate the discharge rate. Figure 4.10 illustrates simulation outcomes demonstrating that an appropriate configuration for these amplifiers and discriminators ensures that sum-ToT is always greater than local-ToT. Furthermore, The maximum ToT signal that the digital circuitry can handle is 320 *ns*. The simulation results indicate a good linearity of the ToT signal in the range from 0 *ns* to 320 *ns*.

Chapter 5

Digital Processing Circuits

This chapter discusses the design details of various modules in the digital circuit part, and also describes in detail how the digital circuit logic implements the charge sharing correction algorithm and the implementation method of digital multi-thresholds. After a frame image's data is collected, the data stored in the energy registers will be read out on a column-by-column basis under the control of the readout peripheral circuitry, and all registers in a column will be chained together and read out bit by bit. The data is then sequentially subjected to 8b10b encoding, CRC check, data serialization and finally transmitted to outside the chip through an LVDS transmitter.

5.1 OR-GATE

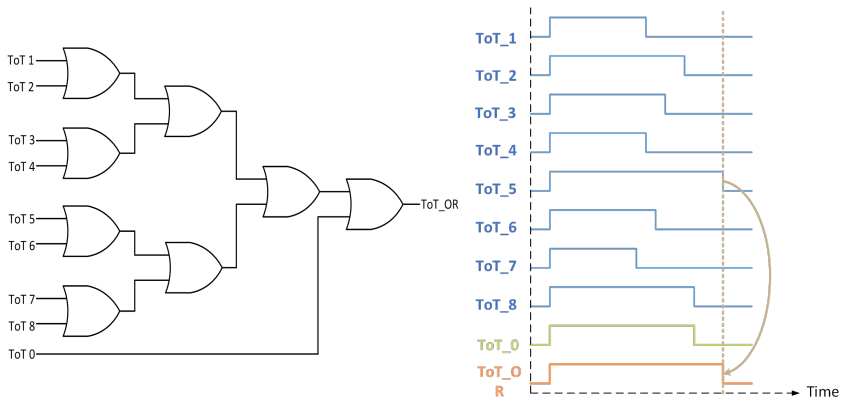

Fig. 5.1 The structure of the OR-GATE which can select the maximum signal from all inputs.

Table 5.1 Truth table for a standard two-input OR gate

Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Table 5.2 Propagation delay of OR gate with different input transition and load capatance

Input Transition [ps]	Load Capacitance [fF]	Propagation Delay [ps]			
		A to Q		B to Q	
		fall	rise	fall	rise
10.00	1.00	58.04	33.04	66.39	36.99
	300.00	406.13	557.92	413.56	563.06
2500.00	1.00	395.44	-43.64	315.89	27.75
	300.00	770.25	506.07	704.05	571.13

To simplify the comparison logic, two OR-GATE units were implemented, each constructed using several standard two-input OR cells (as shown in Figure 5.1) selected from the PDK library provided by the technology vendor. The function of the OR-GATE is to select the maximum of the nine input ToT signals based on the logic gate's standard functionality.

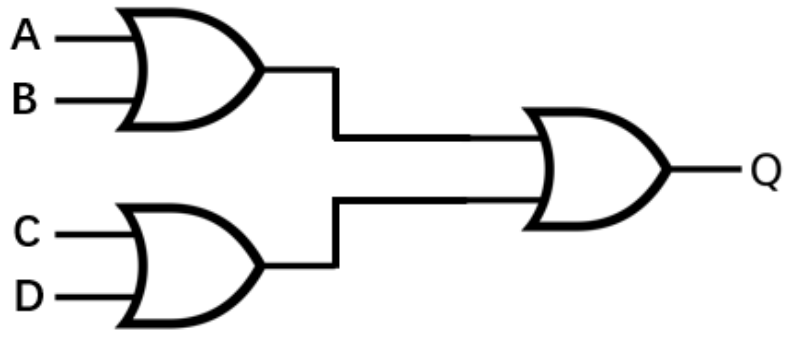

Fig. 5.2 A 4-input OR gate constructed with standart 2 input OR gate.

Table 5.1 is a truth table for a standard two-input OR gate. It can be seen from the table that as long as one input is 1, the output of the OR gate is 1. When two OR gates are connected in parallel as shown in the figure to form a 4-input OR gate. By extension, a 9-input OR gate can be formed, as shown in Figure 5.1. The

OR-GATE's output is high as long as at least one input is high, meaning that it rises with the arrival of the ToT signals and falls with the end of the maximum ToT input. As a result, the duration time of the output signal equals that of the maximum ToT. Consequently, rather than comparing the local ToT with eight neighboring ToTs directly, the comparison logic only needs to compare two signals: the local ToT and the OR-GATE's output. This significantly reduces the complexity of the comparison logic and saves a lot of circuit resources. The delay for each OR-GATE and interconnects between them is only several tens of picoseconds; thus cell delay and interconnect delay can be ignored given that the duration of the ToT signal is several tens or hundreds of nanoseconds. Table 5.2 shows the characteristic of delay and transition time of the OR cell used.

5.2 Comparison logic

The comparison logic determines the true hit pixel by comparing the ToT signals of different pixels. It assigns the collected charge generated by the incident photons entirely to the hit pixel, completing the charge-sharing correction process. The OR-GATE selects the maximum signal from all ToT signals. Hence, the comparison logic only needs to compare the local-ToT with the maximum ToT, significantly simplifying the comparison process. If the comparison result is positive, indicating that the local ToT equals the maximum ToT, it means that the local pixel shares the largest proportion of the generated charge and is thus the hit pixel. Figure 3.12 illustrates how the comparison logic works: the rising edge of sum ToT signals (i.e., the output from summing amplifier) triggers the comparison process, and the falling edge ends it.

There are two scenarios in the charge collection process. In one scenario, the charge generated by incident photons is entirely collected by a single pixel, without any charge-sharing effect. In the other scenario, the generated charge is collected by several neighboring pixels, leading to charge sharing. The following discussion will address these two situations.

- Isolated hit, meaning that the generated charge is spread within the area of only one pixel, and all of the charge is collected by that pixel. In this case, the OR-GATE has only one valid input, which is the ToT from the local pixel.

Therefore, the output copies the local ToT, and the result of the comparison logic is always positive (Figure 5.3).

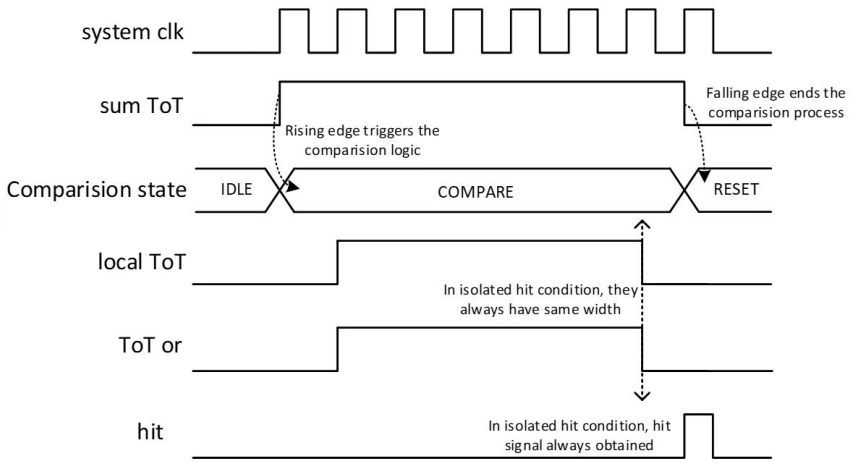

Fig. 5.3 When no charge sharing happen, i.e. isolated hit, local ToT always equal to ToT or.

- Charge shared by a group of pixels. The comparison logic operates simultaneously in every pixel, but only one winner emerges. If local pixel was hit by incident photon, it collects the maximum amount of charge. Consequently, the local ToT is the largest among all the surrounding pixels. The output ToT-OR of the OR-GATE is clearly of the same duration as the local ToT. At this point, the comparison logic will identify the local pixel as the one that has been hit, generating a hit signal (Figure 5.4). In another situation, when the local pixel is not the one that has been hit, its local ToT value is not the largest among all the surrounding pixels. The output ToT-OR from the OR-GATE is evidently longer than local ToT. In this case, the comparison logic will not identify the local pixel as the one that has been hit, no hit signal is generated (Figure 5.5).

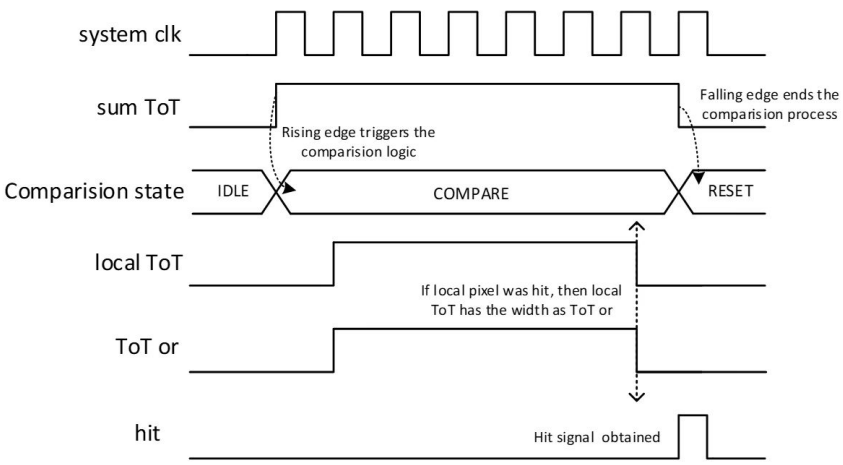

Fig. 5.4 Charge sharing happened and local pixel was hit.

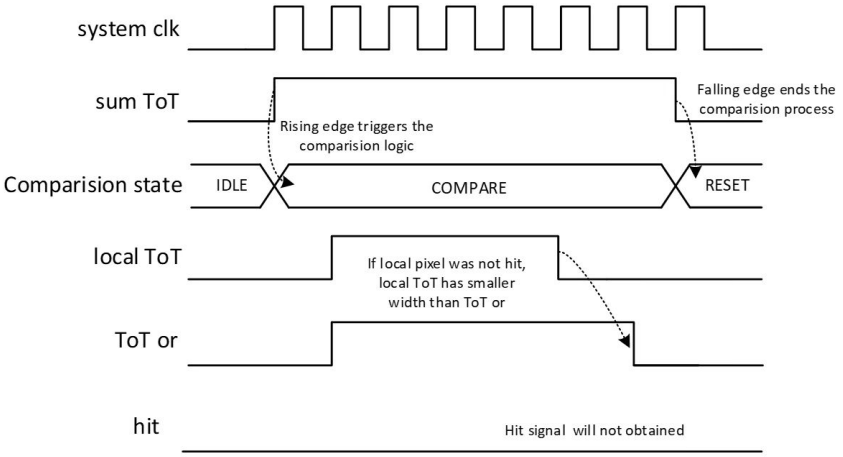

Fig. 5.5 Charge sharing happened but local pixel was not hit.

After the ToT comparison process ends, if the arbitration logic determines that the local pixel has the maximum ToT, it generates a hit signal indicating the current pixel is hit. Simultaneously, the comparison process ends, transitioning into the RESET state, waiting the start of the next comparison cycle. If the arbitration logic determines that the local pixel is not the hit pixel, no hit signal is generated, and it directly enters the RESET state. When the threshold comparison logic receives a hit signal, it triggers the digital threshold comparison process. In the RESET state the comparison logic is reset to the initial state as well as the ToT counter is cleared to 0. During the comparison process works, no photon is recorded, which means dead

time for the digital circuits exits. The dead time is determined by the duration of Sum ToT.

5.3 Digital programmable thresholds and on-pixel configuration

5.3.1 Digital programmable thresholds

The output of the summing amplifier is sampled by the ToT counter at the rising edges of the system clock in the digital domain to generate the summing ToT signal. This signal's content corresponds to the digitized energy, which is compared with four programmable digital thresholds that define the upper and lower limits of four energy bins. Twenty daisy-chained flip-flops provide the digital thresholds. X-ray photons are sorted into appropriate energy bins based on whether they fall above or below the different thresholds, depending on their energies.

5.3.2 Configuration registers

In addition to the 20-bit register defining the energy threshold, there are other configuration registers in the digital circuit of each pixel, including a DAC configuration register (8 bits), a mode selection register (1 bit), and a pixel mask register (1 bit). The digital energy threshold register is also part of the configuration register, with a total of 30 bits. When resetting all the configuration registers in a column, they are chained together, and the configuration data is transmitted from the bottom of the pixel column to the top, bit by bit, until all the registers are configured, as shown in Figure 5.6.

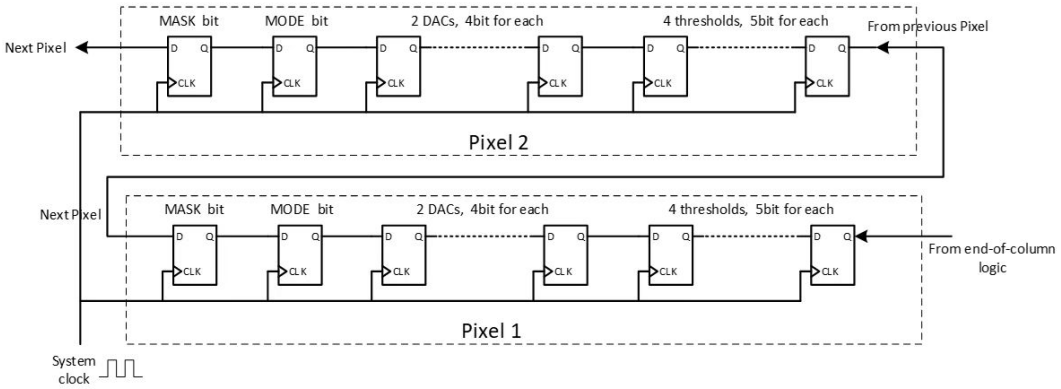

Fig. 5.6 Block diagram of the configuration registers.

5.3.3 Simulation of configuration registers

Each column of the METPC chip's pixel matrix consists of eight pixels, and the registers of these eight pixels are all connected to form a register with 8×30 bits. Therefore, in order to complete the register configuration of a column of pixels, the 8×30 bit data needs to be transmitted from the bottom of the column to the top. We have conducted simulations of the register configuration for a column, which is similar to the SPI protocol. When configuring the registers for each pixel, a control signal "select" is required, and the register configuration starts when the "select" signal is low. The input data is loaded into the register at every rising edge of the system clock, and the lowest bit of each pixel register is connected to the highest bit of the previous pixel register. The simulation results shown in the Figure 5.7 indicate the register configuration process for the top three pixels in a column, and all pixel registers have been correctly configured.

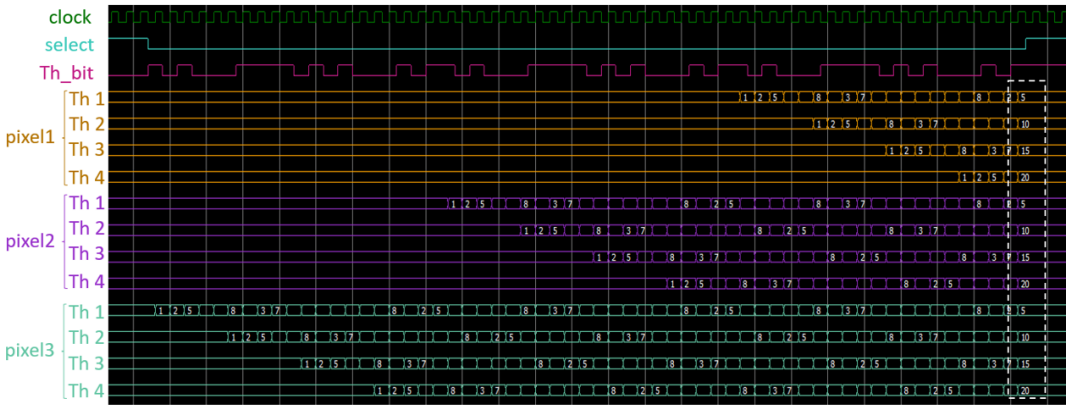

Fig. 5.7 Simulation of configuration registers.

5.4 Energy bins

5.4.1 Structure of energy bins register

Each pixel contains four 12-bit energy bin registers that are implemented using a linear feedback shift register (LFSR) structure [104–106], as shown in Figure 5.8. A LFSR consists of a series of flip-flops connected in a chain. The key feature of a LFSR is its feedback mechanism, which involves XOR (exclusive OR) operations between specific bits in the register. The feedback taps are predetermined positions in the register from where the bits are extracted and fed back into the input, influencing subsequent shifts. By carefully selecting these feedback taps, LFSRs can generate sequences of bits that, while not truly random, exhibit properties of randomness. These sequences are useful in various applications where a pseudo-random sequence is sufficient, such as in generating encryption keys, simulating random events, or testing digital circuits and checking data integrity. The XOR function produces a 1 if the inputs are different, and a 0 if the inputs are the same. The output of LFSR can be represented by a polynomial, for a 12-bit LFSR, the feedback polynomial is

$$f(x) = x^{12} + x^{11} + x^{10} + x^4 + 1 \tag{5.1}$$

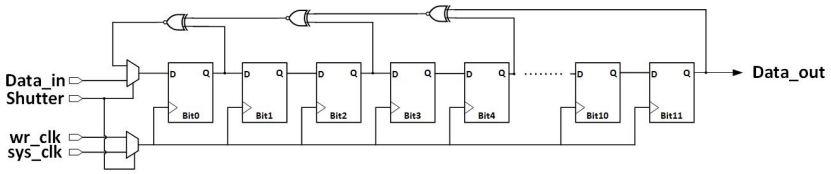

Fig. 5.8 The energy bin register is constructed with LFSR structure. It works in two modes that are controlled by switching the shutter.

In this study, we have undertaken enhancements to the LFSR, enabling its operation in dual modes. The benefit of doing this is that data recording and reading can be accomplished using the same register length, eliminating the need for additional registers and significantly saving circuit resources. Two multiplexers have been strategically integrated into the LFSR's input, both controlled by the same shutter signal as shown in Figure 5.8. One of these multiplexers regulates the input signal, while the other precisely controls the LFSR's clock signal, thereby optimizing its functionality in a streamlined manner. When the control signal shutter is low, the energy bin register operates in counting mode, with the output of the feedback circuit serving as the register's input. This input comprises a sequence of pseudo-random values determined by the XOR feedback circuit's feedback function.

Because of this feedback function, the pseudo-random data stored in the energy bin register must be decoded off-chip (Figure 5.9). The pseudo-random data generated by a LFSR is determined by coefficients of the feedback polynomial and the initial state. Once the feedback polynomial of an LFSR is determined, knowledge of the LFSR's initial state becomes essential for generating pseudo-random sequences accurately. Therefore, after each power-up of the chip, it is common practice to perform a reset operation on the LFSR, setting its initial state to a known value. This ensures that the subsequent pseudo-random sequences generated are predictable. The reset operation typically involves setting all bits of the LFSR to specific values, such as all zeros or all ones. This guarantees that the LFSR starts generating pseudo-random sequences from a defined state. The reset operation can be accomplished using a reset signal within the circuit or through a specific initialization process. This approach ensures that the LFSR is in a known state before it begins operation, enabling the generation of predictable pseudo-random sequences.

During the readout process, all these four energy bin registers in a pixel as well as other registers in the same column are chained together. The feedback circuit is disabled by setting the shutter to high, and all registers operate in their normal

state. The last bit of output from each energy register serves as the input for the next energy register. Consequently, the data stored in the registers is read out bit by bit in sequence.

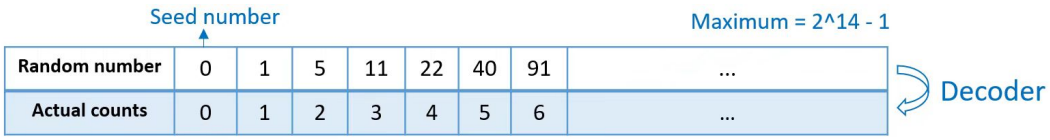

Fig. 5.9 LFSR requires off-chip decode.

5.4.2 Simulation setup and results of LFSR

As described in the previous section, the energy register has two working modes: counting mode and readout mode. In this section, we have conducted simulations to verify both modes. As shown in Figure 5.10 , when operating in counting mode, the shutter signal is low and the register is configured as an LFSR. The writing clock is provided by the front-end threshold comparison module. When the energy of incident photons falls within the energy range corresponding to a certain energy register, one cycle of writing clock will be generated, which will drive the LFSR to change accordingly. Before starting the counting mode, all registers must be reset and provide initial values for the LFSR, which is 0 in this case. After the shutter signal is pulled high, the energy register switches to readout mode.

Similar to configuring registers, in readout mode, eight pixels' energy registers in one column are daisy chained together and read out from the top to the bottom bit by bit. The Figure 5.11 shows the simulation results of energy register readout, which indicates that the energy register data can be read out normally in readout mode.

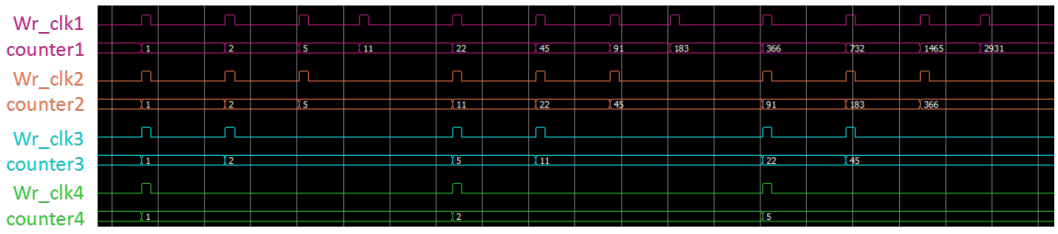

Fig. 5.10 Simulation results for the energy bin registers' counting mode.

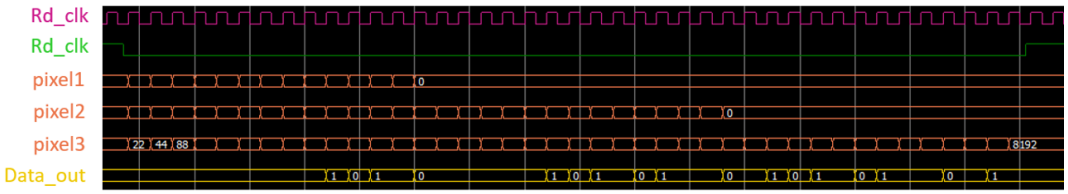

Fig. 5.11 Simulation results for the energy bin registers' readout mode.

5.5 Peripheral circuits

The METPC chip records the number of incident photons in different energy ranges within a certain time interval. Very similar to a digital camera, after a frame of data acquisition is completed, the recorded data from each pixel will be read out to the outside of the chip for further analysis and processing, and the data readout process is controlled by peripheral circuits. When the shutter signal is pulled high, the energy registers of each pixel and all registers on each column will be switched to the readout mode. In the readout mode all registers in the same column are chained together. At every rising edge of the readout clock, the data in the registers will be read out to the peripheral circuits bit by bit. The peripheral circuits first caches the data, then performs 8b10b encoding, CRC data verification and serialization conversion sequentially, and finally transmits the data to the back-end data acquisition system through LVDS transmitter.

The normal operation of each pixel requires correct settings of the configuration register, which is also completed by the peripheral circuits. The peripheral circuits receive the required configuration data through the SPI protocol, and then distributes it to the configuration registers of each pixel. At the same time, a data feedback function is also set in the chip to verify whether the configuration data is correct.

5.5.1 Data buffering

shown in the Figure 5.12, every 16 columns in the pixel array form a column section, and the pixel array is divided into 7 sections, with each section sharing the same readout circuitry. During data readout, the data of each column is read out bit by bit, and the columns are read out in sequence. One column section multiplexes the same 8b10b, CRC and serializer modules.

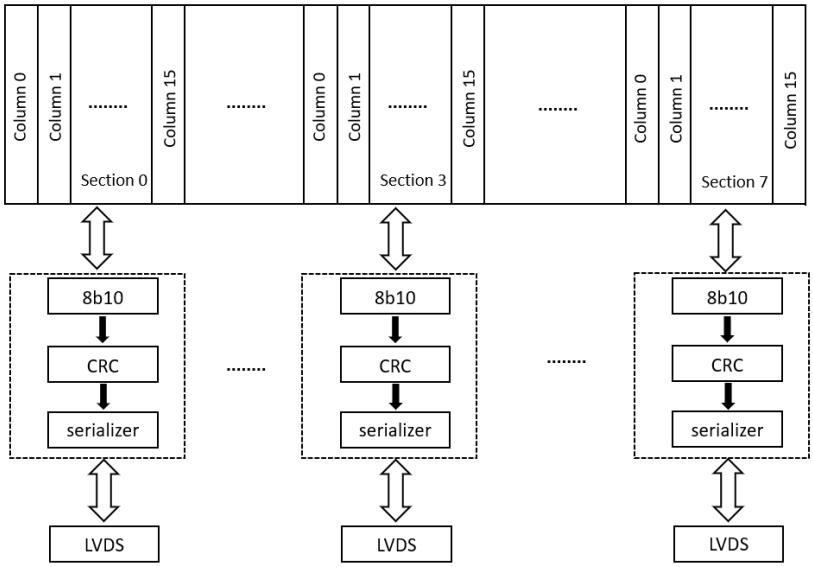

Fig. 5.12 Structure of the peripheral circuits.

8b10b encoding is a line code that maps 8-bit symbols to 10-bit symbols to ensure DC balance (Figure 5.13) and sufficient state changes for reliable data transmission [107, 108]. The encoded data stream has at least a certain amount of data transitions to prevent long streams of 0's or 1's from looking like trying to send DC through the channel. The encoding also provides a run-length limit of 5 consecutive equal bits and ensures the difference between the count of zeros and ones to be no more than two. The 8b10b encoding includes built-in error detection codes that can detect transmission errors in the encoded data stream. It uses a CRC-6 code to detect single-bit errors and some multi-bit errors (up to 5 bits) with high probability.

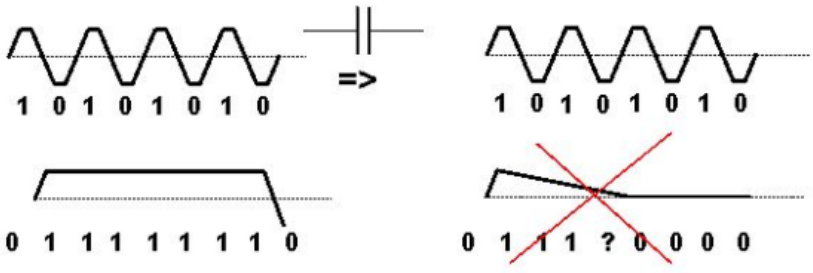

Fig. 5.13 8b10b encoding to ensure DC balance and sufficient state changes for reliable data transmission.

CRC is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to digital data. It is a mathematical algorithm that produces a fixed-size value or hash that represents the original data. The CRC value is calculated by dividing the data into blocks and generating a remainder, which is then appended to the data as a check value. When the data is retrieved, the same algorithm is applied, and the result is compared to the check value. If they match, the data is assumed to be error-free. If not, it indicates that the data has been corrupted or tampered with. The use of CRC is an effective method to ensure the integrity of data transmission and storage [109–111]. The most common polynomial used for generating CRC is the CRC-32 polynomial (also called Ethernet polynomial), which is:

$$x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^{8}+x^{7}+x^{5}+x^{4}+x^{2}+x+1 \quad (5.2)$$

Using a serializer allows the transmitter to take multiple streams of parallel data and convert it into a single, high-speed serial data stream that can be transmitted over the LVDS interface with minimal electromagnetic interference and power dissipation. A Double Data Rate (DDR) serializer (Figure 5.14) was used with the clock frequency of 320 MHz guarantees a maximum throughput of 640 Mb/s per section. The input stage of the serializer comprises a 32-bit data register. Subsequently, the Finite State Machine (FSM) selects bytes 0 to 3 to transmit to the 8b/10b encoder. A single 8b/10b encoder maps each byte of the 32-bit bus of the EoC output FIFO to its corresponding 10-bit symbol. The encoding circuitry can generate any control symbol (comma symbol) as specified in the 8b10b protocol by configuring the KI input signal within the incoming 32-bit data. The encoded data is then divided into even and odd bit positions and transmitted to their corresponding shift registers. Two shift registers perform parallel-to-serial conversion: one shifts even bits triggered by the falling edge of the clock, and the other shifts odd bits triggered by the rising edge of the clock. The clock signal is used to multiplex the two serial data streams to the DDR output. Transmission begins with the least significant bit, and the byte order is organized from 0 to 3.

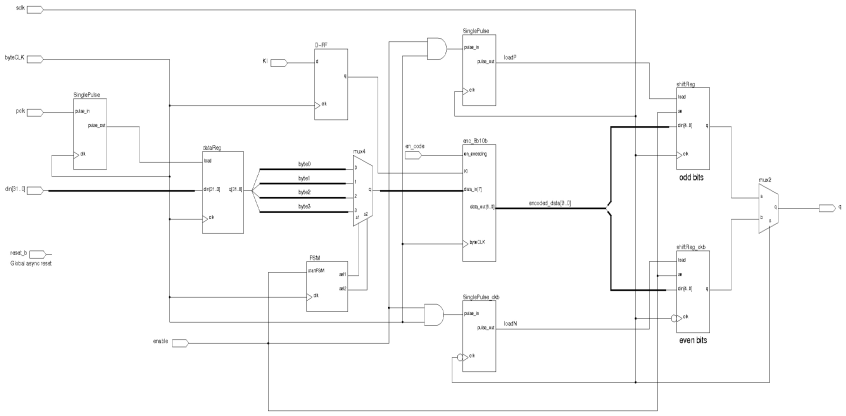

Fig. 5.14 Schematic diagram of the DDR serializer.

5.5.2 Simulation for the data readout

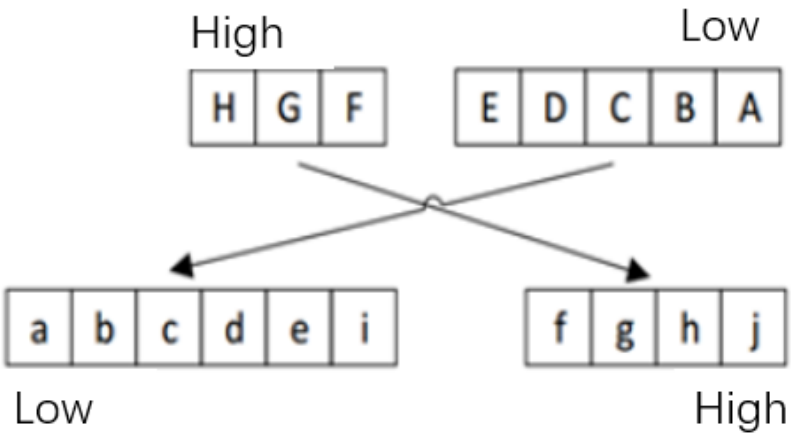

Fig. 5.15 Block diagram of 8b10b encoding.

In the 8b10b encoding process, the original 8-bit code words are divided into two parts: the low 5 bits, denoted as EDCBA (with a decimal value of X), and the high 3 bits, denoted as HGF (with a decimal value of Y). The 8-bit data code is then denoted as D.x.y, similar to the notation for data codes, while the control code is denoted as K.x.y. As shown in Figure 5.15, during 8b10b encoding, the low 5 bits EDCBA are encoded into 6 bits abcdei using 5b6b encoding, and the high 3 bits HGF are encoded into 4 bits fghj using 3b4b encoding. Finally, the two parts are combined to form a 10-bit code abcdeifghj, which is sent in sequence with the low bits first and high bits second. The simulation results are shown in Figure 5.16, "dtin[7:0]"

represents the original 8-bit data, "dcode[9:0]" represents the 10-bit data after being encoded by the 8b10b encoder. From the simulation results, we can see that the entire encoding output process is accurate and error-free.

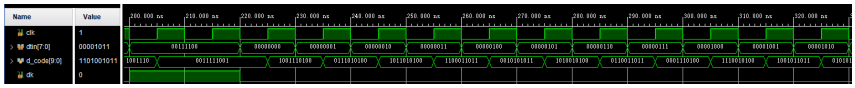

Fig. 5.16 Simulation for the 8b10b encoding.

The basic idea of CRC is to use linear coding theory to generate a check code (i.e. CRC code) of r bits based on certain rules from the k-bit binary code sequence to be sent at the sending end. The CRC code is then appended to the information code to form a new binary code sequence of $k+r$ bits, which is finally sent out. At the receiving end, the transmission process is checked and errors are corrected based on the rules followed between the information code and the CRC code. Generally speaking, the wider the bit width r of the check code, the stronger the error correction ability, for example, the error correction ability of CRC32 is stronger than that of CRC16. The way to obtain the check code in CRC check is to convert the k-bit information code into a polynomial, then divide it by a generating polynomial, and obtain the remainder as the check code. In the simulation shown in Figure 5.15, "din[31:0]" is the test data to be encoded, "dout[31:0]" is the encoded word, which is verified correctly.

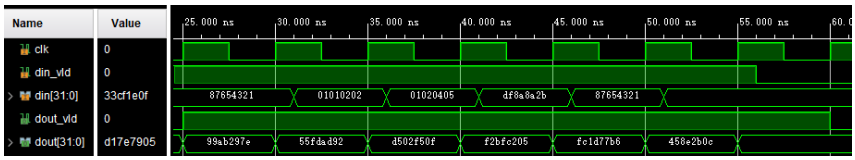

Fig. 5.17 Simulation for the CRC32 encoding.

5.5.3 Chip configuration

The communication for slow control, including configuration and status, between the ASIC and FPGA employs a Serial Peripheral Interface (SPI), where the ASIC functions as the slave. The SPI port comprises four signals, as described in Table 5.3, in accordance with the SPI protocol.

Table 5.3 SPI interfave used for chip configuration.

signals	functions
SCLK	Serial Clock (20MHz)
SDI	Serial Data In
SDO	serial Data Out
SS_n	Slave Select (active low)

As the SPI port utilizes LVDS signals and there is a direct connection between the ASIC and FPGA, a three-state SDO port is unnecessary. Consequently, the SDO output is held low when it is inactive. The SPI serial clock frequency can achieve up to 20 MHz, which corresponds to a system clock frequency divided by 16, with a clock period of 50 ns. The Clock Polarity (CPO) and Clock Phase (CPHA) have been established as 0 and 1, respectively.

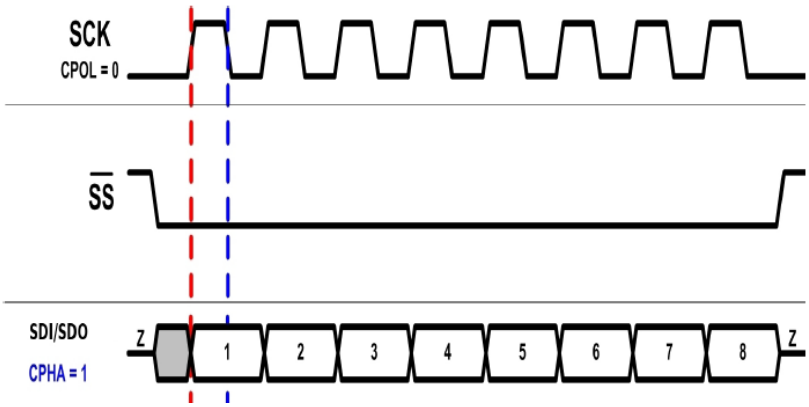

Fig. 5.18 SPI timing diagram.

Figure 5.18 illustrates the resulting timing diagram, with the most significant bit transmitted first. In a write operation (from master to slave), the SDO reflects the command and the payload from SDI to verify whether data have been received correctly. During a read operation, the SDO echoes the command bits, followed by the corresponding 16-bit data value. The ASIC decodes the SPI commands and data, which are presented in Figure 5.19. The SPI word consists of 3 bits for section address, 4 bits for column address and 8 bits for data to be loaded.

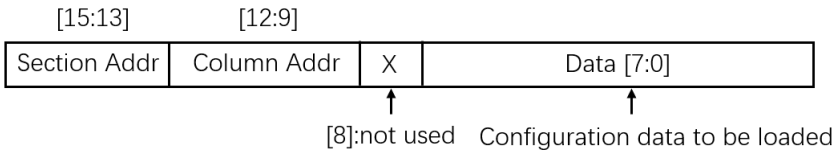

Fig. 5.19 SPI word includes address for sections and columns, configuration data for pixel registers.

The SPI module in the peripheral circuitry can decode the received SPI configuration data, and locate the pixel column that needs to be configured based on the section address and column address. Each pixel's configuration register in the METPC chip can be set individually, and all configuration registers of eight pixels in each column are chained together. Once the pixel column is located using the section address and column address, the configuration process for that column begins, while other pixel columns are in a masked state. Configuring the register of a pixel column requires 8×30 bits.

5.6 Charge sharing correction algorithm simulation

Charge sharing calibration is a very important feature of the METPC chip, and the charge sharing calibration algorithm is mainly implemented in the digital circuitry of the METPC. In this section, the charge sharing calibration algorithm was thoroughly verified under different charge distribution conditions. Simulation validations was done for three charge sharing scenarios: all charges generated by incident photons are collected by the same pixel, meaning no charge sharing; charges are collected by two adjacent pixels; and charges are collected by four adjacent pixels. Assuming an incident X-ray energy of 7.2 keV which produce the total charge of $2000e^-/h^+$ in a silicon sensor, the collected charge was amplified and shaped and the resulting sum-ToT signal length was 200 *ns* after passing through a discriminator. The METPC pixel's internal ToT counter is 5 bits and the clock is 100 MHz, so the maximum ToT signal length that can be processed is 320 ns.

5.6.1 No charge sharing

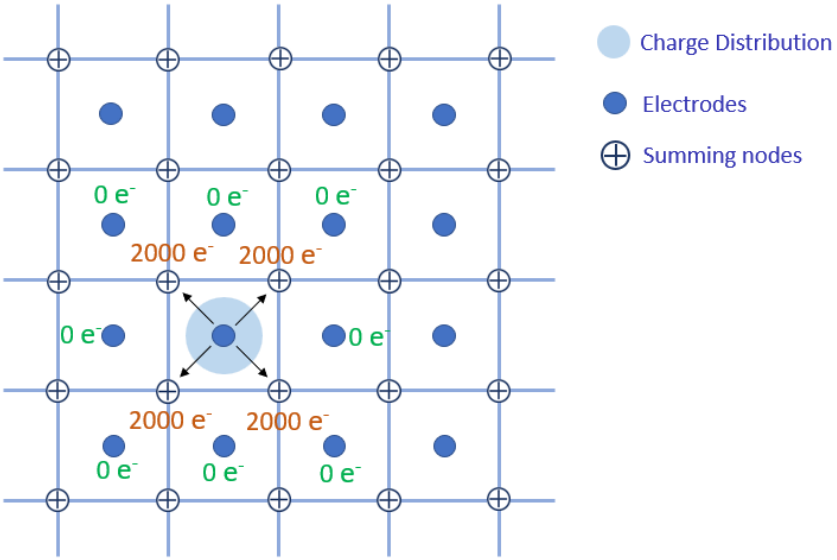

Fig. 5.20 No charge sharing, all generated charge is collected by only one pixel.

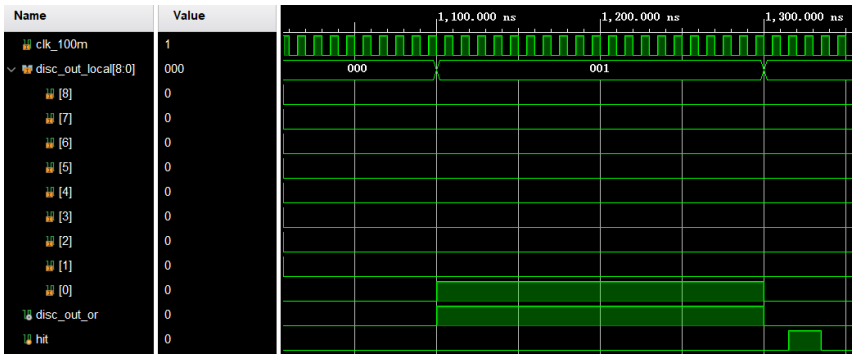

Fig. 5.21 Simulation for no charge sharing.

When no charge sharing occurs (Figure 5.20), all of the charge is collected by the local pixel, and the summed charge collected by the 4 summing nodes around the local pixel is also 2000 e^- . At this condition, the sum-ToT signal and the local-ToT signal of the central pixel are both 200ns. However, the surrounding pixels have local-ToT signals of 0 because they have not collected any charge. The central pixel is clearly the pixel that was hit, and the simulation result is shown in the (Figure 5.21). From the simulation results, it can be observed that the ToT signal duration of

pixel 0 (central pixel) is equal to the Sum-ToT duration. The comparison logic can accurately detect that pixel 0 (central pixel) was hit and generated a hit signal.

5.6.2 Charge sharing between 2 adjacent pixels

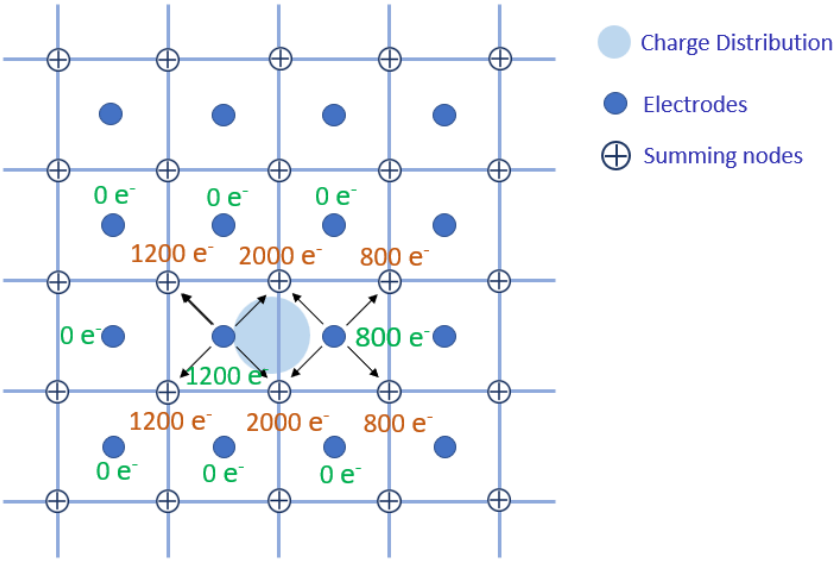

Fig. 5.22 Charge sharing happens between 2 adjacent pixels.

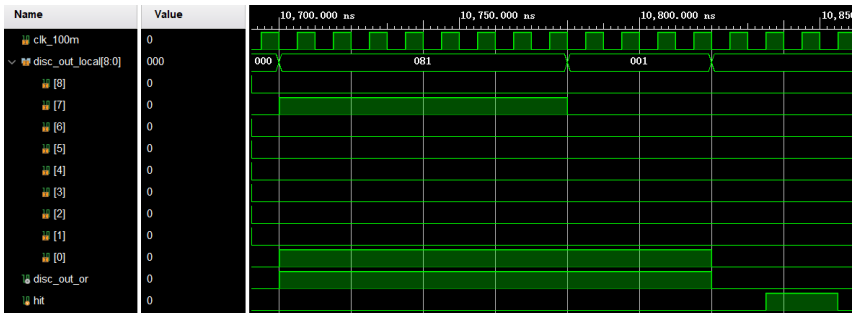

Fig. 5.23 Simulation for charge sharing happens between 2 adjacent pixels.

When charge sharing occurs between two adjacent pixels (Figure 5.22), assume that 60% of the charge is collected by the local pixel and the remaining 40% is collected by another pixel.In this scenario, only the summing nodes adjacent to these two pixels can collect the charge. Moreover, only the summing nodes that are simultaneously adjacent to these two pixels can collect the complete charge (2000

e^-), while the charge collected by other summing nodes is less than the complete charge. From the simulation results (Figure 5.23), it can be seen the local ToT signals produced by the two pixels are 120 *ns* and 80 *ns*, respectively, while the ToT signals of other adjacent pixels are 0. According to the charge sharing calibration logic, the pixel with the larger ToT is recognized as the one that was hit. The charge sharing calibration correctly identified the hit pixel and generated a hit signal.

5.6.3 Charge sharing between 4 adjacent pixels

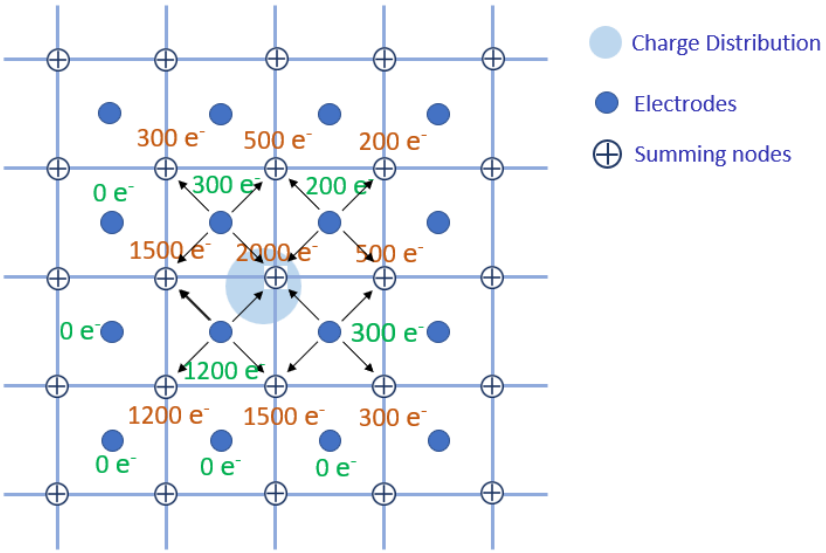

Fig. 5.24 Charge sharing happens between 4 adjacent pixels.

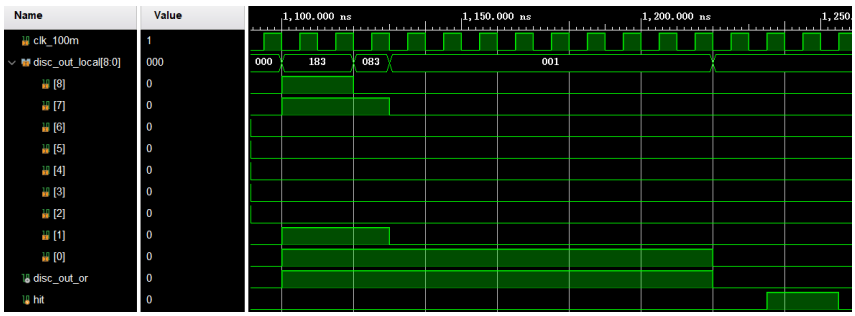

Fig. 5.25 Simulation for charge sharing happens between 4 adjacent pixels.

When charge sharing occurs between four adjacent pixels (Figure 5.24), assume that 60% of the charge is collected by the local pixel, 15% is collected by the pixel

above, 15% is collected by the pixel to the right, and 10% is collected by the pixel to the upper right. In this case, only the summing node between the four pixels collects 2000 e^- of charge. From Figure 5.24, it can be observed that all summing nodes adjacent to these four pixels can collect charge. However, only the summing node located in the middle of these four pixels can collect the complete charge (2000 e^-). The local ToT signals produced by the four pixels are 120 *ns*, 30 *ns*, 30 *ns*, and 15 *ns*, respectively, while the ToT signals of other adjacent pixels are 0. According to the charge sharing calibration logic, the pixel with the larger ToT is recognized as the one that was hit. The simulation result is shown in the Figure 5.25, where the charge sharing calibration correctly identified the hit signal was generated.

Chapter 6

Conclusions

This thesis first introduces the basic principle of multi-energy X-ray imaging and describes in detail the concepts of photon counting detectors and different pixelated semiconductor detectors. The readout chip of the pixel detector is one of the core components of the entire detector system. This work introduces the general architecture of the pixel detector readout chip and analyzes each signal processing channel circuit. In addition, several readout chips that have been designed and applied in the world are compared.

A mixed-type pixel detector readout chip, METPC with multiple thresholds was reported in this thesis, with a pixel size of $110 \times 110 \mu m^2$and an array of 8×112 pixels. Each pixel has four editable digital thresholds, which can simultaneously detect photons in four energy ranges. The depth of the counter for each energy range is 12 bits. When the pixel size is relatively small compared to the detector thickness, or when the incident photons interact with the detector at the pixel boundary, the generated charge will spread to neighboring pixels. This is also called charge sharing effect. This thesis work explores the process of charge collection in semiconductor detectors and proposes a charge sharing correction algorithm based on ToT technology. To implement the charge sharing correction, a two-stage amplification structure is adopted in the analog circuit, and the second-stage amplifier circuit is used as a charge summation node to collect all the charges generated by the incident photons. The charge sharing correction algorithm is implemented in the digital circuit, and the complete charge collected can be assigned to the pixel with the maximum ToT signal. The energy counter adopts a register structure of LFSR, which can simultaneously

realize the photon counting and data readout modes by changing the register structure and adding additional readout registers. The peripheral data readout module, pixel configuration module, analog circuit bias signal module, and chip pins are introduced.

The charge sharing correction circuit is the focus and most challenging part of this chip design. Due to the manufacturing process of the readout chip as well as the limited pixel size, it is challenging to implement more than energy thresholds in each pixel unit while achieving charge sharing correction. To address this challenge, this work proposes a digital thresholds method. This method eliminates the need of discriminator designed in an analog way for implementing multiple thresholds. Instead, the digital thresholds method digitizes the ToT signal and uses registers to achieve adjustable digital thresholds. The digitized ToT is then directly compared with the digital threshold. With this approach, it is possible to implement four energy thresholds, with a counting depth of up to 12 bits for each energy threshold.

Finally, the simulation verification of ToT comparison logic, programmable digital threshold register, energy counter counting and readout modes are carried out, and the simulation verification results are analyzed.

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