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Investigating the properties of interfacial layers in planar Schottky contacts on hydrogen-terminated diamond through direct current/small-signal characterization and radial line small-signal modelling

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Large-area Schottky diodes on hydrogen-terminated diamond are investigated through DC and small-signal characterization and physics-based equivalent circuit modeling. Measured current- and capacitance-voltage characteristics suggest significant distributed resistance effects induced by the relatively low mobility of the 2D hole gas in the diamond sub-surface. A *distributed equivalent circuit model* of the device is proposed aimed at correlating the device physics with the observed electrical behavior. It is shown that a heterostructure-like model of H-diamond Schottky contacts, including a thin non-conductive interfacial layer that separates the 2D hole channel from the Schottky barrier, enables an accurate description of both the device DC and AC behaviour and the extraction of relevant quantitative information on the physical parameters of the interface, channel charge control, and carrier mobility. © *2015 AIP Publishing LLC*.
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The operation of field-effect transistors (FETs) exploiting the hydrogenated diamond[1,2] is based on several physical mechanisms, whose details have not yet been fully clarified. As well known, the H-termination of diamond induces a high *p*-type surface conductivity due to the formation of a hole accumulation layer in the diamond subsurface. This two-dimensional hole gas (2DHG) is then used as the transistor conductive channel, whose control is performed through a gate realized by Schottky rectifying contacts or metal-insulator structures deposited on the H-diamond surface. Surface adsorbates are thought to be responsible for the 2DHG formation through an interfacial exchange of electrons from the valence band into an empty electronic state of the adsorbate (surface transfer doping[3–5]) or through the generation of a dipole layer that electrostatically induces the upward bending of the diamond valence band.[2] Both Metal Semiconductor FETs (MESFETs) and Metal-Insulator-Semiconductor FETs (MISFETs) have been fabricated on H-terminated diamond; in the first case, the gate metal is directly deposited on the diamond surface; whereas in the second case, a few nanometers thick insulating layer is formed on the diamond surface by atomic layer deposition (see Refs. 2, 6, 7, and references therein), aimed at improving the stability of the diamond surface. Indeed, the analysis of the electrical behavior of Schottky contacts on H-terminated diamond, as also discussed in this work, suggests a strong similarity in the basic operation principle of H-diamond MESFETs and MISFETs, which is related to the presence, in both cases, of a thin insulating layer separating the diamond surface from the gate metal. A first interpretation in this direction was proposed in Ref. 8, where a thick barrier layer (around 30 nm) with a large, somewhat unphysical relative dielectric constant (around 50) is postulated to explain the suppression of tunnel currents that would arise if the diamond surface were in direct contact with the metal. The existence of a barrier insulating interfacial layer (IL) was also consistent with capacitance-voltage (C/V) measurements and microstructural characterizations in Ref. 9, which led to an estimation of the thickness of the barrier layer of the order of 5–10 nm. A metal-insulator-metal tunnelling model developed in Ref. 10 was also exploited in Ref. 9 to fit the measured current-voltage (I/V) curves in forward bias, with a barrier height of 2.4 eV and a barrier thickness of 4.7 nm. In contrast, a thermionic emission model is exploited in Ref. 8 to explain the behaviour in forward bias, with an estimated barrier height of 1 eV; the model satisfactorily fits the experimental data immediately above the onset but strongly deviates at high bias, suggesting a bias-dependent series resistance. Schottky-barrier thermionic emission model is also invoked in Ref. 11, where the I/V curves are fitted with a barrier height of 1.6 eV and ideality factor close to one (1.01), and more recently in Ref. 12, from temperature-dependent I/V characterization, with estimated barrier height of 0.59 eV and ideality factor of 1.01.

This letter presents a combined experimental and simulative study of the DC and small-signal characteristics of H-diamond Schottky contacts aimed at gaining a deeper understanding of the underlying charge control and transport mechanisms. Such an understanding is also strictly correlated to the need to solve several technological issues affecting device instability and degradation[13] and to develop suitable physics-based and compact models[14,15] for device design and optimization.

Room temperature I/V and small-signal measurements in the frequency range of 100 kHz–5 MHz were carried out on Schottky diodes realized at the University of Glasgow and at the Università di Tor Vergata on H-terminated diamond with Al as the Schottky metal, see Figure 1 for the

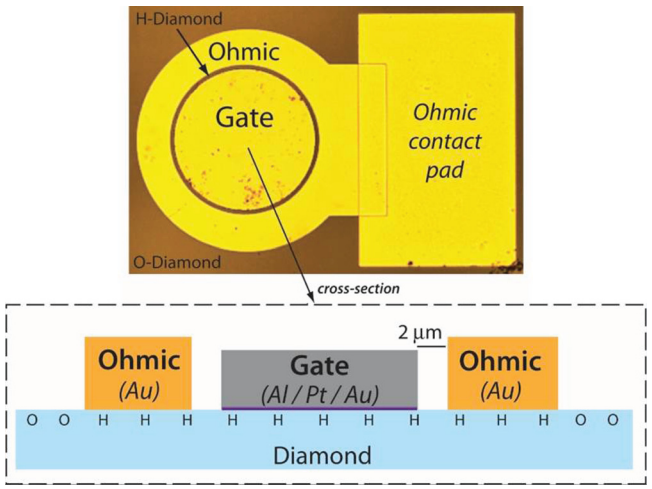

FIG. 1. Layout of test structures used for I/V and C/V characterization; the radius of the circular electrode is 50 μm, the distance between gate and ohmic contact is about 2 μm.

layout of the fabricated diodes. A high-quality intrinsic single crystal diamond film with a thickness of about 2 μm was homo-epitaxially grown by Microwave Plasma Enhanced Chemical Vapour Deposition (MWPECVD) on $4 \times 4 \times 0.5\,\text{mm}^3$ commercial low-cost synthetic High Pressure High Temperature (HPHT) diamond substrate polished on both sides. The intrinsic diamond typical growth conditions were the following: substrate temperature of 650 °C, microwave power 600 W, pressure of 120 mbar, methane (CH_4) and hydrogen (H_2) flow rates were 1 and 100 sccm, respectively. Hydrogen termination was performed by exposing the diamond surface to H plasma in the same microwave CVD reactor, *in-situ*, at the end of the growth. Electrical test structures were then fabricated on the hydrogen-terminated diamond surface using a process that is identical to that reported elsewhere for the production of H-diamond FETs[16] and is summarised as follows: 80 nm of gold (Au) was deposited onto the hydrogen-terminated diamond surface via electron-beam evaporation to simultaneously protect the surface during processing and to form an ohmic contact to the underlying 2DHG. Patterning of the test structures was performed using poly(methyl methacrylate) resist and a Vistec VB6 electron-beam lithography tool operating at 100 keV. Individual test structures were electrically isolated by treating the exposed diamond surface to oxygen plasma after selective removal of the Au layer by potassium iodide (KI) wet etch. KI wet etch was used again to selectively remove the Au before depositing the gate metal (20 nm Al/20 nm Pt/40 nm Au) onto the diamond surface. This process simultaneously acts to form the ohmic contact from the remaining Au and produce a gate-ohmic contact separation of 2 μm.

Measured I/V curves clearly exhibited a rectifying, asymmetric behaviour, while C/V curves showed a steep increase followed by a constant plateau that resemble the onset of a 2D conductive channel separated from the metal by a non-conductive layer.[8,9] Both the I/V and C/V detailed characteristics showed a low amount of hysteresis when repeatedly measured from the ON to the OFF state and vice versa. Moreover, some degradation was noticed by repeating I/V characterizations after the small-signal characterization. Van Der Pauw (VDP) and Transmission Line Method test structures were also fabricated on the same wafer to characterize the electrical behavior of the ohmic contacts and the exposed (i.e., contact free) H-diamond surface. Sheet resistance was found on the average to be 8600 Ω/sq with contact resistance of about 5.8 Ω mm. Mobility of about $80\,\text{cm}^2\text{V}^{-1}\text{s}^{-1}$ and sheet hole density between 0.8 and $1.1 \times 10^{13}\,\text{cm}^{-2}$ were extracted for the exposed regions.

To introduce the discussion, we recall that the electrical behaviour of Schottky barriers coupled with interfacial layers is complex, and many conduction mechanisms can play a role (see, e.g., Chapters 3, 4, and 8 of Ref. 17), also depending on the technological quality of the interface. Due to the different material interfaces of the dielectric layer, the metal-semiconductor potential barrier will be, in general, asymmetric. The main conduction mechanisms that may be invoked are thermionic emission,[18] tunneling through the dielectric layer (see Refs. 17 and 19), and also trap-assisted tunneling (referred to as Poole-Frenkel model, see Ref. 17). Both the thermionic and the tunneling currents are affected by barrier lowering and thinning due to the image force; such effects can be taken into account numerically, e.g., according to the implementation in Ref. 20, which was the basis for the present DC model. Finally, leakage currents associated with local or distributed defects approximately following Ohm's law with a constant leakage conductance are also possible, see Ref. 21.

I/V measurements exhibiting a low amount of hysteresis (and therefore attributed to "technologically successful" devices), showed a number of common features, as can be seen from a representative I/V curve reported in Fig. 2: The I/V curves are almost symmetrical at very low direct or forward bias; strong asymmetry exist at intermediate bias, leading to exponentially large current in forward bias and to soft saturation in reverse bias. Finally, a linear behaviour again prevails in strong forward bias. As a first remark, we notice that the strong asymmetry present at intermediate forward and reverse bias is hardly compatible with a tunneling model, which yields almost symmetrical currents also in the presence of an asymmetric barrier, as remarked, e.g., in

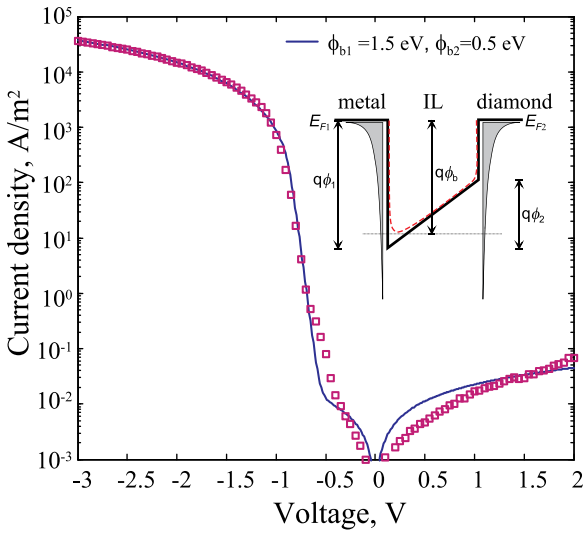

FIG. 2. Measured I/V (symbols) and fitting (solid line) based on thermionic emission model across an asymmetric interfacial potential barrier, whose energy band at thermal equilibrium is depicted in the inset.

Ref. 20. The asymmetry argument is perhaps the strongest in favour of a thermionic interpretation of the current; indeed, as already remarked, a tunneling model (from Ref. 10, Appendix A1) with proper barrier height and thickness are able to accurately fit the I/V characteristics in *forward* bias.[9] Concerning the low and high bias behaviour, this is compatible with a parasitic series resistance and a parallel leakage conductance. Notice that a more accurate fit at large forward bias (i.e., when the current is large) would require a distributed, radial model of the kind developed for the small-signal analysis; however, for small currents, the distributed DC effect is negligible while for large currents it amounts to a slightly nonlinear behaviour of the parasitic series resistance.

Figure 2 shows a fitting of the I/V set through an asymmetric thermionic emission model including image effect barrier lowering (the layer permittivity is assumed to be 9, similar to that reported in Ref. 9). Nominal parameters have been used for the Richardson constant, while the hole effective mass is 0.9 m_0. The barrier height is 1.5 eV and 0.5 eV on the metal and semiconductor sides, respectively, the series resistance is $3.5 \times 10^{-5}\ \Omega\,\mathrm{m}^2$, the leakage conductance is $5\ \mathrm{S/m}^2$. The ideality factor is assumed as 1 and the IL thickness is assumed to be 5.5 nm. Small deviations from this value can result in a good fit if the barrier height is properly adjusted; however, with this barrier thickness and height the tunneling current as derived from the numerical model in Ref. 20 is small with respect to the thermionic emission current. It is worth noting that the derived IL physical parameters are similar to those previously reported in different studies, suggesting that the IL is inherent to the formation of the Al/H-diamond contact, regardless of the specific fabrication process adopted. In particular, the estimated values of energy barrier height and thickness are consistent with those extracted from I/V,[9,10] C/V,[9] and transmission electron microscope characterizations[9] by other research groups. The estimated IL thickness is also compatible with the gate breakdown voltage reported in Ref. 22, Fig. 1, for FETs operating in the linear region.

The measured small-signal C/V and conductance-voltage (G/V) characteristics reported in Fig. 3 also show a behaviour compatible with the charge control expected for a

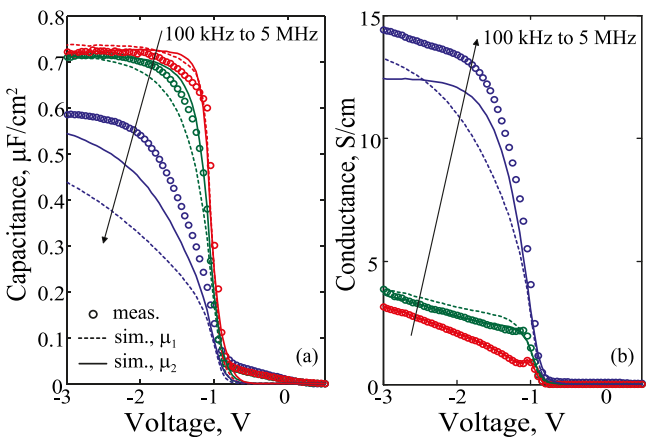

FIG. 3. Experimental (symbols) and fitted (solid and dashed lines) *C/V* (a) and *G/V* (b) characteristics at 100 kHz, 1 MHz, and 5 MHz. Dashed line curves assume hole mobility $\mu_1 = 80\ \mathrm{cm^2V^{-1}s^{-1}}$, while solid lines are an optimized fit with hole mobility $\mu_2 = 180\ \mathrm{cm^2V^{-1}s^{-1}}$.

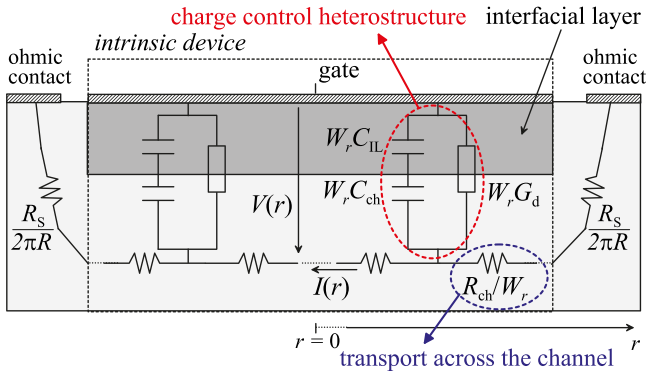

FIG. 4. Radial transmission line equivalent circuit of the circular diodes; the p.u.l. parameters are space-dependent through the scaling factor $W_r = 2\pi r$. R_s models parasitic access and contact resistances. R is the radius of the gate contact.

Schottky barrier separated from the channel by an interfacial layer.[9,22] However, as already mentioned, a marked dependence on the AC frequency signal is observed, that, in principle, can be induced by parasitic lumped resistances (such as those associated with the exposed H-diamond region between the Schottky gate and ohmic contact and to the ohmic contact resistance itself) and/or by distributed effects of the channel resistance.[23,24]

In the present case, due to the large gate contact area of the samples and the relatively low mobility (around $100\ \mathrm{cm^2V^{-1}\ s^{-1}}$) of the 2DHG, a model based on a quasi-static approach, as usually exploited in H-diamond FET equivalent circuits,[22] where the Schottky contact is connected to the ohmic one by a lumped admittance (including capacitance as well as shunt and series resistances), does not provide an accurate description of the observed frequency dispersion. Such non-quasi-static behaviour may be obtained, as depicted in Fig. 4, by modeling the device as a *distributed RC network*, in which the Schottky barrier is described by the gate-IL-diamond heterostructure[22] derived from the I/V analysis, and transport across the channel is modeled by a distributed series resistance. In particular, the circular symmetry of the samples suggested the development of a *radial line* equivalent circuit, extending the approach in Ref. 25. In Fig. 4, C_{IL} and C_{ch} (V) are the per-unit-area IL and channel capacitance, respectively; G_d is the per-unit-area conductance accounting for the gate-channel leakage current; $R_{ch} = 1/(q\mu_h p_s)$ is the equivalent channel sheet resistance, where μ_h and p_s are the 2DHG mobility and sheet density, respectively. The voltage dependent 2DHG concentration is computed by integrating the equivalent gate-channel capacitance provided by the series connection of C_{IL} and C_{ch} (V).

Thus, the device is described by a nonuniform radial transmission line with nonconstant per-unit-length (p.u.l.) parameters that depend on the DC operating point. The input admittance of the radial line admits for an analytic expression, whose detailed derivation is reported in Ref. 26 together with a validation against physics-based simulations. In Fig. 5, the input admittance predicted by the distributed model (Eq. (7) in Ref. 26) is compared with its lumped approximation (Eq. (8) in Ref. 26) for devices with gate radius ranging from 1 μm up to 50 μm and in two different gate

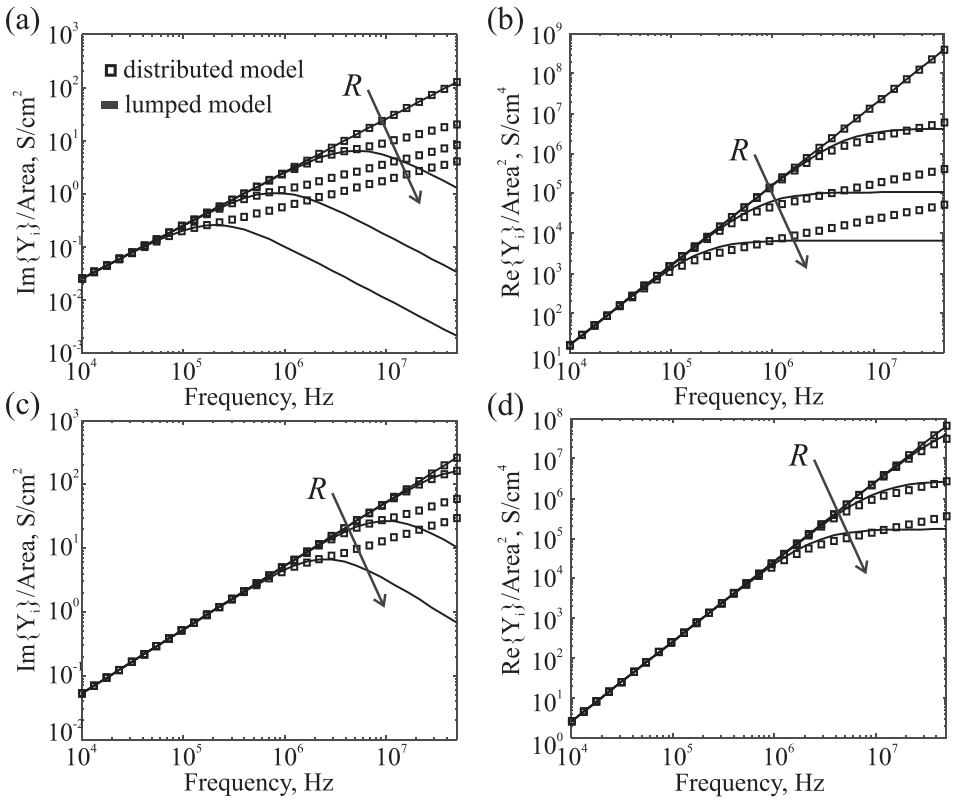

FIG. 5. Frequency behavior of the imaginary and real part of the small signal admittance of circular diodes as predicted by the distributed model (symbols) and lumped model (lines) for different values of the gate radius $R = 1$, 10, 25, and 50 μm, for two different gate bias points: (a) and (b) are calculated at $V = -1$ V (channel at threshold, see Fig. 6), (c) and (d) at $V = -2$ V (above threshold). Carrier mobility is 50 $\mathrm{cm^2V^{-1}\ s^{-1}}$. Note that the imaginary part is scaled by the area, while the real part is scaled by the square of the area.

bias conditions. The analysis clearly shows that in large area samples only the distributed model enables to recover a physics-based description of the channel charge control law. In small area samples, the lumped approximation is accurate enough, provided that the total channel resistance is correctly estimated as $R_{ch}/(8\pi)$, see Ref. 26.

Coming back to the interpretation of the small-signal measurements, Fig. 3 compares the fitted C/V and G/V characteristics calculated from Eq. (7) in Ref. 26 by assuming physical parameters for the Al/IL/diamond cross-section as derived from the I/V analysis. In particular, the interfacial layer capacitance is set to 1.45 μF, corresponding to an IL thickness of about 5.5 nm for a dielectric constant value of 9. Two fitted curves are reported, one assuming a channel mobility of 80 $\mathrm{cm^2V^{-1}\ s^{-1}}$ as extracted from VDP measurement, one with an optimized value of 180 $\mathrm{cm^2V^{-1}\ s^{-1}}$ allowing for a better fit of the experimental curves. A good agreement is found, considering the possible deviations of the measured data due to the nonuniform interface quality of the analyzed samples. Finally, the estimated charge control model p_s (V_G) and voltage dependent channel resistance R_{ch} (V_G) are shown in Fig. 6.

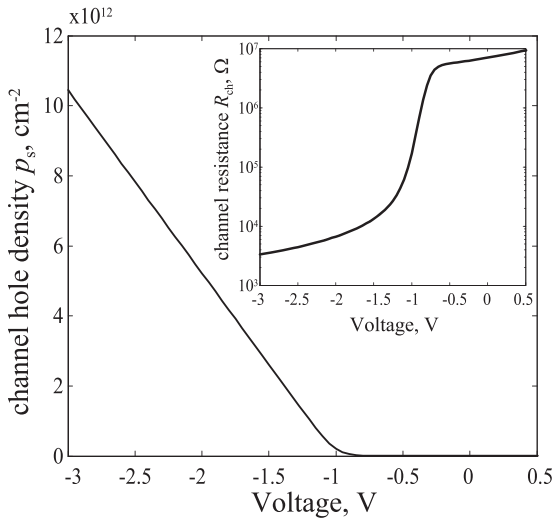

FIG. 6. 2DHG concentration and channel resistance (in the inset) *vs.* gate voltage as extracted from the *C/V* and *G/V* measurements.

In conclusion, physical models have been developed for the interpretation of I/V and frequency-dependent C/V characteristics of large-area Schottky diodes on H-terminated diamond. Based on the physical parameters of the Al/IL/diamond cross-section estimated from the I/V analysis, a radial line model has been developed to correlate the 2DHG charge control and mobility to the small-signal behaviour. The good quantitative agreement between measurements and model further supports the hypothesis[8,9] of a thin non-conductive interfacial layer separating the 2D hole channel from the Schottky barrier, across which transport appears to be dominated by thermionic emission.

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[26]See supplementary material at http://dx.doi.org/10.1063/1.4915297 for the formula and mathematical derivation of the radial line input admittance.

Investigating the properties of interfacial layers in planar Schottky contacts on hydrogen-terminated diamond through DC/small-signal characterization and radial line small-signal modelling

Supplemental Material

Mathematical derivation of the distributed radial line input admittance

We refer in the following to the equivalent circuit in Fig. 4 of the manuscript.

The per-unit-length parameters (p.u.l) of the radial line can be derived by considering a circular section of length dr with radius r, whose parallel capacitance and conductance model the gate/IL/channel cross section, whereas the series resistance describes hole transport across the channel:

$$\begin{aligned} \mathrm{d}C &= C_{\mathrm{GC}} 2\pi r \mathrm{d}r \\ \mathrm{d}G &= G_{\mathrm{d}} 2\pi r \mathrm{d}r \\ \mathrm{d}R &= R_{\mathrm{ch}} \frac{\mathrm{d}r}{2\pi r} \end{aligned} \tag{1}$$

where, with reference to Fig. 4, the gate-channel capacitance $C_{\mathrm{GC}}(V)$ is defined as

$$C_{\mathrm{GC}}(V) = \frac{C_{\mathrm{IL}} C_{\mathrm{ch}}}{C_{\mathrm{IL}} + C_{\mathrm{ch}}}. \tag{2}$$

The parameters C_{IL} and $C_{\mathrm{ch}}(V)$ are the per-unit-area IL and channel capacitance, respectively. In Eq.(1), G_{d} is the per-unit-area conductance accounting for the gate-channel leakage current. Finally, $R_{\mathrm{ch}} = 1/(q\mu_h p_s)$ is the equivalent channel sheet resistance, where μ_h and p_s are the 2DHG mobility and sheet density, respectively. The 2DHG concentration is evaluated self-consistently with the gate-channel capacitance of the circular section as

$$p_{\mathrm{s}}(V_{\mathrm{G}}) = -\frac{1}{q} \int_{V_{\mathrm{G0}}}^{V_{\mathrm{G}}} C_{\mathrm{GC}}(V)\, \mathrm{d}V \tag{3}$$

where V_{G0} is a bias point in the off state, such that $p_{\mathrm{s}}(V_{\mathrm{G0}}) = 0$.

Applying the Kirchhoff's voltage and current laws to a line section of radial length dr located in r, the line equations result as

$$\begin{aligned} \frac{dV}{dr} &= -\frac{R_{\mathrm{ch}}}{2\pi r} I \\ \frac{dI}{dr} &= -Y_{\mathrm{p}} 2\pi r V \end{aligned} \tag{4}$$

with $Y_\mathrm{p} = G_\mathrm{d} + j\omega C_\mathrm{GC}$. Differentiating, substituting and exploiting the variable change $x = \sqrt{Y_\mathrm{p} R_\mathrm{ch}}r$, we have for the line voltage

$$x^2 \frac{\mathrm{d}^2 V}{\mathrm{d}x^2} + x\frac{\mathrm{d}V}{\mathrm{d}x} - x^2 V = 0 \tag{5}$$

i.e. a zero-order Bessel differential equation, admitting a closed-form solution in terms of modified Bessel functions of the first (I) and second (K) kind. The resulting values for the line current and voltage are, respectively:

$$\begin{aligned} I(r) &= A2\pi r\sqrt{\frac{Y_\mathrm{p}}{R_\mathrm{ch}}} I_1(kr) + B2\pi r\sqrt{\frac{Y_\mathrm{p}}{R_\mathrm{ch}}} K_1(kr) \\ V(r) &= AI_0(kr) + BK_0(kr), \end{aligned} \tag{6}$$

where A and B are integration constants, and $k = \sqrt{Y_\mathrm{p} R_\mathrm{ch}}$. The line current is derived from the voltage by differentiation. Finally, considering a line with radius R and applying the boundary conditions $I(r=0) = 0$ and $V(r=R) = V_0$, the line input admittance is calculated as

$$Y_\mathrm{i} = \frac{I(R)}{V(R)} = 2\pi R\sqrt{\frac{Y_\mathrm{p}}{R_\mathrm{ch}}}\frac{I_1(kR)}{I_0(kR)}. \tag{7}$$

The total equivalent impedance of the device is then computed by including the effect of the parasitic access and contact resistances (R_s) as $1/Y_\mathrm{i} + R_\mathrm{s}$.

The analytic model has been validated against 3D physics-based simulations[1], under AC condition, of a planar device with 5 nm thick IL ($\epsilon_r = 9$), carrier mobility of 50 $\mathrm{cm^2 V^{-1} s^{-1}}$, and radius of 25 μm. Fig. S1 shows the parallel capacitance and conductance associated with the small-signal admittance $Y_\mathrm{i} = G_\mathrm{i} + j\omega C_\mathrm{i}$ as derived from the physics-based simulation and as predicted by Eq. (7), demonstrating the high accuracy of the analytic distributed model.

As discussed in the manuscript, reducing the gate radius to a few μm will make the dispersive effect of the channel resistance (R_ch in Fig. 4 of the manuscript) negligible, thus allowing the accurate extraction of the physical paramaters by a lumped model that can be derived from the series expansion of Eq. (7) when $kR \to 0$. Truncating the series at the 4th order, one obtains

$$Y_\mathrm{i,lumped} = \pi R^2 Y_\mathrm{p} - \frac{\pi R^4}{8} Y_\mathrm{p}^2 R_\mathrm{ch}. \tag{8}$$

The approximation admits for an interpetation in terms of a lumped equivalent circuit made by the series of the admittance $\pi R^2 Y_\mathrm{p}$ and the resistance $R_\mathrm{ch}/8/\pi$, as can be demonstrated from the series expansion of the input impedance $1/Y_\mathrm{i}$. Thus, in the lumped limit,

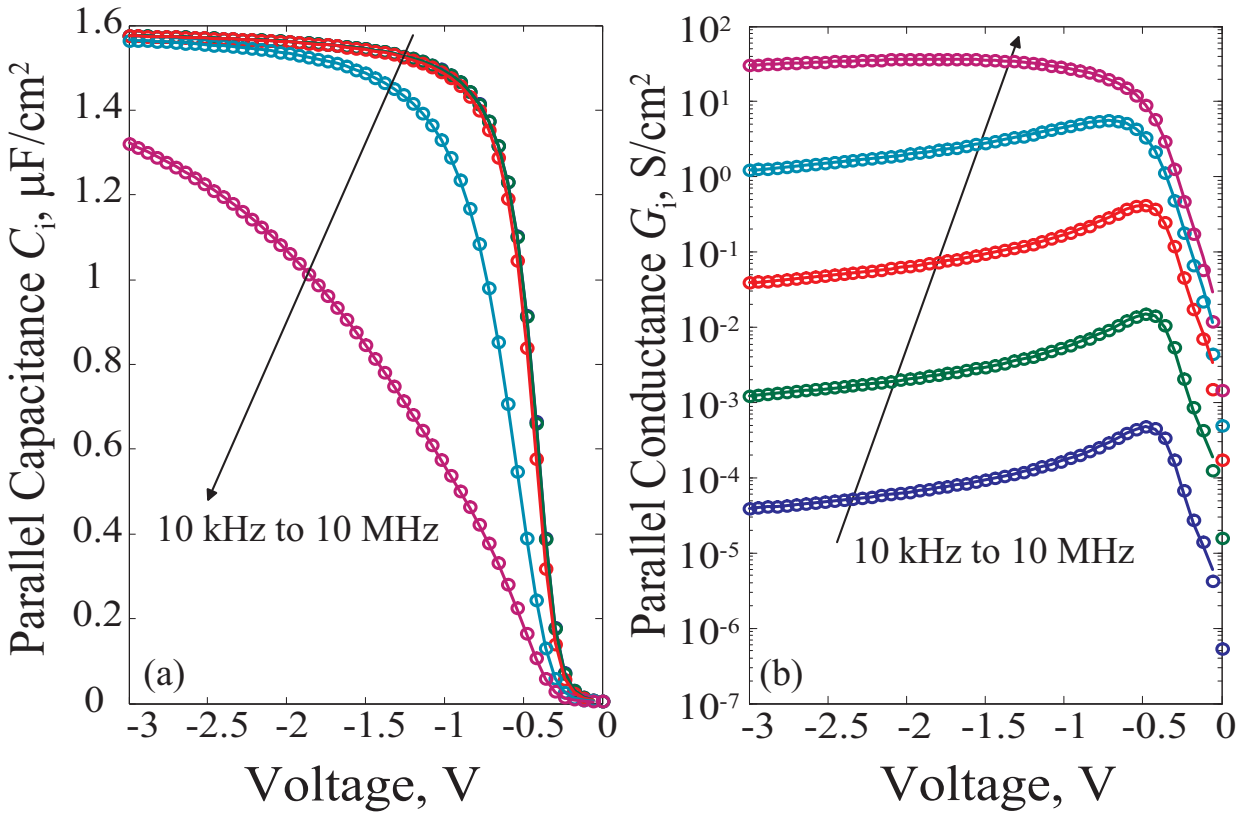

FIG. S1. C_i/V (a) and G_i/V (b) curves at various frequencies of a large area planar device as predicted by physics-based simulations (symbols) and by the analytical distributed model in Eq. (7) (solid lines). Frequency points are logarithmically equally spaced between 10 kHz and 10 MHz.

the equivalent resistance of the line is the sheet resistance (R_{ch}) corrected by a suitable scale factor ($1/8/\pi$).

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[1] "Sentaurus Device, Synopsys Inc." (2014).