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Full-Stack Implementation and Platform-Aware Optimization of Hybrid Quantum–Classical Methods on NISQ Devices

Applications in Quantum Machine Learning and Combinatorial Optimization

By

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Declaration

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Current quantum processors, Noisy Intermediate-Scale Quantum (NISQ) devices, offer tens to a few hundred qubits with limited coherence and non-negligible error rates. In this regime, purely quantum solutions are not feasible for most practical problems. Hybrid quantum–classical algorithms, where a quantum processor executes specific computational kernels within a classical workflow, have emerged as the most promising near-term approach. However, the performance of such hybrid methods depends not only on circuit design but on the entire computational stack: execution models, resource management policies, and platform-level integration within High-Performance Computing (HPC) infrastructures.

This dissertation investigates hybrid quantum–classical computation from a cross-layer perspective, spanning algorithmic design, workload characterization, resource management, and platform integration. The central argument is that meaningful quantum-enhanced computation in the NISQ regime does not arise from isolated algorithmic improvements. It emerges from coordinated co-design across abstraction layers: algorithms matched to hardware capabilities, execution models that account for hybrid workflow latency and asymmetry, and resource management strategies reflecting the operational realities of shared, heterogeneous HPC–QC systems.

Three case studies are developed and evaluated. The first applies Quantum Reservoir Computing (QRC) to credit-card default prediction, using a 256-qubit neutral-atom platform as a nonlinear feature transformer within a classical classification pipeline. The second introduces the Quantum Evolution Kernel (QEK), a hardware-native graph kernel for protein graph classification that exploits analog quantum dynamics to construct similarity measures between graphs. The third presents BBQ-mIS, a hybrid Branch-and-Bound solver for graph coloring that uses a neutral-atom device as a maximal Independent Set generator within a classical decomposition framework.

Three complementary resource management strategies are introduced and evaluated. The vQPU (Virtual Quantum Processing Unit) abstraction enables time-based

multiplexing of a physical QPU across concurrent hybrid jobs within a SLURM-compatible HPC environment, demonstrated on a real gate-based device at Politecnico di Torino integrated with the Leonardo supercomputer at CINECA. Workflow decomposition reduces idle classical reservations by separating quantum and classical phases into independently scheduled steps. Dynamic malleability allows running applications to release and reacquire classical nodes in response to changing phase requirements, improving cluster utilization without requiring explicit workflow declarations.

Experimental evaluation spans noiseless statevector emulation, shot-based simulation, and real-device execution on QuEra's Aquila neutral-atom platform. QRC achieves classification scores competitive with a deep neural network baseline in emulation, with hardware degradation absorbed by the classical readout at larger data scales. QEK matches the Shortest Path Kernel on the PROTEINS benchmark (65.6% vs. 65.3% F1) under both emulation and hardware conditions. BBQ-mIS reproduces optimal graph colorings across all emulation instances; real-device execution on Aquila yields non-trivial maximal Independent Set recovery rates, validating the neutral-atom device as a viable offline candidate generator within a classical solver.

The results do not support broad claims of quantum advantage. They demonstrate narrowly scoped usefulness under realistic NISQ conditions: the hardware access model and classical scaffolding are decisive factors in all three case studies. The cross-layer perspective developed in this dissertation is not a temporary workaround for immature hardware. It is a durable framework for reasoning about quantum computing as an integral component of future HPC infrastructures.