Quantum Conductance and Temperature Effects in Titanium Oxide-Based Memristive Devices

Quantum Conductance and Temperature Effects in Titanium Oxide-Based Memristive Devices

Itır Köymen, *Member, IEEE*, Ivan De Carlo, Matteo Fretto, and Gianluca Milano

***Abstract*— A thorough investigation of quantum conductance properties and the effects of temperature on Cr/Au/TiO_2/TiO_x/Cr/Au memristive devices is presented. Besides fabrication and resistive switching characteristics, two different programming strategies have been explored to observe quantum conductance effects. The first strategy was based on device stimulation with slow current sweeps to observe quantum levels in the SET region, while the second aimed to achieve quantum steps during RESET using slow sweep stimulation. The effects of the two different programming strategies are compared. It is also shown that these devices can be programed to achieve stable quantum levels, as revealed by retention measurements performed after programming the device to 1 G_0. Furthermore, the temperature-dependent electronic conduction mechanism of the device after being programed to different internal resistance states has been analyzed, revealing a semiconductor behavior with an increase in resistance by lowering the temperature in either a pristine state, low-resistance state, or resistance states close to the quantum conduction regime.**

***Index Terms*— Memristive devices, memristor, quantum conductance, resistive switching, temperature effects.**

I. Introduction

THE scaling of electronic microchips is beginning to slow down as transistors approach a physical limit [1]. The gradual switch from conventional planar transistors to 3-D structures, namely finFETs is also being followed by innovative computing principles as well as emerging devices to satisfy the growing computational needs for cognitive processing, big-data analysis, and low-power intelligent systems based on the Internet of Things [2], [3]. Power consumption of devices and switching speeds are significant bottlenecks for implementing these data-heavy applications. Hybrid memristor + CMOS systems are particularly suitable for resistive and neuromorphic computing [4]. Memristive devices offer near-zero standby power [5], fast write/read [6], nanoscale nonvolatile memory, scalability [7], and CMOS compatibility [8], [9].

Redox-based memristive devices have commonly been classified into two categories: cation or electrochemical metallization (ECM) devices, anion or valence change memory (VCM) devices [10], and dual ionic devices [11], [12]. These categories define the physical mechanisms that are responsible for switching in memristive devices. In VCM devices, the electrically-driven formation and rupture of a conductive filament, which connects the two electrodes, lead to the distinct resistive states: the high-resistive state (HRS) and low-resistive state (LRS) [13]. The movement of oxygen ions inside the metal-oxide matrix is responsible for the formation of a conductive filament rich in oxygen vacancies due to the application of an electrical signal to the device, but it has also been observed that cations also have a role in the switching of these devices [14]. In VCM cells, where it was shown that the Schottky barrier at metal/metal oxide interfaces has an active role in regulating resistance states [15], transition metal oxide active layers such as HfO_2 [16], VO_2 [17], and TiO_2 [18], [19] are usually coupled with electrochemically inert electrodes.

As a result of device miniaturization, quantum conductance has been observed in memristive devices [14], [18], [20], [21], [22], [23]. Quantum conductance refers to the conductance of a quantum point contact, which, in memristive devices forms due to the conductive filament made up of metal ions, oxygen vacancies or both as explained previously. Quantum conductance is expressed as multiples of the fundamental unit of conductance G_0, where $G_0 = 2e^2/h$ (e is the electron charge and h is Planck's constant) [14] (where $1/G_0 \approx 12.9$ kΩ). This characteristic of memristive devices has recently started drawing attention since this physical phenomenon can be exploited for a wide range of applications including multilevel data storage, logic applications (exploiting the bistable switching characteristics of quantum conductance), neuromorphic computing (constructing and tuning conducting filaments),

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and hardware security (memristive devices exhibiting quantum conductance used as random number generators) [14], for use as a standard of resistance for developing embedded self-calibrating systems and in metrology for the development of new standards [24]. Memristive devices employing different structures such as gap-type devices [25], nanotube arrays [26], planar devices employing 2-D materials [27], [28], and more traditional vertical devices (Au/VO_2/NSTO [17], Cu/HfO_2/Pt [9], and $SrTiO_3$/TiO_2/Ti/Au [18]) have been observed to exhibit quantum conductance effects.

While TiO_2 as an active layer for memristive devices has been well studied [29], [30], [31], a potential for attaining controlled quantum effects [18] and structural investigations concerning this characteristic have been recently reported [32]. Through the present work, a statistical analysis of quantum effects, attained by two distinct programming strategies, sheds light on the quantum conductance characteristics of TiO_2/TiO_x memristive devices. Moreover, temperature effects on similar devices to the one presented in this work (i.e., stacked memristive devices employing transition metal oxide active layers) report encouraging results to enable accurate modeling and explore operational capacity in a narrower range of higher temperatures [33], [34]. This work exposes the memristive devices to temperatures down to 8 K to investigate the electronic conduction mechanism in fixed states (one $\sim 5\ G_0$) with varying temperatures. The well-studied memristive dynamics of the TiO_2/TiO_x active layer was preferred in this work to enable the temperature-dependent measurements at various resistance states and acquiring repeatable quantum conductance behavior to carry out statistical analysis.

This work presents characterization results of TiO_2/TiO_x memristive devices with Cr/Au top electrodes. These results present: 1) a thorough statistical analysis of their quantum conductance effects measured by using two distinct programming strategies: applying a slow current input to SET the device and applying a slow voltage input to RESET the device; 2) a demonstration of G_0 retention; and 3) a temperature-dependent (8–230 K) electronic conduction mechanism of pristine states, low-resistance states, and resistance states close to the quantum regime.

II. Experiments

Cr/Au/TiO_2/TiO_x/Cr/Au devices were fabricated on a 3-in Si+SiO_2 wafer (oxide thickness 400 nm). Both top and bottom capping layers are Au. Cr was used as an adhesion layer for Au, and 5-nm Cr was deposited by E-beam evaporation. 40-nm Au was deposited using thermal evaporation. Electrodes were patterned using a negative photoresist and lift-off was performed. The active layer consists of stoichiometric TiO_2 and doped TiO_x. The stoichiometric TiO_2 is conventionally deposited through sputtering a TiO_2 target with argon allowed in the chamber only. The TiO_x layer was attained by sputtering a Ti target while allowing 5% O_2 plasma into the chamber along with argon, similar to what is described in [11]. This layer is patterned using a positive photoresist. Finally, Cr+ Au is deposited again through thermal evaporation and patterned by liftoff. All deposition steps were carried out in Leybold L560 Boxcoater. Photolithography was carried out using a Karl Suss MJB3 mask aligner. The cross section of the resulting structure and the top-down view from the microscope are shown in Fig. 1. I–V characterization was carried out using Keithley 4200 connected to an EverBeing probe station by applying the excitation signal to the top electrode and grounding the bottom electrode.

Low-temperature measurements were performed in a two-stage cryocooler (Leybold ROK 10-300) connected to a vacuum chamber ($\sim$10–3 mbar). The devices were wire-bonded to a sample holder made of copper, which was screwed to the cryocooler cold head. A spontaneous temperature increase was obtained by switching off the cryocooler, allowing to obtain electrical measurements by applying a current sweep to the devices at different temperatures. Temperature was measured using a silicon diode sensor (LakeShore DT-670), embedded in the cold head, controlled by a LakeShore 331 temperature controller. The V–I measurements were performed by applying a current signal, supplied by a Keithley 6430 Sub-Femtoamp SourceMeter, and the voltage was measured by an Agilent 34 401A multimeter. The instruments were controlled remotely using Python, and the V–I acquisitions were set to be fast enough to reduce temperature fluctuations. During the electrical measurements, the temperature fluctuations were in the order of 0.1 K. The amplitude of the current signal was kept low enough such that variations in the electronic conductivity of the device were not induced by switching events.

III. Results and Discussion

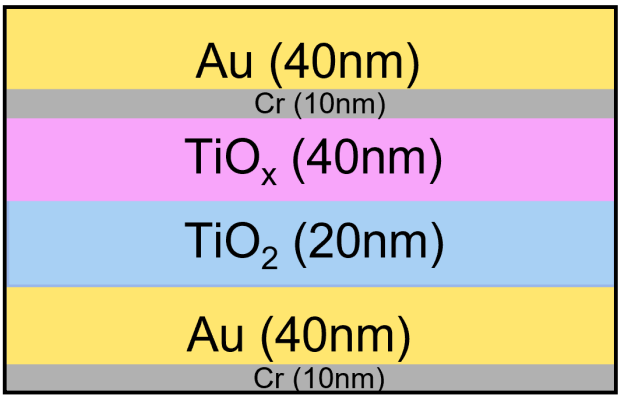
A. Electrical Characterization

Before exhibiting resistive switching behavior, the device underwent a forming process to initiate the conductive filament. This forming process was performed by applying a voltage ramp to the device, where the forming voltage was observed to be about 2 V.

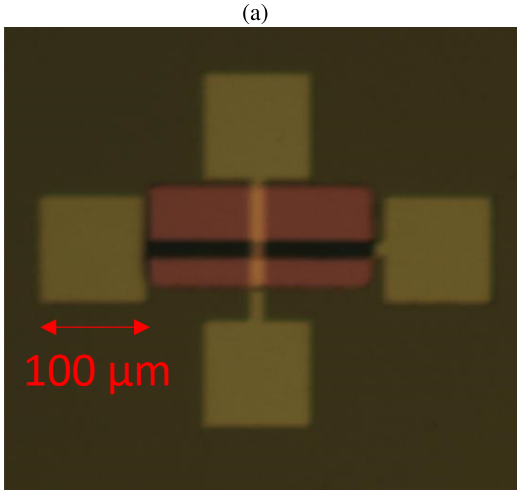
Following this forming step, electrical characterization was carried out and repetitive switching behavior was observed. Fig. 2 shows examples of consecutive hysteresis loops and the distinct LRS and high HRS (2 and 1 in the positive quadrant and 3 and 4 in the negative quadrant respectively).

A compliance current (I_{cc}) of 1 mA is used for the positive loop since this is the cycle where the SET operation occurs and the resistance drops to the LRS value. It is important to limit the maximum value of current that can flow through the device to avoid breakdown. In the negative cycle, however, there is no compliance current. The device RESETs between -0.4 and -0.8 V and the device resistance increases back up to its HRS value. As such, a lower current begins to flow through the device following the RESET. This is demonstrated in Fig. 2 complete with the switching direction of the device. The device exhibits clear LRS and HRS values of about 400 Ω and 8 kΩ, respectively (the resistance values were acquired at $V_{read} = \pm 0.4$ V).

While Fig. 2 shows repetitive switching between LRS and HRS for an I_{cc} of 1 mA, Fig. 3 shows the variation LRS values due to different values of I_{cc}. As can be observed, lower I_{cc} results in higher LRS, whereas higher I_{cc} renders much lower



(a)



(b)

Fig. 1. Cr/Au/TiO_2/TiO_x/Cr/Au memristive devices, (a) showing cross-sectional structure of the completed device and (b) showing the microscope image of the completed memristive device.

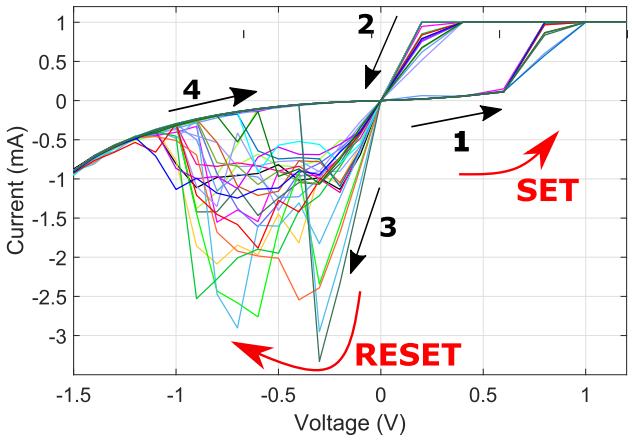


Fig. 2. Indicative hysteresis plots showing *I–V* behavior between −1.5 and 1 V input voltage and $I_{cc} = 1$ mA.

LRS. This demonstrates that the internal LRS of the device can be tuned through the applied I_{cc} value. Similar behavior has been reported and deemed useful for multilevel switching [35].

B. Quantum Conductance

The devices were excited using two distinct setups to observe quantum conductance behavior. The first method as

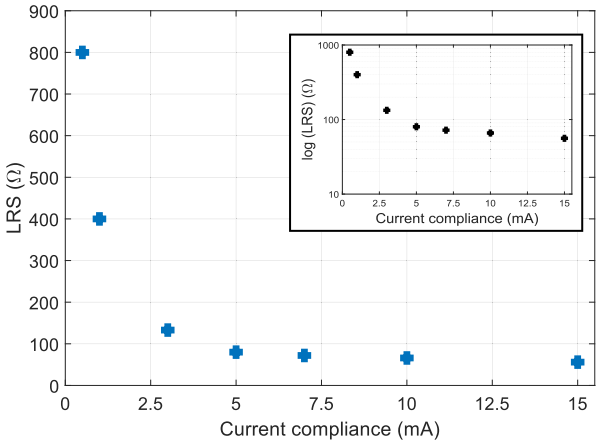


Fig. 3. Variation of LRS at different I_{cc} values, the inset showing LRS in the log scale against I_{cc}.

seen in Fig. 4(a) utilizes a positive current input signal. The device starts from its HRS value, quantum conductance effects are observed in the first quadrant, while the conductance is increasing. The results and statistical analysis of this method are shown in Fig. 4. The second method utilizes a negative voltage ramp to trigger quantum effects. Therefore, the device starts from its LRS value, quantized states are observed in the third quadrant while the conductance is decreasing, and the programming strategy is depicted in Fig. 5(a). These results are shown in Fig. 5.

As mentioned above, as shown in Fig. 4(a), a slow current ramp of duration 100 s and amplitude 20 μA is applied to the top electrode to SET the device, followed by a fast RESET with a voltage input of duration 2 s and amplitude −1.5 V. As such, at the beginning of the measurement, the memristive device starts from HRS, and the conductance increases as a conductive filament (or filaments) forms. This behavior is presented in Fig. 4(b); six measurements from the same device show the occurrence of quantum conductance steps during the positive slope of the input current. Distinct integer G_0 values are recorded. The amplitude of the ramp was determined to be high enough to trigger quantum effects but low enough to allow for repetitive measurements without causing breakdown. These measurements were conducted to observe if certain integer conductance states occur more readily and frequently. Results of 200 cycles, with responses similar to and including ones shown in Fig. 4(b), were analyzed statistically. The histogram obtained by more than 70 000 conductance points in Fig. 4(c) shows a clear tendency of the device to exhibit 1 G_0 conductance. It can be seen from the six indicative plots in Fig. 4(b) that the devices start from a low conductance state and quickly jump to an integer G_0 state due to the positive current input. This initial quantum conductance jump commonly happens to be to 1 G_0 and can last for longer than half of the positive ramp. A retention measurement of this state is also presented in Fig. 6.

In Fig. 5(a), the second programming strategy is depicted. The device is set with a fast voltage ramp of 3-V amplitude and 12-s duration, it is then excited by a slow voltage ramp of −0.8-V amplitude and 760-s duration. The device RESETs

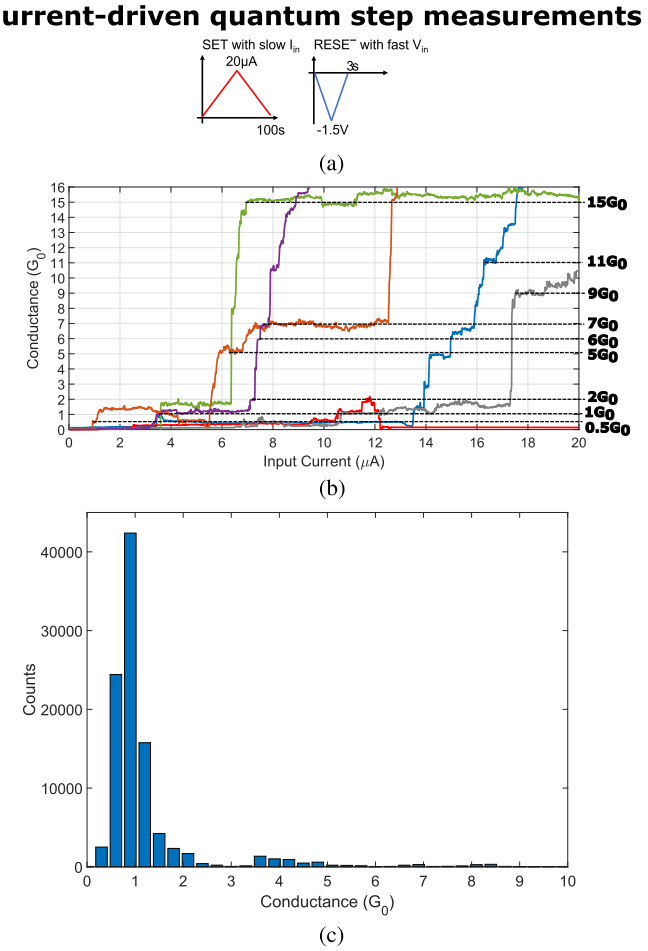


Fig. 4. Quantum conductance effects in current-driven devices. (a) Current-driven programming strategy for measuring quantum steps occurring due to slow current input. (b) Indicative results exhibiting quantum conductance steps in the SET cycle due to input current ramp. (c) Histogram showing the frequency of occurrence of G_0 states of a device that has been driven with a slow positive current ramp for 200 cycles.

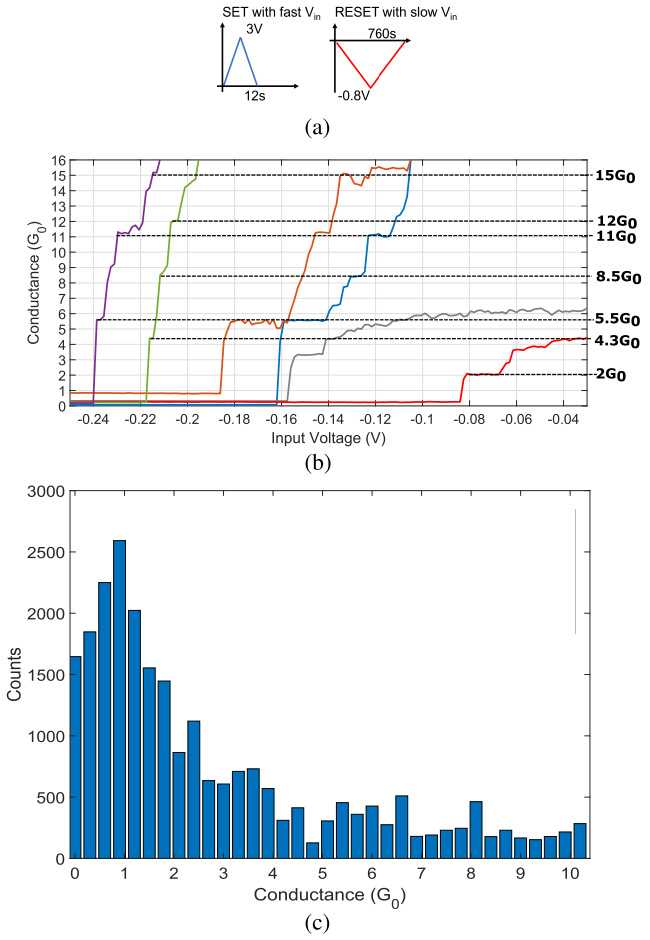


Fig. 5. Quantum conductance effects in voltage-driven devices. (a) Voltage-driven programming strategy for measuring quantum steps occurring due to slow voltage input. (b) Indicative results exhibiting quantum conductance steps in the RESET cycle due to input voltage ramp. (c) Histogram showing the frequency of occurrence of G_0 states of a device that has been driven with a slow negative voltage for 240 cycles.

during this negative cycle and exhibits quantum conductance. Distinct integer and half-integer values of G_0 are observed as shown in Fig. 5(b). The graph shows the decrease in conductance from LRS to HRS between the voltage values of 0 and -0.24 V. Similar to the current-driven measurement, the frequency of occurrence of G_0 states was investigated. This device was tested with the same input sequence 240 times. The resulting quantum conductance behavior was analyzed statistically to render the histogram, resulting from more than 20 000 conductance points, shown in Fig. 5(c). Once again 1 G_0 is observed frequently.

After programming the device to 1 G_0, the stability of this resistance state over time was analyzed through retention measurements by applying a dc read voltage of 10 mV. As can be observed from Fig. 6, the device retained the conductance state for 4000 s. Here, the device exhibited a mean conductance value of 1.024 G_0 (median of 1.03 G_0), with a standard deviation of 3.48% (number of sampling points: 73 789). After this point, the device began to behave less stably, exhibiting a larger standard deviation but remained in a conductance state of around 1 G_0–1.1 G_0.

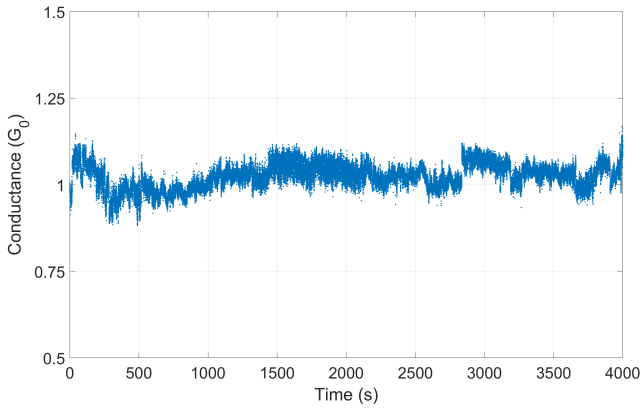


Fig. 6. 1 G_0 retention $V_{read} = 0.01$ V.

C. Temperature-Dependent Measurement Results

To investigate the electronic conduction mechanism, the evolution of resistance over temperature was investigated in devices programed to different conductance values. The first

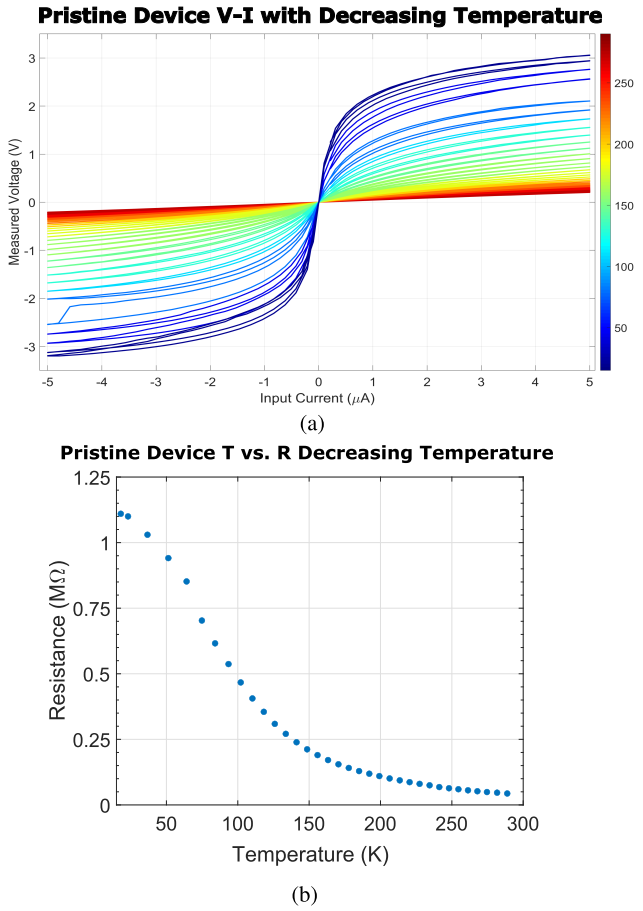


Fig. 7. Pristine device with current input in decreasing temperature (a) showing the V–I plot and (b) showing the variation of resistance.

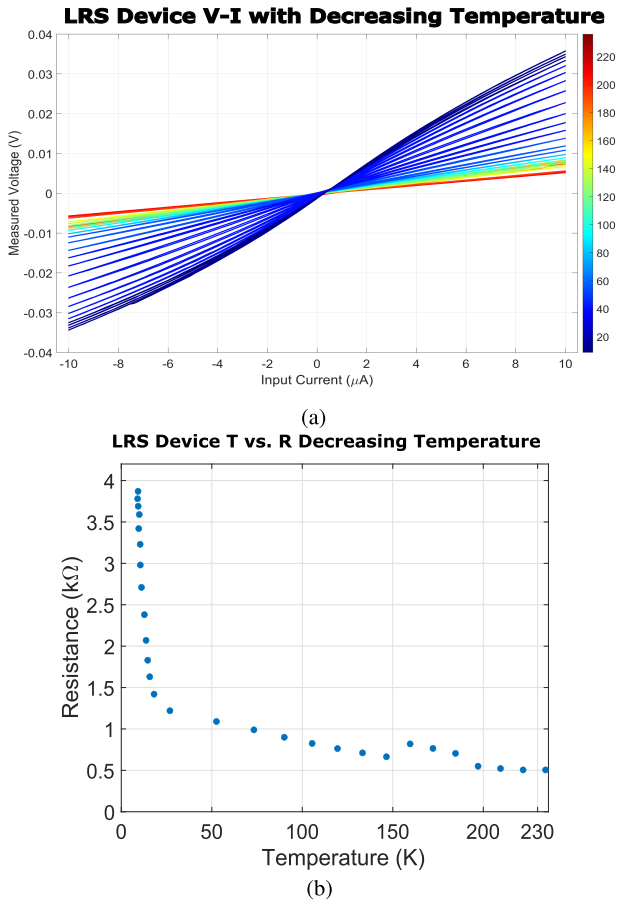


Fig. 8. Device set to LRS with current input in decreasing temperature (a) showing the V–I plot and (b) showing the variation of resistance.

device was considered in its pristine state (i.e., without being previously stimulated). The second device was set to an LRS of about 500 Ω. The last device was set at a resistance state near the quantum conduction regime (of ∼5 G_0). For this purpose, V–I sweeps were acquired by progressively decreasing temperature (shown in Figs. 7(a), 8(a), and 9(a). Note that the current range was selected such that reprogramming the device (i.e., switching) was avoided during characterization. In this way, it is possible to assess the evolution of the device's resistance to temperature without inducing any morphological change of the device. As mentioned previously, the measurements were taken fast enough to minimize temperature fluctuations in one cycle. Temperature-dependent measurements were performed by decreasing temperature down to at least 20 K for each device.

Fig. 7 shows the response of the pristine device to input current along with decreasing ambient temperature from 290 to 18 K. Nonlinear behavior of the V–I characteristics can be observed due to the insulating nature of TiO_2 and due to inversely polarized Schottky barriers at the metal–insulator interfaces. At room temperature, the device exhibited a resistance of 43 kΩ. This value of resistance was observed to progressively increase with decreasing temperature reaching a value of 1.1 MΩ at 18 K [Fig. 7(b)], in accordance with the insulating nature of the metal oxide. Similar behavior was observed in devices programed to LRS and in conductance values of ∼5 G_0, where both cases are characterized by nonlinear V–I characteristics and by an increase of resistance with decreasing temperature. Note that the pristine device, having not formed any filaments or been SET before this measurement, is exhibiting largely dielectric properties. The V–I plot shown in Fig. 7(b) also validates that the pristine device exhibits more nonlinearity in resistance variation. This departure from linear V–I characteristics starts from higher temperatures compared to the LRS and ∼5 G_0 devices.

In the case of the LRS-programed device, V–I measurements taken during the decreasing temperature (from 235 K to around 10 K) measurements are presented as shown in Fig. 8. It can be seen from Fig. 8(b) that resistance reads around 500 Ω at the very beginning of the temperature measurement cycle. The resistance of the device increases up to a maximum value of 4 kΩ, measured at 10 K. This variation in resistance due to temperature is not as drastic as the variation exhibited by the pristine device (the resistance of this device increased 8-fold, whereas the pristine device's resistance increased to 26 times its value at room temperature). Even though the device is in a more conductive state when it has been set to LRS, the active layer clearly acts as a semiconductor since it is still more conductive at higher temperatures. The V–I plots for the LRS device for decreasing temperature shown in Fig. 8(a) demonstrate that the device

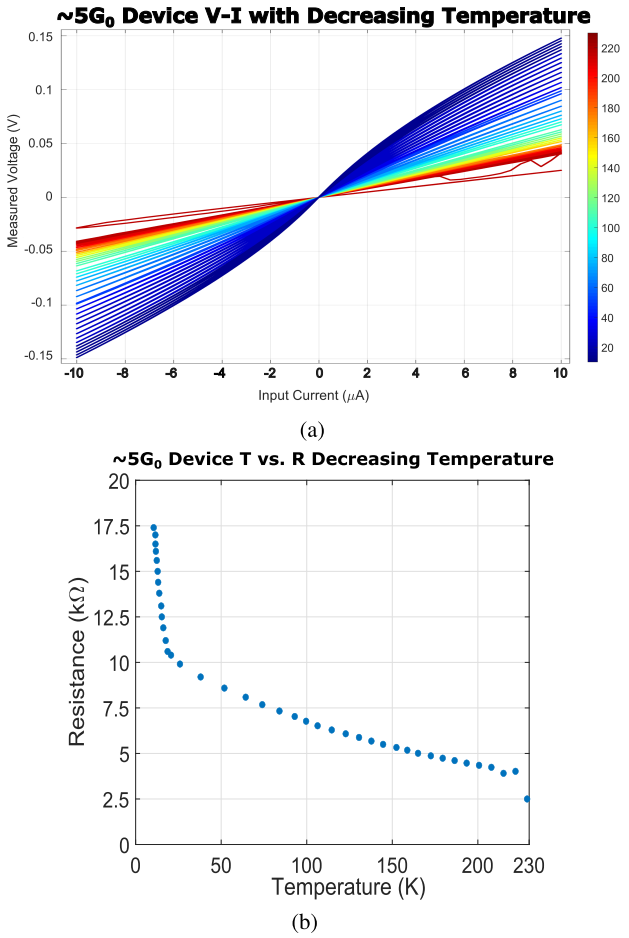


Fig. 9. Device set to ~5 G_0 with current input in decreasing temperature: (a) showing the V–I plot and (b) showing the variation of resistance.

remained stable throughout the temperature measurement, and the resistance changed gradually, ultimately exhibiting nonlinearity when exposed to exceedingly low temperatures. The temperature-dependent measurements reveal that the electronic transport properties in LRS are semiconductor-like despite the linear-like behavior of the V–I characteristics at higher temperatures.

Finally, the device programed to ~5 G_0 (~2.5 kΩ). Fig. 9(b) shows the resistance of the device as a function of temperature. It can be seen that as the temperature dropped, the resistance of the device continuously increased to 7 times its initial value, 17.5 kΩ, and the highest resistance value was measured at 12 K. The resistance increase is gradual until around 26 K. After this point, the temperature leads to a much more drastic resistance increase, and nonlinear behavior is exhibited, also clearly depicted in the V–I behavior is presented in Fig. 9(a).

Even though the devices were set to different states, the same overall behavior was observed. In all cases, the highest conductivity was recorded at the highest temperatures and as the devices were exposed to low temperatures, they became increasingly more resistive. This is in line with the previously reported temperature-dependent resistance of TiO_2 memristors [33]. Further work will be necessary to disentangle the effect of Schottky metal–insulator interfaces and the insulator itself in the R–T characteristics [36], [37].

IV. Conclusion

A thorough analysis of Cr/Au/TiO_2/TiO_x/Cr/Au memristive devices has been conducted and presented. Quantum conductance was observed for two different programming strategies: stimulating the device with a current input to observe quantum effects in the SET region and stimulating the device with a voltage input to observe quantum effects in the RESET region. Statistical analysis revealed that electrical stimulation tends to drive the device into quantum conductance levels close to G_0. Retention measurements revealed the possibility of programming the device to stable conductance states of ~G_0 that are almost stable for 4000 s. Temperature-dependent measurements were investigated to study the electronic conduction mechanism in these devices, revealing a semiconductor behavior characterized by an increase of resistance with decreasing temperature in devices in the pristine state, programed to LRS and ~5 G_0. Besides shedding light on programming strategies to achieve quantum conductance levels, this work also gives new insights into the electronic conduction mechanism in memristive devices based on TiO_2 active layers.

References

[1] H. He et al., "A Hamming weight calculation of binary string in one nMOS transistor–one Ag/Hf_2/black phosphorus/pt memristor," *IEEE Trans. Electron Devices*, vol. 69, no. 9, pp. 4920–4923, Sep. 2022.

[2] M. A. Zidan, J. P. Strachan, and W. D. Lu, "The future of electronics based on memristive systems," *Nature Electron.*, vol. 1, no. 1, pp. 22–29, Jan. 2018. [Online]. Available: https://www.nature.com/articles/s41928-017-0006-8

[3] D. V. Christensen et al., "2022 roadmap on neuromorphic computing and engineering," *Neuromorphic Comput. Eng.*, vol. 2, no. 2, Jun. 2022, Art. no. 022501, doi: 10.1088/2634-4386/ac4a83.

[4] H. D. Nguyen, J. Yu, L. Xie, M. Taouil, S. Hamdioui, and D. Fey, "Memristive devices for computing: Beyond CMOS and beyond von Neumann," in *Proc. IFIP/IEEE Int. Conf. Very Large Scale Integr. (VLSI-SoC)*, 2017, pp. 1–10.

[5] D. Ielmini and R. Waser, *Resistive Switching: From Fundamentals of Nanoionic Redox Processes To Memristive Device Applications*. Hoboken, NJ, USA: Wiley, 2016.

[6] S. Dong et al., "Performance estimation for the memristor-based computing-in-memory implementation of extremely factorized network for real-time and low-power semantic segmentation," *Neural Netw.*, vol. 160, pp. 202–215, Mar. 2023. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S0893608023000084

[7] M. Lanza et al., "Memristive technologies for data storage, computation, encryption, and radio-frequency communication," *Science*, vol. 376, no. 6597, Art. no. eabj9979. [Online]. Available: https://www.science.org/doi/full/10.1126/science.abj9979

[8] *International Roadmap for Devices and Systems 2021 Update: Beyond CMOS*, IEEE, 2021. [Online]. Available: https://irds.ieee.org/editions/2021/beyond-cmos

[9] J. J. Yang, D. B. Strukov, and D. R. Stewart, "Memristive devices for computing," *Nature Nanotechnol.*, vol. 8, no. 1, pp. 13–24, 2012. [Online]. Available: https://www.nature.com/articles/nnano.2012.240

[10] S. Tappertzhofen, H. Mündelein, I. Valov, and R. Waser, "Nanoionic transport and electrochemical reactions in resistively switching silicon dioxide," *Nanoscale*, vol. 4, no. 10, p. 3040, 2012. [Online]. Available: https://pubs.rsc.org/en/content/articlelanding/2012/nr/c2nr30413a

[11] C. Chang et al., "Direct observation of dual-filament switching behaviors in Ta_2O_5-based memristors," *Small*, vol. 13, no. 15, Apr. 2017, Art. no. 1603116. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/smll.201603116

[12] W. Sun et al., "Understanding memristive switching via in situ characterization and device modeling," *Nature Commun.*, vol. 10, no. 1, p. 3453, Aug. 2019. [Online]. Available: https://www.nature.com/articles/s41467-019-11411-6

[13] A. Mehonic et al., "Quantum conductance in silicon oxide resistive memory devices," *Sci. Rep.*, vol. 3, no. 1, p. 2708, Sep. 2013. [Online]. Available: https://www.nature.com/articles/srep02708

[14] G. Milan et al., "Quantum conductance in memristive devices: Fundamentals, developments, and applications," *Adv. Mater.*, vol. 34, no. 32, Aug. 2022, Art. no. 2201248. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/adma.202201248

[15] M.-K. Song et al., "Recent advances and future prospects for memristive materials, devices, and systems," *ACS Nano*, vol. 17, no. 13, pp. 11994–12039, Jul. 2023, doi: 10.1021/acsnano.3c03505.

[16] C. Mahata, M. Ismail, D. H. Kim, and S. Kim, "Quantized synaptic characteristics in HfO2-nanocrystal based resistive switching memory," *J. Mater. Res. Technol.*, vol. 21, pp. 981–991, Nov. 2022. [Online]. Available: https://www.sciencedirect.com/science/article/pii/S2238785422015022

[17] J. Zhao et al., "Realization of long retention properties of quantum conductance through confining the oxygen vacancy diffusion," *Appl. Phys. Rev.*, vol. 9, no. 2, Jun. 2022, Art. no. 021419. [Online]. Available: https://aip.scitation.org/doi/10.1063/5.0082919

[18] C. Hu, M. D. McDaniel, A. Posadas, A. A. Demkov, J. G. Ekerdt, and E. T. Yu, "Highly controllable and stable quantized conductance and resistive switching mechanism in single-crystal TiO_2 resistive memory on silicon," *Nano Lett.*, vol. 14, no. 8, pp. 4360–4367, Aug. 2014, doi: 10.1021/nl501249q.

[19] J. Ge and M. Chaker, "Oxygen vacancies control transition of resistive switching mode in single-crystal TiO_2 memory device," *ACS Appl. Mater. Interfaces*, vol. 9, no. 19, pp. 16327–16334, May 2017, doi: 10.1021/acsami.7b03527.

[20] W. Xue, S. Gao, J. Shang, X. Yi, G. Liu, and R. Li, "Recent advances of quantum conductance in memristors," *Adv. Electron. Mater.*, vol. 5, no. 9, Sep. 2019, Art. no. 1800854. [Online]. Available: https://onlinelibrary.wiley.com/doi/10.1002/aelm.201800854

[21] K. Krishnan, M. Muruganathan, T. Tsuruoka, H. Mizuta, and M. Aono, "Quantized conductance operation near a single-atom point contact in a polymer-based atomic switch," *Jpn. J. Appl. Phys.*, vol. 56, no. 6S1, Jun. 2017, Art. no. 06GF02. [Online]. Available: https://iopscience.iop.org/article/10.7567/JJAP.56.06GF02

[22] W. Yi et al., "Quantized conductance coincides with state instability and excess noise in tantalum oxide memristors," *Nature Commun.*, vol. 7, no. 1, p. 11142, Apr. 2016. [Online]. Available: https://www.nature.com/articles/ncomms11142

[23] X. Zhu et al., "Observation of conductance quantization in oxide-based resistive switching memory," *Adv. Mater.*, vol. 24, no. 29, pp. 3941–3946, 2012. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/adma.201201506

[24] G. Milano, F. F. Lupi, M. Fretto, C. Ricciardi, N. De Leo, and L. Boarino, "Memristive devices for quantum metrology," *Adv. Quantum Technol.*, vol. 3, no. 5, May 2020, Art. no. 2000009. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/qute.202000009

[25] K. Terabe, T. Hasegawa, T. Nakayama, and M. Aono, "Quantized conductance atomic switch," *Nature*, vol. 433, no. 7021, pp. 47–50, Jan. 2005. [Online]. Available: https://ezproxy.etu.edu.tr:2468/articles/nature03190

[26] A. Vokhmintsev, I. Petrenyov, R. Kamalov, and I. Weinstein, "Quantum conductors formation and resistive switching memory effects in zirconia nanotubes," *Nanotechnology*, vol. 33, no. 7, Feb. 2022, Art. no. 075208, doi: 10.1088/1361-6528/ac2e22.

[27] B. Standley, W. Bao, H. Zhang, J. Bruck, C. N. Lau, and M. Bockrath, "Graphene-based atomic-scale switches," *Nano Lett.*, vol. 8, no. 10, pp. 3345–3349, Oct. 2008, doi: 10.1021/nl801774a.

[28] R. D. Nikam, K. G. Rajput, and H. Hwang, "Single-atom quantum-point contact switch using atomically thin hexagonal boron nitride," *Small*, vol. 17, no. 7, 2021, Art. no. 2006760. [Online]. Available: https://ezproxy.etu.edu.tr

[29] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008. [Online]. Available: https://www.nature.com/articles/nature06932

[30] J. J. Yang, J. Borghetti, D. Murphy, D. R. Stewart, and R. S. Williams, "A family of electronically reconfigurable nanodevices," *Adv. Mater.*, vol. 21, no. 37, pp. 3754–3758, Oct. 2009. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/adma.200900822

[31] J.-J. Huang, C.-W. Kuo, W.-C. Chang, and T.-H. Hou, "Transition of stable rectification to resistive-switching in Ti/TiO2/Pt oxide diode," *Appl. Phys. Lett.*, vol. 96, no. 26, Jun. 2010, Art. no. 262901, doi: 10.1063/1.3457866.

[32] M. C. Sahu, S. K. Mallik, S. Sahoo, S. K. Gupta, R. Ahuja, and S. Sahoo, "Effect of charge injection on the conducting filament of valence change anatase TiO_2 resistive random access memory device," *J. Phys. Chem. Lett.*, vol. 12, no. 7, pp. 1876–1884, Feb. 2021, doi: 10.1021/acs.jpclett.1c00121.

[33] D. Vaidya et al., "Compact modeling of the switching dynamics and temperature dependencies in TiO_x memristors—Part II: Physics-based model," *IEEE Trans. Electron Devices*, vol. 68, no. 10, pp. 4885–4890, Oct. 2021.

[34] Y. Huang, R. Hopkins, D. Janosky, Y.-C. Chen, Y.-F. Chang, and J. C. Lee, "Effect of temperature on analog memristor in neuromorphic computing," *IEEE Trans. Electron Devices*, vol. 69, no. 11, pp. 6102–6105, Nov. 2022. [Online]. Available: https://ezproxy.etu.edu.tr:2217/document/9903412

[35] A. Bricall et al., "Resistive switching device technology based on silicon oxide for improved ON-OFF ratio—Part I: Memory devices," *IEEE Trans. Electron Devices*, vol. 65, no. 1, pp. 115–121, Jan. 2018.

[36] G. Milano, L. Boarino, and C. Ricciardi, "Junction properties of single ZnO nanowires with asymmetrical Pt and Cu contacts," *Nanotechnology*, vol. 30, no. 24, Jun. 2019, Art. no. 244001, doi: 10.1088/1361-6528/ab0a9c.

[37] G. Milano, E. Miranda, M. Fretto, I. Valov, and C. Ricciardi, "Experimental and modeling study of metal–insulator interfaces to control the electronic transport in single nanowire memristive devices," *ACS Appl. Mater. Interfaces*, vol. 14, no. 47, pp. 53027–53037, Nov. 2022, doi: 10.1021/acsami.2c11022.