Assessing the Effectiveness of the Test of Power Devices at the Board Level

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***Abstract* — Power devices have an increasing relevance in many applications, including some safety-critical ones. In the latter case, the effectiveness of the test performed at the end of the manufacturing, when the device is already mounted on the final board, is crucial. Unfortunately, assessing such effectiveness is not trivial, since it requires defining a metric that could be measured in an objective manner. Following a trend that is common to the whole world of analog components, in a previous paper we proposed a fault model based on the availability of the electrical model of the power device. Using this fault model, the test engineer can assess and possibly improve the quality of the developed test solution, and optimize the overall test plan so that a given fault coverage is achieved with minimum cost. The proposed fault requires the availability of the electrical model of the power device. In this paper we adopt this approach on a case of study using a power device, and analyze the effectiveness provided by a set of functional tests and an in-circuit one. Results are reported and discussed, showing the advantages and limitations of the approach.**

Keywords — Power electronics; Functionally test; End-of-manufactory test; PCB test; Safety-Critical applications

I. INTRODUCTION

Power electronics plays a fundamental role in modern technology. It is used in many industrial applications, for example in the transport and generation of electricity, and to supply electrical loads with variable AC or DC voltages and currents necessary for their operation. Power electronics are also widely used in many safety-critical applications, e.g., in industrial, automotive, medical applications and household appliances. In safety-critical systems, a fault can lead to significant consequence for the health or life of the users. Hence, safety-critical systems require accurate test mechanisms at the end of the production and in the field. Moreover, safety standards require to adopt metrics to assess the effectiveness of the adopted test schemes. All the aspects of safety-critical systems must be tested: the digital control part, the analog part, the power components and the Printed Circuit Board (PCB). Many test approaches are available to test the digital circuits, e.g., resorting to Design for Testability [11]. Other test strategies are available to test the analog and power circuits [12] and to evaluate the fault coverage [13][14][15] of the analog test procedures. Some efforts to define suitable metrics for PCB testing have also been performed [18]. In recent years, a special effort has been made to propose fault models for analog and mixed-signal circuits, able to trade-off the ability to provide meaningful metrics in terms of test quality with the feasibility of their computation [10][16]. Following this effort, some commercial software tools appeared on the market. Tools like DefectSim® [15] allow to inject different faults considering different fault models or to define new fault models customized for specific needs or applications. The new commercial software tools, thanks to the underlying fault models, allow to compute metrics able to assess the quality of a test procedure and thus also pave the way towards the automatic generation of effective test procedures for mixed-signal circuits and modules. On the other side, the growing adoption of analog and power devices and modules in applications where safety is a crucial parameter asks for techniques to estimate the probability of failures, and thus the reliability of the whole system. For example, electronic systems adopted in the automotive domains must match the constraints mandated by the ISO 26262 standard, which mandatorily requires adopting a suitable metric to assess the quality of the adopted test procedures. Hence, the ability to compute the likelihood that the end-of-production test is able to successfully identify all faulty products becomes an important step towards the certification of the quality of any power-related system. In [5] the authors focused on a possible approach to combine the recent developments in the area of fault models with the emerging need to grade the quality of a test for any system including a power device. A method to assess the quality of the test for a power device was proposed, mainly suitable for the incoming inspection test performed on single devices before they are mounted on a board. In this paper, we consider the test of a PCB [17] including a power device. Specifically, this work aims at proposing solutions to assess the quality of a test to be performed at the end of PCB manufacturing and aimed at detecting possible defects affecting the power device, since they may significantly impact the behavior of the resulting system. When considering this purpose, the most common approach lies on performing a combination of an in-circuit test, checking whether the device has been correctly mounted and whether it still works correctly after the PCB manufacturing, and a functional end-of-line test, checking the correctness of the final system behavior. Unfortunately, the ability to quantitatively measure the effectiveness of all test steps is severely limited by the lack of a well-accepted fault coverage metric, especially when focusing on internal defects affecting the power component. Our proposal is to rely on an electrical model of the power device, then adopting the fault models already proposed in [5], and finally performing the simulation of each fault to label it as detected or not. For the purpose of this work, we selected as a case study a boost power system including an Isolated Gate Bipolar Transistor (IGBT). Some functional tests are considered, plus some simplified versions of an in-circuit test. The analysis of the experimental results we gathered provides useful guidelines to optimize the test steps (e.g., deciding what to observe and when) and decide about the most suitable mix of functional and in-circuit test. The method also provides information about the defects that may result not to be detected by some or any of the test steps. The paper is organized as follows: Section 2 summarizes the state of the art in terms of fault models proposed in the literature for analog and power

components and describes the electrical model we used for the IGBT device. In Section 3, the proposed approach to compute the Fault Coverage attained by a given test is outlined. Section 4 describes the case of study we considered for our experiments, as well as the different tests. Section 5 reports the gathered experimental results and discusses them. Finally, some conclusions are drawn in Section 6.

II. BACKGROUND

This section first provides the reader with the required information about the typical fault models used in analog and power circuits. In the second subsection, the IGBT equivalent electrical model (describing its behavior using an electrical network) we used in this paper is presented.

A. Analog fault models

In the analog and power electronics all the electrical quantities are continuous over time. This behavior makes more complex the definition of a unique fault model, as it happens in digital electronics. The binary behavior of the digital circuits allows the definition of the widely adopted stuck-at fault model. According to it, the fault can be modeled assuming that the logic value of an input or an output of a gate is always fixed at one logical value (stuck-at zero) or at the other (stuck-at one). Coming back to analog components, the electrical quantities characterizing them depend on many external factors such as the operating temperature, the tolerance, the aging and the presence of electrical disturbances (electrical noise). Many of these parameters are random and external to the circuit itself. All these undesirable phenomena have negligible impact on the circuit only if the circuit has been correctly designed and its components correctly sized. It is therefore difficult to univocally define a fault model applicable to analog and power circuits. Out of the different possible fault models for analog circuits, the most used models can be distinguished into *catastrophic* faults and *parametric* faults [1][2]. *Catastrophic* faults correspond to open circuits or short circuits in the electrical network. In practice, catastrophic faults correspond to very large variations of the nominal parameters of the component. For example, considering a resistor, a *catastrophic* fault corresponds to turning it into a resistor of zero resistance (short circuit) or into a resistor of infinite resistance (open circuit). The *catastrophic* fault is normally modeled in the electrical network by inserting an electrical switch. In the case of the resistor, a switch in series with the component is used to model the open circuit, or a switch in parallel with the resistor is used to model the short circuit. Moreover, the electric circuit can be considered as a graph. In the graph, it is possible to insert other *catastrophic* faults. In particular, it is possible to insert short circuits between nodes that are normally not connected. The *parametric* faults are modeled with variations of one of the nominal parameters of a component outside its nominal range. Usually, all the parameters of a component are associated with a range of validity. For example, considering a resistor belonging to the E12 standard series, the resistance value has a nominal range of ±10%. A *parametric* fault on the resistor corresponds to varying the value of the component by more than ±10%. As it happens for digital circuits, also for analog ones it is possible to consider both the *single fault* scenario and the *multiple fault* scenario [2]. In the *single fault* scenario, only one fault is considered at a time. In the *multiple fault* scenario, more faults are considered simultaneously at the same time. Furthermore, it is possible to distinguish faults into two further categories, the *permanent* faults and the *temporary* faults. The permanent faults are faults that are always present in the circuit. Usually, they are associated to broken devices or non-functioning devices. On the other side, the *temporary* faults are faults that occur only occasionally for a limited time. The *temporary* faults occur only in particular conditions; for example, due to high temperatures or due to electric welding not correctly performed. For the purpose of this paper we will only consider single permanent faults belonging to the catastrophic category.

B. IGBT equivalent electrical model

The aim of this section is to show the equivalent electrical model of the *Insulated Gate Bipolar Transistor* (IGBT) device. Such a kind of model is often provided by the device manufacturer. In other cases, it can be built by the user, knowing the characteristics of the device. For the purpose of this paper we followed the latter approach. Using the basic model proposed in [3], and adding the parasitic components proposed in the model suggested in [4], we built an equivalent electric model of the IGBT. The equivalent electric model we adopted is broadly discussed in [5] and shown in Figure 1.

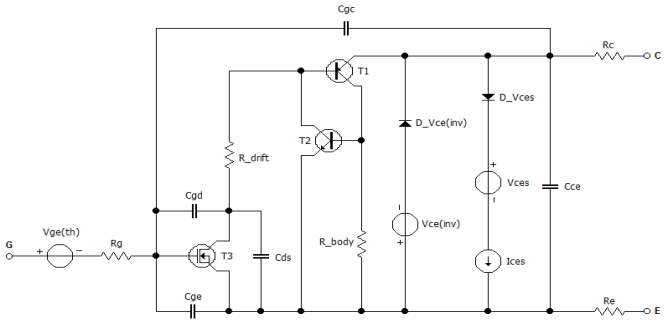

Figure 1: The adopted IGBT equivalent electrical model

The IGBT transistors are designed to combine the advantages of the Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) with the advantages of the Bipolar Junction Transistor (BJT) [6]. In particular, the success of the IGBT lies in its ability to merge the high input impedance of the MOSFET and the output characteristic of the BJT. The IGBTs are driven by low power signals and they can manage the high current flows between the collector and the emitter. However, the IGBT has lower switching speeds than those of power MOSFETs. The model considered here is based on the basic electrical scheme of the IGBT, composed of the MOSFET T3 transistor and the BJT T1 transistor. The electrical and physical significances of all the components present in the electrical model is discussed in [5]. With respect to the basic circuit composed of the T1 and T3 transistors, the model has been improved considering other parasitic aspects. The access resistances Rc and Re, the parasitic capacitances (Cgd, Cds, Cge, Cgc, Cce), the drift resistance (R_drift) [7], the body resistance (R_body) and the parasitic transistor T2. The electrical branch composed of the D_Vces diode and the generators Vces and Ices allows to model the behavior of the device when it is subjected to the maximum tolerable voltage with the device turned off [7]. The last electrical branch, composed of the D_Vce(inv) diode and the generator Vce(inv),

describes the anti-parallel diode. The anti-parallel diode is integrated in the device and it is connected in parallel between the collector and emitter of the IGBT. The equivalent electric model with all the considered *catastrophic* faults is shown in Figure 2. In such a model an electrical switch is added for each *catastrophic* fault, as discussed in the *Analog fault models* subsection. In Table 1 the description of each fault considered in the equivalent electric model is reported. For each fault some corresponding possible physical defect is given.

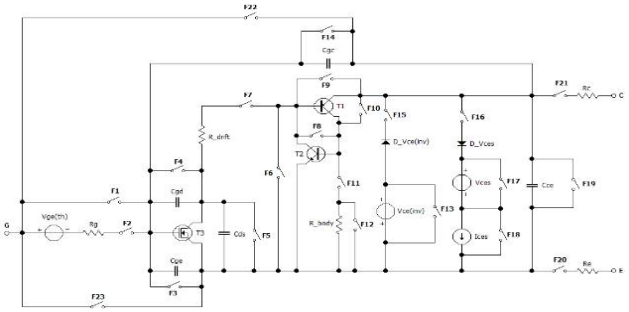

Figure 2: The IGBT equivalent electrical model with fault switches

Fault	*Description*
F1	The oxide is broken down on the gate terminal
F2	Disconnect gate terminal
F3	Short-circuited gate-emitter
F4	Short-circuited parasitic capacitance Cdg
F5	Short-circuited parasitic capacitance Cds
F6	Shorted MOS T3 transistor
F7	Open MOS T3 transistor
F8	Shorted PNP T1 BJT
F9	Shorted PNP T1 BJT
F10	Shorted PNP T1 BJT
F11	Breaking body region
F12	Breaking body region
F13	Short-circuited free wheel diode
F14	Short-circuited gate-collector
F15	Open anti-parallel diode
F16	Exclude the block phenomenal behavior
F17	Exclude the block phenomenal behavior
F18	Exclude the block phenomenal behavior
F19	Short-circuited collector-emitter
F20	Disconnect emitter terminal
F21	Disconnect collector terminal
F22	Short-circuited gate-collector
F23	Short-circuited gate-emitter

Table 1: The IGBT fault models

III. Proposed Approach

The aim of this work is to propose a method to evaluate the effectiveness of a test performed at the end of the PCB production to check the correct behavior of an IGBT device. In particular, to evaluate the ability of the test to detect some possible permanent faults present inside the Power Device Under Test (PDUT). In contrast to the approach described in [5], in this paper the PDUT is already mounted on the board and the test can be performed only by acting on the electrical stimuli applied to the inputs of the whole system and by only observing its outputs. The fault simulation is performed resorting to a circuit simulator. The proposed evaluation method to compute the Fault Coverage (FC) figure is shown in Figure 3. In a circuit simulator, the electrical circuit is ideally replicated.

The first circuit, called Reference Circuit, use the SPICE model of the PDUT. The output signal of the Reference Circuit is used as the reference signal. In the second circuit, called Circuit Under Test (CUT), the electric SPICE model of the PDUT is replaced with its equivalent electric model. Both circuits are driven with the same stimuli. The output of the reference circuit (called reference output) and the output of the CUT are compared. The error signal is computed according to equation (1), while the equation (2) computes the percent error signal.

$$error(t) = reference\ output(t) - cut\ output(t) \quad (1)$$

$$error\%(t) = \frac{|\ reference\ output(t) - cut\ output(t)\ |}{reference\ \ output(t)} \quad (2)$$

The error signal is used to evaluate the FC. The error signal is evaluated continuously at each time instant, thus obtaining a continuous curve over time.

The Fault Coverage figure is evaluated by different simulations in free-faults scenario and in presence of a fault. Each fault is individually injected in the equivalent electrical model using the electric switches, as described in Section 2. An error signal is produced during the simulation performed in presence of a single fault. The reference error signal produced during the simulation without fault and the error signal produced during the simulation in presence of the injected fault are compared. The comparison algorithm used to evaluate the fault uses a validity region. The validity region is defined by a pair of thresholds around the reference error, as shown in Figure 4. If the error signal produced during the simulation in presence of the injected fault is always contained in the validity region, the injected fault is labeled as *not detected*. On the other side, if the error signal produced during the simulation in the presence of the injected fault exits the validity region, the injected fault is labeled as *detected*.

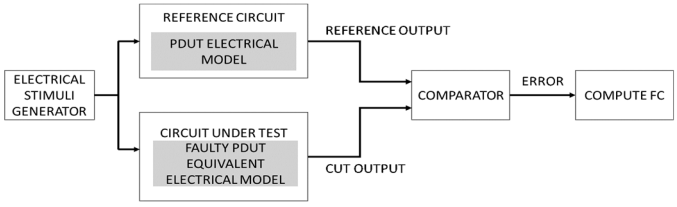

Figure 3: The FC evaluation method

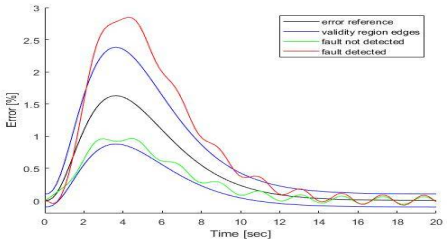

Figure 4: Example to show the adopted detection mechanism

This approach allows to detect the fault both during the initial transient or in the permanent regime. Very wide thresholds have been adopted in this work, corresponding to ±50% around the reference output, so that the fault is detected only if a substantial variation of the output is observed. The electrical stimuli generator is able to provide to both circuits the electrical signals used to perform the test. The stimulus generator is able to generate different types of signals consistent with the specifications provided in the design phase of the CUT. The input signals always respect the operating limits indicated by the technical specifications of the CUT.

IV. CASE STUDY

This section describes the adopted case study, corresponding to a boost converter. The features of the PDUT are then described. Finally, the list of stimuli used during the test are reported and discussed.

A. Boost Converter

The boost converter consists of 3 parallel sub-boosts driven by the FAN9673 analog controller produced by ON Semiconductor. Overall, the boost converter supplies an output voltage of 400V, with a ripple of ±7V, and a maximum current of 12A. The inverter is used as the first stage of a power supply system for a three-phase electrical motor. The boost converter works with an input voltage between 110V and 250V, with a frequency of 50Hz or 60Hz. The topology used in the converter is reported in Figure 5, where it is possible to see the sequence of the stages that are used.

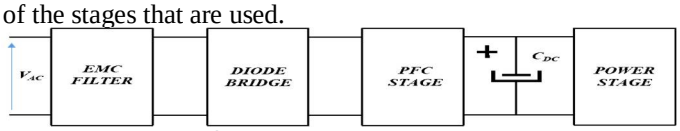

Figure 5: Sequence of the stages in the application

The Electro Magnetic Compatibility (EMC) Filter consists of a common mode choke and film capacitor used for reducing the conduced electromagnetic emission caused by the Power Factor Correction (PFC) switching. In the PFC stage there are the three legs of the interleaved PFC structure, as reported in Figure 6. Each leg is a simple boost cell composed by an inductor, a diode, and an IGBT. The output capacitor is in common on the DC-Link. The measures of the currents are obtained with 4-points shunt resistors placed in series to the IGBT. The FAN9673 controller measures the current on the IGBT in differential mode through the shunt resistance. Moreover, it measures the input voltage on the C_{IN} capacitor and in feedback the output voltage on the C_{DC} capacitor. The results of the control are the three different commands (QG_1, QG_2, QG_3) that are applied to the IGBTs to obtain the sinusoidal shape of the current absorbed from the grid and with a power factor almost unitary. The output is then connected to a DC load, which in this specific case is a classic three phase inverter for the motor control.

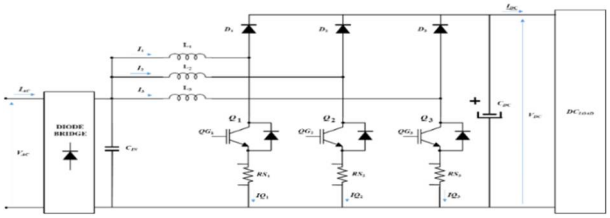

Figure 6: Three legs interleaved PFC

B. The STG19NC60 IGBT

The PDUT considered is the IGBT STGB19N produced by STMicroelectronics. This power device belongs to the Power MESH family [8], which is composed of power devices designed to control electric motors. It is a very fast IGBT, with a switching time of 200ns, and an ultrafast anti-parallel diode. The device has an excellent trade-off between switching performance and low on-state behavior. The chosen device is assembled in the TO-220FP package; it is able to handle a maximum voltage of 600V and a maximum current of 19A. The parameters indicated by the manufacturer and used in the equivalent electric model are shown in Table 2.

Parameter	Value	Condition
Collector-emitter breakdown voltage	V(BR)CES = 600V	Vge= 0V ICES = 1mA
Gate-emitter threshold voltage	Vge(th) = 4V	-
Collector-emitter saturation voltage	Vce(sat) = 2V	Vge = 15V IC = 15A
Input capacitance	Cies = 1180 pF	-
Output capacitance	Coes = 130 pF	-
Reverse transfer capacitance	Cres = 36 pF	-
Free anti-parallel diode threshold voltage	Vf = 2.5V	If = 12A

Table 2: The equivalent electrical model parameters

C. Test procedure

Four electrical stimuli applied to the converter during the test are used. These stimuli are compliant to the technical specifications of the boost converter under test. Moreover, these input patterns are compliant with the mission of the system; Europe, Asia, and America power network standards are considered. The sinusoidal stimuli are: S1:230V RMS 50Hz; S2:110V RMS 50Hz; S3:230V RMS 60Hz; S4:110V RMS 50Hz.

V. EXPERIMENTAL RESULTS

The proposed methodology discussed in Section III is used to assess the effectiveness of the test proposed in Section IV. The Boost converter described in Section IV.A is used as case study. The IGBT equivalent electrical model proposed in Section II and the fault model proposed in Section II are considered. Initially, this section describes the results concerning the validation of the equivalent electrical model of the IGBT under test. Then, the FC results considering a purely functional test approach are reported. In a purely functional approach, it is possible to interact with the system only through its interfaces, i.e., applying some electrical stimuli to its inputs and verifying the behavior of the circuit only through its outputs. Then, an in-circuit test approach is considered. In an in-circuit test approach some electrical quantities of the circuit are measured during the functional test by resorting to suitable probes[1]. The results of the in-circuit approach are also discussed. The FC results with the different test approaches (purely functional and in-circuit) are compared and discussed.

A. Electrical equivalent model validation

Usually, the PDUT model is provided by its manufacturer. If this model is not available, its equivalent electric model must be built and validated. In the case of the PDUT used in the CUT, the model is not available. The equivalent electrical model proposed in Section 2, with the parameters indicated in Section 4, is used. The model is validated with the method proposed in [5]. The error introduced to the equivalent electrical model is evaluated with a first simulation in free-fault scenario. The error is calculated with the equation (1) as indicated in Section 3. The error signals obtained with the four different stimuli are shown in Figure 7. As the reader can see,

[1] An In-Circuit Tester often allows to force specific voltages and currents on some test points in the PCB, and observe similar quantities in other points. For the purpose of the experiments reported this paper we assumed to only be able to use In-Circuit Test to increase observability.

the maximum error obtained comparing the output of the reference circuit with the output of the CUT is always less than 10%. In particular, the error signal is very low in steady state.

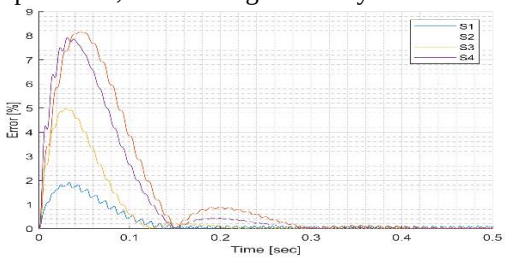

Figure 7: The validation of the equivalent electrical model

B. Fault Coverage evaluation

Once the equivalent electrical model is validated, some simulations were performed to evaluate the effects of each fault. Table 3 reports the result of each experiment with the S1 stimulus. The test performed with the purely functional approach, considering only the behavior of the boost circuit in the steady state, is first considered. As it is possible to note, in this way we cannot detect any injected fault. In fact, since the case study system consists of 3 sub-boosts in parallel, the single injected fault in the PDUT of one of the three sub-inverters is masked by the control system: the feedback system compensates the effects of the injected fault by acting on the command of the other two sub-boosts. In order to observe the injected fault, it is necessary to observe also the initial transient behavior of the circuit. Similar considerations are present with the stimuli S2, S3, and S4. Table 3 shows the result for each experiment with the S1 stimulus during the initial transient. The FC figure, considering the initial transient, reaches 69.6%. However, many system testers may have difficulty to observe the electrical transients. In case of a tester is unable to observe the initial transient, an additional in-circuit test may be introduced to observe the injected fault during the steady state. Some additional electric probes may be used to observe the voltage drop between the collector and the emitter of the IGBT under test, the IC current that flows through the device and the command activity produced by the control system. Three new error signals are thus introduced for the Vce, the Ic and the command activity, as discussed in Section 3. These new error signals are used to evaluate the FC achieved by the considered test. Table 4 shows the results of each simulation considering the in-circuit test approach. The obtained FC is 82.6%. It is interesting to note that the command activity is a good discriminant to observe the injected fault. In cases where the transistor is unable to switch to the ON state, the controller always keeps the high command value on the gate terminal of the IGBT. Normally, a square wave of about 60KHz is present on the IGBT gate terminal. In the presence of a fault that does not switch the transistor to the ON state, a fixed constant voltage at zero frequency is present on the gate terminal. Therefore, an error of 100% is found if the frequency of the square wave of the command signal is considered. Summarizes the FC values obtained by considering the three approaches: the purely functional approach with the steady state system, the purely functional approach extended to the initial transient and the in-circuit test approach. The results reported in Table 5 consider all the four stimuli described in Section 4. The faults F12, F15, F16 and F18 are never detected. These faults are associated with unused IGBT features, such as the anti-parallel diode. Overall, the results show that in the feedback systems the purely functional test may not be effective considering the system only in the steady state. With a sufficiently accurate tester it is possible to detect more faults also by analyzing the initial transient. However, the transient analysis requires particularly accurate tools that are not always available. A good compromise that allows to observe a fault is the in-circuit test. The in-circuit test is possible only if the tester has the possibility to directly contact the PDUT pins; in other words, if there are no obstructions above the PDUT (e.g., corresponding to heat sinks). In other cases, the PDUT is not accessible because it is assembled in a position that does not allow access by the tester.

Fault	Steady state		Initial transient		
	Max Vout error [%]	Detected	Max Vout error [%]	Detected	Transient duration [ms]
F1	<0.2	NO	5	YES	230
F2	<0.2	NO	5	YES	250
F3	<0.1	NO	1.9	NO	270
F4	<0.2	NO	5	YES	240
F5	<0.2	NO	5	YES	250
F6	<0.2	NO	5	YES	230
F7	<0.2	NO	5	YES	250
F8	<0.1	NO	0.9	NO	220
F9	<0.2	NO	5	YES	270
F10	<0.2	NO	5	YES	250
F11	<0.2	NO	5	YES	250
F12	<0.1	NO	1	NO	230
F13	<0.2	NO	5	YES	260
F14	<0.1	NO	1.9	NO	280
F15	<0.1	NO	1.9	NO	270
F16	<0.1	NO	1.9	NO	280
F17	<0.1	NO	4.5	YES	240
F18	<0.1	NO	1.9	NO	270
F19	<0.2	NO	5	YES	250
F20	<0.2	NO	5	YES	260
F21	<0.2	NO	5	YES	280
F22	<0.2	NO	5	YES	260
F23	<0.2	NO	5	YES	250

Table 3: The FC functional test results

Fault	Steady state			
	Max Ic error [%]	Max Vce error [%]	Max command frequency error [%]	Detected
F1	98	62	100	YES
F2	98	62	100	YES
F3	98	65	100	YES
F4	98	62	100	YES
F5	98	62	100	YES
F6	98	62	100	YES
F7	98	62	100	YES
F8	95	68	100	YES
F9	95	62	100	YES
F10	27	62	12	YES
F11	98	62	100	YES
F12	<1.5	<1	3	NO
F13	95	62	100	YES
F14	98	66	100	YES
F15	<1.5	<1	2.5	NO
F16	<1.5	<1	2.4	NO
F17	27	<1	4.4	YES
F18	<1.5	<1	2.4	NO
F19	95	62	100	YES
F20	98	62	100	YES
F21	98	62	100	YES
F22	95	62	100	YES
F23	95	62	100	YES

Table 4: The FC in-circuit test results

For sake of completeness, the example of a possible effect of a fault on the system is reported and analyzed. Figure 8 shows four graphs related to the output voltage of the whole inverter,

the Ic of the PDUT, the Vce of the PDUT and its command gate activity. Each graph shows the trend obtained in the fault-free scenario and in the presence of the injected fault in the PDUT. In particular, the case of the F11 fault with the S1 stimulus is reported. In the first figure it is possible to note the correction actuated by the control system to compensate the injected fault. The second and third figures show the Vce and Ic of the IGBT under test, respectively. The different trends of the voltage and current of the IGBT in the presence/absence of the F11 fault can be noted. The last figure shows the activity of the command in the absence and in the presence of the injected fault.

Functional test approach	FC [%]
Purely functional: steady state only	0%
Purely functional: extended to the initial transient	69.6%
In-circuit test	82.6%

Table 5: FC results summary

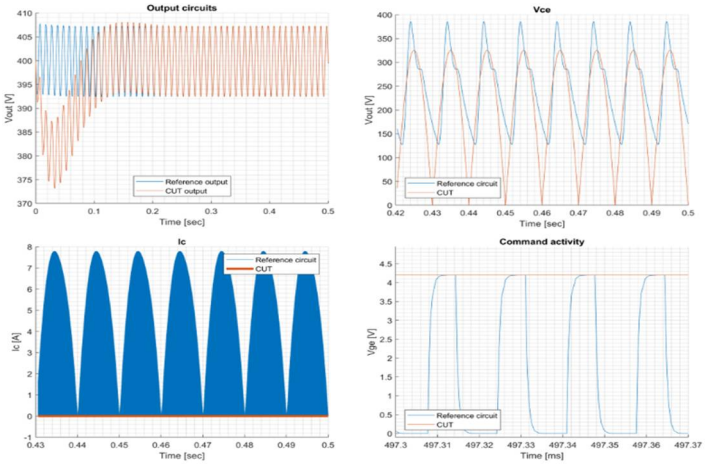

Figure 8: The F11 catastrophic fault effects

The Matlab-Simulink® software environment was used to perform the simulations. In particular, the PLECS® tool by Plexim® is used. PLECS® is a circuit simulator tool integrated in the Simulink® environment. It is specifically designed to simulate the electrical and electronic power systems. The analysis of the PLECS® simulation results are performed with MATLAB®, taking advantage of the computational capabilities of its scripts. The numerical solver used in Simulink® is the ODE45 [9], which is able to operate using an adaptive variable integration step during the simulation. Each simulation of the whole system and the evaluation of the injected fault has required about 4 hours of computation. The system is simulated for a time of 0.5 seconds. This time is sufficient for completing the initial transient and to observe a sufficient number of cycles in the steady state. The experiments were performed on a PC equipped with an 8 cores AMD FX-8370 processor operating at 4GHz. The PC is equipped to 32 GB of 1333 RAM memory.

VI. Conclusions

This paper shows a possible method to evaluate the effectiveness of a PCB test strategy when considering the test of a power device after PCB manufacturing. The use of an equivalent electric model of a PDUT allows the unambiguous definition of a set of possible models for permanent faults. The ability of the test to detect these faults can thus be measured. This metric is useful in order to understand the real effectiveness of the test and to be able to improve it. The proposed method was evaluated on a power device in a real case. We are now working towards further solutions to improve the Fault Coverage we can achieve at the end of the PCB manufacturing, e.g., resorting to thermal measurements. The example case proposed considered a power IGBT, but the proposed method is independent of the power device to be tested.

VII. Acknowledgments

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VIII. References

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