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10 November 2026

Comparison of Doherty PAs for Wideband Watt-level GaAs MMIC Implementations

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***Abstract*—Two fully integrated GaAs Doherty power amplifiers are presented for 5G FR1 applications requiring operation over the n77 (3.3–4.2 GHz) and n79 (4.4–5.0 GHz) bands. To assess the capabilities of different Doherty combiners in wideband scenarios, two versions are designed and compared: a first implementation using a direct quarter-wave-based combiner and a second version employing an inverted topology, theoretically expected to offer more broadband performance. Both designs employ stacked transistor cells and a balanced architecture to enhance output power and load mismatch resilience. Experimental results show that both implementations achieve comparable performance as the additional losses introduced by the inverted combiner limit its theoretical benefits in terms of efficiency and gain uniformity over the full band. Both achieve more than 34.5 dBm saturated output power, 20 dB small-signal gain, and power-added efficiency above 22% over a 6-dB output back-off.**

***Index Terms*—Balanced architecture, Doherty power amplifier, GaAs, stacked transistors.**

I. Introduction

Power amplifiers for 5G radio access networks must deliver high efficiency and linearity across wide bandwidths to support operation in multiple bands, such as n77 (3.3-4.2 GHz) and n79 (4.4-5.0 GHz). The Doherty Power Amplifier (DPA) is a well-established solution for improving efficiency in output power back-off (OBO), but maintaining proper load modulation and phase alignment and thus efficient operation over such wide frequency ranges remains challenging [1], [2]. Moreover, modern active antenna systems and massive MIMO arrays introduce dynamic load conditions, requiring PAs to be resilient to mismatches that would otherwise degrade performance [3].

While GaN is the standard technology for high-power PAs, GaAs offers a viable alternative for medium-power, cost-sensitive applications. Despite its lower power density, GaAs can support watt-level output through transistor stacking [4], [5] and balanced layouts [6].

This work compares two fully integrated GaAs DPAs with identical active device architectures but different Doherty combining networks: a direct and an inverted topology. The inverted approach was expected to improve efficiency and linearity uniformity, but measurements show its advantages are offset by higher combiner losses. Both designs achieve > 34.5 dBm saturated power, > 20 dB gain, and $> 22\%$ PAE over 6-dB OBO, validating GaAs as a suitable option for compact, broadband 5G front-ends.

II. Combiner design and comparison

The aim of this work is to develop fully integrated DPAs with 6-dB OBO and saturated output power of the order of 3 W adopting a low-supply voltage transistor technology. The 150-nm-gate-length high-power GaAs pHEMT process (PPH15X-20) by United Monolithic Semiconductors (UMS) is adopted, which features a power density around 0.8 W/mm at the nominal 6 V supply and has a cutoff frequency of 70 GHz.

The non-linear transistor model is scalable in number and width of the gate fingers and is validated for a maximum size of $12 \times 150\,\mu$m. Since the Main and Auxiliary branches contribute equally to the saturated output power in a 6-dB DPA, the target output power cannot be achieved by adopting a single power device in each branch, unless *ad-hoc* models for larger transistors were extracted. Even so, the optimum load would become very low and the design of a Doherty combiner that can be feasibly implemented and covers the target band would be impractical. As the combination of several transistors is necessary and an increase in the optimum load is beneficial for wideband output matching, transistor stacking is a promising technique. Its adoption in this case is facilitated by the operating frequency being a decade lower than the process cutoff frequency, which reduces the need for complex interstage matching and the detrimental effect of crosstalk [7], thus increasing the stacking efficiency [4].

The final stage is composed by two $8 \times 150\,\mu$m stacked transistors, which have an optimum load of $R_{\mathrm{opt}} = 32\,\Omega$ when supplied with 12 V at the top-most drain. The Doherty combiner should thus perform a two-point real-to-real matching, as the reactive parasitic effects of the transistors have limited effect at these frequencies, on a relative bandwidth that exceeds 40%. To achieve such performance, distributed implementation based on microstrip quarter-wavelength lines is selected. Implementations based on lumped circuit elements (C and L) are discarded as they would both have higher losses and narrower bandwidth. However, as this integrated process is conceived for high-frequency operation, the distributed implementation is quite area consuming and has non-negligible losses.

While the inverted (two-section peaking) Doherty topology, featuring two quarter-wavelength lines of the Auxiliary path in addition to the impedance inverter on the Main, is well-known to provide better matching capabilities over wide bands [2], [8], [9], this is typically more area consuming than the

conventional direct topology, where the Auxiliary device is directly connected to the common output node.

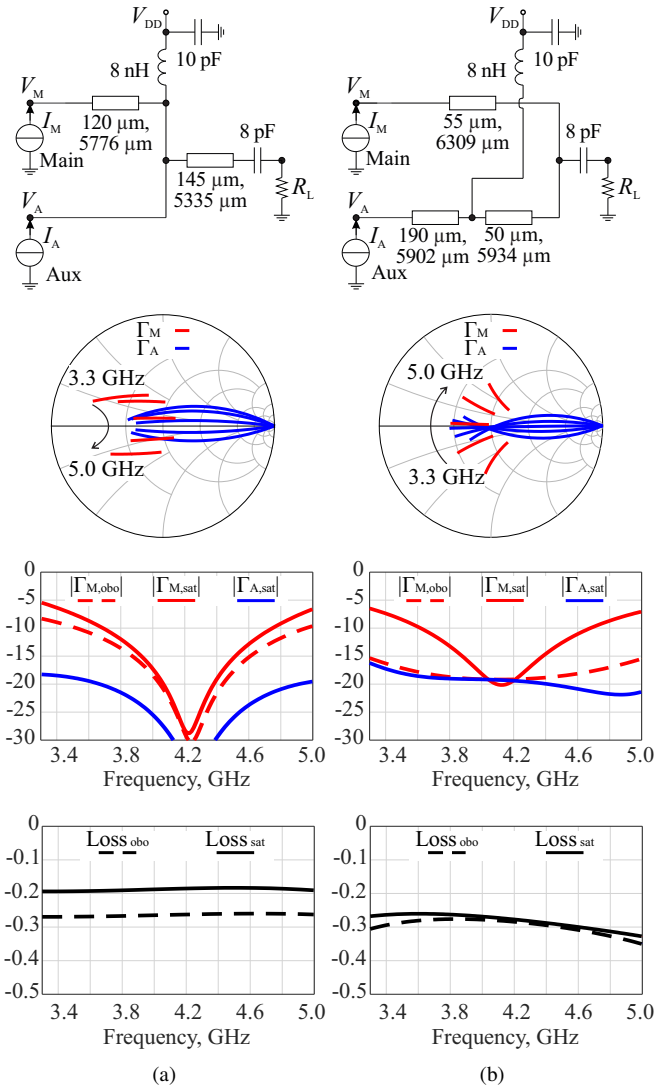


Fig. 1: Comparison of (a) direct and (b) inverted Doherty combiners. From top to bottom: schematic, load modulation and matching of Main and Aux, losses at saturation and OBO.

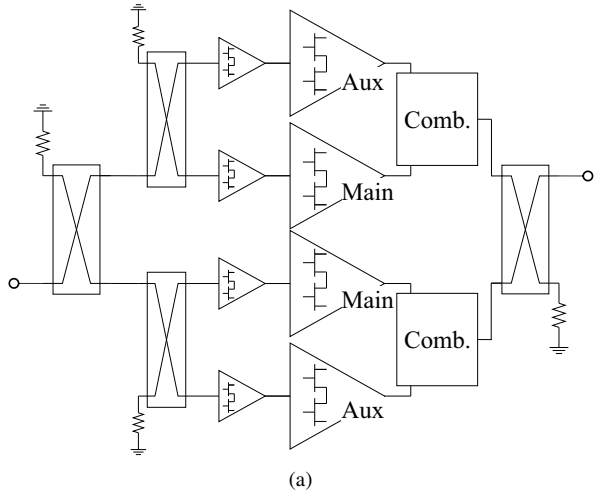
To compare the capabilities of the two topologies, the simulation setup of Fig. 1 is adopted. The stacked cells, which can be considered equivalent to a single active device with same current and double voltage swing compared to the individual common source, are represented by ideal current sources. The impedance matching of the Main and Auxiliary is evaluated by computing their drain impedance $Z_{M,A} = V_{M,A}/I_{M,A}$ and then normalizing it to the impedance to be synthesized at saturation (R_{opt}) and, for the Main, at OBO ($2R_{opt}$), in the form of reflection coefficients:

$$\Gamma_{M,A,sat} = \frac{Z_{M,A,sat} - R_{opt}}{Z_{M,A,sat} + R_{opt}}, \quad (1)$$

$$\Gamma_{M,obo} = \frac{Z_{M,obo} - 2R_{opt}}{Z_{M,obo} + 2R_{opt}}. \quad (2)$$

The losses are evaluated as the difference (in dB) between the power delivered to the load R_L (which is 50 Ω in both cases) and the total power input by the two devices.

Fig. 1 reports the schematics of the two combiner topologies, with microstrip dimensions indicated as width, length (in µm), and the simulated performance. The inverted topology (b) can indeed achieve equal or better matching than the direct one (a) over the whole band, the most evident advantage shown by $|\Gamma_{M,obo}|$, but at the price of higher losses, especially at OBO.



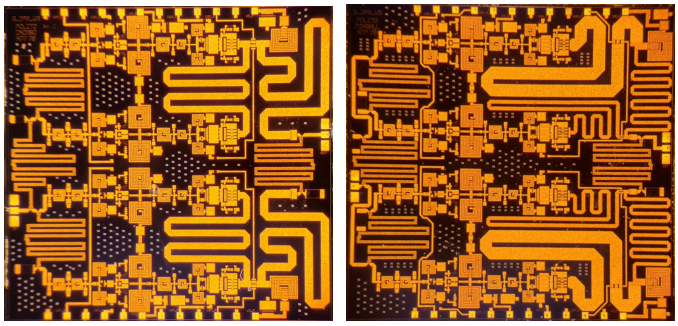


Fig. 2: Block diagram (a) and microscope photographs of the (b) direct and (c) inverted DPA MMICs ($5 \times 5\,mm^2$).

The full DPA architecture is then developed, in an analogous way for each of the two combiners. Each stacked power cell is matched through an interstage Matching Network (MN) to a driver stage, which is also a staked cell with smaller periphery and is in turn matched to 50 Ω at the input through an input MN. All MNs are band-pass filters implemented adopting lumped elements, in order to minimize area occupation. A 50-Ω meandered Lange coupler embeds the even input power splitting and the required 90° phase delay. Two so-formed

DPA cells are used in a balanced configuration implemented on-chip by means of similar meandered Lange couplers. The Lange couplers introduce significant losses of nearly 1 dB in this low-frequency fully integrated implementation, which limits the maximum achievable efficiency but provide a robust power combination which also enhances the tolerance to load mismatch. The block diagram and chip photographs of the direct and inverted balanced DPAs are shown in Fig. 2. In both cases, the layout has been tailored to fit a maximum chip area of $5\times5\,\mathrm{mm}^2$.

The simulated continuos wave (CW) performance of the two DPAs is summarized in Fig. 3, which shows comparable output power, PAE and gain throughout the band. The inverted topology (dotted) retains a moderate advantage of few percentage points on PAE at 6-dB OBO compared to the direct (dashed) one. The PAE ranges from 22% to 32% in all conditions, which is in line with the losses of the passive structures estimated above.

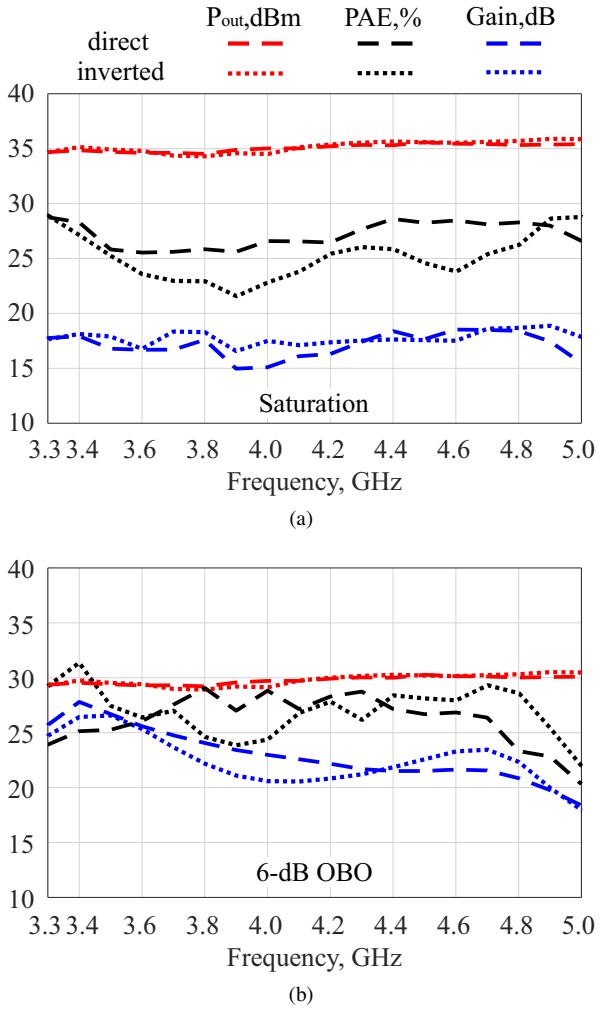


Fig. 3: Comparison of the simulated CW performance of the direct (dashed) and inverted (dotted) DPAs: at (a) saturation and (b) 6-dB OBO.

III. Measurements

The MMICs are mounted on brass carriers using solder paste and measured on-wafer using standard 150 µm pitch RF probes along with custom-designed DC probes. The characterization of the direct DPA MMIC has been presented in [10].

The CW measurements on the inverted DPA, performed over the 3.3–5.0 GHz frequency range using a real-time calibrated vector measurement setup, are compared to simulations in Fig. 4. The agreement is very good across the entire frequency range. Output power consistently exceeds 34.5 dBm, while gain remains above 20 dB in small-signal conditions and above 15 dB at saturation. The PAE is also well predicted, although a slightly larger discrepancy is observed at saturation, where measured values exceed simulations by up to 6 percentage points.

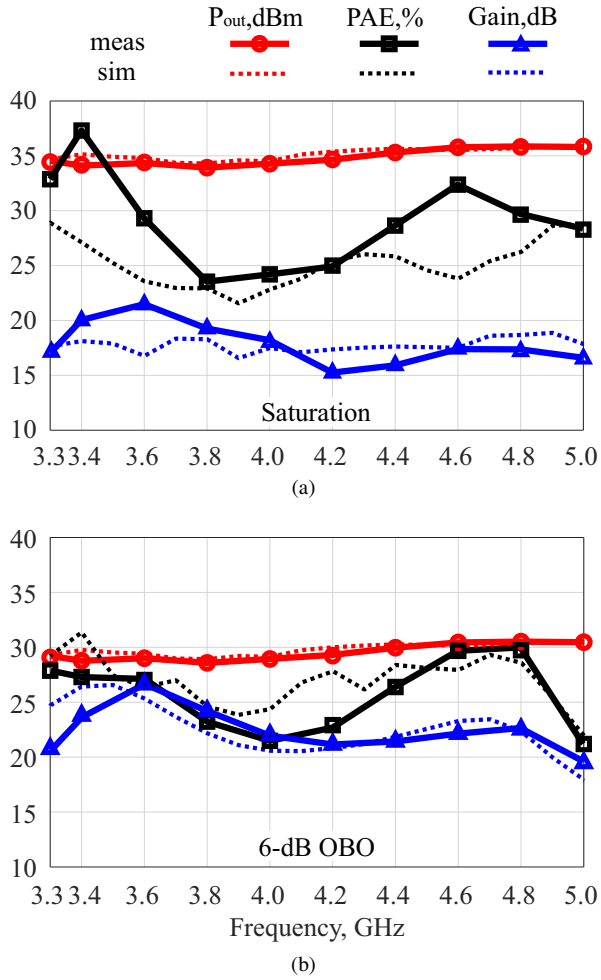


Fig. 4: Comparison of the simulated (dotted) and measured (solid with symbols) CW performance of the inverted DPA: at (a) saturation and (b) 6-dB OBO.

Table I summarizes the performance of the proposed inverted DPA and of the direct DPA reported in [10] in comparison with recent state-of-the-art Doherty amplifiers operating in the sub-6 GHz range. Despite being implemented in GaAs

TABLE I: State-of-the-art DPAs for sub-6 GHz operation.

	T.W.	[11]	[12]	[13]	[14]	[10]
Technology	**GaAs**	GaAs	GaN	GaN	GaN	GaAs
Freq.,GHz	**3.3-5**	3.3-3.5	4.5-6	3.2-4.7	3.3-5	3.3-5
BW, %	**41**	6	29	31	41	41
V_{DD},V	**12**	5	28	9, 18	28	12
P_{sat},dBm	**34.5**	38	35	29	37	34.7
$\mathrm{PAE}_{\mathrm{sat}}$,%	**24**	47	32	37	25	30
$\mathrm{PAE}_{\mathrm{6dB}}$,%	**22**	30	23	30	20	25
G_{ss},dB	**20**	34	8	11	19	20

technology and operating at a relatively low supply voltage of 12 V, the proposed DPA achieves competitive performance in terms of output power, efficiency at back-off, and small-signal gain. Notably, it is one of the few monolithic implementations capable of simultaneously covering both the n77 and n79 bands, with a 41% fractional bandwidth. While some GaN-based solutions achieve higher peak efficiency or output power, they often do so at the expense of bandwidth, gain, or integration complexity. However, despite offering potentially wider matching bandwidth than the direct topology of [10], the presented DPA does ultimately show comparable performance as the losses of the passive structures are higher in this implementation.

Given the inherently higher thermal resistance of GaAs technology compared to GaN, both on SiC and on Si substrates, further developments of this work could consider the impact of stacking and of dense integration on the junction temperature of the transistors and thus on the reliability of the chip [15]. For this reason, a non-fully MMIC implementation of the proposed architecture may also be of potential interest for similar applications.

IV. Conclusion

This work has presented the comparative design of fully integrated balanced DPAs based on different combiner topologies, developed on a GaAs power pHEMT technology for sub-6 GHz communications. Despite the inverted combiner being potentially more wideband, the losses contribute to making its performance comparable to the simpler direct topology. The experimental characterization shows that thanks to the transistor stacking, the inverted DPA MMIC can achieve an output power comparable to that of GaN, while also achieving a PAE always higher than 22% over a 6-dB back-off range, from 3.3 GHz to 5 GHz.

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