Abstract

The channel model is the most computationally demanding element in link-level simulations for multiple-input and multiple-output (MIMO)-based fifth-generation new radio (5G-NR) communication systems. Accurately modeling the wireless channel is crucial for developing and assessing wireless networks beyond 5G-NR. The use of realistic geometry-based channel models, such as the three-dimensional spatial channel model (3D-SCM), requires more computational resources for simulation. Channel emulation is employed to validate the functionality and performance of channel models during the network planning phase. General-purpose central processing unit (CPU)-based emulation platforms have limitations in accurately replicating propagation environments because they are either too simplified or have impractical execution time. Hardware accelerators based on specialized computing platforms such as FPGAs and GPUs can be employed to alleviate the load of complex computations and enhance the quality of results.

This study aims to tackle this matter by investigating diverse methodologies and optimization techniques for building an efficient hardware accelerator from a high-level specification. The process of developing applications for specialized architectures is intricate and requires thorough knowledge of hardware design languages and target architectures.

The first part of this study proposes an efficient re-configurable implementation of the 3rd Generation Partnership Project (3GPP) 3D-SCM for 5G-NR on Xilinx and Intel FPGA platforms using high-level synthesis (HLS)-based design flow. It explores the effect of various HLS optimization techniques on the total latency and hardware resource utilization on the target acceleration platforms. By using the proposed methodologies, the accelerated designs on Xilinx Alveo U280 and Intel Arria 10 FPGA achieved speedups of **65X** and **95X**, respectively, compared to the baseline CPU implementation. This speedup enhances to **173X** by optimizing the

design to utilize specialized resources present on Xilinx FPGA, such as UltraRAM (URAM) and High-Bandwidth Memory (HBM).

This study's second part focuses on accelerating the 3GPP channel model using GPU platforms. This study investigates different optimization techniques to exploit the parallelism and memory hierarchy of the GPU, specifically focusing on CUDA-based approaches. The experimental results demonstrate that the developed system achieves a significant speedup of approximately **240X** over CPU-based implementation. The GPU design exhibits a 33.3 % increase in single precision performance compared to the design accelerated on a datacenter-class FPGA. However, it also consumes 7.5 % more energy.