A novel Digital OTA topology with 66-dB DC Gain and 12.3-kHz Bandwidth

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M. Privitera, *Member*, P. S. Crovetti, *Senior Member*, A.D. Grasso, *Senior Member*

***Abstract*—The paper introduces an enhanced digital OTA topology which allows increasing the DC gain thanks to the adoption of an inverter-based output stage. Moreover, a new equivalent small-signal model is proposed which allows to simplify the circuit analysis and paves the way to new frequency compensation strategies. Designed using a 28-nm standard CMOS technology and working at 0.3-V power supply, post-layout simulations show a 66-dB gain and a 12.3-kHz gain bandwidth product while driving a 250-pF capacitive load. As compared to other ultra-low-voltage OTAs in literature, an increase of small and large signal performance, respect to area occupation, equal to 4.6X and 1.5X, respectively, is obtained.**

***Index Terms*—fully-digital, operational transconductance amplifier (OTA), ultralow power, ultralow voltage.**

I. Introduction

The design of analog circuits has become a difficult task in applications requiring ultra-low power consumption, such as implantable biomedical devices, sensor nodes for the Internet of Things (IoT), and energy-harvested battery-less devices [1]. In these applications, the digital section benefits from technology scaling in terms of reduced power consumption and increased performance, and optimal energy efficiency is obtained at near-threshold operation, i.e. when the power supply is in the order of 0.3 V-0.5 V and the overall input power budget in the order of 1.0-10 μW. On the contrary, analog circuits performance is degraded when the technology scales down due to the reduction of the transistor intrinsic gain and of the signal to noise ratio [2]. These drawbacks are exacerbated when the supply voltage is reduced down to 0.3 V to withstand large fluctuations of the harvested power or to enable direct harvesting which suppresses intermediate dc–dc power conversion [3].

The design of the Operational Transconductance Amplifier (OTA), which constitutes a ubiquitous and fundamental building block of any analog front-end, is particularly challenging at supply voltages below 1 V. When the supply voltage is in the range 1 V to 0.5 V, the most widely adopted methodology is sub-threshold biasing, also known as weak inversion biasing [5]-[7]. When operation below 0.5 V is requested, with rail-to-rail input capabilities, the bulk driving (body driving) technique, even in combination with the sub-threshold one, has been proven to be an effective solution [8]-[15]. However, compared with conventional gate-driven circuits, body-driven counterparts are characterized by lower voltage gain because of the limited value of bulk transconductance, which is only about 10–20% of the gate transconductance [5]. When targeting supply voltages down to 0.2 V inverter-based architectures are often used [16]-[19]. Recently, different approaches to exploit digital-based architectures to mimic the behavior of analog functions were explored [19]. Among these, digital-based OTAs (DigOTAs) have been proposed in [21]–[24]. DigOTAs use time-domain processing and digital standard cells with zero bias current, thus enabling digital-like area scaling, reduced design effort, and portability across technology nodes. While DigOTAs have shown enhanced performance as compared to conventional solutions, one of the main drawbacks is represented by the low gain below 0.5-V operation [22].

In this paper we propose an improved DigOTA topology in a 28-nm Bulk CMOS technology. It allows boosting the gain up to 66 dB at 0.3 V, thus improving the previously reported value by 36 dB. Moreover, the bandwidth is increased up to 12.3 kHz while driving a 250 pF load capacitance. Furthermore, the average power consumption is 44 nW and the area occupation is 625 μm^2, thus revealing the potential of the proposed solution in battery-less IoT devices. Finally, a novel simplified equivalent small-signal model is introduced in which the parameters can be simply evaluated.

The paper is organised as follows. In Section II the proposed High-Gain DigOTA is described and design guidelines are discussed adopting a simplified small-signal model. In Section III post-layout simulations results are reported. Finally, some conclusions are drawn in Section IV.

II. The proposed High-Gain DigOTA

The schematic of the proposed OTA is shown in Fig. 1. As detailed in [21] and [22], the circuit exploits two Muller C-elements driven by the input voltages $IN+$ and $IN-$, whose outputs drive a digital common-mode extractor for dynamic common-mode input voltage compensation. For a detailed description of the circuit operation the reader can refer to [23]. As compared to the original version in [23], the novelty of the circuit in Fig. 1 is the differential-to-single ended (D2S) output stage, which is implemented in this work by inverters only. In particular, inverters INV1B and INV2B constitute an inverting voltage buffer while inverters INV1A and INV3B act as a transconductance amplifier driving the same output node [18]. As a result, the DigOTA can be considered as the cascade of three gain stages, namely the Muller C-element, the inverter, and the output stage, as highlighted in Fig. 1.

In addition, it is worth noting that, differently from previous works on DigOTA [20]-[23], a simplified small-signal equivalent model is here adopted and validated by simulations.

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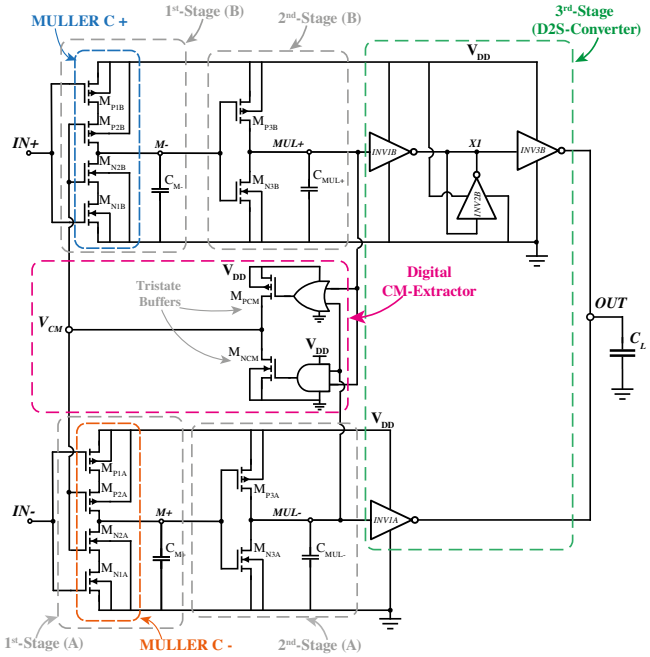

Fig. 1. Schematic of the proposed high-gain DigOTA

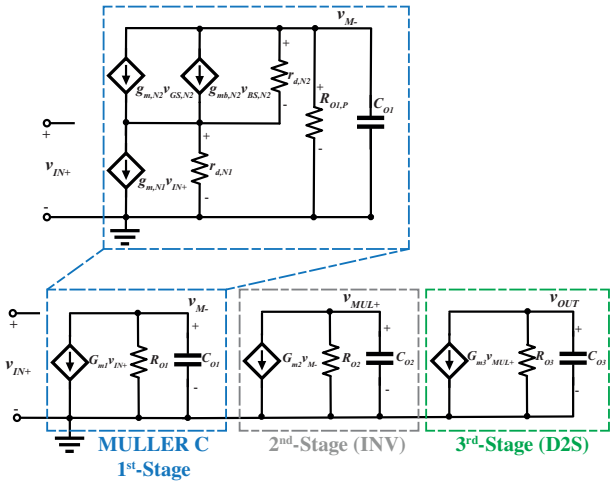

Fig. 2. Small-signal equivalent model of the circuit in Fig. 1

The model has been carried out by taking into account that the three gain stages, although implemented by using digital circuits, give rise to an analog-domain amplification path. Hence, it is possible to observe an almost constant bias voltage (when input variations are small) that is given out by the digital CM-extractor and fixed around $V_{DD}/2$. The equivalent small-signal model of the DigOTA is reported in Fig. 2. It is extracted assuming that the v_{IN+} ad v_{IN-} signal paths are symmetrical and that the common mode voltage, V_{CM}, and the input/output voltage of all the stages is equal to $V_{DD}/2$. The equivalent transconductance of the first, second, and third stage, is respectively equal to[1]

$$\begin{aligned} G_{m1} &= {g_{m,N1}}^* + {g_{m,P1}}^* \\ G_{m2} &= g_{m,N3} + g_{m,P3} \\ G_{m3} &= 2 \cdot (g_{mN,INV1A} + g_{mP,INV3B}) \end{aligned} \tag{1}$$

[1]For simplicity $g_{m,N1} = g_{m,N1A,B}$, $r_{d,N1} = r_{d,N1A,B}$ and the same holds for PMOS transistors. $C_M = C_{M+,-}$ and $C_{MUL} = C_{MUL+,-}$.

where, as it can be appreciated from Fig. 2, the first gain-stage is equivalent to a cascode amplifier. Indeed, the signal enters the stage through n-type (p-type) active devices $M_{N1A,B}$ ($M_{P1A,B}$) while V_{CM} can be considered as a fixed bias voltage for M_{N2} (M_{P2}). Moreover, the bulk terminals of the same devices are connected to ground, giving rise to a non-negligible effect in the body-transconductances, $g_{mb,N2}$ ($g_{mb,P2}$). As a results, the equivalent transconductance of this stage, G_{m1} is

$$g^*_{m,N1} \approx g_{m,N1}\left[1 - \frac{1}{1 + (g_{m,N2} + g_{mb,N2})r_{d,N1}}\right] \tag{2}$$

where $g_{mb,N2}$ is around the 10% of $g_{m,N2}$ and similar reasonings have been adopted for PMOS transistors. Moreover, the small-signal equivalent output resistances for each amplification stage depicted in Fig. 2 are given by

$$\begin{aligned} R_{O1} &= R_{O1,N} \parallel R_{O1,P} \\ R_{O2} &= r_{d,N3} \parallel r_{d,P3} \\ R_{O3} &= \frac{r_{d,NINV3} + r_{d,PINV3}}{2} \end{aligned} \tag{3}$$

where the output small-signal equivalent resistance is evaluated by the complete equation of the output resistance of a cascode gain stage as follows

$$\begin{aligned} R_{O1,N} &= [(g_{M,N1} r_{d,N1} r_{d,N2}) + r_{d,N1} + r_{d,N2}] \\ R_{O1,P} &= [(g_{M,P1} r_{d,P1} r_{d,P2}) + r_{d,P1} + r_{d,P2}]. \end{aligned} \tag{4}$$

In addition, in Eq. (3) is it assumed that inverters INV3B and INV1A are equally sized. It should be noted that the small-signal transconductance values in the sub-threshold working region are evaluated as $g_{m,sub} = I_D/nV_T$, where I_D is the biasing current n the sub-threshold slope and V_T the thermal voltage. On the other side, the intrinsic output resistance of the transistors operating in weak inversion regime is given by $r_d = 1/(g_{m,sub}\lambda_{DIBL})$ being λ_{DIBL} the DIBL effect coefficient. Hence, the intrinsic gain of a sub-threshold transistor is conversely proportional to λ_{DIBL}. In addition, these parameters have been first evaluated by a "pencil-and-paper" approach, assuming that all the nodes of the amplifiers are DC biased around $V_{DD}/2$. The hand-calculation of those parameters has been, then, verified with simulations.

The DC Gain is evaluated by exploiting the following equation

$$A_V = \prod_{i=1}^{3} A_{V,i} = \prod_{i=1}^{3} G_{m,i} R_{O,i}. \tag{5}$$

Finally, the capacitive load at the output of the first, second, and third stage, is respectively expressed by

$$\begin{aligned} C_{O1} &= C_M + C_{par1} \approx C_M \\ C_{O2} &= C_{MUL} + C_{par2} \approx C_{MUL} \\ C_{O3} &= C_L + C_{par3} \approx C_L \end{aligned} \tag{6}$$

where $C_{par,i}$ (with $i = 1 \ldots 3$) represents the total parasitic contribution at the output of each stage.

Assuming $C_L \gg C_{O,j}$, with $j = 1, 2$, the amplifier has a dominant pole, equal to $p_1 = 1/(2\pi R_{O3} C_L)$ and two non-dominant poles, $p_i = 1/(2\pi R_{O,j} C_{O,j})$. In order to control the position of the non-dominant poles, the physical capacitors,

C_{M+} and C_{M-} are added at the output of the first stage; moreover, together with C_{MUL+} and C_{MUL-}, they are used also to reduce the switching frequency of the Digital CM-Extractor block by increasing the propagation delay of the second stage. Indeed, as described in [22] the oscillation period is given by

$$T_0 \approx V_{DD} \cdot \frac{C_M}{I_{D1}} + 2(\tau_{INV} + \tau_{CM}) \tag{7}$$

where I_{D1} is the static current of the first stage, τ_{INV} and τ_{CM} are the propagation delay of the second stage and of the Digital-CM Extractor path, respectively.

The amplifier is therefore stable when driving a sufficiently large load capacitance and the phase margin (PM) is given by

$$PM\,(^\circ) = 180^\circ - \sum_{i=1}^{3} \tan^{-1}\left(\frac{GBW}{p_i}\right) \tag{8}$$

and the gain-bandwidth product (GBW) is expressed by

$$GBW = \frac{G_{m1}G_{m3}G_{m3}R_{O1}R_{O2}}{2\pi C_L} \tag{9}$$

III. Post-Layout Simulation Results

The proposed DigOTA reported in Fig. 1 has been designed and implemented using a 28-nm bulk CMOS technology provided by TSMC.SVT-09 transistors have been used with threshold voltages $V_{\rm tn} \sim 400\,{\rm mV}$ and $|V_{\rm tp}| \sim 460\,{\rm mV}$, for NMOS and PMOS, respectively. In addition, the capacitors are MOM and implemented between metal1 and metal6. The circuit was simulated in Cadence Virtuoso environment.

TABLE I
Components Sizes

Section	Component	Size	Unit
Muller C+	$M_{P1,2,A,B}$	900/30	nm/nm
Muller C-	$M_{N1,2,A,B}$	100/30	-
2^{nd}-Stages (A,B)	$M_{P3,A,B}$	900/30	nm/nm
	$M_{N3,A,B}$	100/30	-
D2S	$M_{P,INVi}$	32/0.3	μm/μm
	$M_{N,INVi}$	10.8/0.3	-
Digital CM Extractor	$M_{P,NOR}$	1800/30	nm/nm
	$M_{N,NOR,INV}$	100/30	-
	$M_{P,NAND,INV}$	900/30	-
	$M_{N,NAND}$	200/30	-
	M_{NCM}	450/300	-
	M_{PCM}	900/300	-
Capacitors	C_{M-}, C_{M+}	27	fF
	C_{MUL+},C_{MUL-}	190	-

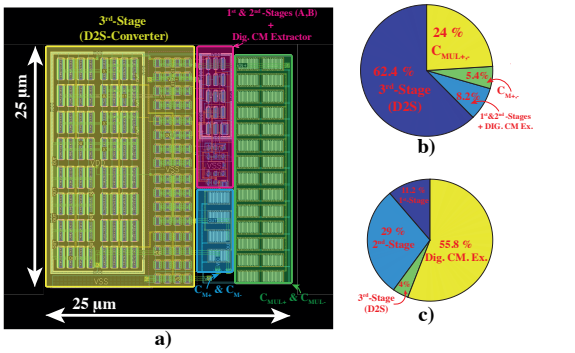

Fig. 3. a) Layout of the proposed DigOTA. b) Area breakdown. c) Power breakdown.

TABLE II
Small-Signal Parameters of Each Stage of the DigOTA

Param.	Value	Param.	Value	Param.	Value	Unit
G_{m1}	120	G_{m2}	1210	G_{m3}	560	nA/V
R_{O1}	33	R_{O2}	6.2	R_{O3}	114	MΩ
C_{O1}	0.030	C_{O2}	0.20	C_{O3}	250	pF

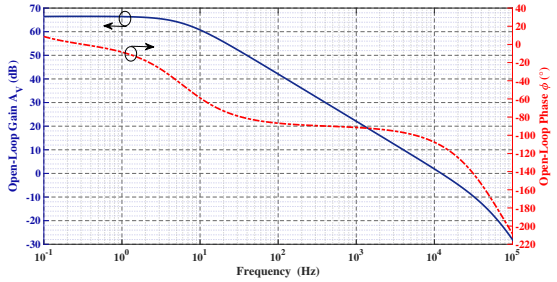

Fig. 4. Post-layout open-loop AC response.

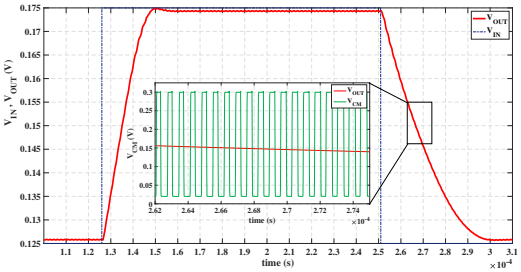

Fig. 5. Post-layout step response in unity-gain configuration to a 50-mVpp input step (V_{IN}) with emphasis on the V_{CM} voltage during transition around $V_{DD}/2$. It is worth noting the variation of the V_{CM} duty-cycle.

The dimensions of the components are reported in Tab. I and the layout of the circuit is shown in Fig. 3. Overall area occupation is equal to 625 μm^2.

The small-signal parameters have been reported in Tab. II. Using (5), (8) and (9), the estimated value of the DC gain, the PM, and the GBW is equal to 66 dB, 80°, and 10.6 kHz, respectively, which are close to the simulated ones (66 dB, 68°, and 12.3 kHz, respectively). The degradation of the expected phase margin is mainly due to un-perfect cancellation of the pole/zero doublet introduced by the D2S output stage. In addition, by exploring Tab. I, it is observed that the lengths of the transistors embedded in the D2S output stage are ten times larger than the minimum one to increase R_{O3}.

It is worth noting that the design can be obtained by using just standard cells and place-and-route layout, thus reducing the design effort to a minimum. To optimize performance, however, standard cell sizing must be customized, as done in the proposed amplifier. In addition, the AC simulations perfectly match with PAC and transient simulations, verifying, thus, the validity of the extracted small-signal model.

Extensive post-layout simulation results are reported in the following assuming $V_{DD} = 0.3\,{\rm V}$ and $C_L = 250\,{\rm pF}$. Fig. 3 reports the simulated open-loop AC response. DC gain, GBW and PM are equal to 66 dB, 12.3 kHz, and 68°, respectively. Being the amplifier compensated by a dominant-pole technique, it is asymptotically stable for any load capacitor larger than 110 pF, where the PM is equal to 45°.

As concerns the Digital CM-extractor, the self-oscillating frequency of the common mode voltage node V_{CM} is around 1.4 MHz, while with Eq. (7) it results around 1.2 MHz. The

TABLE III
STATE-OF-THE-ART COMPARISON

Parameters	[7]	[8]	[9]	[15]	[21]	[10]	[11]	[22], [23]	[12]	[13]	[17]	[16]	[14]	**T.W.**
Year	2014	2015	2018	2019	2019	2020	2020	2021	2022	2022	2022	2022	2022	**2023**
Techn. (nm)	130	65	180	130	180	180	65	180	130	130	130	130	130	**28**
Type of Work	Meas.	Meas.	Meas.	Meas.	Sim.	Meas.	Meas.	Meas.	Sim.	Sim.	Sim.	Sim.	Sim.	**Sim.**
Mode[a]	BD	BD	BD	IB	DIG	BD	BD	DIG	BD	BD	STD	STD	BD	**DIG**
Ref. Required	Y	Y	Y	Y	N	Y	Y	N	Y	Y	Y	N	Y	**N**
Pass. Required	Y	Y	Y	Y	Y	Y	Y	N	N	N	N	N	N	**Y**
V_{DD} (V)	0.25	0.35	0.3	0.3	0.3	0.3	0.25	0.3	0.3	0.3	0.3	0.3	0.3	**0.3**
DC Gain (dB)	60	43	63	49.8	35	98.1	70	30	38.07	52.92	28.3	34.97	41.28	**66**
GBW (kHz)	1.88	3600	2.8	9100	0.85	3.1	9.5	0.25	24.14	35.16	15420	12690	7.95	**12.3**
PM (°)	52.5	56	61	76	76	52.4	89	90	60	52	54	62.5	51	**68**
C_L (pF)	15	3	30	2	80	30	15	150	50	50	1.5	2.0	250	**250**
SR_{av} (V/ms)	0.7	5600	7.1	3800	0.5	9.1	2	0.085	14.23	15.06	9075	5680	1.25	**3.2**
CMRR (dB)	-	46	72	-	-	60	62.5	41	54.88	42.11	41.07	27.08	35.28	**105**
PSRR (dB)	-	35	62	-	-	-	38	30	51.05	56.13	-	-	74.71	**74**
IN ($\mu V/\sqrt{Hz}$)	3.3	0.92	1.8	0.035	-	1.8	-	21	3.15	1.60	0.49	-	1.4	**0.8**
THD (%)	1.0	0.6	1.0	-	3.0	0.49	-	2.0	1.63	0.67	1.0	3.38	3.15	**1.72**
P_{DD} (nW)	18	17000	16.8	1800	2.0	13	26	2.4	59.88	21.89	4406	6100	120	**44**[b]
Area (μm^2)	8300	5000	980	14000[b]	1426	9840	2000	982	2700	5200	164	217.85	2350	**625**
FOM_S	1.56	0.63	5.0	10.11	34	7.15	5.48	15.62	20.16	80.31	5.25	4.16	16.56	**69.88**
FOM_L	0.58	0.99	12.68	4.22	20	21	1.15	5.31	11.88	34.40	3.09	1.86	2.80	**18.18**
$FOM_{S,A}$	19	126	5102	722	23842	727	2740	15906	7463	15444	32012	19095	7046	**111818**
$FOM_{L,A}$	7	196	12938	301	14025	2134	575	5407	4400	6615	18840	8548	1106	**29090**

[a]: BD: Bulk-Driven; IB: Inverter-Based; STD: Standard-Cells; DIG: Digital-Based. *b*: Evaluated w. buffer configuration and $V_{IN} = V_{DD}/2$

$FOM_S = \frac{GBW(MHz)\cdot C_L(pF)}{P_{DD}(\mu W)}$. $FOM_{S,A} = \frac{FOM_S}{Area(mm^2)}$. $FOM_L = \frac{SR_{av}(V/\mu s)\cdot C_L(pF)}{P_{DD}(\mu W)}$. $FOM_{L,A} = \frac{FOM_L}{Area(mm^2)}$

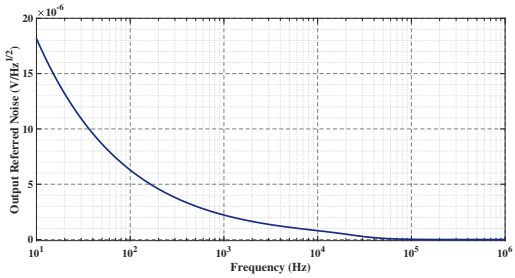

Fig. 6. Post-layout output referred noise in unity-gain configuration @ 1 kHz input sine voltage.

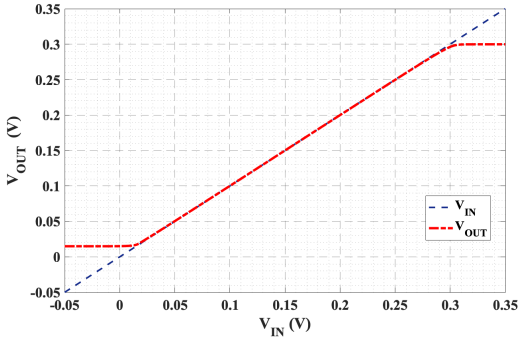

Fig. 7. Post-layout Voltage transfer characteristic and dynamic in unity-gain configuration.

transient response in unity-gain configuration to a 50-mV_{pp} input step is shown in Fig. 5. The positive/negative slew rate and 1%-settling time (with 5-mV_{pp} input step) are equal to +3.51/-2.87 V/ms and 25.67/44.66 μs, respectively.

The output-referred noise spectral density plot of the Dig-OTA is depicted in Fig. 5. The noise density at 1 kHz is equal to about 2 $\mu V/\sqrt{Hz}$. Fig. 7 reports the voltage trans-characteristic of the amplifier, showing an almost rail-to-rail operation and Fig. 8 shows the Total Harmonic Distortion (THD) versus the amplitude for a 1 kHz sine signal in unity-gain configuration.

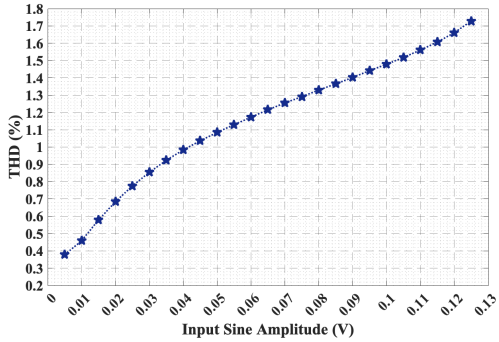

Fig. 8. Post-layout total harmonic distortion vs. input sine amplitude @ 1 kHz.

TABLE IV
CORNER POST-LAYOUT SIMULATION RESULTS @ $V_{DD} = 300\,\text{mV}$, $C_L = 250\,\text{pF}$ AND 27 °C

Parameter	**FF**	**FS**	**SF**	**SS**	**TT**
A_V (dB)	63.19	62.95	63.26	66.75	66.39
GBW (kHz)	25.1	13.51	10.04	5.41	12.29
PM (°)	80.31	72.9	62.86	48.34	68.42
SR_+ (V/ms)	6.85	2.48	4.39	1.72	3.51
SR_- (V/ms)	7.11	4.81	2.25	0.82	2.87
SR_{av} (V/ms)	6.98	3.64	3.32	1.27	3.19
CMRR (dB)	75.45	80.3	88.78	101	105.7
PSRR (dB)	77.7	73.26	68.42	72.88	74.59

TABLE V
EFFECT OF SUPPLY VOLTAGE AND TEMPERATURE VARIATIONS

Parameter						Unit
V_{DD}	0.25	0.3	0.35	0.3	0.3	V
Temperature	27	27	27	0	70	°
A_V	61.3	66.39	69.83	67.42	63.56	dB
GBW	3.83	12.29	34.75	3.25	58.87	kHz
PM	78.37	68.42	59.5	73.2	64.26	°
SR_+	0.654	3.51	16.89	1.18	12.87	V/ms
SR_-	0.591	2.87	12.06	1.31	9.61	V/ms
SR_{av}	0.622	3.19	14.47	1.24	11.24	V/ms
CMRR	97.44	105.7	121.3	101	88.87	dB
PSRR	70.72	75.49	77.35	75.07	77.72	dB
Power, P_{DD}	15.82	44.2	126.4	13.95	198.6	nW

TABLE VI
GLOBAL-LOCAL MC POST-LAYOUT SIMULATION RESULTS @ $V_{DD} = 300\,\text{mV}$, $C_L = 250\,\text{pF}$ AND 27 °C

Parameter	Mean value, μ	std deviation, σ	Unit
A_V	64.88	3.34	dB
GBW	12.74	5.22	kHz
PM	66.15	8.98	°
SR_+	3.43	0.72	V/ms
SR_-	3.05	0.90	V/ms
SR_{av}	3.24	0.81	V/ms
CMRR	98.67	8.146	dB
PSRR	76.47	9.71	dB
Offset, V_{OS}	0.5	29.08	mV
Power, P_{DD}	46.18	11.46	nW

The robustness of the circuit against process, voltage and temperature variations is assessed through corner analysis and Monte Carlo simulations. Tab. IV summarizes the corner analysis results at 27°C, while Tab. V reports the voltage and temperature corners. The results show a good robustness of the amplifier which is stable across all the considered process corners for $C_L = 250\,\text{pF}$.

Monte Carlo analysis results over 250 runs (under global and local variations) are reported in Tab. VI. It can be observed that, while the amplifier is stable, the GBW exhibits a high relative standard deviation. As for the simulated offset voltage, it is in-line with previous works. Note, indeed, that the offset is fixed by the first stage [24] which is the same as in the original version of the amplifier [23].

Tab. III summarizes the amplifier performance and compares the results with other sub-0.5 V amplifiers in literature. The comparison, carried out considering the commonly adopted figures of merit reported at the bottom of the Table, shows very good small- and large-signal performance. Indeed, among the compared solutions only [13] exhibits a slightly higher of FOM_S and a double value of FOM_L. However, if also area is accounted in the comparison, the proposed amplifier outperforms the other solutions, showing a 4.6X and 1.5X increase in the value of $FOM_{S,A}$ and $FOM_{L,A}$, respectively.

IV. CONCLUSIONS

A novel topology of DigOTA has been reported in this paper. Compared to previous solutions, it presents a third-gain stage made implemented by using inverters, thus allowing to reach 66-dB gain, while operating at 0.3-V power supply. Moreover, the GBW is increased to 12.3 kHz with a load capacitance equals to 250 pF. These specification, together with the average power consumption around 44 nW and the area occupation of $625\,\mu\text{m}^2$, makes the proposed solution well suitable for battery-less IoT devices. In addition, an increase of $FOM_{S,A}$ and $FOM_{L,A}$ of a factor 4.6X and 1.5X, respectively, compared to previous arts is hence obtained. Furthermore, a simplified small-signal model has been carried out and validated through simulations. While the DigOTA still relies on dominant pole compensation at the output node, the introduction of the simplified small-signal model paves the way to Miller-based compensation topologies, typically adopted in conventional multistage OTAs, which should further allow an increase of the amplifier bandwidth while driving capacitive loads in the picoFarad range.

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