Regenerative Approaches for V/UHTS Feeder Links: System Analysis and On-Board Complexity Reduction

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I. Introduction

The growing demand for high-speed broadband satellite services drives the development of very/ultra high throughput satellite (V/UHTS) systems. With the deployment of hundreds of geographically separated user beams where frequency bands are reused, aggregated capacities exceeding several Tbit s^{-1} in the forward link are deemed feasible in a mid-term perspective. However, this immense traffic load will raise significant challenges for the ground segment design if conventional approaches with a transparent payload are used. Since the available uplink bandwidth is limited (e.g. 5 GHz maximum in the Q/V band), several tens of spatially separated links with a full reuse of the uplink frequency resources would be necessary to support the aggregated user link bandwidth. A solution to cope with this bottleneck is to transition from transparent to fully regenerative payloads. Benefiting from the favorable link budget in feeder links, this approach would indeed permit to significantly increase the uplink spectral efficiency and, hence, reduce the number of ground stations required to support the data traffic. Meanwhile, the demodulation and the decoding of data streams on-board multi-terabit satellites is not a viable option if conventional communication standards (e.g. DVB-S2) are used. Payload power is indeed a scarce resource and efforts must be invested in the development of low-complexity demodulation and decoding solutions. In this work, we thus investigate the potential of the regenerative approach for V/UHTS systems and discuss ways in which the best trade-off between the on-board power requirements and the achieved spectral efficiency can be found. In the following sections, an overview of the aspects that will be discussed in the full paper are provided.

II. Feeder Link Dimensioning

A first step of the present study is to evaluate the benefit of a regenerative solution for the dimensioning of feeder links given certain constraints on the available uplink frequency resources and the expected link quality. To this end, the required number of gateways as a function of the uplink spectral efficiency was determined for two different V/UHTS scenarios as shown in Fig.1. This preliminary evaluation enables to formulate a recommendation on the target spectral efficiency of a regenerative approach to find an acceptable trade-off between the on-board processing complexity and the simplification of the ground segment infrastructure in comparison to a system with a transparent payload. Assuming a bandwidth per carrier around 500 MHz, it is worth mentioning that each on-board receiver will have to support several Gbit s^{-1} of throughput.

III. On-Board Complexity Reduction

As mentioned in the introduction, a major problem for a multi-terabit regenerative payload is the availability of a sufficient amount of on-board power to supply the electronic components which implement the receiver architecture. It has been shown in [1] that the dominating power requirement in current DVB-S2 receivers derives from the Forward Error Correcting (FEC) decoder. That latter study is an FPGA implementation but the comparative results carry over to silicon implementations, as well. Synchronization tasks (e.g. frame synch., freq. synch.) represent also a non-negligible part of the receiver power consumption. In the full paper version of this work, candidate approaches for the complexity reduction of these receiver blocks will thus be discussed. Due to limited space, this abstract only succinctly address the synchronization complexity issue and a few more details are already provided on the most challenging block, i.e. the channel decoder.

A. Synchronization

The synchronization complexity of the on-board receiver could be significantly reduced by relying on network synchronization mechanisms for the alignment of the transmitted frames instead of using a correlation-based frame synchronization like in DVB-S2. Moreover, complex carrier recovery mechanisms can be avoided if a non-coherent modulation is used. In the final paper, the potential of differential amplitude and phase shift keying (DAPSK) to avoid the need of frequency and phase synchronisation while guaranteeing a satisfying spectral efficiency will be reviewed.

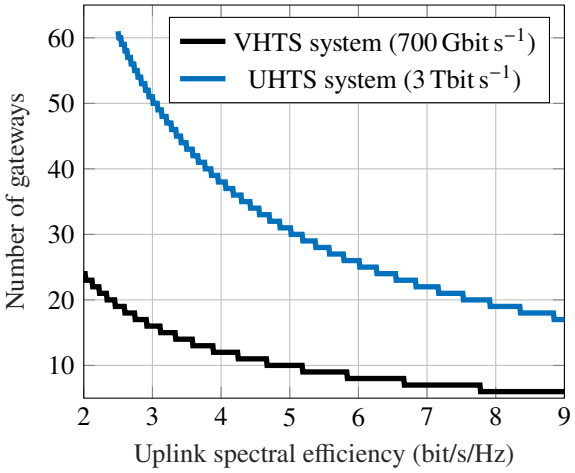

Fig. 1 Num. of GWs vs. UL spectral efficiency

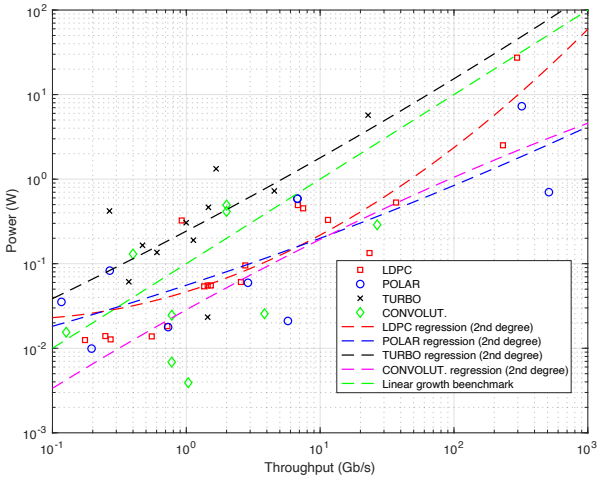

Fig. 2 Dissipated power vs. decoder throughput.

B. Channel Decoding

We focused on the optimization of the power consumption of the FEC decoder for several classes of channel codes. Specifically, our focus was to compare the performances of the following code classes:

- Turbo codes
- LDPC codes
- Polar codes
- Convolutional codes

To this purpose, we collected a large number of results from the literature concerning specific implementations of FEC decoders. The available results are rather scattered and unharmonized so that we had to resort to equivalence relationships in order to be able to compare them. We extracted from the literature results the following data (corresponding to the i-th literature record):

- μ_i: Size of the technology (nm)
- V_i: Supply voltage (V)
- R_i: achievable information bit rate (Gb/s)
- P_i: overall dissipated power

Our goal was to derive a representative behavior of the dissipated power versus the achievable information bit rate (aka throughput) of the implementation. Thus, we set the following target parameters: $\mu_0 = 45$ nm, $V_0 = 1$ V. As for the throughput, we cover quite a wide range of values reported in the considered publications; however, the actual throughput of interest for each decoder in the regenerative payload is expected to be in the order of tens of Gbit s^{-1}. Then, the dissipated power from the i-th literature record was renormalized according to the following formula: $\tilde{P}_i = P_i \times (\mu_0/\mu_i) \times (V_0/V_i)^2$. The resulting data have been reported in Fig. 2. The figure also contains second-order regression curves in log-log scale of the record data which extrapolate the expected behavior and smoothen the variability of the different implemenations. From the analysis of the regression curves we extracted the following considerations.

- Turbo codes dissipate more power than the other code classes, also because they require longer codeword size, so that they seem to be a poor choice when the goal is reducing the dissipated power. From a different point of view, it must be highlighted that Turbo codes offer better flexibility in terms of code rate than other codes.
- LDPC codes tend to increase the dissipated power versus the throughput. Therefore, they exhibit a super-linear behavior which is not desirable if the goal is aggregating several FEC decoders into a single unit.
- Convolutional and polar codes exhibit a similar behavior as far as dissipated power is concerned. However, the error performance of the former is worse, at the same level of complexity, than the latter. This is why polar codes seem to have the best characteristics for this implementation scenario.

Acknowledgments

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References

[1] E. R. de Lima, A. F. R. Queiroz, D. C. Alves, G. S. da Silva, C. G. Chaves, J. G. Mertes, and T. M. Marson, "A Detailed DVB-S2 Receiver Implementation: FPGA Prototyping and Preliminary ASIC Resource Estimation," in 6th IEEE Latin-American Conference on Communications (LATINCOM 2014), Cartagena, Colombia, November 2014, pp. 1-6