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# A Design Approach for Bandwidth Enhancement of 3-Way Doherty PAs

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***Abstract* — The paper presents a comparison of two design strategies for 3-way Doherty power amplifiers, highlighting the main differences in terms of achievable performance and bandwidth behavior. The proposed approaches have been applied to carry out the design of two microwave monolithic integrated circuits (MMICs) for 28-GHz 5G applications in a 0.15µm gate length GaN-SiC technology. The experimental characterization of the bandwidth-optimized MMIC confirms the theoretical predictions, placing the chip well in line with the current state of the art.**

***Keywords* — back-off, Doherty, efficiency enhancement, power amplifiers, 5G.**

## I. Introduction

The high capacity and low latency requirements of today's wireless communication systems require a partial redefinition of the entire transmitter architecture. The power amplifier (PA) must be operated over wide bandwidths with non-constant envelope signals, the working frequency is expanding from the crowded sub-6 GHz bands toward mm-waves, and output power back-off (OBO) is pushed toward unprecedented levels of the order of 9 to 12 dB. Therefore, research activities aimed at exploring the feasibility of mm-wave Monolithic Microwave Integrated Circuit (MMIC) PAs capable of meeting such stringent requirements are of great interest.

Solutions capable of operating efficiently in this very demanding scenario have been presented in the literature by re-adapting popular solutions such as the Doherty Power Amplifier (DPA) [1] or the Envelope Tracking (ET) [2], or proposing new architectures such as the Load Modulated Balance Amplifier (LMBA) [3] or the Distributed Efficient Power Amplifier (DEPA) [4]. In terms of technology, compound semiconductors still dominate the market for power levels exceeding the watt level, with Gallium Nitride (GaN) gaining momentum also in the K band due to the availability of sub-150 nm gate length Microwave Monolithic Integrated Circuit (MMIC) processes.

This paper discusses the design strategy of GaN MMIC 3-way DPAs (DPA3W) that targets a deep enhancement of the OBO efficiency, i.e. up to 10-12 dB in the 5G FR2 bands around 28 GHz. The MMICs adopted as the case study are manufactured in the 150 nm GaN-SiC High-Electron-Mobility Transistor (HEMT) process of WIN Semiconductors. Two versions are compared, resulting from the same DPA combiner theory but different design trade-offs. The first version has been presented in [5]. The second version [6] optimizes some critical aspects of the design highlighted in the first one, focusing on bandwidth and combiner loss minimization.

## II. Design Strategy and Optimization

The design of the output section is based on the theory presented in [5]. Both MMICs are manufactured on the same technology (150 nm GaN-SiC HEMT process of Win Semiconductors) and target 3.5 W output power at 28 GHz while maximizing the efficiency at 6 dB and 12 dB OBO. Therefore, the initial estimation of the parameters of the combiner and active devices, with reference to Fig 1, is common to both. A lumped implementation of all transmission lines is foreseen to enhance compactness, leading to the topology shown in Fig.6(b) of [5]. The common node resistance is $R_{\mathrm{L}} = 11.3\,\Omega$, therefore requiring a real-to-real postmatching network (PMN) to the output 50 Ω impedance.

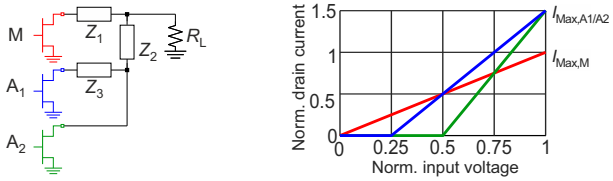



Fig. 1. Combiner topology and current stimuli for a 6-12 dB OBO DPA3W.

The DPA3W called MMIC1, presented in [5], is based on a design methodology that optimizes separately the combiner and PMN functional blocks. To avoid limiting the bandwidth achievable by the combiner, the PMN is based on a two-section $\lambda/4$ transformer. The DPA3W architecture is analogous to that adopted in [7] for a 2-way DPA, i.e., it is made up of a driver and a power device in each of the three branches, with an additional pre-driver in front to boost gain. Inter-stage (ISMN) and input (IMN) matching networks are low-order band-pass filters that embed the DC feeds and DC blocks. Finally, the input splitter is based on a two-section branch line topology optimized on the targeted 1-GHz bandwidth around 28 GHz. The MMIC photograph and its block diagram are shown in Fig. 2. The experimental characterization of MMIC1 has reported performance in line with the simulation at the design frequency but was affected by some frequency shift that led to performance degradation in the targeted frequency band.

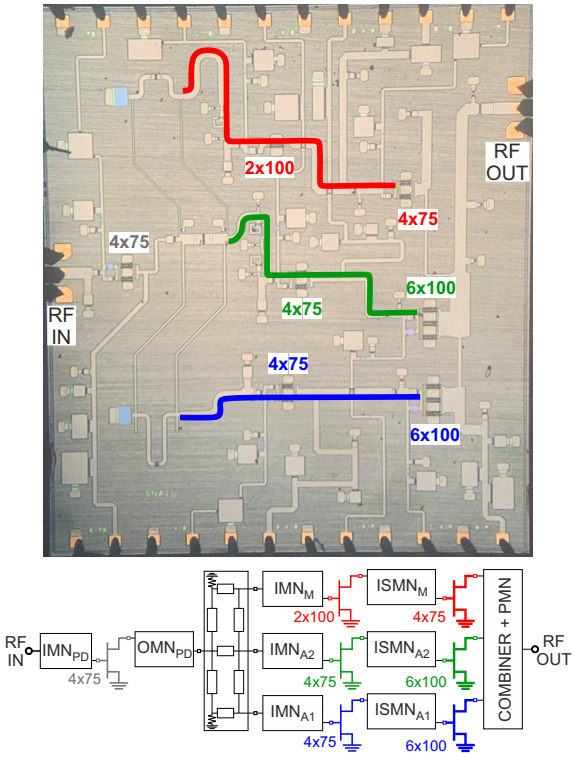



Fig. 2. Chip photograph (top, area: $3.73 \times 4.2\,\mathrm{mm}^2$) and block diagram (bottom) of MMIC1.

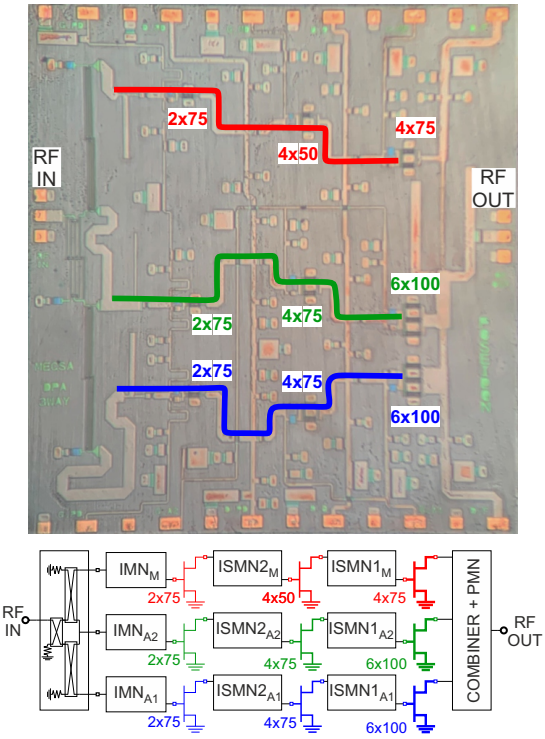



Fig. 3. Chip photograph (top, area: $3.63 \times 3.9\,\mathrm{mm}^2$) and block diagram (bottom) of MMIC2.

The main causes of this deviation have been identified in the sensitivity of the architecture to process variations, especially the input section, but also the PMN due to the presence of very small capacitors.

The redesigned version of the DPA3W, called MMIC2, is shown in Fig. 3. It targets similar performance, but with a wider bandwidth (2-GHz, from 27 to 29 GHz) and is based on a different design methodology, where the functional blocks in the output section are co-designed and optimized to minimize output losses. The main modifications are as follows.

- the reduction of complexity of the PMN, to maintain equally good matching while strongly reducing the output losses;
- the addition of one class-AB pre-driver stage ($2\times75\,\mu$m) in each of the three DPA3W branches, to decouple the input splitter from the strongly varying input impedance of the class-C Auxiliary devices;
- the adoption of a more wideband input splitter topology, to minimize the sensitivity to process variations and model inaccuracies.

The details of the design strategies, with a focus on the main differences, are provided below.

To quantify the ability of the combiner to synthesize the desired loads, we define the following reflection coefficients:

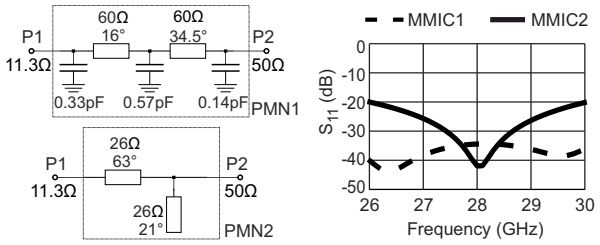
$$\Gamma_{sub}(x) = \frac{Z_{sub}(x) - R_{\mathrm{ref},sub}(x)}{Z_{sub}(x) + R_{\mathrm{ref},sub}(x)},$$
$$\text{where} \quad sub = \mathrm{M},\ \mathrm{A1},\ \mathrm{A2}, \quad x = x_1,\ x_2,\ 1 \qquad (1)$$

The variable $x$ represents the normalized input voltage and all impedances are defined at the drain current generator plane of the transistors. Hence, the optimum loads are $R_{\mathrm{ref,M}}(x) = R_{\mathrm{opt,M}}/x$ for the Main, whereas for the Auxiliary devices $R_{\mathrm{ref,A1}}(x_2) = 3R_{\mathrm{opt,A1}}$ and $R_{\mathrm{ref,A1}}(1) = R_{\mathrm{ref,A2}}(1) = R_{\mathrm{opt,A1,2}}$, where $R_{\mathrm{opt},sub}$ is the optimum load of the transistor at saturation. Note that $\Gamma_{\mathrm{M}}$ is defined and finite at all three break points, while $\Gamma_{\mathrm{A1}}$ and $\Gamma_{\mathrm{A2}}$ are only defined where the active device is already on, that is, at $x = x_2$, 1 and $x = 1$, respectively.

The $|\Gamma_{sub}(x)|$ synthesized by the combiner are verified to be all below -10 dB in the 27–29 GHz range. The PMNs of the two MMICs and the corresponding $|S_{11}|$ they synthesize are reported in Fig. 4. The lumped two-section $\lambda/4$ transformer of PMN1 can maintain the mismatch at the common node below -30 dB in a broader frequency range than the targeted one, which ensures it is not the limiting factor for bandwidth. In fact, if PMN1 is replaced to the ideal $R_{\mathrm{L}}$ , the synthesized $\Gamma_{sub}(x)$ is unchanged. The simpler line-stub of PMN2, instead, can only maintain the mismatch below -20 dB from 26 GHz to 30 GHz, which has an effect on the synthesized $\Gamma_{sub}(x)$. However, this solution is promising since it can maintain significantly lower losses.

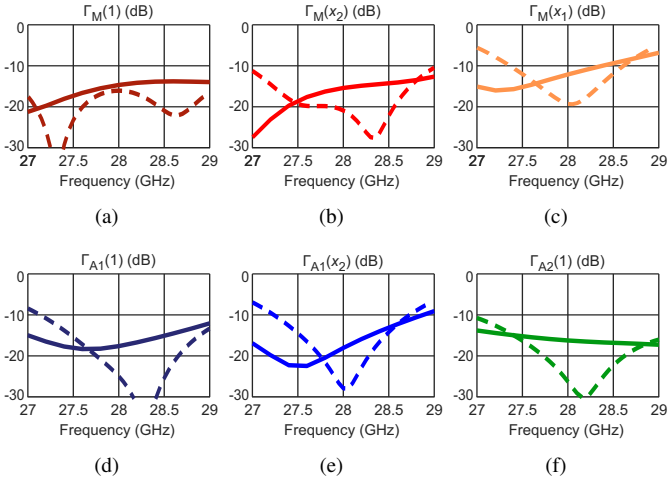
If the combiner and PMN are optimized simultaneously, in a multi-goal optimization that trades-off between losses and matching, the topology of PMN2 can provide better results. It follows from (1) that the optimization of the combiner here performed, based on the best achievable $|\Gamma_{sub}(x)|$, is a six-goal optimization. A seventh goal imposes the minimization of

output losses, estimated as the difference between the output power delivered to the external termination and the overall power available at the drain terminal of the three active devices. Fig. 5 reports the $|\Gamma_{sub}(x)|$ obtained as a result of the optimization for MMIC2 (solid lines) compared to the corresponding ones achieved by the MMIC1 output section (dashed lines). It is noticeable that MMIC2 can maintain the mismatch below -10 dB in the range 27–29 GHz, which is equal to or better than MMIC1. Additionally, Fig. 6 shows that MMIC2 has significantly lower output losses than MMIC1, mainly limited to below 1 dB in the whole frequency range.




(a) (b)

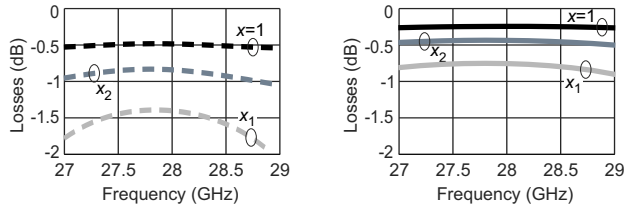
Fig. 4. PMNs implemented in the two DPA3W MMICs: (a) schematics and (b) reflection coefficients synthesized at the common node.




(a) (b) (c)

(d) (e) (f)

Fig. 5. Reflection coefficients synthesized at the drain current source planes in MMIC1 (dashed) and MMIC2 (solid): (a)–(c) Main, (d),(e) Auxiliary1 and (f) Auxiliary2.




(a) (b)

Fig. 6. Losses of the output section (power combiner and PMN) of (a) MMIC1 (dashed) and (b) MMIC1 (solid).

## III. Simulated and Measured Performance of MMIC2

The continuous wave (CW) simulated performance of the complete MMIC2 DPA3W is reported in Fig. 7. It delivers a saturated output power greater than 34 dBm from 27 GHz to 29 GHz while maintaining PAE higher than 25% up to 6 dB OBO and higher than 15% at 12 dB OBO. The power gain is around 15 dB in linearity and remains above 10 dB at saturation.

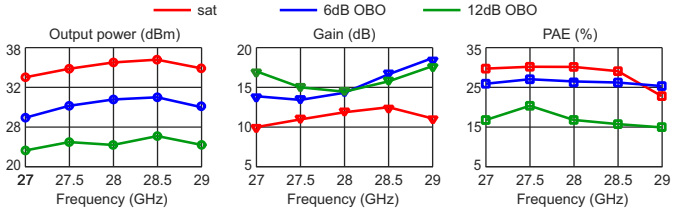



Fig. 7. Simulated performance of MMIC2 at saturation (red), 6 dB (blue) and 12 dB (green) OBO, over the frequency range 27–29 GHz.

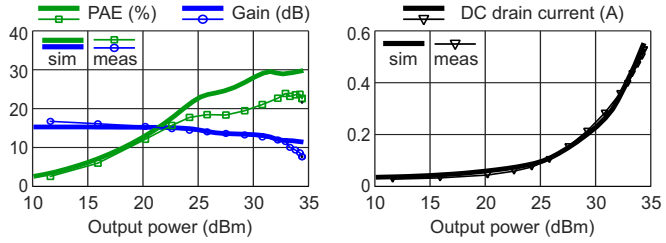



Fig. 8. Comparison of simulated (solid) and measured (symbols) performance of MMIC2 at 27.5 GHz.

The best performance, especially in terms of efficiency enhancement in the back-off, is achieved at 27.5 GHz. The slight shift compared to the original center frequency is likely due to the successive optimization of the passive networks, which heavily relies on electromagnetic (EM) simulations and thus makes fine-tuning hard to achieve and somewhat sensitive to the adopted EM simulation setup.

The measured performance of MMIC2 under analogous bias conditions is compared with the simulated one at 27.5 GHz in Fig. 8. The agreement in terms of gain, output power, and DC current consumption is very good. Although the measured PAE is slightly lower, around 5%, the position of the efficiency peaks is well captured, thus confirming the expected Doherty operation. The observed discrepancy in terms of absolute values may be partially due to an underestimation of power and to some model inaccuracy, which could not be verified with *ad hoc* load pull campaigns on the bare active devices.

The chip has been characterized throughout the band, and the full characterization results are detailed in [6]. A slight shift towards higher frequencies is observed, thus the DPA3W covers the 27.5–29.5 GHz band. The results are summarized and compared to the state of the art (SOA) in Table 1. While GaN-based examples demonstrate superior power levels compared to those of their GaAs and Si

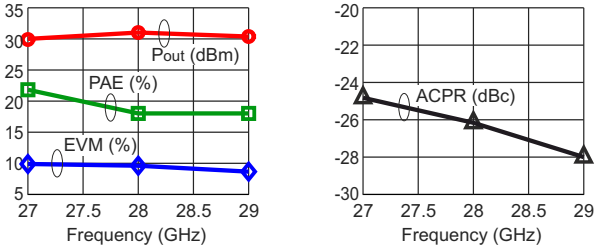



Fig. 9. Measured performance of MMIC2 under 10-dB PAPR 50-MHz bandwidth modulated signal excitation.

counterparts, the presented DPA3W highlights competitive results with bandwidth and deep back-off efficiency in line with the best results presented so far in any technology.

Finally, the system-level characterization that adopts a 64-QAM standard 5G signal with 10 dB PAPR and 50 MHz bandwidth is summarized in Fig. 9. Without any pre-distortion, the DPA3W features an intrinsic linearity that is in line with the standard requirements. It maintains ACPR<-25 dBc and EVM<10% across the whole band, with a PAE higher than 18% at an average output power of 30 dBm.

Table 1. Comparison with SOA Ka-band DPAs

| **Techn.** | **Freq. (GHz)** | **$P_{out,sat}$ (dBm)** | **$PAE_{sat}$ (%)** | **$PAE^{\#}_{OBO}$ (%)** | **$G_{sat}$ (dB)** | **Ref** |
|---|---|---|---|---|---|---|
| Si | 28 | 22.4 | 40* | 18* | 10* | [8] |
| Si | 26 | 18.7 | 32* | 8* | 12.5* | [9] |
| GaAs | 27.25–29.75 | 27 | 37 | 12* | 18 | [10] |
| GaAs | 28 | 30 | 38 | 10* | 15* | [11] |
| GaN | 26–30 | 36.1 | 26.7 | 15* | 7 | [12] |
| GaN | 28.5–29.5 | 29* | 30* | 18* | 4* | [13] |
| GaN | 28–29 | 34 | 20 | 12 | 8 | [5] |
| **GaN** | **27.5–29.5** | **34** | **18–23** | **8–16** | **8–9** | **T. W.** |

# PAE at 10 dB OBO
* Value extrapolated from graphs

## IV. Conclusion

A critical discussion has been presented on the pros and cons of different design choices for the design of 3-way Doherty power amplifiers, adopting as a case study two MMICs implemented in GaN-SiC technology for 28-GHz 5G applications. The optimized MMIC presents a wider bandwidth than the initial version, and its experimental characterization results in line with the present state of the art, confirming the successful development of the presented strategy.

## Acknowledgment

This research was supported by the Project Programma Operativo Nazionale (PON) Ricerca e Innovazione "Tecnologie abilitanti e architetture innovative per future generazioni (6G) di trasmettitori intelligenti green" (DM 1062/21, CUP E15F21003760001) funded by the Italian Ministry of Universities and Research (MUR).

The authors also thank WIN Semiconductors for the fabrication of the prototype, within the framework of the "mmWave Multi-Project Runs for Selected Universities" agreement with the Italian Microwave Engineering Center for Space Applications (MECSA), and Keysight Technologies for providing the measurement instruments adopted for the system-level characterization.

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