Novel pixel CMOS sensors for radiation detection applications and sub-nanosecond timing measurements

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1 Summary

The need for cost-effective, large-area sensors with improved timing resolution and low power consumption is currently growing across various fields of physics research and applications for the detection of high-energy charged particles and photons. Silicon detectors are extensively adopted, thanks to their adaptability and the rapid progress in the semiconductor industry. Among silicon detectors, Monolithic Active Pixel Sensors (MAPS) represent a cutting-edge technology in particle detection and imaging, combining high spatial resolution with cost-effectiveness and scalability.
This thesis is focused on the simulation and characterisation of Complementary Metal-Oxide-Semiconductor (CMOS) pixel sensors for radiation detection and high resolution timing measurements. Among the different fields of applications, a particular focus is given to high-energy physics. In particular, this research work fits in the context of two distinct upgrades of A Large Ion Collider Experiment (ALICE) at the CERN LHC: the third generation Inner Tracking System (ITS3), where the Tower Partners Semiconductor Co. (TPSCo) 65 nm CMOS Image Sensor Process will be employed and ALICE 3, a proposal for the next-generation detector, designed as a follow-up to the present ALICE experiment in 2033.

Chapters 1, 2 and 3 provide an introduction covering the fundamental principles of silicon detectors, the aspects that influence their timing performance and the basics of charged particle tracking, with a particular focus on the above mentioned ALICE upgrades. An overview of several existing silicon-based technologies is subsequently provided.
A complete outline of the research approach is presented, aimed at predicting the performance of MAPS through simulations and then validating the results through test campaigns. For this reason, the first part of the research work, in Chapter 4, describes a combined approach of TCAD and Monte Carlo simulations, while the following part reports on the characterisation activities carried

out on MAPS. The activities have been accomplished in the framework of the Advanced Readout CMOS Architecture with Depleted Integrated sensor Arrays (ARCADIA) collaboration, a project funded by the Istituto Nazionale di Fisica Nucleare (INFN) that aims to develop Fully Depleted-MAPS, for which improved charge collection efficiency and timing performance are granted by a backside bias voltage for the complete sensor depletion. By importing the electric fields and weighting potentials extracted from TCAD in the Monte Carlo software, accurate simulations can be performed in an acceptable computing time. Both MAPS with small and large collection electrodes have been simulated and their timing performance extracted, demonstrating the impact of the weighting field uniformity, and therefore, of the sensor geometry, on the time resolution. A dedicated CMOS prototype, featuring a large collection electrode and integrated electronics, was produced in the LFoundry 110 nm CMOS commercial process to investigate the ARCADIA technology capabilities for fast timing applications, demonstrating sub-nanosecond timing performance. However, a larger collected charge or a higher power consumption were needed to improve the jitter.

To accomplish this goal, an innovative sensor concept was developed, as presented in Chapter 5, with the addition of a gain layer, allowing signal amplification by impact ionization. Experimental results on the first 110 nm CMOS avalanche detector prototype, demonstrated the presence of a gain between 2 and 3 and a time resolution around 230 ps. Following measurements with optimised working point led to a reduced and promising time resolution of approximately 150 ps.

Further investigation of the commercial technological nodes for High Energy Physics (HEP) applications was carried out through the validation of the 65 nm TPSCo CMOS imaging technology for the ALICE ITS3 upgrade, presented in Chapter 6. In particular, the Analog Pixel Test Structure with Operational Amplifier (APTS-OA) was characterised both in the laboratory and in test beam facilities. After the definition of the working point, optimised for the fast front-end response, an ^{55}Fe source was employed to calibrate the chip response using soft X-rays.

To assess the APTS-OA performance in terms of time resolution, spatial resolution, and detection efficiency with minimum ionizing particles, the chip was proficiently incorporated into a beam telescope. The modified pixel process demonstrated an impressive time resolution of 63 ps, a spatial resolution of 2 μm and a detection efficiency higher than 99%, with a substrate voltage of -4.8 V and a clusterisation threshold of 100 e^-.