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High Step-Up Multimode Input-Parallel-Output-Series Power Optimizer for Wide-Range Photovoltaic Applications

Stefano Cerutti, *Member, IEEE*, Francesco Gennaro, *Senior Member, IEEE*, Francesco Musolino, *Member, IEEE*, and Paolo Stefano Crovetti, *Senior Member, IEEE*

***Abstract*—This article introduces an efficient high step-up multimode input-parallel-output-series (IPOS) converter designed for wide-range photovoltaic applications. The proposed solution is based on the asymmetric splitting of the input power between a fixed-gain series resonant converter (SRC) used as DC transformer, and a synchronous boost operated in the boundary conduction mode, responsible for the gain modulation. The SRC includes a topology-morphing rectifier, which can be used as a voltage doubler or a voltage quadrupler according to the required voltage gain. The combination of the multimode and the partial power processing approaches allow to achieve a high efficiency on a wide range of operating powers and input voltages, overcoming the efficiency drop of resonant converters operating outside the resonance frequency. At the same time, the design flexibility offered by the IPOS architecture allows to achieve the best performance in the neighborhood of a desired rated voltage. Tests on a 700 W prototype validate the converter operation on the wide 15 V–45 V input voltage range, with an efficiency always above 90.5 %. The converter prototype exhibits a measured peak efficiency of 97.8 % and a California Energy Commission efficiency of 97.15 % at the rated voltage.**

***Index Terms*—DC–DC power converters, partial power processing (PPP), photovoltaic systems, power optimizers, topology-morphing, zero-voltage switching (ZVS).**

I. Introduction

THE decreasing cost and degradation rate [1] of all photovoltaic (PV) module technologies, combined with their inherent scalability, is fostering a rapid penetration of solar generation into the energy mix of many countries [2]. PV systems rely on power converters to effectively interface the generator to the grid, while implementing the maximum power point tracking (MPPT). Among the various power conversion architectures, module-level power converters (MLPCs) offer increased flexibility and MPPT efficiency, thanks to the distributed MPPT [3], [4].

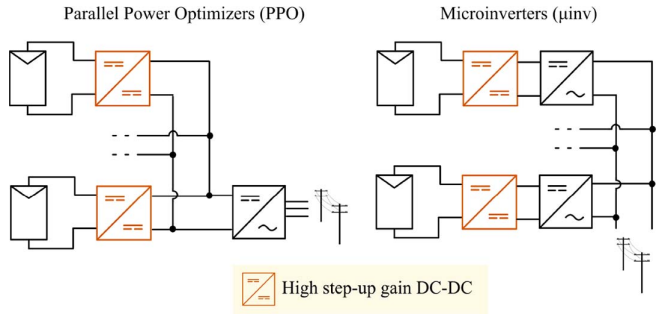


Fig. 1. Block diagrams of PPO and microinverters (μinv).

The maximum flexibility and immunity to mismatches is offered by parallel power optimizers (PPO) and microinverters (μinv), schematically shown in Fig. 1, thanks to their connection in parallel to the high-voltage DC-rail or directly to the grid [5]. Both PPO and μinv require a high gain DC–DC converter to boost the PV panel voltage while implementing the MPPT. While the variable solar irradiance significantly affects the available power of the PV module, opaque and partial shading conditions, common in residential scenarios, can dramatically shift the global MPP voltage V_{MPP}, as qualitatively shown in Fig. 2 [6], [7], [8]. As a result, DC–DC converters for this application should be very efficient at the most frequent working points, while still able to operate on a wide range of input powers and voltages. The demanding requirements of the high-gain DC–DC stage were addressed in the literature exploiting different operating techniques [9].

Many of the converters proposed in the literature are derived from conventional boost converters, equipped with voltage multipliers (VM) or switched capacitors (SC) networks to further increase the voltage gain and reduce the voltage stresses in the semiconductor devices [10], [11], [12], [13]. The main drawbacks of these solutions are the high number of electrolytic

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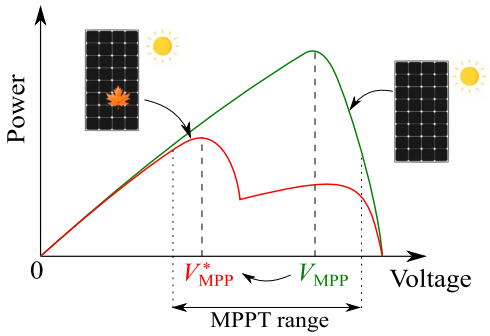


Fig. 2. Qualitative representation of the impact of a localized shading on the power-voltage curve of a PV panel.

capacitors and diodes, which affect the reliability and conversion efficiency of the converters, the hard switching of the semiconductor devices and the increased electrical stresses at higher duty cycle operation.

LLC or series resonant converters (SRC) have become widespread solutions for this application, as they exploit a high frequency transformer to achieve a high step-up gain and the soft-switching of the converter semiconductor devices. Compared to boost-derived topologies, resonant converters allow to reduce the number of passive components, but are usually optimized to operate in a narrow range of working points. For this reason, multimode converters based on the schematic of Fig. 3(a) were proposed to extend the converter operation outside the rated input voltage [6], [7], [14], [15]. The main drawback is that the resonant converters are forced to operate outside resonance in the majority of the working points, causing significant efficiency drop.

A potential solution to this limitation consists in cascading a fixed-gain resonant stage (DC transformer, DCX) with a low-gain auxiliary stage for gain modulation [Fig. 3(b)], allowing an optimal design of the resonant stage at the expense of a moderate increase in component count [16]. Two-stage full-power architectures like [16], however, exhibit the following fundamental limitation: both the stages need to be designed according to the full rated power, potentially leading to multiple bulky magnetic components. In addition, the overall conversion efficiency is unavoidably constrained by the least efficient stage.

Partial power processing (PPP) topologies, such as asymmetric input-parallel-output-series (IPOS) converters, overcome this limitation by modulating the gain through auxiliary stages that process only a small fraction of the total PV power, as shown in Fig. 3(c). Various examples in the literature exploited a low power active-clamp flyback [17], a buck [18], a hybrid boost integrated in the SRC full-bridge [19] and a buck-boost [20]. However, the inherent benefits of these solutions are lost whenever the auxiliary stage is forced to provide a high gain and process a high power, limiting the operation on a narrow voltage range.

To overcome the limitations of the existing solutions, this article introduces a new DC–DC converter topology combining the high efficiency of DCX-SRC, the wide-range operation of multimode approaches, and the design flexibility of PPP-IPOS converters. The proposed architecture, shown in Fig. 3(d), integrates for the first time a DCX-SRC with topology-morphing rectifier into an IPOS-PPP architecture, allowing to reduce the electrical stresses of the auxiliary stage and extend the converter voltage range. The main innovative contributions of this work are the following.

1) The proposed converter synergically combines for the first time the PPP technique and the multimode operation to address the wide voltage range and high efficiency requirements of PPO.
2) It introduces a new design procedure that tunes the transformer ratio as a system-level design parameter to optimally split the input power and reduce the electrical stresses of the auxiliary stage. Experimental tests validate the effectiveness of this methodology in maximizing the conversion efficiency in a desired voltage range.
3) The proposed converter exploits the boundary conduction mode (BCM) to enhance the light load efficiency and reduce the size of the inductor in the auxiliary stage, differently from previous boost-derived solutions [11], [16], [19].

This manuscript significantly extends our previous work [22] by including a more detailed mathematical description of the operating modes, a systematic design flow from realistic PV panel specifications to the components selection, the experimental characterization of a prototype to validate the operation in the three modes, the smooth transition between modes, and the converter efficiency, and a comparison of the proposed solution with the state of the art.

The rest of the article is organized as follows. Section II describes the converter topology and its multimode operation. Section III illustrates the design methodology for the converter components and derives its static gain. Section IV presents the experimental characterization of a prototype of the proposed converter, while the conclusions are drawn in Section V.

II. Converter Topology and Operation

In an IPOS converter, the parallel connection of the input ports allows to split the current stresses between the two stages, while the series connection of the output ports allows to reduce the individual gain requirements and voltage stresses. By construction, the following relationship holds between the voltage gains and the fraction of power processed by each stage [22]

$$\frac{P_i}{P_{\mathrm{TOT}}} = \frac{G_i}{G_{\mathrm{TOT}}} = \frac{G_i}{G_1 + G_2}, \quad i \in [1;2]. \tag{1}$$

To fully exploit the benefits of the IPOS configuration, a DCX-SRC is selected for the high gain G_1 stage, to convert most of the input power with the highest attainable efficiency. The DCX-SRC was selected among other converters thanks to its inherent soft switching and galvanic isolation, imposed by the construction of the IPOS architecture [23]. This stage is equipped with a topology-morphing rectifier, allowing to significantly reduce the gain requirements of the auxiliary stage at low input voltage operation, and relax its design. As a result, the simplest step-up topology, namely a synchronous boost converter, is chosen for its minimal component count.

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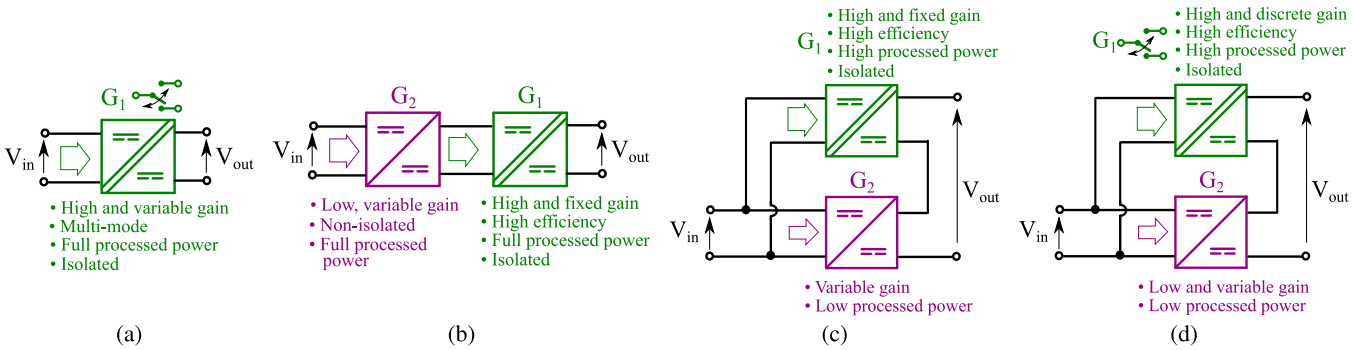


Fig. 3. Block diagrams of various converter topologies for wide-range PPO proposed in the literature. (a) Single-stage, multimode resonant converters [6], [7], [14], [15], [21]. (b) Cascaded dual stage with DCX-SRC [16]. (c) Asymmetric IPOS with DCX-SRC [17], [18], [19], [20]. (d) Proposed asymmetric IPOS with topology-morphed DCX-SRC.

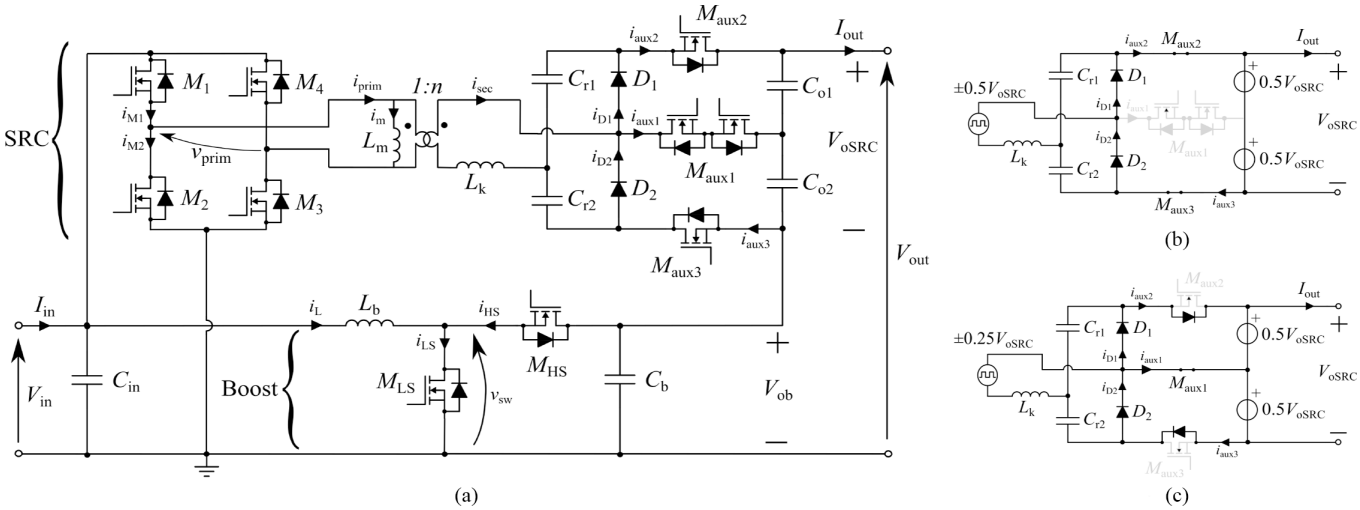


Fig. 4. Schematic of the proposed converter. (a) Complete schematic. Equivalent circuits of: (b) VDR; and (c) VQR.

Due to the IPOS configuration, the proposed converter topology is globally nonisolated, despite the presence of the transformer in the DCX-SRC. The galvanic isolation, however, is not a mandatory requirement for PPO, as long as the leakage currents are kept within specified limits [24]. The proposed converter exhibits shared ground between input and output ports, thereby minimizing the generation of leakage currents.

The complete schematic of the converter is shown in Fig. 4(a). The resonant tank of the SRC is at the secondary side of the transformer and consists of the leakage inductance $L_{\rm k}$ and capacitors $C_{\rm r1} = C_{\rm r2} = C_{\rm r}$. The resonant capacitors also make a voltage doubler rectifier (VDR) with diodes D_1 and D_2. The topology-morphing rectifier exploits the conduction state of the auxiliary transistors $M_{\rm aux1}$, $M_{\rm aux2}$ and $M_{\rm aux3}$ to implement either a duplication or quadruplication of the rectified voltage at the secondary side of the transformer.

According to the input voltage, the proposed converter can operate in three modes. The mathematical description of the converter operation is based on the following assumptions: the converter transistors are ideal, except for their output parasitic capacitances; the diodes of the SRC rectifier are ideal; the filter capacitors $C_{\rm in}$, $C_{\rm b}$ and $C_{\rm o1-o2}$, are sufficiently large to keep stable voltages at the input and output ports of the two converter stages.

A. Medium Voltage (MV) Mode

In the voltage range including the rated input voltage, denoted as MV mode, the SRC operates at the resonance frequency expressed in (2), with a VDR achieved by turning ON $M_{\rm aux2}$ and $M_{\rm aux3}$ and keeping $M_{\rm aux1}$ OFF, as shown in Fig. 4(b)

$$f_{\rm res} = \frac{1}{2\pi\sqrt{2C_{\rm r}L_{\rm k}}}. \tag{2}$$

Therefore, the SRC gain is fixed and can be expressed by $G_1 = 2n$, where n is the transformer turns ratio. At resonance, the SRC waveforms are characterized by the zero-voltage switching (ZVS) of the input transistors $M_1 - M_4$, assisted by the circulating magnetizing current $i_{\rm m}$ during the dead-time, and by the zero-current switching (ZCS) of the rectifier diodes [7], [22].

The synchronous boost converter is operated in the variable -frequency BCM that takes advantage of a negative current extension period $dt_{\rm ext}$ to assist the ZVS of the low-side

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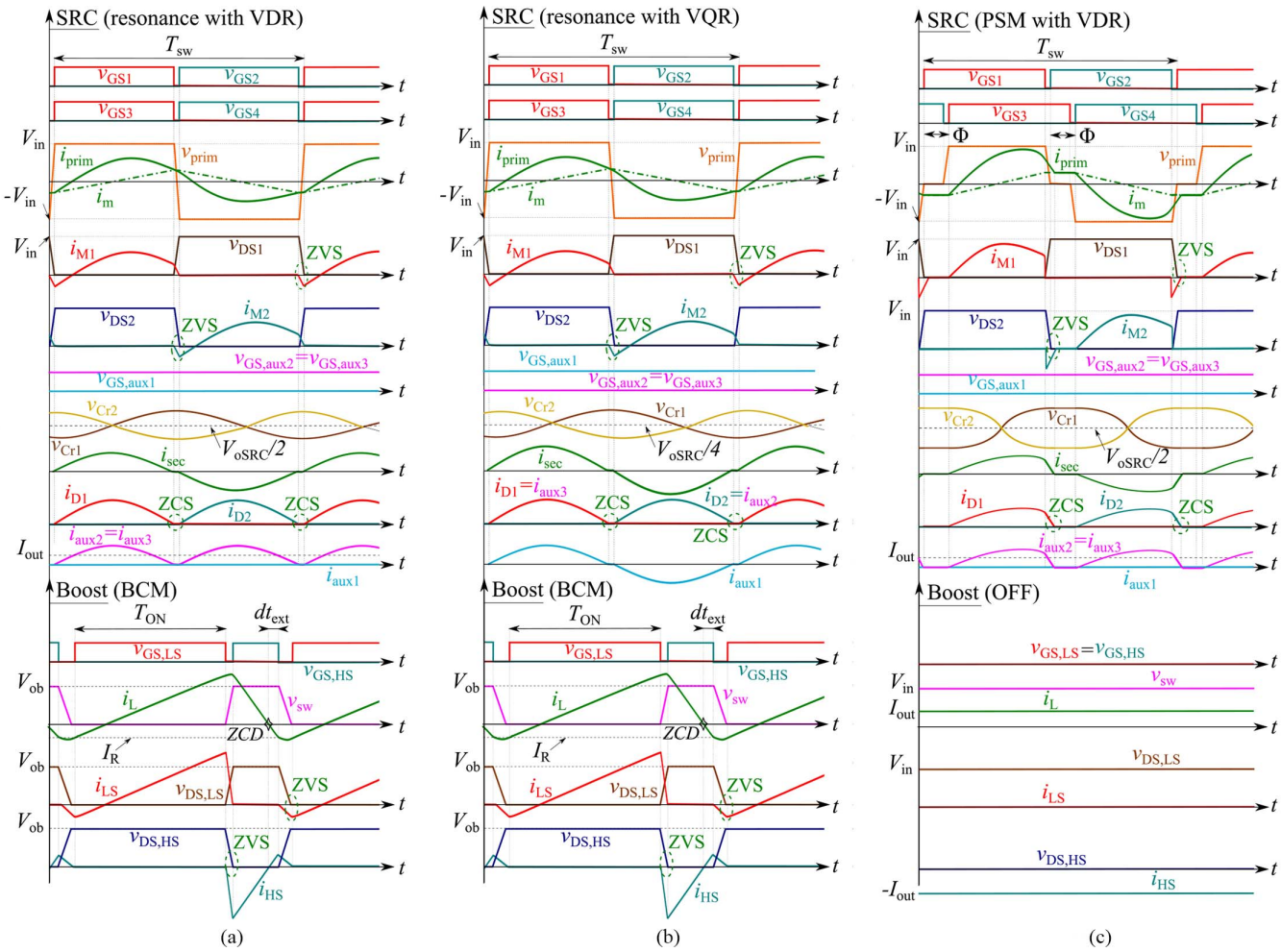


Fig. 5. Main steady-state current and voltage waveforms of the converter: (a) MV mode. (b) LV mode. (c) HV mode.

metal-oxide-semiconductor field-effect transistor (MOSFET) M_{LS} [22], [25]. Despite the larger ripple on the inductor current i_{L}, this operating mode allows to achieve the soft switching of both transistors and to significantly reduce the inductance value, compared to the continuous conduction mode (CCM). The achievement of the soft switching is particularly desirable to improve the light-load efficiency, as low-irradiance conditions are very common in PV applications. In the literature, indeed, the variable-frequency BCM was proved to enhance the part-load efficiency by more than 3 % compared to a constant frequency pulse-width-modulation (PWM) operation [25].

The main voltage and current waveforms of the converter in the MV mode are qualitatively shown in Fig. 5(a).

B. Low Voltage (LV) Mode

At LVs, in the so called LV mode, the VDR can be controlled to morph into a voltage quadrupler rectifier (VQR) [22], by turning ON M_{aux1} and keeping M_{aux2} and M_{aux3} OFF, as shown in Fig. 4(c). This approach allows to significantly reduce the required voltage gain of the synchronous boost at LVs, while maintaining the resonant operation of the SRC. The SRC gain is fixed and equal to $4n$, while the boost provides the gain modulation operating in the BCM. The threshold between the MV and LV ranges corresponds to the voltage V_{th}^{-} at which the boost gain is reset to 1

$$G_2 = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} - 4n = 1 \longrightarrow V_{\mathrm{in}} = V_{\mathrm{th}}^{-} = \frac{V_{\mathrm{out}}}{4n+1}\,. \qquad (3)$$

Similarly to the MV mode, the resonant operation and the soft switching of the SRC devices are preserved. The BCM operation of the boost is analogous to the LV mode. The main voltage and current waveforms of the proposed converter in this mode are shown in Fig. 5(b).

C. High Voltage (HV) Mode

The maximum input voltage V_{th}^{+} at which the boost can still regulate the gain in the MV mode is constrained by its intrinsic step-up capability

$$V_{\mathrm{th}}^{+} = \frac{V_{\mathrm{out}}}{2n+1}\,. \qquad (4)$$

When $V_{\mathrm{in}} > V_{\mathrm{th}}^{+}$, the synchronous boost is kept OFF and the phase-shift modulation (PSM) of the SRC full bridge is exploited to regulate the gain [7], [26]. Fig. 5(c) shows the qualitative voltage and current waveforms of the proposed converter

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TABLE I
SUMMARY OF THE CONTROL LOGIC FOR THE CONVERTER TRANSISTORS IN THE THREE OPERATING MODES

Switch	LV Mode	MV Mode	HV Mode
M_{1-4}	f_{res}, $\Phi = 0°$	f_{res}, $\Phi = 0°$	f_{res}, $\Phi \neq 0°$
$M_{\text{LS,HS}}$	PWM (BCM)	PWM (BCM)	OFF
M_{aux1}	ON	OFF	OFF
$M_{\text{aux,1-2}}$	OFF	ON	ON

TABLE II
MAIN SPECIFICATIONS OF THE PROPOSED CONVERTER

Specification	Value
Rated input voltage	36.5 V
Rated power	700 W
Input voltage range $V_{\text{in,min}} - V_{\text{in,max}}$	15 V–45 V
Output voltage V_{out}	350 V
Required voltage gain G_{TOT}	7.78–23.33

in the HV mode. The phase shift Φ between the gate signals of the two legs increases the rms currents in the SRC, thus larger conduction losses are expected in this operating mode compared to the MV mode, for the same transferred power.

The boost inductor and the high-side MOSFET conduct the output DC current I_{out} and the boost converter is expected to achieve nearly 100 % efficiency and unity voltage gain.

The closed-loop controller should be designed to switch between the operating modes in correspondence of the threshold voltages V_{th}^{+} and V_{th}^{-}. Local efficiency peaks are expected at both V_{th}^{+} and V_{th}^{-}, where the gain and processed power of the boost converter are minimum. Table I summarizes the control logic of the converter transistors in the various operating modes.

III. CONVERTER DESIGN

Table II lists the main design specifications of the converter, based on a commercial PV module [27]. In the case of PV applications, the rated voltage can be selected to coincide with the MPP voltage of a target PV panel, where it is more likely to work. The proposed converter is designed to step-up the input voltage, varying in the wide 15 V–45 V range, to 350 V, standard voltage level adopted in DC microgrids [6], [28]: as a result, the required gain lies in the interval $[7.78;\ 23.33]$. The design flow adopted for the proposed converter begins from the careful selection of the transformer ratio n: this design variable, indeed, has direct influences on the design of both the SRC and of the boost. This is an innovative aspect of this work, which highlights the need for a comprehensive system level design taking into account performance, electrical stresses and size.

As the boost converter is supposed to process only a small fraction of the total power, it is relevant to analyze the impact of n on its share of power (P_2/P_{TOT}), which can be computed from (1) as follows:

$$\frac{P_2}{P_{\text{TOT}}} = \frac{G_2}{G_{\text{TOT}}} = \begin{cases} 1 - 4n\frac{V_{\text{in}}}{V_{\text{out}}},\ V_{\text{in}} \in \left[V_{\text{in,min}},\ V_{\text{th}}^{-}\right] \\ 1 - 2n\frac{V_{\text{in}}}{V_{\text{out}}},\ V_{\text{in}} \in \left(V_{\text{th}}^{-},\ V_{\text{th}}^{+}\right] \\ \frac{V_{\text{in}}}{V_{\text{out}}},\ V_{\text{in}} \in \left(V_{\text{th}}^{+},\ V_{\text{in,max}}\right]. \end{cases} \tag{5}$$

Fig. 6(a) plots the share of boost power in the target voltage range, for three values of n. As shown in Fig. 6(b), the transformer ratio also affects the normalized peak inductor current $(I_{\text{L,peak}}/I_{\text{out}})$, which constrains the minimum saturation current of L_{b} and affects the conduction losses in every component [22]

$$\frac{I_{\text{L,peak}}}{I_{\text{out}}} = \begin{cases} 2G_2,\ V_{\text{in}} \in \left[V_{\text{in,min}},\ V_{\text{th}}^{-}\right] \\ 2G_2,\ V_{\text{in}} \in \left(V_{\text{th}}^{-},\ V_{\text{th}}^{+}\right] \\ 1,\ V_{\text{in}} \in \left(V_{\text{th}}^{+},\ V_{\text{in,max}}\right]. \end{cases} \tag{6}$$

In general, a larger n reduces the share of power of the boost and its current stresses at the rated MPP voltage, at the expense of increased peak currents at $V_{\text{in}} = V_{\text{th}}^{-}$. Finally, as shown in Fig. 6(c), n determines the extension of the HV range, where the SRC is required to work outside the most efficient resonant operation.

Considering the above-mentioned trade-offs, in this work n is designed to minimize the power processed by the boost while ensuring the resonant operation of the SRC in proximity of a target rated voltage V_{rated} [22]

$$G_2 = \frac{V_{\text{out}}}{V_{\text{rated}}} - 2n = 1 \longrightarrow n = \frac{1}{2}\left(\frac{V_{\text{out}}}{V_{\text{rated}}} - 1\right) \tag{7}$$

to be normalized to feasible numbers of turns. In this design, $n = 4$, resulting in $V_{\text{th}}^{-} \approx 20.6\,\text{V}$ from (3) and $V_{\text{th}}^{+} \approx 38.9\,\text{V}$ from (4).

Once n is defined, the required voltage gains profiles of the SRC and boost can be derived from (3) and (7). Fig. 7(a) shows G_1, G_2 and G_{TOT} as functions of V_{in}, highlighting how the topology-morphing allows to significantly reduce G_2 in the LV range. The boost gain is minimized in the neighborhood of V_{th}^{+} and immediately below V_{th}^{-}, and is unitary in the entire HV mode. By applying (5) to the power-voltage characteristic of a real PV module at Standard Test Conditions [27], the share and peak values of power can be graphically visualized for both the stages, as shown in Fig. 7(b).

After these system-level considerations, the design of the two stages can be carried out independently, based on the worst-case voltage and current stresses of the converters components.

A. Multimode SRC Design

Beside the turns ratio, the SRC transformer is designed to magnetically integrate both the magnetizing inductance L_{m} and the leakage inductance L_{k}, designed to resonate with capacitors C_{r1} and C_{r1}. The magnetizing inductance L_{m}, shown in Fig. 4(a) as referred to the primary side, is designed to achieve the ZVS turn-ON of the full bridge MOSFETs M_{1-4} [22], [26].

L_{k} and C_{r} are designed from two simultaneous constraints. First, the resonance frequency was set, as design choice, to a typical value of $f_{\text{res}} = 100\,\text{kHz}$ for step-up SRC converters [7], [14]. A second constraint consists in limiting the peak-to-peak sinusoidal ripple across the capacitors below the SRC output voltage V_{oSRC}

$$\Delta V_{C\text{r}} = \frac{I_{\text{out}}}{2f_{\text{res}}C_{\text{r}}} < V_{\text{oSRC}} \longrightarrow C_{\text{r}} > \frac{I_{\text{out,max}}}{2f_{\text{res}}V_{\text{oSRC}}}. \tag{8}$$

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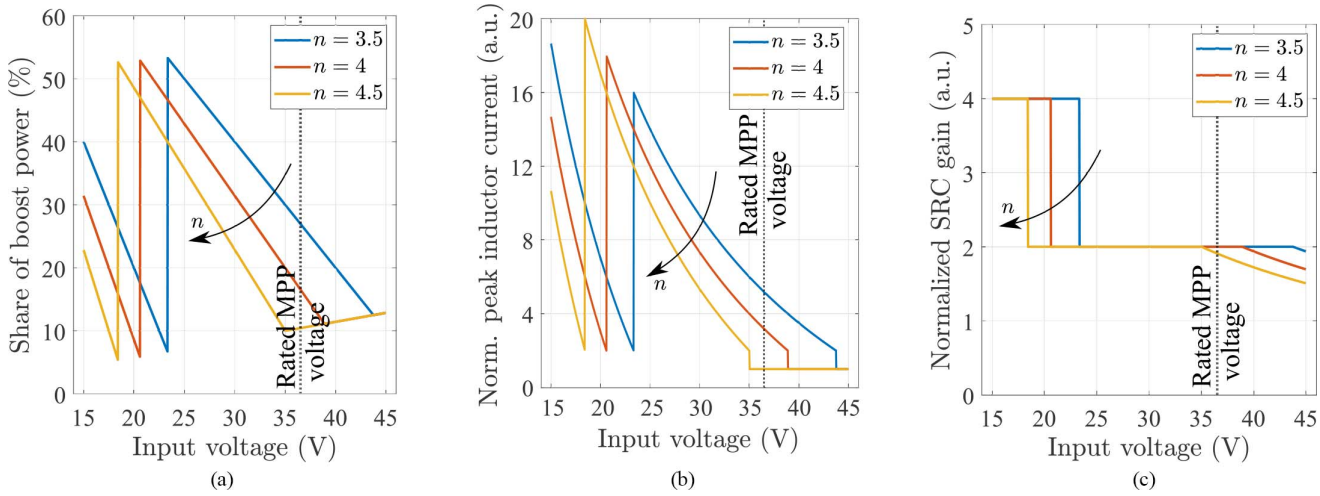


Fig. 6. Quantitative influence of transformer ratio $n \in \{3.5,\ 4,\ 4.5\}$ on various relevant design variables or stresses. (a) Share of boost power VS V_{in} according to (5). (b) Normalized peak inductor current $I_{\text{L,peak}}/I_{\text{out}}$ according to (6). (c) SRC gain.

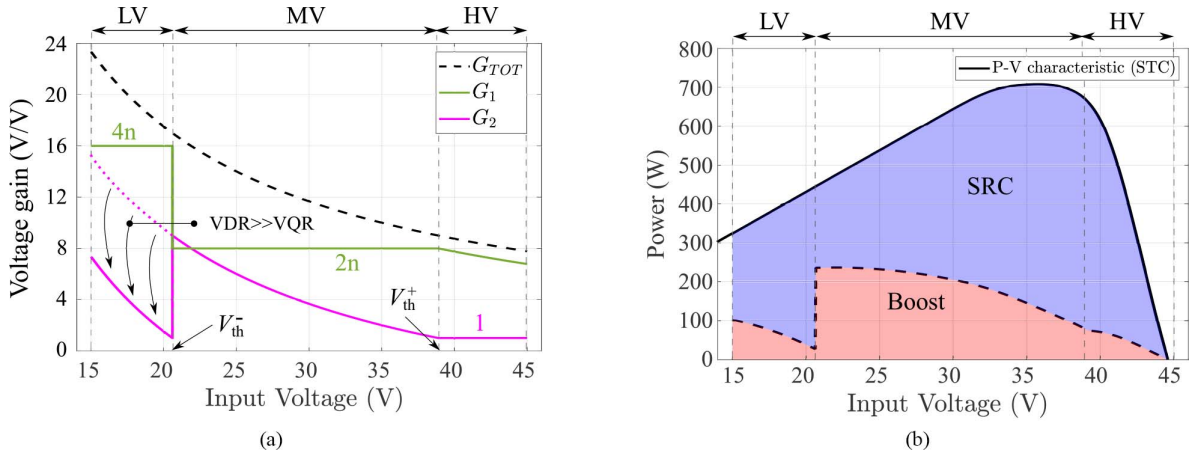


Fig. 7. Gain profiles and share of power of the SRC and boost in the target MPPT range. (a) Behaviour of G_{TOT}, G_1 and G_2. (b) Share of power between SRC and boost considering a realistic power-voltage profile at STC.

TABLE III
SELECTED COMPONENTS FOR THE CONVERTER PROTOTYPE

Component	Part Number	Value
Full-bridge MOSFETs $M_{1\text{–}4}$	STL120N10F8	3.6 mΩ (typ.)
Transformer core	ETD 54/28/19, N97	
Transf. primary coil	4 turns, 2400 x AWG 44	$L_{\text{m}} = 56\ \mu$H,
Transf. secondary coil	16 turns, 225 x AWG 41	$L_{\text{k}} = 29.3\ \mu$H
Rectifier diodes $D_{1\text{–}2}$	STTH10R04G-TR	
Rectifier MOSFETs $M_{\text{aux, 1–3}}$	STB45N30M5	37 mΩ (typ.)
Resonant capacitors $C_{\text{r1–r2}}$	R76PI268050H7J	68 nF
Output capacitors $C_{\text{o1–o2}}$	R76PR4330AA30K	3.3 μF
Boost MOSFETs $M_{\text{HS–LS}}$	STB45N30M5	37 mΩ (typ.)
Boost inductor L_{b}	AGP4233-333ME	33 μH
Boost output capacitor C_{b}	R75MW51004030J	10 μF
Input capacitor C_{in}	8x CB182D0475JBC	37.6 μF

The resulting values of the tank parameters from (2) and (8) are reported in Table III. Their values also affect the voltage gain of the SRC in the HV mode [26], but the primary goal of this design was to optimize of the SRC efficiency and limit the voltage stresses in the MV mode.

The analysis of the worst-case voltage stresses [22] guided the selection of low on-resistance $R_{\text{DS,ON}}$ MOSFETs for both the full-bridge and rectifier of the SRC. The bipolar switch M_{aux1}, required to ensure balanced voltages across the output capacitors, is implemented using a back-to-back transistor configuration.

All DC filtering capacitors of the circuit are selected in film technology, ensuring low equivalent series resistances (ESR) and improved reliability. Their minimum capacitance value and rated voltage can be computed on the basis of the worst-case current stresses [22] and voltage stresses, respectively.

B. Boost Design

Differently from the conventional BCM operation, in which the high-side MOSFET M_{HS} turns OFF when the inductor current is null, the conduction of M_{HS} is extended until the inductor current reaches a minimum negative current $I_{\text{R}}^* < 0$, required to assist the ZVS turn-ON of the low-side transistor M_{LS} [22], [25].

While the voltage gain is still determined by the duty cycle, as in CCM [11], this modified version of the BCM exhibits a variable switching frequency $f_{\text{sw,b}}$ depending on the input

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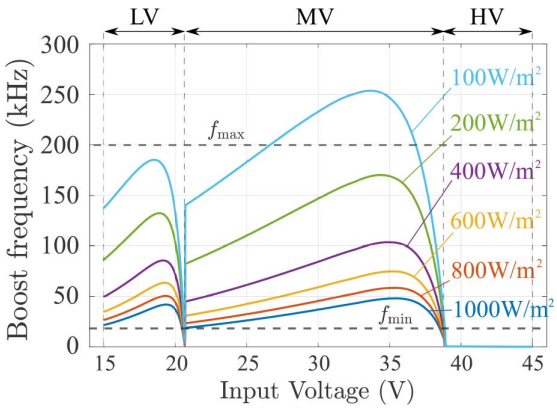


Fig. 8. Boost frequency at various irradiance conditions in the target MPPT range, with $L_b = 33\,\mu H$.

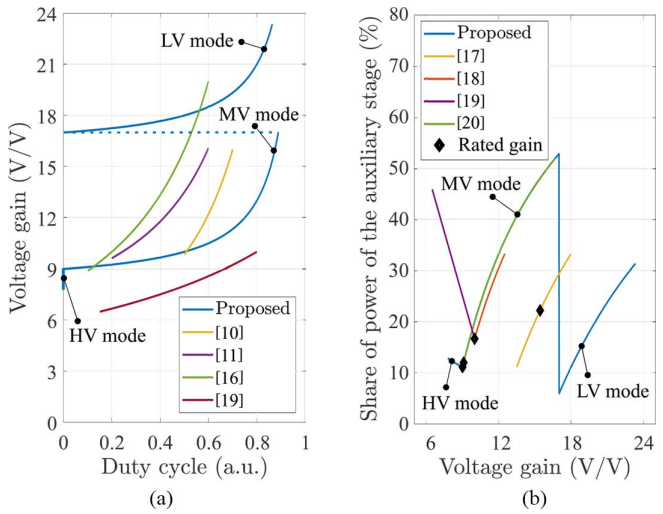


Fig. 9. Comparison of the proposed converter with other state-of-the-art converters. (a) Gain profile VS duty cycle of some boost-derived topologies. (b) Fraction of power processed by the auxiliary stage VS converter gain of some PPP topologies.

voltage and power, the required voltage gain and the selected boost inductance L_b

$$f_{sw,b} = \frac{V_{in} V_{out}}{2 L_b \alpha P_{out}} \frac{G_2 - 1}{G_2^2} \tag{9}$$

where $\alpha \geq 1$ is defined as follows:

$$\alpha = 1 - \frac{I_R^*}{G_2 I_{out}} . \tag{10}$$

According to the gain profiles of Fig. 7(a) and (9), for a given power-voltage curve of a PV panel and a required I_R^*, the boost inductance L_b is the only design variable that determines the switching frequency of the BCM boost. In this work, $L_b = 33\,\mu H$ was selected to bound $f_{sw,b} \in [f_{min}, f_{max}] = [20\,kHz, 200\,kHz]$ for most of the uniform irradiance scenarios, considering the electrical characteristic of the target PV module [27]. The lower bound was set to avoid interference in the audio bandwidth, while the upper bound to limit the turn-OFF losses and frequency-related core losses. The resulting profile of $f_{sw,b}$ is plotted in the target voltage range in Fig. 8, with $I_R^* = -500\,mA$.

After the gain profile of the boost is set from (1) and the target worst-case power profile is defined, the voltage and current stresses of every component can be computed [22]. In particular, the maximum voltage stress of the boost MOSFETs and output capacitor is experienced just above V_{th}^-, where the boost gain peaks

$$V_{DS_{HS,LS},max} = V_{out} - 2nV_{th}^- = \frac{2n+1}{4n+1} V_{out} . \tag{11}$$

The input capacitance $C_{in} = 37.6\,\mu F$ was sized through simulations to limit the worst-case voltage ripple below the recommended 8.5 % of the rated input voltage [29], in the worst case current stress scenario, which occurs at V_{th}^-.

To further underline the advantages of the proposed approach, Fig. 9 shows the comparison of the multimode IPOS converter with other state-of-the-art boost-derived and PPP converters. More in details, Fig. 9(a) compares the gain profile VS duty cycle of multiple boost-derived topologies, highlighting that, thanks to the topology-morphing rectifier, the proposed converter can achieve at the same time the widest gain range and the highest voltage gain without incurring in extremely high duty cycles. Fig. 9(b) compares the fraction of power processed by the auxiliary stage in multiple PPP topologies, as a function of the total converter gain G_{TOT}. The graph shows that, among similar topologies, the proposed approach allows to obtain the widest gain range and, at the same time, the minimum power processed by the auxiliary stage at the rated voltage gain ($\approx 11\,\%$), which can be computed from (5).



Fig. 10. Picture of the PCB prototype.

IV. Experimental Results

A 700 W prototype was built and tested in open loop to validate the converter operation and its performance on a wide range of operating voltages and powers. The final bill of material is listed in Table III. The PCB prototype is shown in Fig. 10. The STMicroelectronics NUCLEO-G474RE development board [30] was used to generate the gate signals.

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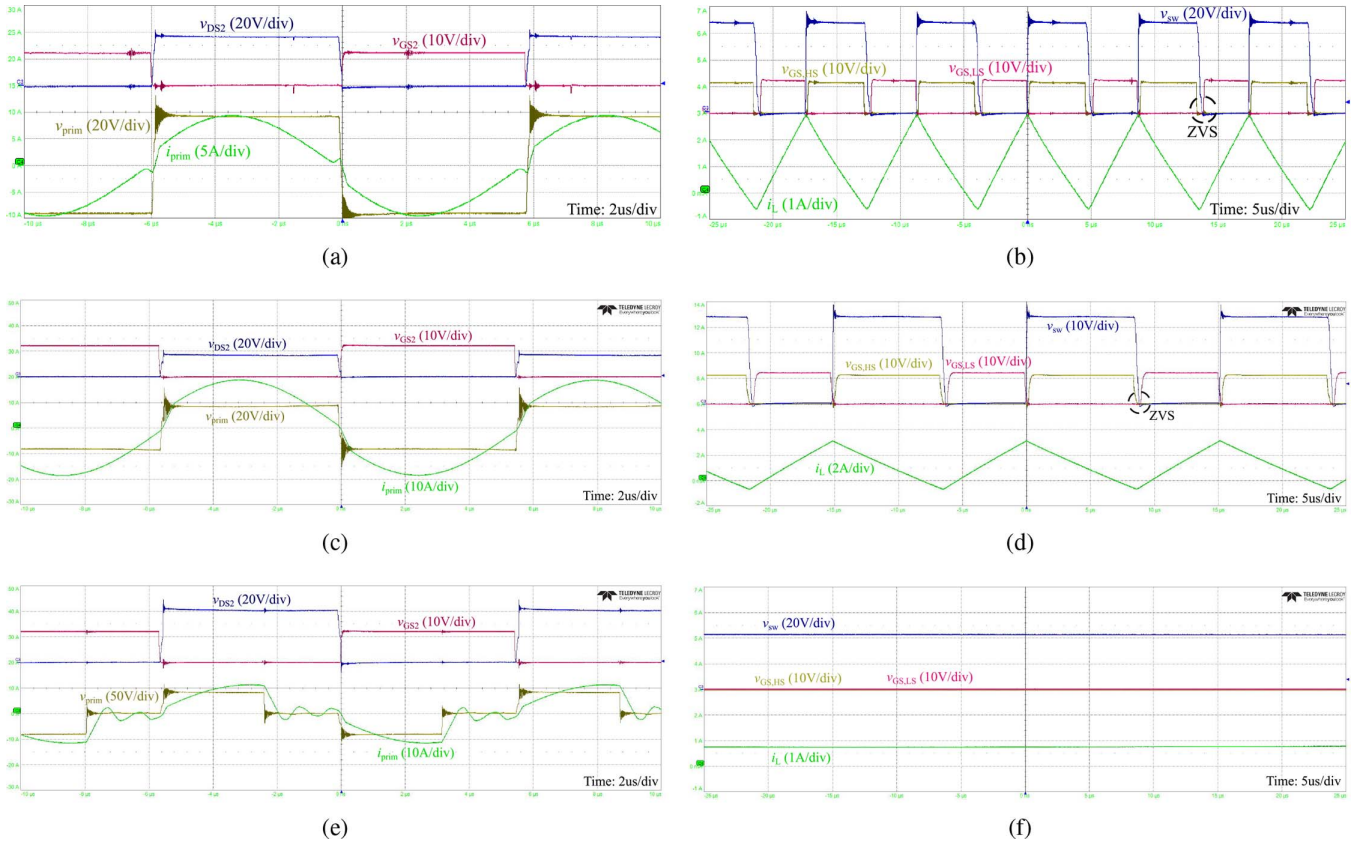


Fig. 11. Main SRC and boost waveforms in three working points: $V_{\rm in} = 36.5\,{\rm V}$ (MV mode), $V_{\rm in} = 20\,{\rm V}$ (LV mode), and $V_{\rm in} = 43\,{\rm V}$ (HV mode): (a) SRC, MV, (c) LV, and (e) HV mode; (b) Boost, MV, (d) LV, and (f) HV mode.

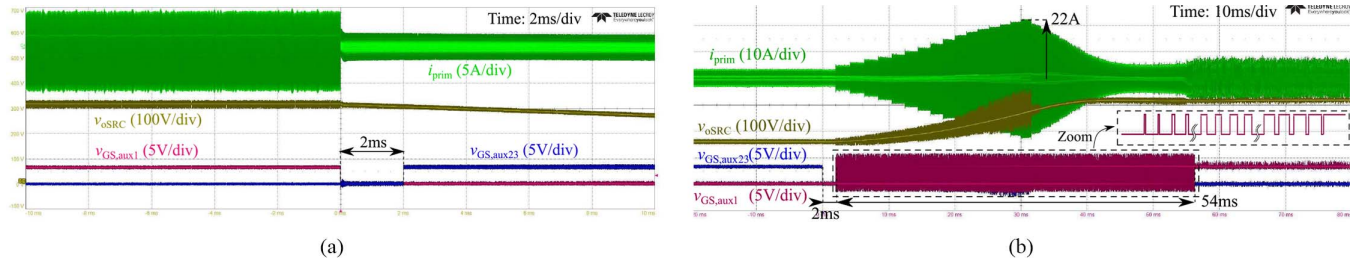


Fig. 12. Main SRC waveforms ($V_{\rm oSRC}$, $v_{\rm GS,aux1}$, $v_{\rm GS,aux23}$ and $i_{\rm prim}$) during the transitions from: (a) LV and MV mode; and (b) MV to LV mode, at $V_{\rm in} = 20.5\,{\rm V}$ and $P_{\rm out} = 100\,{\rm W}$.

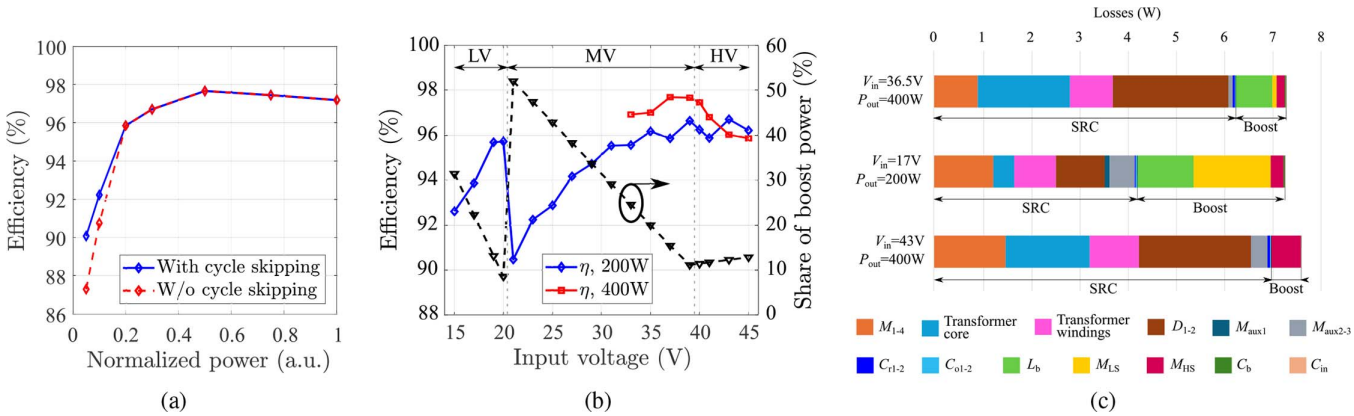


Fig. 13. Measured converter efficiency η and simulated loss breakdown at various input voltage and power conditions. (a) η VS normalized output power, at 39 V. (b) η and share of boost power VS $V_{\rm in}$, at $200\,{\rm W}$ and $400\,{\rm W}$. (c) Loss breakdown at $V_{\rm in} = 36.5\,{\rm V}/P_{\rm out} = 400\,{\rm W}$ (MV mode), $V_{\rm in} = 17\,{\rm V}/P_{\rm out} = 200\,{\rm W}$ (LV mode), and $V_{\rm in} = 43\,{\rm V}/P_{\rm out} = 400\,{\rm W}$ (HV mode).

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A. Converter Waveforms

Fig. 11 shows the main relevant waveforms of both the SRC and the boost stage at three representative working voltages ($V_{\rm in} = \{36.5\,{\rm V}, 20\,{\rm V}, 43\,{\rm V}\}$) and 300 W power, which validate the theoretical operation described in Section II. Fig. 10(a), (c), and (e) show the primary transformer current $i_{\rm prim}$ and voltage $v_{\rm prim}$, and the MOSFET M_2 control and output voltages of the SRC, while Fig. 10(b), (d), and (f) show the inductor current $i_{\rm L}$, the two gate signals and the switching node voltage $v_{\rm sw}$ of the boost. In the proposed BCM with negative current extension, both transistors turn ON at zero voltage under all operating conditions. On the other hand, the SRC transistors exhibit near-ZVS turn ON due to the slightly oversized $L_{\rm m}$ compared to the designed value.

As shown in Fig. 7(a), the SRC and boost gains are discontinuous at the MV–LV transition. Despite far from the most likely working voltages, this mode change must be carefully managed to prevent excessive electrical stresses, especially in the SRC, as it processes the largest fraction of power. The MV–LV transition is triggered by variations in the conduction state of the auxiliary MOSFETs, which can cause massive inrush currents to redistribute charge in the output capacitors $C_{\rm o1}$ and $C_{\rm o2}$ [31]. In the transition from VQR to VDR, when $M_{\rm aux1}$ turns OFF and $M_{\rm aux2}$ and $M_{\rm aux3}$ turn ON, the quality factor of the tank is temporarily reduced, causing a damping of the transformer currents and a smooth decrease of $V_{\rm oSRC}$ from $4nV_{\rm in}$ to $2nV_{\rm in}$. The experimental waveforms in Fig. 12(a), referred to $V_{\rm in} = V_{\rm th}^- = 20.5\,{\rm V}$ and $P_{\rm out} = 100\,{\rm W}$, confirm the absence of overcurrents and overvoltages (OV) when moving from the LV to MV mode. Conversely, in the VDR-to-VQR transition, the turn ON of $M_{\rm aux1}$ induces temporary resonant overcurrents due to the increased quality factor of the tank. To mitigate the risk of destroying the SRC components during the mode change, a soft-transition algorithm was implemented: the duty cycle of $M_{\rm aux1}$ is gradually increased from 0 % to 100 % [32]. The experimental waveforms in Fig. 12(b) show that the proposed approach limits the peak resonant current to approximately 22 A, significantly lower than the $\approx 81\,{\rm A}$ observed in simulations in the same conditions. Such a peak current amplitude does not require to oversize the SRC components, as it is comparable with the amplitude of typical steady-state resonant currents in the LV mode, as shown in Fig. 11(c). In the final application, the controller should adjust the duty cycle of the boost PWM signals during the transitions, to compensate the variation of the SRC gain.

B. Converter Efficiency

Fig. 13(a) shows the measured efficiency profile of the converter at $V_{\rm in} = 39\,{\rm V}$, where the boost gain and power are minimized and the maximum efficiency is expected. The converter exhibits $> 96\,\%$ efficiency starting from 20 % load power with a peak of 97.8 % at 50 % of the rated power. A cycle-skipping technique [7], [16] was implemented to enhance the efficiency at 5 % and 10 % of the rated power by $\approx 2.5\,\%$ and $\approx 1.2\,\%$, respectively. The measured EURO and California Energy Commission (CEC) efficiencies of the converter at the rated voltage are 96.81 % and 97.15 %, respectively.

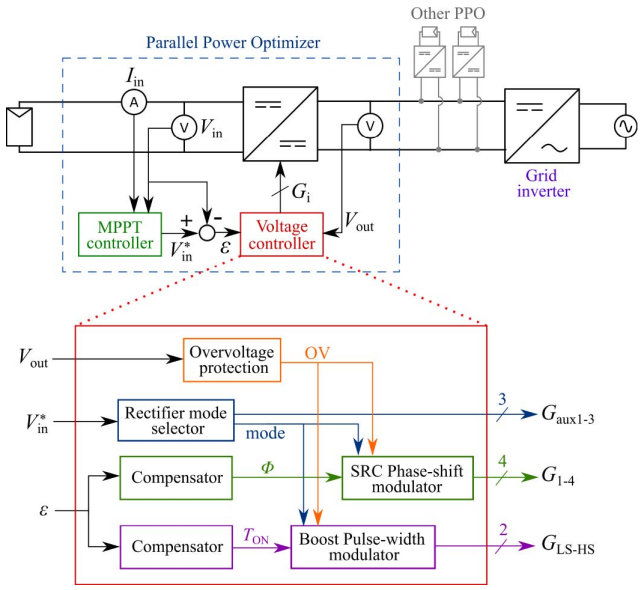


Fig. 14. Block diagram of the closed-loop control scheme of the proposed converter.

Fig. 13(b) shows the behavior of the converter efficiency as a function of the input voltage, for two exemplary operating powers, 200 W and 400 W. The share of power processed by the boost, computed according to (5), is also plotted to prove that the efficiency decreases as the boost gain (and power) increases, as expected. The highest efficiencies are measured in the neighborhood of the MV-HV modes boundary, consistently with the design goal. At 200 W, the efficiency is maintained above 90 % in the entire wide 15 V–45 V range. During the search of the MPP while scanning the P-V curve, the converter may be forced to operate outside the most efficient working points: this is quite typical of converters optimized to operate in the neighborhood of a target rated voltage [7], [14]. In the proposed converter, the most critical condition occurs in correspondence of the LV-MV mode transition, for which a soft-transition algorithm is needed to improve the reliability, as shown in Fig. 12(b). At 400 W, the efficiency rapidly drops in the HV mode due to the increased current stresses of the PSM of the SRC.

Fig. 13(c) shows the loss breakdown of the converter at three different working points, extracted in simulations performed in Simetrix [33] and using the SPICE models of the components listed in Table III. At $V_{\rm in} = 36.5\,{\rm V}/P_{\rm out} = 400\,{\rm W}$ (MV mode), the boost processes a low fraction of the input power ($\approx 16.6\,\%$), resulting in a high converter efficiency. At $V_{\rm in} = 17\,{\rm V}/P_{\rm out} = 200\,{\rm W}$ (LV mode), despite the reduced power, the converter exhibits comparable losses, due to the increased dissipation in the full-bridge MOSFETs, in the transformer windings, and in the boost components due to the increased gain (≈ 4.6). At $V_{\rm in} = 43\,{\rm V}/P_{\rm out} = 400\,{\rm W}$ (HV mode), the only relevant loss contribution of the boost is the high-side MOSFET, which conducts a continuous current through its body diode. Increased conduction losses are obtained in M_{1-4} and in the transformer windings, compared to the MV mode.

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TABLE IV
COMPARISON OF THE PROPOSED POWER OPTIMIZER WITH OTHER STATE OF THE ART SOLUTIONS

Reference	[10]	[11]	[14]	[7]	[15]	[16]	[18]	[19]	[20]	Proposed
Step-up technique	VM	VM + SC	MM LLC	MM LLC	MM LLC	Cascaded MS	A-IPOS	A-IPOS	A-IPOS	MM A-IPOS
Isolation	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
Switches	4	1	5	5	6	6	6	6	6	9
Diodes	7	8	2	2	7	2	2	2	4	2
Magnetic components	6 L	1 CL	1 T	1 T + 1 CL	1 T	1 T + 1 L	1 T + 1 L	1 T + 1 L	2 T + 1 L	1 T + 1 L
Capacitors	9	8	4	5	8	4	6	3	11	6
Rated power	1 kW	200 W	300 W	300 W	300 W	250 W	200 W	250 W	400 W	700 W
Peak efficiency at rated voltage	97.9 %	97.1 %	97.9 %	97.4 %	95.6 %	96.3 %	95.3 %	95.0 %	94.0 %	97.8 %
CEC efficiency at rated voltage	97.45 %	N/A	97.50 %	96.80 %	N/A	95.5 %	N/A	N/A	N/A	97.15 %
Input voltage range	25–40 V	25–40 V	22–36 V	10–60 V	20–50 V	20–45 V	32–40 V	24–37 V	24–44 V	15–45 V
Output voltage	400 V	400 V	315 V	400 V	500 V	400 V	400 V	240 V	400 V	350 V
Min/max efficiency in the voltage range	97.2 %–97.9 %	92.7 %–95 %	95.5 %–97.5 %	79 %–97.4 %	94.5 %–95.5 %	95.0 %–97.0 %	94.7 %–95.3 %	92.3 %–95.0 %	92.0 %–94.0 %	90.5 %–96.7 %

Note: VM = Voltage multipliers; SC = Switched capacitors; MM = Multi-mode; MS = Multi-stage; A-IPOS = Asymmetric input-parallel-output-series; L = Inductor; T = Transformer; CL = Coupled inductors.

Overall, the rectifier diodes and the transformer introduce the major contributions to the converter losses.

C. Control Architecture

In a closed-loop operation, the controller should be designed to implement the MPPT while ensuring stable operation, in every operating region. In addition, the controller should ensure a soft startup to avoid excessive temporary electrical stresses that could damage the converter components [31]. A block scheme of the closed-loop control architecture for the proposed converter is shown in Fig. 14. Every PPO monitors the current and voltage of the input PV panel, which are used to implement the MPPT. Standard incremental approaches such as the perturb & observe (P&O) or incremental conductance (InC) algorithm have become wide-spread due to their simple implementation and low computational complexity [34]. The voltage error between the acquired and reference input voltages $\epsilon = V_{\text{in}}^{*} - V_{\text{in}}$ feeds a voltage controller, which, in accordance with the control mode strategies illustrated in Table I, updates the PWM signals of the SRC (G_{1-4}) and boost MOSFETs ($G_{\text{LS}-\text{HS}}$), and the conduction state of the auxiliary MOSFETs ($G_{\text{aux},1-3}$). At the same time, for safety purposes, the DC rail voltage V_{out} should be monitored to turn OFF the PPO in case of OV, indicating failures at the inverter side. The design of a closed-loop controller for a multimode converter is based on the derivation of the control-to-input transfer functions in every operating mode, as done in [7], [14]. As this approach is standard, the detailed design and implementation of a closed-loop control is not reported in this article.

D. Comparison With the State of the Art

Table IV compares the main features of the proposed converter with the state of the art of power optimizers exhibiting similar specifications. The proposed solution shares the widest voltage range with the multimode converters in [7], [14], [15]. The PWM converters based on VM and/or SC [10], [11] allow to achieve high peak efficiencies at the rated voltage but employ a large number of capacitors and diodes, and operate on a narrower MPPT range. Among the other asymmetric IPOS solutions [18], [19], [20], the proposed converter achieves the highest peak efficiency 97.8 %, 2.5 % more than [18], and, at the same time, the widest voltage range. In general, thanks to the design flexibility and multimode features, the proposed power optimizer represents an efficient solution for PV applications requiring high performance in the neighborhood of a target voltage, while still ensuring satisfactory efficiency when operating far from the rated power and voltage. The designed prototype was mainly optimized in terms of maximum efficiency: the inclusion of cost and power density, not considered at this stage, could be object of further future optimization.

V. CONCLUSION

This article has introduced a new high step-up DC–DC converter for PPO applications. The proposed converter is based on an asymmetric IPOS architecture and on a multimode control approach to achieve at the same time high efficiency at a desired operating point and the possibility to work on a wide range of input voltages, desirable features for flexible and efficient PV systems. A prototype designed for a rated 700 W and for the 15 V–45 V input voltage range was built and tested to validate the proposed approach. The measurements highlight a CEC efficiency of 97.15 % at the rated voltage. The wide-range operation of the converter and its high performance align it to the state of the art and make it a valid solution for PPO.

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