Capacitance-to-digital converter in dual-mode logic: power consumption vs conversion time trade-off

Capacitance-to-Digital Converter in Dual-Mode Logic: Power consumption vs Conversion time Trade-off

(Invited paper)

Orazio Aiello[1], Paolo Crovetti[2]
[1] DITEN, Università di Genova, Italy, [2]DET, Politecnico di Torino, Italy
orazio.aiello@ieee.org,paolo.crovetti@polito.it

Abstract. This paper deals with the trade-off between conversion time and power in nW-power capacitance-to-digital converters (CDCs). The CDC used in this work operates at nW power and low voltage down to 0.3 V without the need for any additional circuitry, references, or voltage regulation. It is built on swappable oscillators and takes advantage of the delay-power flexibility of dual-mode logic. Its self-calibration corrects PVT changes and mismatches at any point in the chip lifecycle, doing away with the necessity for cutting during testing. A CDC's test chip in 180nm demonstrates that its power consumption can be dynamically modified from 1.37 nW down to 418 pW at a conversion time down to hundreds of ms, making it suited for harvesting systems with a very tight power budget and changing power sources.

Keywords: Capacitive-to-Digital converter (CDC), Power consumption versus Time conversion trade-off, Ultra-Low Voltage, nW Power, Dual-Mode (DM) Logic.

1 Introduction

Widely dispersed, long-lasting sensor nodes for the Internet of Things (IoT) need inexpensive, battery-free sensor interfaces [1], [2]. Particularly when powered directly by harvesters, when intermediate DC-DC conversion is prohibited to further reduce power [3]–[13], such systems must function under uncertain and aggressively reduced supply voltages and power down to the nW range.

Among the most popular sensor interfaces, capacitive sensor interfaces support a variety of sensing modalities, including proximity, displacement, pressure, humidity, and others [14], [15]. Capacitance-to-digital converters (CDCs) have recently been proposed [1] as its primary building block, with power within the power budget provided by millimeter-scale harvesters (e.g., solar cells) under realistic lighting conditions. The problem in such directly harvested CDCs is to maintain their peak power below the harvested power across large variations. To put it another way, the design goal in the aforementioned application domain is considerably different from that of traditional battery-powered systems, which places a strong emphasis on energy efficiency represented as energy/conversion step [1], [2].

Regarding the basic trade-off between power and resolution, CDCs with a resolution larger than 14 bits have been demonstrated at tens of microWatts or higher [16]–[20], whereas 10–12 bit resolution can be obtained at microwatt power [21]–[23] The effective resolution of sub-μW CDC architectures is 7 to 8 bits or less [24], [25]. Although CDCs can reach
the same resolution with power consumption in the sub-nW range, their need for supply voltages above 0.6 V precludes them from being directly powered by energy harvesters [22].

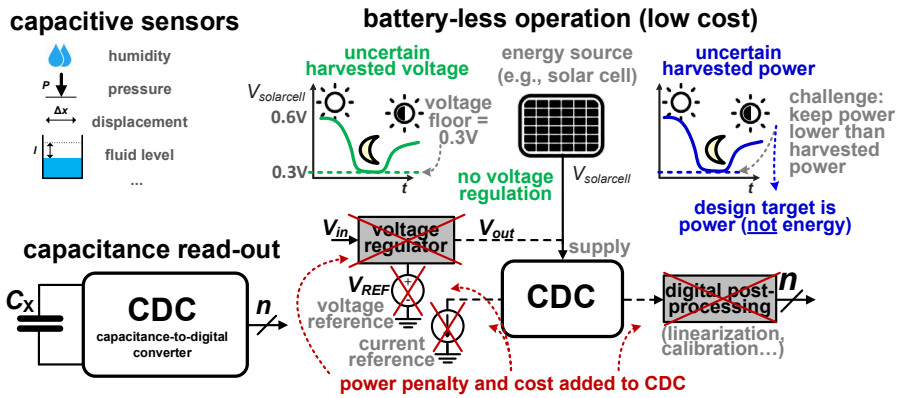

Fig. 1. Pictorial representation of a capacitive sensing in low-cost systems without additional circuitry for direct harvesting with harvester in the millimeter scale.

Other CDCs with sub-nW operation at 0.6 V at 7-bit resolution have been proven [25], but their power benefit is negated by the additional contribution of digital post-processing (nanoWatts), which was not taken into account. Although a fully-digital CDC working at 0.45 V was presented in [27], it still needs a supply voltage of 1 V and is unsuitable for direct harvesting. A CDC functioning at voltages as low as 0.3 V was proposed in [28], despite its input range is constrained and its power, which is in the hundreds of nanoWatts, is insufficient for direct harvesting at the millimeter scale.

Along with resolution considerations, operation at aggressively low power in the nW region and down naturally results in conversion times that are sub-second or second scale [25], which are still within the acceptable range for many continuous monitoring applications [26]. (e.g., temperature, humidity, proximity, fluid level monitoring). Additionally, although they are still required for the proper operation of CDCs, the power budget of prior art typically does not account for the contribution of voltage and current references, voltage regulators, and post-processing circuits (such as linearization).

A CDC for low-cost directly-harvested systems is considered as a starting point in this study [1] because it enables the pursuit of real nW power targets with no further assistance (and power) from any of the above additional circuits, as depicted in Fig. 1. By utilizing the dual-mode logic style's circuit features, this work introduces more flexibility in the conversion time-power tradeoff [29]. The entire CDC has been implemented in dual-mode logic. For this purpose, dual-mode standard cells have been designed and included in an automated digital design flow (logical synthesis and automated place&route). To the best of the authors' knowledge, the power consumption versus conversion time trade-off has not been so thoroughly investigated for capacitive sensing and for an integrated sensor in general.

This is how the paper is organized. The CDC's architecture and guiding principles are introduced in Section II. Regarding the experimental findings from a 180-nm CDC test chip demonstration, the conversion time-power tradeoff is discussed in Section III. Section IV is where the conclusions are ultimately reached.

2 Operation of CDC with Dual-Mode Logic

Figs. 2 and 3 [3] illustrate the CDC's basic functioning concept. The two relaxation oscillators OSC1 and OSC2, which are shown as gray boxes in Fig. 2, represent the core of the circuit. As a result, the load capacitances, or the unknown capacitance C_x to be measured and the reference capacitance on-chip C_{ref}, are proportional to their respective periods, T_x and T_{ref}. C_{ref} was set to 500 fF. The CDC is assumed to be correctly calibrated as in [3] and C_x is assumed to be bigger than the reference on-chip capacitance C_{ref} for the sake of simplicity. As a result, they are made nominally equivalent within less than 1 LSB.

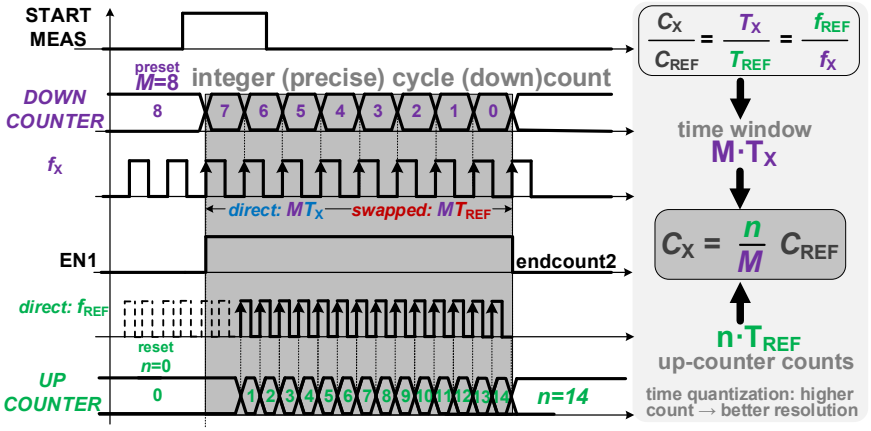

Fig. 2. Digital-based CDC operation and main waveforms.

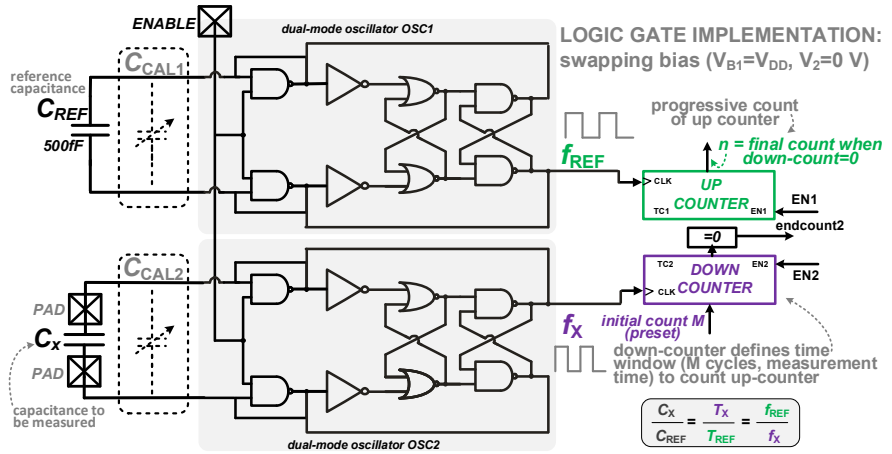

Fig. 3. Digital-based CDC architecture.

As a result, the oscillator period capacitance accurately reflects the ratio of load capacitances:

$$\frac{C_x}{C_{ref}} = \frac{T_x}{T_{ref}} \qquad (1)$$

Since the two oscillators track each other in terms of overall process fluctuations, voltage and temperature, once mismatch has been addressed through the aforementioned calibration, (1) holds regardless of process, voltage, and temperature variations.

From (1), the period ratio can be calculated by counting the number of periods of one of the two oscillators within a measurement window that is proportionate to the other period. This calculation can then be used to calculate the capacitance ratio of the two oscillators. To put it another way, as shown in Fig. 2, the measurement window $t_{MEASURE}$ is made up of an exact number of periods of the other oscillator that can be digitally configured. For this reason, an oscillator is connected to an up counter (see top-right in Fig. 3) initially reset to zero, and the other oscillator is connected to a down counter (see bottom-right in Fig. 3) initially preset to a digitally-configurable integer M.

Assuming that in Fig. 3 C_{REF} and C_x are connected to OSC1 and OSC2, respectively, let n be the total number of periods T_{ref} inside the time window $t_{MEASURE} = M \cdot T_x$ As a result, the following equality is true up to a quantization error of $\pm T_{\mathrm{REF}}$.

$$M \cdot T_x = n \cdot T_{\mathrm{REF}}. \qquad (2)$$

The capacitance C_x to be measured can be expressed using the count n and the setting M as shown in (1)–(2).

$$C_x = \frac{n}{M} C_{REF} \qquad (3)$$

due to the time quantization of $n \cdot T_{\mathrm{REF}}$ in (2) inside the precise time window $M \cdot T_x$, with a maximum absolute error below $\delta C_x = C_{REF}/M$. The up-counter count n has an inverse relationship with the relative quantization error, i.e. $\delta C_x / C_x = 1/n$. From (2), raising n and subsequently the preset M results in lesser quantization error (i.e., higher resolution). By increasing the former at the expense of the latter, the latter can be used as a knob to tradeoff the CDC resolution with the conversion time $t_{MEASURE}$. The same design can be reused across several capacitance ranges and applications thanks to this versatility. In order to gain better conversion time-power flexibility, as detailed in the following section, all logic gates in Fig. 3 are based on the dual-mode logic approach. The quantization noise constraint on the resolution was removed by selecting a bit width of 12 for both the up counter and the down counter. This decision should provide for a minimum theoretical absolute resolution that is limited by quantization to:

$$C_{LSB} = \frac{C_{REF}}{M} > \frac{C_{REF}}{2^B} = 0.125\mathrm{fF} \qquad (4)$$

whereas a worse resolution is expected when considering noise and non-linearity.
The aforesaid CDC may operate at aggressively low supply voltages without the requirement for voltage control because of its digital and differential nature from Fig. 3. This reduces the need for voltage regulation. Since direct harvesting is used in this study, it is necessary for dual-mode logic to function below 0.3 V [23].

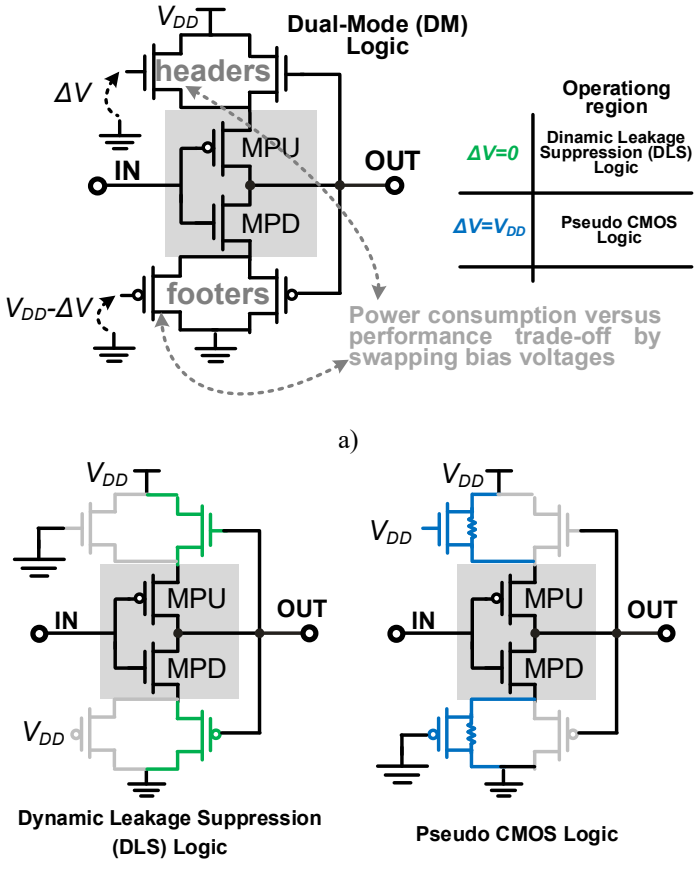

Fig. 4. a) Dual-mode logic inverter that explores the power-performance trade off by swapping the header/footer bias voltage ΔV. b) Swapped bias voltages that realized the equivalent of Dynamic Leakage Suppression Logic inverter and Pseudo-CMOS Logic inverter.

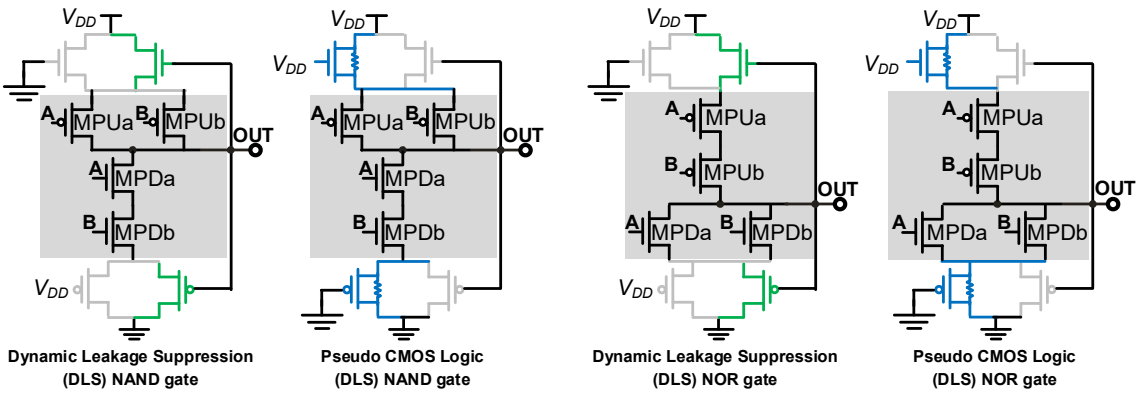

Fig. 5. Dual-mode logic: equivalent Dynamic Leakage Suppression Logic and Pseudo CMOS Logic for a) NAND gate and b) NOR gate

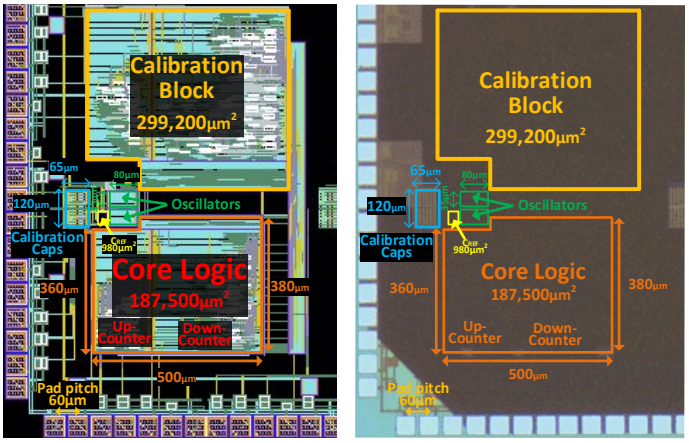

Fig. 6. Layout and Die micrograph of the CDC.

3 Benefits of Dual-Mode Logic in CDC: Conversion Time-Power Trade off

Dual-mode logic with is demonstrated in Fig. 4 with reference to an inverter gate [29]. The dual-mode logic gate closely resembles the Dynamic Leakage Suppression (DLS) logic [30] type when the header and footer bias voltages are set to ground and the supply voltage V_{DD} respectively (i.e., ΔV=0 in Fig. 4). When their strength is minimal, however, they are no longer present. Due to the super-cutoff behavior of transistors MPU and MPD in Fig. 4, this case's leakage is diminished by 2–3 orders of magnitude compared to the typical transistor leakage (see [29] for details). Such leakage reduction is essential in the targeted applications, even though it results in ms-scale gate delays, as the limited power budget available in directly harvested systems tends to be leakage-dominated [1]. Similar as the dual-mode logic inverter is represented in Fig. 4, the dual-mode logic (both the equivalent DLS and pseudo-CMOS configuration) for a NAND and NOR gate is reported in Fig. 5.

The strength of the header and footer transistors is significantly higher than that of all other transistors within the gate, however, when the header/footer biasing is switched (i.e., ΔV=V_{DD}=0.3 V). As a result, the logic gate functions as source-degenerated standard CMOS logic; the associated mode is referred to as "pseudo-CMOS" in the following. The pseudo-CMOS mode greatly reduces gate latency in comparison to DLS mode while increasing leakage and dynamic power, the latter of which is primarily caused by an increase in operating frequency. Dual-mode logic in pseudo-CMOS mode reduces leakage by at least ~4× when compared to normal CMOS logic.

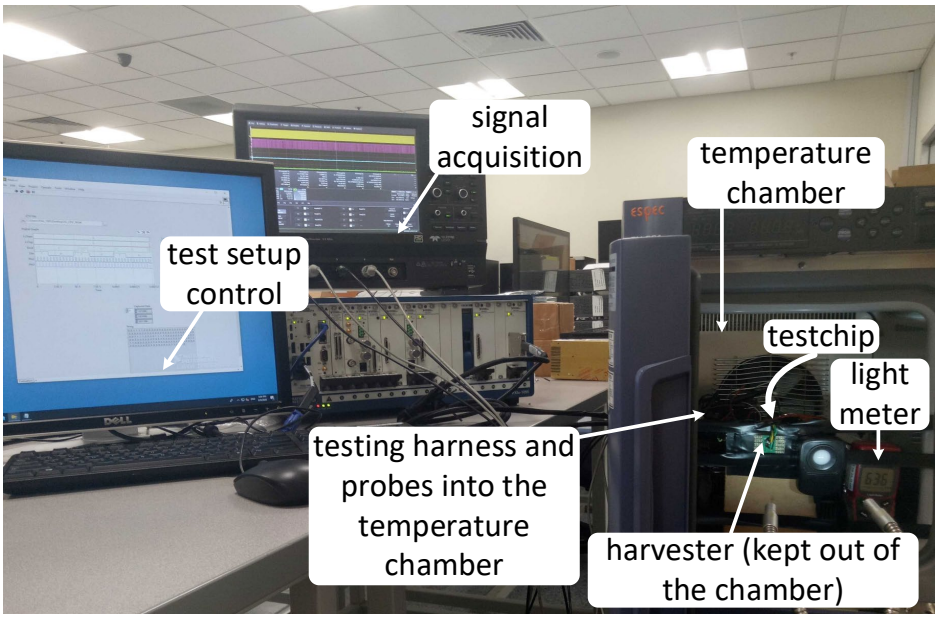

Fig. 7. Testing Setup.

The CDC working in pseudo-CMOS logic only has been explored in [4] where the circuit has been proven offering an unique property of suppressing any voltage regulation within the wide 0.3-1.8 V supply range and eliminates its additional power (not accounted for in all prior art). Based on this, the CDC can be characterized under direct harvesting with a 1mm^2 solar cell from very dim light (10 lux) to sun light [3]. Thus, the novelty of this paper is showing the power consumption versus conversion time trade-off can be enabled to further lower the power consumption whenever the conversion time is not a relevant specification. For instance, environmental monitoring such as humidity monitoring, as a broad class of humidity sensors (including several commercial products) is simply based on a capacitor with a humidity-dependent dielectric material. Such monitoring could be demanded from an always-on and environmental-friendly small energy harvester (i.e. 1mm^2 solar cell) and having a conversion time in order of several seconds.
In conclusion, dual-mode logic favors low power operation at the expense of speed in the DLS mode, whereas the reverse is true in the pseudo-CMOS mode. Dual-mode logic performs successfully in both modes over the wide supply voltage range of 0.3-1.8 V, and its latency is far less supply voltage sensitive than that of regular CMOS [31].

4 Measurements results

The CDC with extended conversion time-power tradeoff in dual-mode circuitry was built in a 180-nm testchip (see Fig. 6) and experimentally characterized.
The test chip was powered with a sourcemeter for characterization across voltages, and by a 1mm^2 light harvester under controlled light intensity (as measured by a light meter) to demonstrate direct harvesting capabilities as shown in Fig. 7.
Unless specified otherwise, the measurements were performed with the down-counter preset M=32 as a compromise between measurement time and resolution, which was targeted to be C_{LSB}=125fF. The considered dynamic range of the off-chip capacitance to be digitized is 30pF.

The CDC characterization across header/footer bias voltages is presented in this Section. In particular, the following investigates the related tradeoff under various header/footer bias voltages ΔV ranging from 0 V (DLS mode) to 0.3 V (pseudo-CMOS mode) under the influence of the available knobs. On this purpose, the capacitance to be digitized C_x was tuned with a step of approximately 500fF, and measured with fF-range resolution through a Precision E4980AL LCR meter.

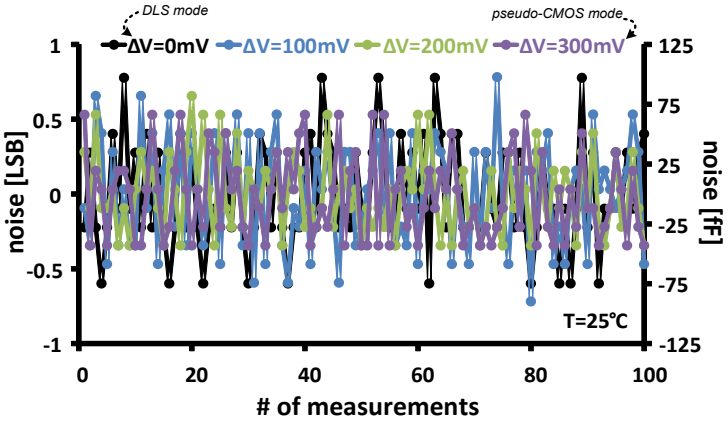

Fig. 8. Impact of noise across repeated measurements for different values of the header/footer bias voltages ΔV in Fig. 4 for C_x =10 pF. M=32.

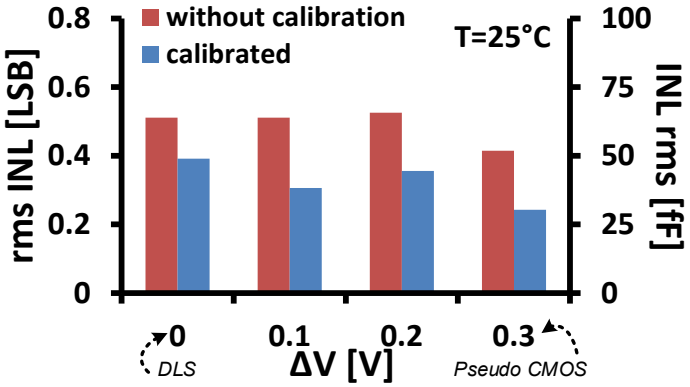

Fig. 9. RMS integral non-linearity (INL) versus header/footer bias voltages ΔV in Fig. 4 for C_x ranging from 2 pF to 30 pF and M=32.

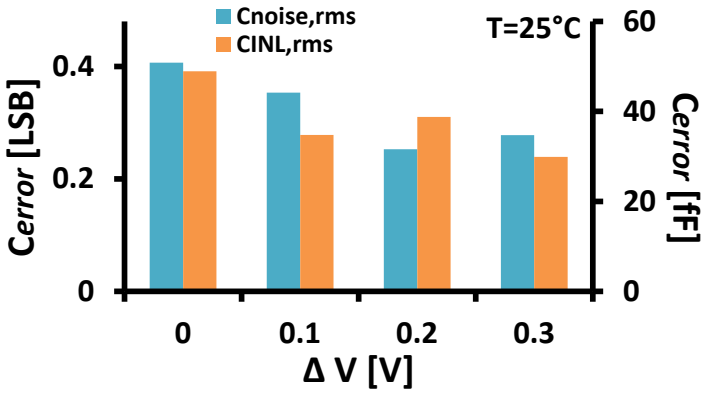

Fig. 10. Capacitance error due to noise and non-linearity vs. header/footer bias voltages ΔV for C_x ranging from 2 pF to 30 pF and M=32.

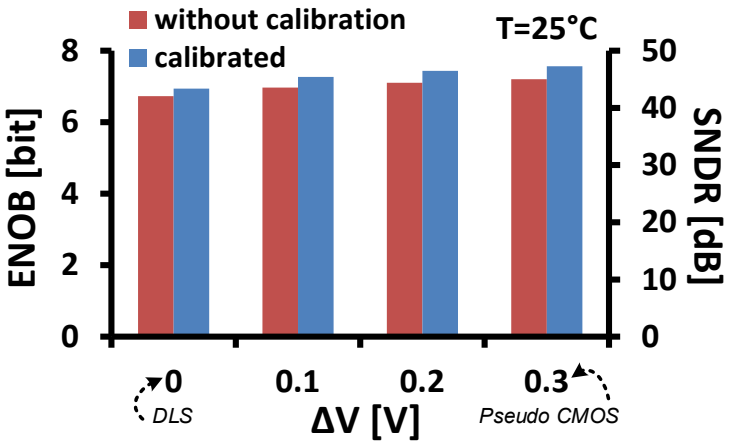

Fig. 11. SNDR and Effective number of bits (ENOB) and SNDR vs. header/footer bias voltages ΔV for C_x ranging from 2 pF to 30 pF and M=32.

Lower values of the down-counter setting M improve (shorten) the conversion time and energy at the expense of more quantization noise, as mentioned in Section III. Contrarily, by adjusting the header/footer voltage through ΔV in Fig. 4, it is possible to increase the conversion time and energy without weakening the influence of quantization noise, preventing it from becoming the main source of noise throughout the conversion process. The effect of noise is depicted in Fig. 8 for various values of ΔV between 0 and 0.3 V with C_x=10 pF and M=32. According to this graph, switching from DLS to pseudo-CMOS mode results in a reduction in output-referred RMS noise, which is to be expected given the higher transistor current at higher ΔV.

Figure 9 illustrates the RMS value of the integral non-linearity (INL) over a capacitance range of 2 pF to 30 pF. The minimum value of the considered capacitance is limited by the parasitic capacitance associated with pads and wires, which are connected in parallel and hence add to the externally connected C_x. The nominal LSB capacitance of C_{LSB}=125 fF corresponds to 0.23-0.34LSB at the post-calibration RMS INL range of 29-48 fF for ΔV ranging from 0 V (DLS mode) to 0.3 V (pseudo-CMOS mode).

According to Fig. 10, for ΔV ranging from 0 V to 0.3 V, the linearity-limited resolution $C_{INL,RMS}$ ranges from 49 fF (0.39 LSB) to 30 fF (0.24 LSB). The resulting SNDR is

$$SNDR = 20\log_{10}\frac{C_{range}}{2\sqrt{2}\,C_{err}} \qquad (5a)$$

where the evaluation of the total error C_{error}, which takes into account both noise and non-linearity, is

$$C_{error} = \sqrt{C_{noise,RMS}^2 + C_{INL,RMS}^2}. \qquad (5b)$$

From Fig. 10, it can be seen that the overall error capacitance C_{error} in pseudo-CMOS mode is 1.53X lower than in DLS mode. As shown in Fig. 11, the SNDR after calibration is between 43.5 dB and 45.2 dB, or 6.9 bits and 7.2 bits effective bits (ENOB). Notice that ENOB increases at larger down-counter preset values M, thanks to the improved accuracy and noise immunity at longer measurement time $t_{MEASURE}$. The benefits of larger M were experimentally quantified by increasing its value from 32 (as reported in all the above figures) to 64 and 128. Referring to pseudo-CMOS configuration, the RMS value of the INL at M=64 is reduced by 1.7X, and further doubling of M to 128 further reduces the RMS INL by another 1.3X. This improvement comes at the cost of a proportionally higher conversion time [3].

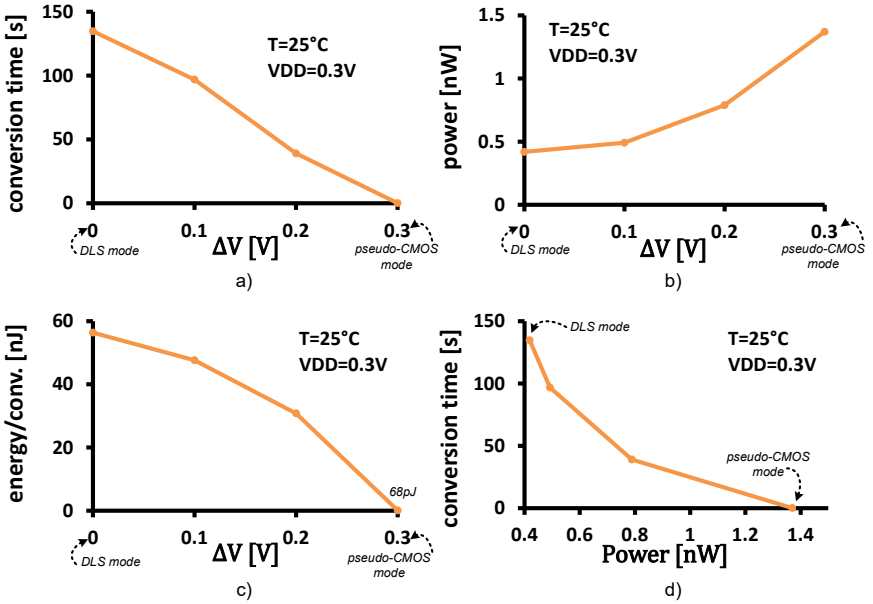

Fig. 12. Measurement results for V_{DD}=0.3V : a) conversion time vs. header/footer bias voltages ΔV, b) power consumption vs. ΔV, c) energy per conversion vs. ΔV, d) conversion time-power tradeoff for M=32 and C_x=10 pF.

According to Fig. 12a, the conversion time is in the 50-ms range for ΔV values approaching 0.3 V (i.e., pseudo-CMOS mode), whereas it significantly increases for low V (i.e., DLS mode). In contrast, as shown in Fig. 12b, the power consumption in DLS mode is 418 pW, which is 3.3X less than in pseudo-CMOS mode (1.37 nW). Because of this, ΔV is a useful knob to boost speed at a moderate increase in power because the sensitivity of the conversion time to it is considerably higher than the sensitivity of the power consumption.

As shown in Fig. 12c, the energy per conversion in pseudo-CMOS mode is minimal and equivalent to 68 pJ. The substantially greater sensitivity of the conversion time to V, as described above, is confirmed by the conversion time/power consumption tradeoff in Fig. 12d. Fig. 13 shows how the overall power consumption that changes over the header/footer bias voltages ΔV as in Fig. 12b, is differently distributed among the timing oscillators and the remaining digital counterpart of the CDC. In particular, for header/footer bias voltages ΔV ranging from 0 V (DLS mode) to 0.3 V (pseudo-CMOS mode), the percentage of the power consumption related to the timing oscillators move from 5.4% to the 11%.

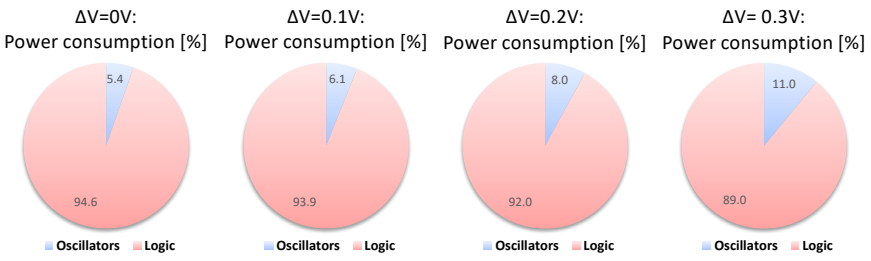

Fig. 13. Power consuption distribution among the oscillators and the logic counterparts for different header/footer bias voltages ΔV for V_{DD}=0.3V; M=32 and C_x=10 pF.

The wide voltage range of the circuit follows from the characteristics of dual mode gates, which have been shown to work consistently over such a wide power supply voltage range in previous works [29]. Being the CDC digital in concept, the wide supply voltage range of the Dual-Mode gates is immediately translated in a wide voltage range

of the CDC. Based on multi-dice measurements on 5 dice, they work properly in the 0.3V to 1.8V supply voltage range. The effect of temperature on the error under a temperature range from -25°C to 75°C is well below the LSB, and ranges from -0.66 LSB to 0.21 LSB [3].

The same measurements reported in Fig. 12 have been repeated for V_{DD}=0.4V in Fig. 14. The plots in Fig. 14 show how the conversion time, the power, and the energy/conversion change with ΔV for a 100mV increment of the supply voltage V_{DD}, resulting in a further (conventional) trade-off: the higher the V_{DD}, the faster the operation at the cost of increased power consumption on the basis of the supply voltage.
Similarly to what is reported in Fig. 13 referring to V_{DD}=0.3V, for header/footer bias voltages ΔV ranging from 0 V (DLS mode) to 0.4 V (pseudo-CMOS mode), the percentage of the power consumption related to the timing oscillators move from 5.4% to the 17%.

The PVT variations have been extensively investigated in [3]. The effect of temperature on the error under a temperature range from -25°C to 75°C is well below the LSB, and ranges from -0.66 LSB to 0.21 LSB [3].

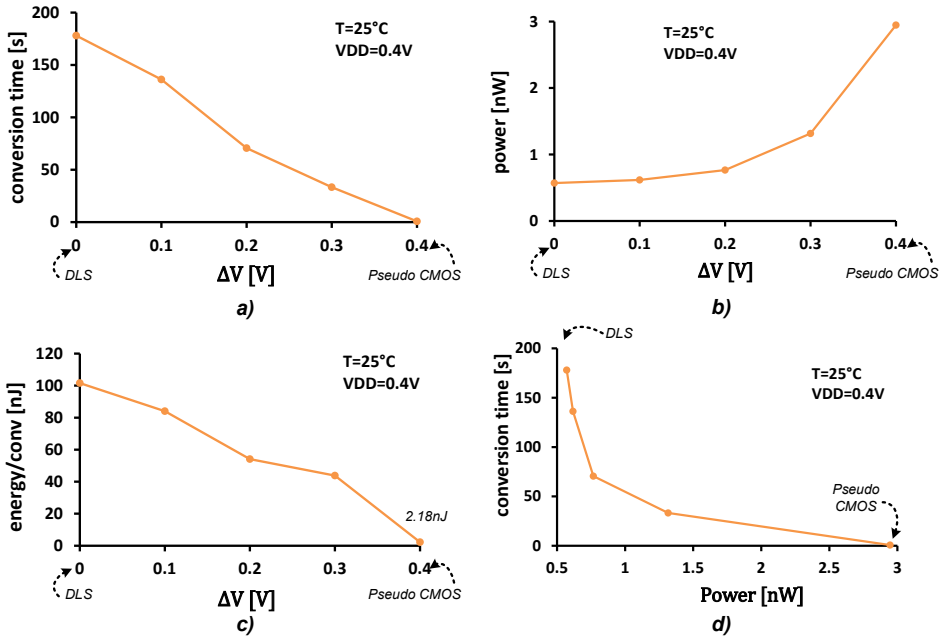

Fig. 14. Measurement results for V_{DD}=0.4V; a) conversion time vs. header/footer bias voltages ΔV, b) power consumption vs. ΔV, c) energy per conversion vs. ΔV, d) conversion time-power tradeoff for M=32 and C_x=10 pF.

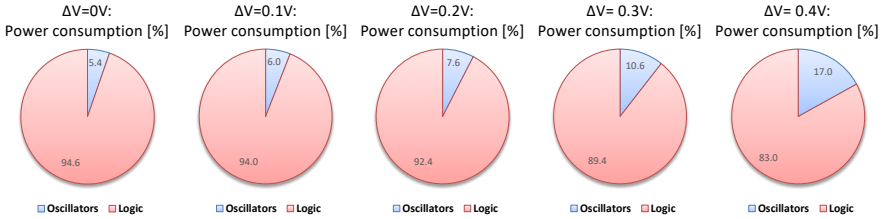

Fig. 15. Power consuption distribution among the oscillators and the logic counterparts for different header/footer bias voltages ΔV for V_{DD}=0.4V; M=32 and C_x=10 pF.

5 Conclusions

The fully-digital conversion time-power tradeoff of CDCs based on dual-mode logic has been investigated in this work. Dual-mode logic's tuning voltage allows for flexible operation across a variety of conversion time and power targets, allowing for the adaptation of the same architecture to many applications.
The experimental characterization of a 180-nm testchip has demonstrated that dual-mode logic tuning enables dynamic power adjustment from 418 pW to 1.37 nW. It is possible to cut the conversion time to a range of 50 ms. In other words, dual-mode logic enables the conversion time to be adjusted while power increases gradually. Measurements at 0.3-V supply show that the CDC can also function at extremely low voltages.
The CDC is suited for directly-harvested devices with no intermediary DC-DC conversion and an extremely constrained power budget because of its capability to operate at nW (or sub-nW) power at voltages as low as 0.3 V. Additionally, the CDC's ability to function at any voltage between 0.3 and 1.8 V negates the requirement for voltage regulation. Furthermore, the CDC maintains true nW-power operation at the system level without requiring any extra support circuitry for voltage/current references.

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