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Dead-Time Effect on Two-Level Grid-Forming Virtual Synchronous Machines

Vincenzo Mallemaci, *Student Member, IEEE*, Fabio Mandrile, *Member, IEEE*, Enrico Carpaneto, *Member, IEEE*, and Radu Bojoi, *Fellow, IEEE*

Abstract—The concept of Virtual Synchronous Machine (VSM) is a promising solution to integrate renewable energy sources into the grid. Thanks to this approach, renewable energy sources can provide grid services (e.g., inertial behavior), grid support during faults and island operation. Moreover, VSMs can enhance the voltage quality at the point of connection to the grid by behaving as harmonic and unbalance sinks under non-ideal conditions (i.e., grid harmonic distortion and unbalance). However, the inverter dead-time affects the harmonic and unbalance sink capability of grid-forming VSMs with no closed loop current control. Although the literature contains several papers concerning the dead-time issues, the negative influence of the switching dead-time on the harmonic and unbalance sink capability of VSMs has not been analyzed. Therefore, this paper demonstrates through experiments that: (1) the inverter dead-time effect limits the harmonic and unbalance sink capability of grid-forming VSMs under non-ideal grid voltage conditions and (2) a dead-time compensation is mandatory to make grid-forming VSMs behave according to the theoretical analysis. A first experimental test shows that both the dead-time and its compensation do not influence the VSM response under normal operating conditions (i.e., symmetrical and sinusoidal grid voltage). Next, two experimental tests under a 5% grid voltage unbalance and a 10% grid voltage fifth harmonic distortion validate the negative influence of the dead-time and the beneficial effect of its compensation.

Index Terms—dead-time, grid-forming, harmonic sink, unbalance sink, virtual synchronous machine

I. INTRODUCTION

ACCORDING to the recent grid codes, inverter-interfaced renewable energy sources (e.g., solar and wind) are required to provide grid services (e.g., inertial behavior, active and reactive power regulation), grid support during faults and island operation [1], [2]. Control algorithms based on the Virtual Synchronous Machine (VSM) concept can make power electronic converters behave as conventional synchronous machines (SMs), and provide the aforementioned grid services [3]–[5]. Moreover, VSMs can operate as harmonic and unbalance sinks, improving the voltage quality at the point of connection to the grid, i.e., the point of common coupling (PCC), through an harmonic current flow [1], [6]–[10]. Among the several VSM models available in the literature, grid-forming VSMs are wide-employed solutions to make the converter able to operate both in grid-connected and island configuration [2], [11]–[16]. Their main advantage compared to other solutions is their better capability to stably operate in case of weak grids [17], [18]. Many grid-forming VSMs

available in the literature provide the voltage reference v_i^* directly to the PWM modulator with no closed loop current control. However, when implemented on power hardware, the converter dead-time effect introduces a non-negligible voltage error between the reference and the actual voltage provided by the converter. Nevertheless, this error does not affect the VSMs performance under normal grid operating conditions (i.e., symmetrical and sinusoidal voltage), because the error is compensated by the power loop control of the VSMs. However, in case of non-ideal grid voltage conditions (i.e., voltage unbalance, harmonic distortions), the voltage error cannot be compensated because of the lack of a closed loop current control. Therefore, under non-ideal conditions, the inverter dead-time reduces the voltage imposed by the VSMs and their harmonic current flow, thus limiting their harmonic and unbalance sink capability.

In the literature, the dead-time issues have been widely studied both for electrical drives [19]–[23] and for grid-connected converters [24]–[27]. Papers [19]–[23] analyze the dead-time effect in three phase PWM inverters for drives application and propose different strategies to compensate for the dead-time. In [19], [20] the voltage reference for the PWM modulator is corrected by a constant term function of the dead-time, the switching frequency and the dc-link voltage. The effect of the turn-on and turn-off delay time is also considered in [20]. Paper [21] proposes a logarithmic compensation technique, based on the analysis of the real characteristics of the power switching devices. An adaptive dead-time compensation as a function of the operating point is described in [22]. In [23] a simple solution is proposed for the identification and compensation of the inverter voltage error with no need of information about the dead-time duration.

With reference to grid-connected applications, [24]–[27] propose small-signal models of grid-connected converters including the dead-time effect. More in detail, [24] presents a modified small-signal model of a voltage source converter, working both as inverter and active front end, that takes the dead-time effect and the non-linearities of the modulation technique into account. Paper [25] experimentally validates a small-signal model that includes the dead-time effect and the inverter current ripple influence. In [26] the stability analysis of voltage sources converters connected to weak grids has been investigated also considering the dead-time effect. Finally, [27] shows that the voltage error caused by the dead-time can be modeled with a dead zone, a slope, and a saturation limit as a function of the inductor current amplitude.

Although the literature contains several papers concerning

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the dead-time issues, the negative influence of the switching dead-time on the harmonic and unbalance sink capability of VSMs has not been analyzed. Therefore, the paper main contribution is the analysis of the dead-time effect on grid-forming VSMs, demonstrating through experiments that:

- The dead-time limits the harmonic and unbalance sink capability of grid-forming VSMs with respect to the theoretical behavior;
- The dead-time compensation is mandatory to make the harmonic and unbalance sink capability of grid-forming VSMs almost match the theoretical behavior;
- The dead-time compensation does not alter the normal operating condition of grid-forming VSMs.

The generality of the proposed study is demonstrated by considering it on two of the most representative grid-forming VSM solutions available in the literature, namely the Osaka model [12], [13] and the VISMA II model [14]. The results of this paper can be extended to other grid-forming VSMs, such as the first version of the Synchronverter [11]. The VSMs models have been implemented on a grid-tied two-level IGBT inverter connected to the grid through an LC filter, as depicted in Fig. 1.

This paper is an extended version of [28] and brings in additional value as follows:

- Experimental test (called Test 1) demonstrates that the dead-time and its compensation do not influence the grid-forming VSMs performance under normal grid operating conditions;
- Two experimental tests (Test 2 and Test 3) under non-ideal grid voltage conditions are performed with different values of dead-time and switching frequency;
- The unbalance and the harmonic sink capabilities of grid-forming VSMs are respectively evaluated through the calculation of the PCC voltage unbalance factor (VUF) (Test 2) and the Discrete Fourier Transform (DFT) of the PCC fifth harmonic voltage distortion (Test 3).

This paper is organized as follows. Section II describes the VSM models under study and the method used to foresee their theoretical behavior under non-ideal grid voltage conditions. Next, the theory of the dead-time effect and the employed dead-time compensation method are described in Section III. Section IV shows the experimental tests with and without dead-time compensation under ideal and non-ideal grid voltage conditions. Finally, Section V concludes the paper.

II. VSM MODELS

In general, most of the grid-forming VSMs available in the literature do not feature a closed loop current control. Indeed, these models generate a voltage reference v_i^* that is provided to the PWM modulator. This voltage reference v_i^* can be:

- Equal to the VSM electromotive force e_v , as happens for the Osaka model;
- Calculated as the difference between the VSM electromotive force e_v and the voltage drop on a tunable virtual impedance Z_v , as happens for the VISMA II model.

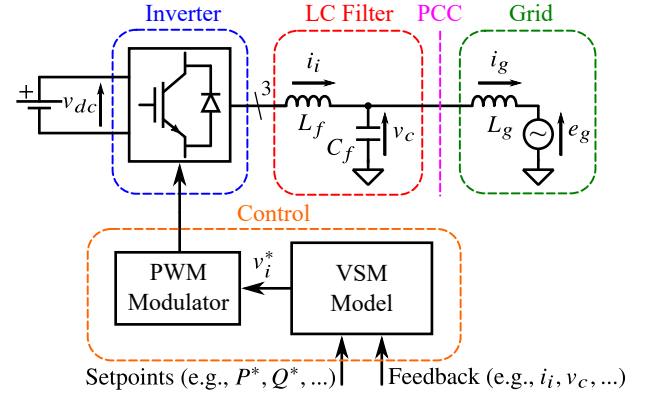


Fig. 1. Considered hardware for VSM implementations.

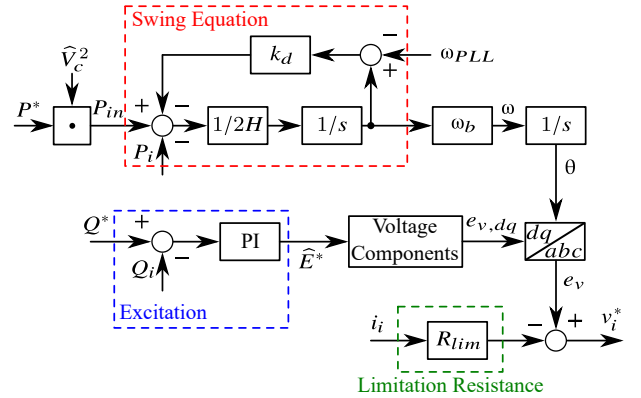


Fig. 2. Scheme of the Osaka model in the Laplace domain.

As already stated in Section I, the Osaka and VISMA II models are considered in this paper, as they are representative grid-forming VSMs available in the literature.

The scheme of the Osaka model is illustrated in Fig. 2. The swing equation is used to retrieve the VSM speed ω and the virtual angle θ . The amplitude of the virtual electromotive force \hat{E}^* is calculated by the excitation control, consisting of a PI controller. Finally, the three phase virtual electromotive force e_v can be obtained through the Park transformation. The limitation resistance R_{lim} is used to limit the current in case of faults. For the scope of this paper, R_{lim} is set to zero. Therefore, the voltage reference v_i^* is equal to the electromotive force e_v . The original scheme of the Osaka model embeds also the frequency and voltage droop control loops. As they are disabled for the purpose of this paper, they are not included in the scheme of Fig. 2. All the quantities are in per unit (pu), referred to the base values listed in Table I.

The scheme of the VISMA II model is depicted in Fig. 3, showing some differences with respect to the Osaka model. Indeed, the VISMA II model employs a modified version of the swing equation written in terms of torque to retrieve the virtual speed ω and consequently the virtual angle θ . The virtual electromotive force amplitude \hat{E}^* is directly set by the user (1 pu) and used to retrieve the three phase virtual electromotive force e_v . Next, as stated before, the voltage reference v_i^* can be computed as the difference between e_v and the voltage drop on a tunable virtual impedance Z_v (which

consists of a virtual resistance R_v and a virtual inductance L_v). The numerical derivative implies the use of a low pass filter (LPF) on the three phase current i_i . A complete description of the two models together with the parameter tuning procedure can be found in [4], [12]–[14].

The single phase equivalent circuit of connection between the VISMA II model and the grid is depicted in Fig. 4a, where Z_v is the tunable virtual impedance, L_f , R_f and C_f are, respectively, the inductance, resistance, and capacitance of the LC filter, L_g is the grid inductance and R_g is the grid resistance. For the Osaka model, the equivalent circuit is the same assuming a zero virtual impedance.

The theoretical behavior of the VSM models under non-ideal grid voltage conditions is studied according to the method proposed in [29].

In the (d, q) reference frame rotating at the fundamental frequency ω , the generic quantity \bar{x} can be written as follows:

$$\bar{x} = x_d + jx_q \quad (1)$$

where j is the imaginary unit, while x_d and x_q are the two components of \bar{x} on the d -axis and the q -axis, respectively.

Considering the circuit in Fig. 4a, the Kirchhoff's voltage law, in the (d, q) reference frame rotating at ω , is the following:

$$\bar{e}_v = (R_v + R_f)\bar{i}_i + (L_v + L_f)\frac{d\bar{i}_i}{dt} + j\omega(L_v + L_f)\bar{i}_i + \bar{v}_c \quad (2)$$

Assuming $i_i \approx i_g$ (i.e., capacitor current negligible), for the generic harmonic h , (2) becomes:

$$\begin{aligned} \bar{e}_v^h &= (R_v + R_f)\bar{i}_i^h + j(h+1)\omega(L_v + L_f)\bar{i}_i^h + \bar{v}_c^h \\ &= \underbrace{(R_v + R_f + R_g)}_{R_{eq}}\bar{i}_i^h \\ &\quad + j(h+1)\omega(L_v + L_f + L_g)\bar{i}_i^h + \bar{e}_g^h \\ &= \underbrace{(R_{eq} + jX_{eq}^h)}_{X_{eq}^h}\bar{i}_i^h + \bar{e}_g^h \\ &= (R_{eq} + jX_{eq}^h)\bar{i}_i^h + \bar{e}_g^h \end{aligned} \quad (3)$$

The equivalent circuit is shown in Fig. 4b. The virtual electromotive force e_v is zero for each harmonic $h \neq 0$ (h is zero for the fundamental frequency). Therefore, the harmonic current amplitude $|\bar{i}_i^h|$ can be computed as follows:

$$|\bar{i}_i^h| = \frac{|\bar{e}_g^h|}{\sqrt{R_{eq}^2 + X_{eq}^{h,2}}} \quad (4)$$

where $|\bar{e}_g^h|$ is the grid voltage amplitude of the harmonic component. In case of voltage unbalance $h = -2$, i.e., 100 Hz in the (d, q) reference frame. In case of fifth harmonic distortion $h = -6$, i.e., 300 Hz in the (d, q) reference frame.

These results are valid for the VISMA II model and also for the Osaka model, assuming $R_v = 0$ and $L_v = 0$.

Compared to other solutions available in the literature (e.g., grid-following VSMs), grid-forming VSMs can operate both in grid-connected and island operation. Moreover, they show a better capability to stably operate in case of weak grids [17],

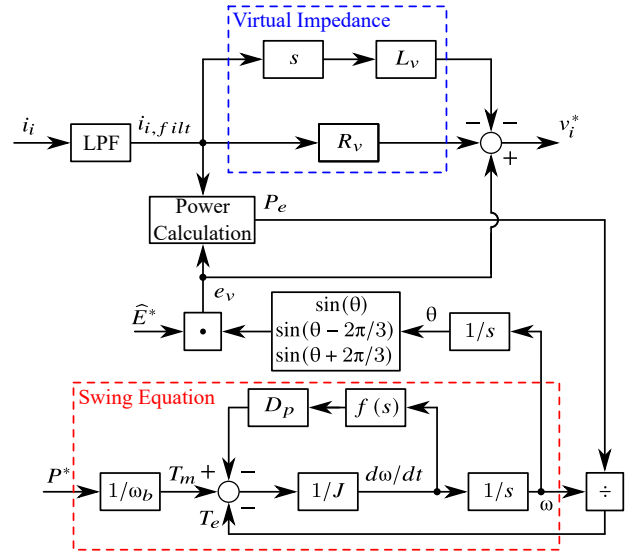


Fig. 3. Scheme of the VISMA II model in the Laplace domain.

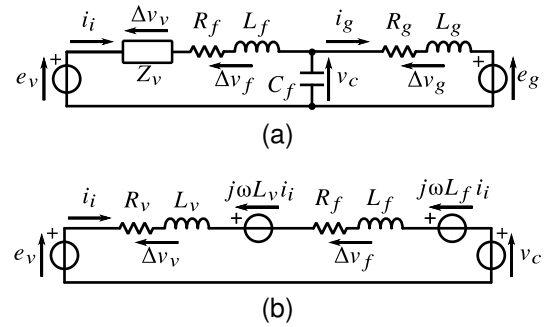


Fig. 4. (a) single phase equivalent circuit of connection between a grid-forming VSM and the grid; (b) equivalent circuit in the (d, q) reference frame rotating at ω .

[18]. However, the lack of a closed loop current control leads to two main disadvantages. First, they need a backup strategy to preserve the operation of the converter even during fault conditions [4], [30]. Second, under non-ideal conditions (harmonics or unbalance), their harmonic and unbalance sink capabilities are adversely altered by the switching dead-time. The dead-time does not affect their response at the fundamental frequency as it is compensated by the active and reactive loop controls. However, for a generic harmonic $h \neq 0$, the dead-time introduces a non-compensated voltage error on the voltage reference v_i^* , which reduces the actual current drawn by the inverter with respect to the theoretical value of $|\bar{i}_i^h|$, and thus the VSM harmonic and unbalance sink performance.

III. DEAD TIME EFFECT

In a two-level inverter, a dead-time t_d between the switching commands of the switches belonging to the same leg is necessary to avoid the leg shoot through during switching operation. Fig. 5 shows the scheme of a two-level inverter leg for the phase a , where $q_{h,a}$ and $q_{l,a}$ are the switches commands for the high switch and low switch, respectively. The dead-time generation is illustrated in Fig. 6, where T_{sw} is the switching period, v_{tr} is the triangular carrier signal

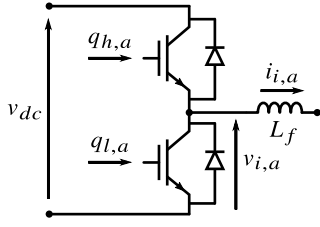


Fig. 5. Phase a leg of the IGBT inverter.

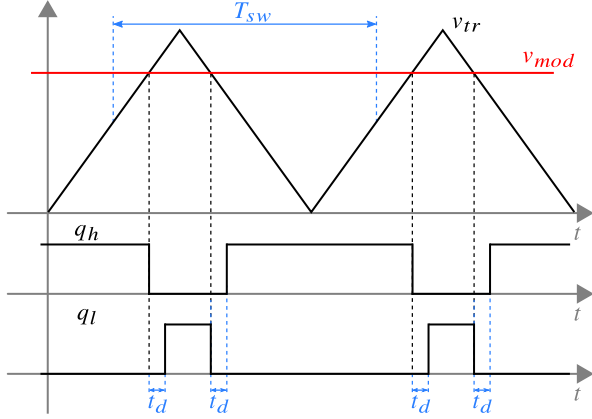


Fig. 6. Dead-time generation on the inverter control signals by the PWM technique.

and v_{mod} is the modulation control voltage. The dead-time introduces a non-linear phase voltage error v_d , expressed as follows [21]:

$$v_d = \frac{4}{3} t_d f_{sw} v_{dc} \text{sign}(i_i) \quad (5)$$

where f_{sw} is the switching frequency and $\text{sign}(i_i)$ is the sign function of the three phase inverter current space vector i_i in a stationary reference frame [21].

The dead-time effect can be observed on the output inverter voltage v_i . Fig. 7 shows the difference between the phase voltage reference $v_{i,a}^*$ and the moving average of the output inverter voltage $v_{i,a}$ for phase a . As a result of the dead-time, the inverter voltage waveform is distorted. The current zero crossing determines the sign of the voltage deviation from the reference value [19]. Moreover, to better appreciate the effect of the voltage error, the sign function can be represented in the (α, β) stationary reference frame and in the (d, q) reference frame rotating at the fundamental frequency ω [21]. The results are shown in Fig. 8a. On the d and q axes, a voltage error whose frequency is six times the fundamental frequency is added to the mean value. These errors slightly influence the performance of VSMs at the fundamental frequency. However, under non-ideal grid voltage conditions, to counteract negative sequence distortions (e.g., voltage unbalance, fifth harmonic), the inverter current sequence is negative as well. In such conditions, the sign functions appear as illustrated in Fig. 8b for the voltage unbalance and in Fig. 8c for the fifth harmonic distortion. It is evident that a non-negligible voltage error is present on both axes for these two cases. In case of voltage unbalance, an error two times the fundamental frequency appears on both axes. Moreover, the error on the d -axis has a

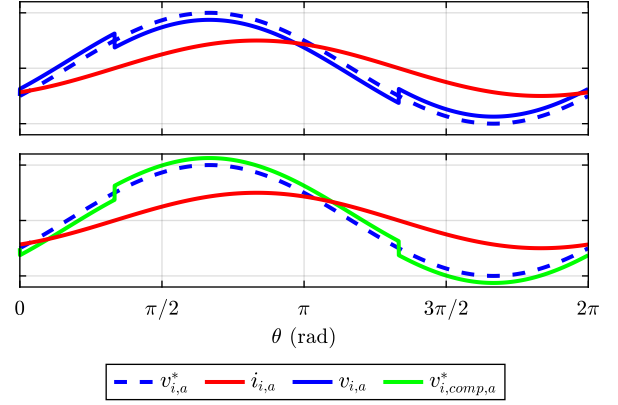


Fig. 7. Waveforms of the voltage reference v_i^* , the actual inverter current i_i , the inverter voltage moving average v_i and the compensated voltage reference $v_{i,comp}^*$ for phase a .

non-zero mean value. The same applies to the fifth harmonic distortion, with the difference that the error has a frequency six times the fundamental one.

As mentioned before, grid-forming VSMs cannot compensate for these errors because of the lack of a closed loop current control. Therefore, the dead-time compensation must be included to guarantee their harmonic and unbalance sink capabilities. Many dead-time compensation techniques have been proposed in the literature [19]–[23]. In this paper, the adopted method refers to [19], because it is one of the simplest solutions available in the literature. However, every technique proposed in the literature can be used as the analysis performed in the paper has general validity. According to [19], the average voltage deviation ΔV , caused by the cumulative of the dead-time pulses, is computed as follows:

$$\Delta V = t_d f_{sw} v_{dc} \quad (6)$$

The deviation ΔV can be used to compensate for the dead-time by modifying the three phase voltage reference v_i^* . The compensated three phase voltage reference $v_{i,comp}^*$ can be calculated as follows:

$$v_{i,comp,k}^* = \begin{cases} v_{i,k}^* + \Delta V, & \text{if } \text{sign}(i_{i,k}) > 0^- \\ v_{i,k}^* - \Delta V, & \text{if } \text{sign}(i_{i,k}) < 0^+ \end{cases} \quad (7)$$

where k indicates the phase (i.e., a , b or c). The compensated voltage reference waveform is shown in Fig. 7 for phase a .

IV. EXPERIMENTAL TESTS

The experimental setup is illustrated in Fig. 9. A three phase, two-level, IGBT inverter (IGBT power module MIXA40WB1200TED) is connected to a grid emulator through an LC filter. The grid emulator imposes the voltage e_g . The main data are collected in Table I, where R_f is the sum of the measured LC filter resistance and the ON resistance of the converter. The two VSM models have the same design parameters (e.g., virtual inertia, damping coefficient, etc.), tuned according to the procedure described in [4].

An initial test is performed to show the null effect of the switching dead-time on the normal VSMs operating condition.

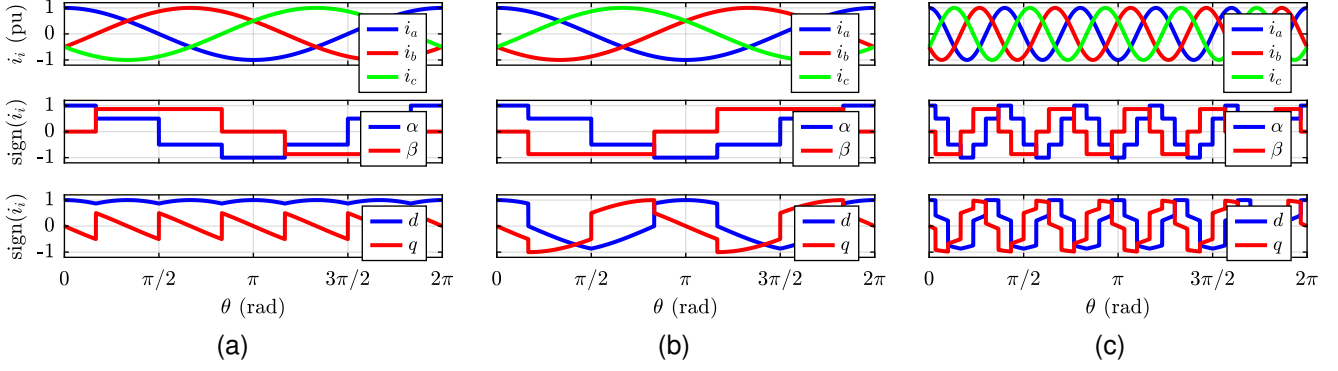


Fig. 8. From left to right: (a) direct sequence; (b) negative sequence; (c) fifth harmonic distortion. From top to bottom: three phase current i_i ; $\text{sign}(i_i)$ in the (α, β) reference frame; $\text{sign}(i_i)$ in the (d, q) reference frame rotating at the fundamental frequency.

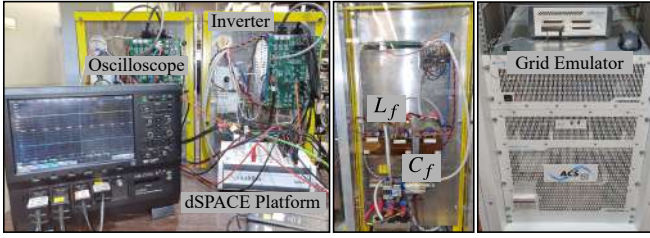


Fig. 9. Picture of the experimental setup.

TABLE I
EXPERIMENTAL SETUP AND VSM PARAMETERS.

Inverter		Base Values		
S_N	15 kVA	S_b	15 kVA	f_b 50 Hz
I_N	30 A	V_b	$230\sqrt{2}$ V	ω_b 314 rad/s
V_{dc}	650 V	I_b	30 A	L_b 33.7 mH
		Z_b	10.6 Ω	C_b 0.3 mF
Virtual Impedance		LC Filter		Grid
R_v	0.02 pu	R_f	0.024 pu	\tilde{E}_g $230\sqrt{2}$ V
L_v	0.15 pu	L_f	0.059 pu	R_g 0.009 pu
		C_f	0.017 pu	L_g 0.01 pu

Next, two experimental tests have been carried out to validate the negative influence of the dead-time on the harmonic and unbalance sink capability of VSMs and the beneficial effect of the dead-time compensation. The tests are the following:

- Test 1: active power reference step from 0.3 pu to 0.4 pu. This test shows the dynamic behavior of the VSM models if requested to change their power setpoint, such in case of a variation of the power generated by a renewable energy source connected to the dc side of the converter;
- Test 2: grid voltage e_g with 5% of negative sequence. The grid voltage can contain negative sequence, for instance, in case of asymmetrical faults;
- Test 3: grid voltage e_g with 10% of fifth harmonic distortion. In three phase systems, the fifth harmonic is typically generated by non-linear loads and it is the most dominant non-fundamental harmonic component.

For Test 2 and Test 3, the expected sink capabilities of the VSMs are respectively translated in the reduction of the voltage unbalance factor (VUF) and the fifth harmonic distortion on the PCC voltage $v_{c,II}$. The values chosen for the tests are arbitrary and sufficient to appreciate the effect of the dead-time and its compensation. Moreover, the active and reactive power references are set to 0 pu to focus only on the harmonic and unbalance sink behavior.

A. Test 1: Active power reference step

Test 1 is performed to demonstrate that the switching dead-time does not influence the VSM performance at the fundamental frequency, since the voltage error is compensated by the power loop control. The dead-time is set to 3 μ s and

the switching frequency is 10 kHz. The results of the test are illustrated in Fig. 10. Even without dead-time compensation, it can be observed that the power reference is properly tracked by both the Osaka model and VISMA II model with no steady-state error. Moreover, the dead-time compensation does not alter the steady-state operation of the VSMs, as shown in Fig. 10a. Therefore, the dead-time compensation can be enabled to guarantee the harmonic and unbalance sink capability, while preserving the VSM performance during normal operating conditions. Finally, the test is repeated with a dead-time of 1.1 μ s with and without compensation. The value of 1.1 μ s is the minimum dead-time recommended by the inverter manufacturer. The result is shown in Fig. 10b. Even in this case the VSM performance during normal operating conditions is preserved.

B. Test 2: 5% of voltage unbalance

Considering (4), the theoretical current peak values for Osaka and VISMA II are 20.12 A and 6.82 A, respectively. The results of the test are shown in Fig. 11 and summarized in Table II. During the first time interval of 100 ms, the dead-time compensation is disabled. It is evident that the current amplitudes are much lower than the expected values (1.77 A against the expected 20.12 A for Osaka and 1.62 A against the expected 6.82 A for VISMA II). Then, the dead-time compensation is enabled. After a transient, the current amplitudes reach the values of 19.88 A for Osaka and 6.62 A for VISMA II (against the expected 20.12 A and 6.82 A, respectively). They almost match the theoretical values,

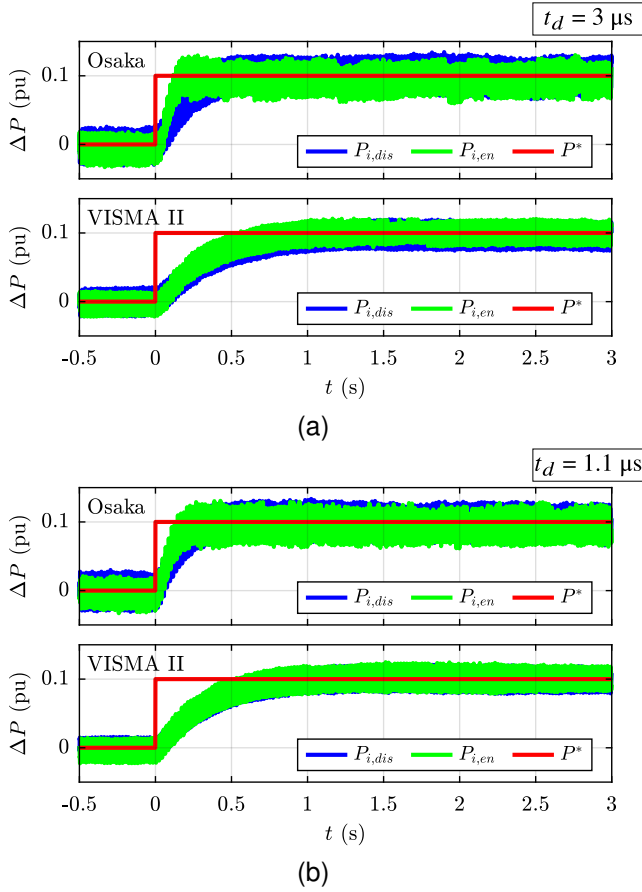


Fig. 10. Active power variation injected by the inverter after a reference step of 0.1 pu when the dead-time compensation is disabled ($P_{i,dis}$) and enabled ($P_{i,en}$): (a) $t_d = 3 \mu s$; (b) $t_d = 1.1 \mu s$.

demonstrating the validity of both the modeling method and the dead-time compensation. Next, Test 2 is repeated by reducing the dead-time value from 3 to 1.1 μs and the results are shown in Fig.12 and Table II. As expected, the negative dead-time effect is much lower than in the previous case, since the dead-time is reduced by a factor of circa 3. However, the dead-time compensation is still needed to match the theoretical value.

Finally, Test 2 is repeated by increasing the switching frequency at 15 kHz and 20 kHz, while the dead-time is set to 1.1 μs . The value of 20 kHz is the maximum switching frequency which guarantees a safety steady-state operation of the converter up to its nominal power. The results are illustrated in Fig. 13, Fig. 14 and Table II. The increase of the switching frequency leads to a reduction of the injected current without dead-time compensation, as the voltage error is proportional to it. In each test, the dead-time compensation makes the injected current almost equal to the theoretical one, demonstrating again the need to compensate for the dead-time. The VUF, defined in the standard EN 50160, is calculated for the PCC line to line voltage $v_{c,ll}$ to quantify the share of the negative sequence. When the VSM control is disabled, the VUF is equal to 5%. Table II shows the values of the VUF for all the tests, both without and with dead-time compensation. It can be observed that the increase of the injected current due to

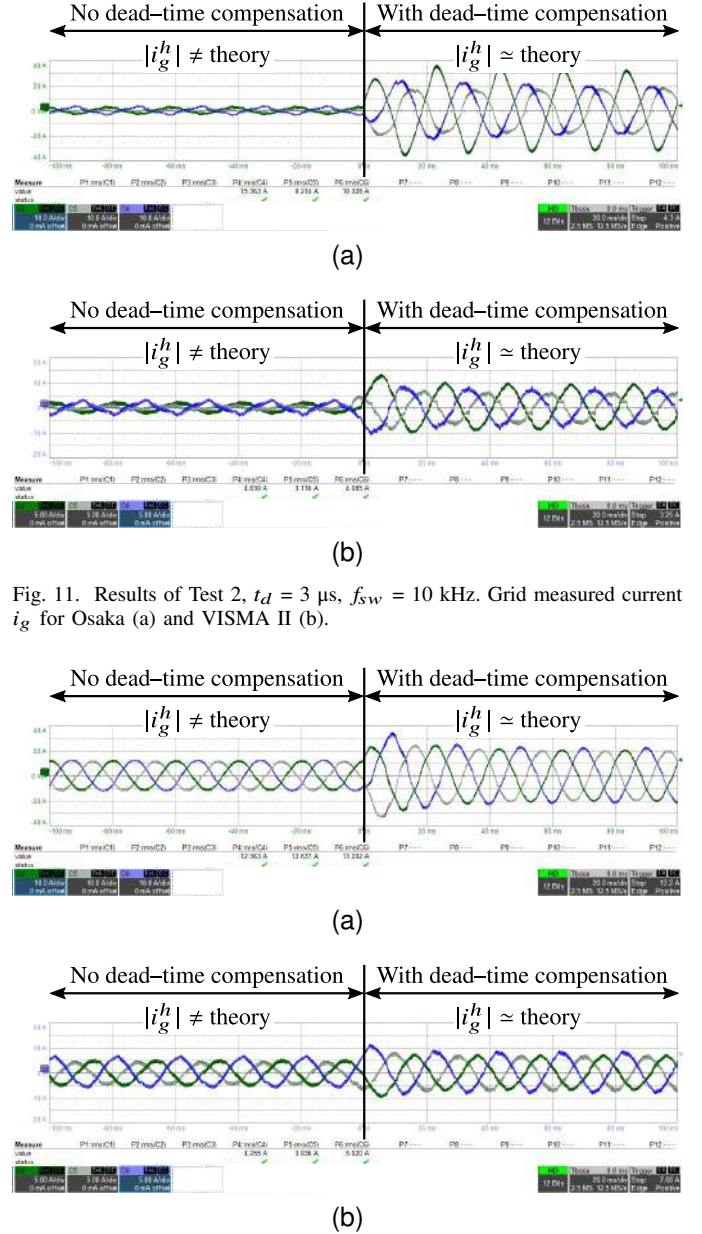


Fig. 11. Results of Test 2, $t_d = 3 \mu s$, $f_{sw} = 10 \text{ kHz}$. Grid measured current i_g^h for Osaka (a) and VISMA II (b).

Fig. 12. Results of Test 2, $t_d = 1.1 \mu s$, $f_{sw} = 10 \text{ kHz}$. Grid measured current i_g^h for Osaka (a) and VISMA II (b).

the dead-time compensation leads to a reduction of the VUF, thus demonstrating the need to compensate for the dead-time to enhance the unbalance sink capability of VSMs.

C. Test 3: 10% of fifth harmonic distortion

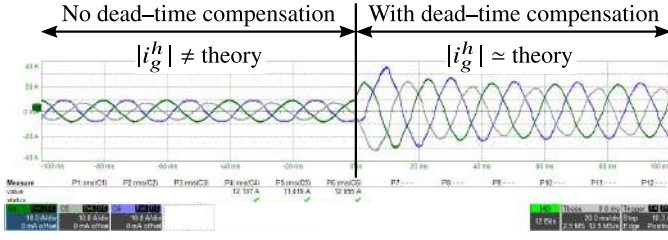
The results of the test are proposed in Fig. 15 and Table III. As in the previous test, in the first interval of 100 ms the dead-time compensation is disabled. The current amplitudes are lower than the theoretical values calculated by (4): 4.61 A against 8.86 A and 1.73 A against 2.80 A, respectively for Osaka and VISMA II. Then, the dead-time compensation is enabled and also in this case the current peak values almost match the theoretical ones (8.48 A against 8.86 A for Osaka and 2.66 A against 2.80 A for VISMA II). Even Test 3 is repeated for a different value of dead-time and switching

TABLE II
RESULTS OF TEST 2: 5% OF GRID VOLTAGE UNBALANCE.

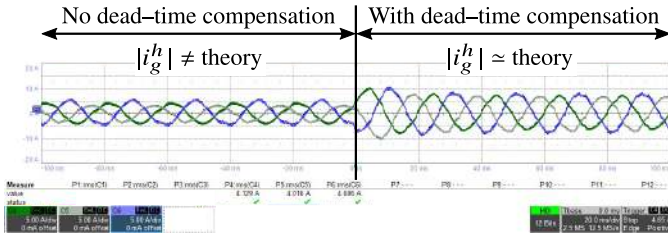
VSM	t_d (μ s)	f_{sw} (kHz)	$t_d f_{sw}$ (%)	No Comp.	$ \bar{i}_i^h $ (A) With Comp.	Theoretical	VUF (%) No Comp.	With Comp.
Osaka	3	10	3	1.77	19.88	20.12	4.84	4.13
	1.1	10	1.1	10.56	19.98		4.23	4.15
	1.1	15	1.65	7.70	20.09		4.37	4.10
	1.1	20	2.2	5.02	20.15		4.66	4.19
VISMA II	3	10	3	1.62	6.62	6.82	4.74	4.59
	1.1	10	1.1	4.79	6.72		4.69	4.67
	1.1	15	1.65	3.90	6.80		4.73	4.65
	1.1	20	2.2	3.10	6.89		4.82	4.58

TABLE III
RESULTS OF TEST 3: 10% OF GRID VOLTAGE FIFTH HARMONIC DISTORTION.

VSM	t_d (μ s)	f_{sw} (kHz)	$t_d f_{sw}$ (%)	No Comp.	$ \bar{i}_i^h $ (A) With Comp.	Theoretical	$ \bar{v}_{c,II}^h $ (V) No Comp.	With Comp.
Osaka	3	10	3	4.61	8.48	8.86	51.71	48.16
	1.1	10	1.1	7.30	8.61		48.12	47.70
	1.1	15	1.65	6.83	8.60		47.87	47.10
	1.1	20	2.2	6.39	8.68		48.35	47.00
VISMA II	3	10	3	1.73	2.66	2.80	55.63	53.74
	1.1	10	1.1	2.66	3.02		53.84	53.70
	1.1	15	1.65	2.55	2.98		53.33	52.86
	1.1	20	2.2	2.46	3.01		53.10	52.62

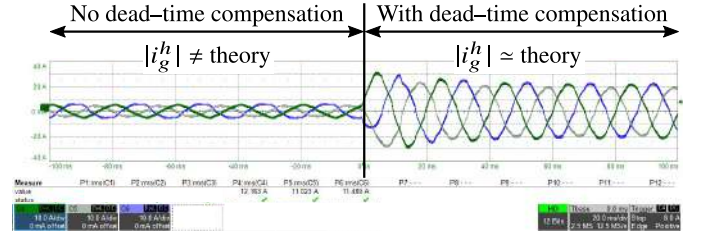


(a)

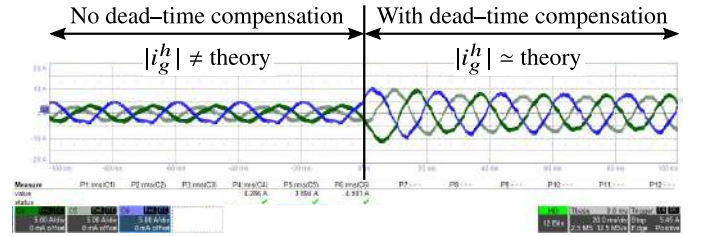


(b)

Fig. 13. Results of Test 2, $t_d = 1.1 \mu$ s, $f_{sw} = 15$ kHz. Grid measured current i_g for Osaka (a) and VISMA II (b).



(a)



(b)

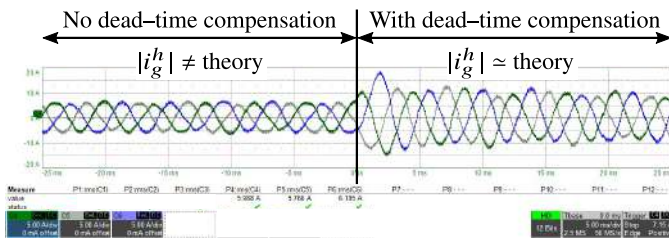
Fig. 14. Results of Test 2, $t_d = 1.1 \mu$ s, $f_{sw} = 20$ kHz. Grid measured current i_g for Osaka (a) and VISMA II (b).

frequencies. The results are shown in Figs. 16, 17, 18 and Table III. As expected, the lower the switching dead-time, the lower the current reduction with respect to the ideal case. On the opposite, an increase in the switching frequency implies a reduction of the current amplitude if the dead-time is not compensated. When the VSM control is disabled, the DFT of the PCC line to line voltage $v_{c,II}$ measures about 56 V on the fifth harmonic. The fifth harmonic voltage amplitudes $|\bar{v}_{c,II}^h|$ calculated for all the testing conditions are listed in Table III. It can be noted that the increase of the harmonic current flow due to the compensation reduces the fifth harmonic voltage distortion. Therefore, Test 3 demonstrates the validity

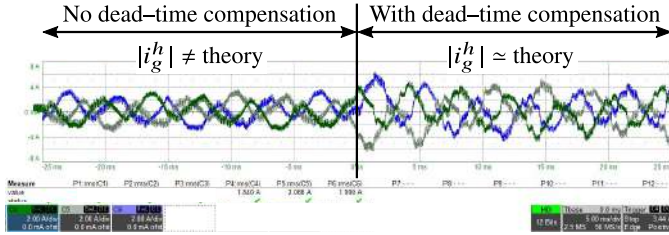
of the dead-time compensation in enhancing the harmonic sink capability of VSMs.

V. CONCLUSION

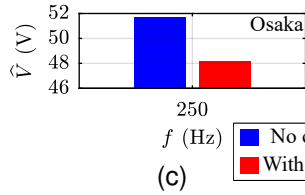
Grid-connected converters controlled as VSMs can enhance the voltage quality at the point of connection to the grid as they behave as harmonic and unbalance sinks. This paper highlights the limitation of the grid-forming VSMs performance caused by the switching dead-time. Two representative grid-forming VSM models available in the literature (i.e., Osaka and VISMA II) are tested against a 5% of voltage



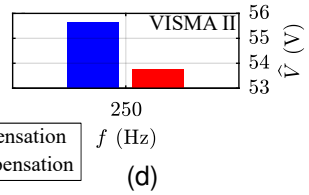
(a)



(b)

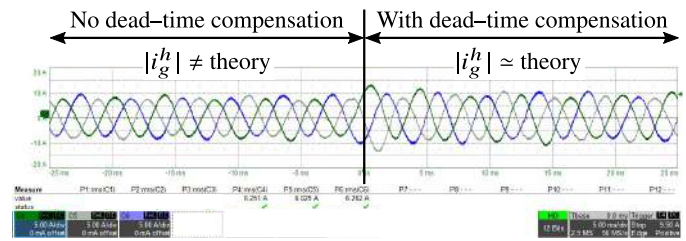


(c)

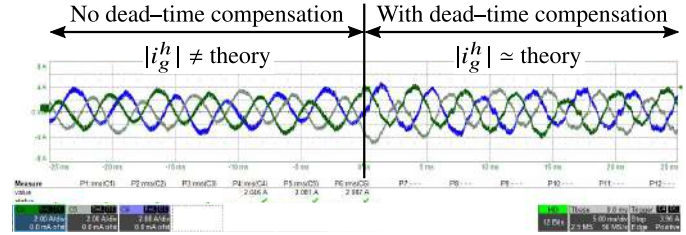


(d)

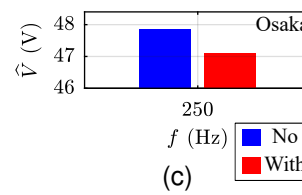
Fig. 15. Results of Test 3, $t_d = 3 \mu s$, $f_{sw} = 10$ kHz. Grid measured current i_g for Osaka (a) and VISMA II (b). Mean DFT of the PCC measured line to line voltage for Osaka (c) and VISMA II (d).



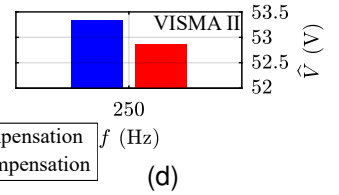
(a)



(b)

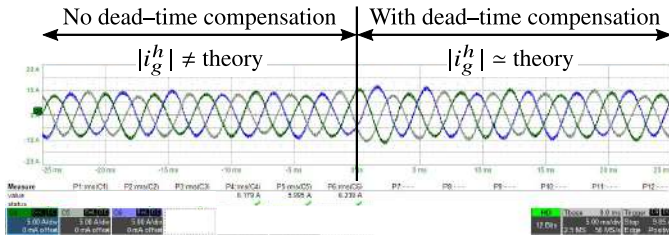


(c)

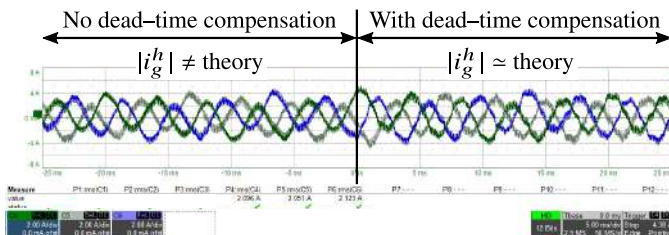


(d)

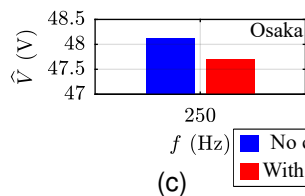
Fig. 17. Results of Test 3, $t_d = 1.1 \mu s$, $f_{sw} = 15$ kHz. Grid measured current i_g for Osaka (a) and VISMA II (b). Mean DFT of the PCC measured line to line voltage for Osaka (c) and VISMA II (d).



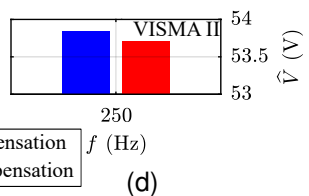
(a)



(b)

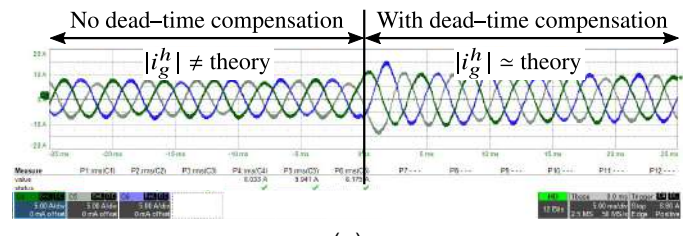


(c)

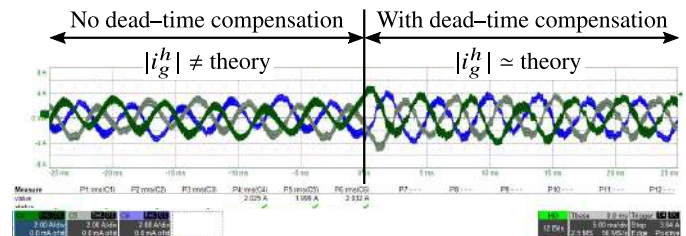


(d)

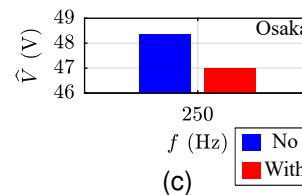
Fig. 16. Results of Test 3, $t_d = 1.1 \mu s$, $f_{sw} = 10$ kHz. Grid measured current i_g for Osaka (a) and VISMA II (b). Mean DFT of the PCC measured line to line voltage for Osaka (c) and VISMA II (d).



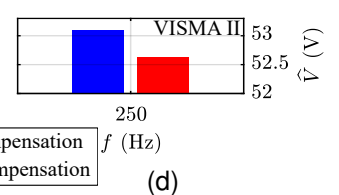
(a)



(b)



(c)



(d)

Fig. 18. Results of Test 3, $t_d = 1.1 \mu s$, $f_{sw} = 20$ kHz. Grid measured current i_g for Osaka (a) and VISMA II (b). Mean DFT of the PCC measured line to line voltage for Osaka (c) and VISMA II (d).

unbalance and a 10% of fifth harmonic distortion for different values of dead-time and switching frequency. With no dead-time compensation, the injected current is much lower than the expected one, thus limiting the harmonic and unbalance sink capabilities of the VSMs. Thanks to the dead-time compensation, the experimental results almost match the theoretical behavior expected by the foreseeing method. Moreover, the dead-time compensation leads to the reduction of the VUF and the fifth harmonic voltage amplitude with respect to the non-compensated cases, thus demonstrating the validity of the dead-time compensation in enhancing the harmonic and unbalance sink capability of grid-forming VSMs. Finally, it is shown that both the dead-time and its compensation do not alter the VSM behavior during normal grid operating conditions (e.g., active power injection and reference change). Therefore, this paper demonstrates that the dead-time compensation is mandatory to guarantee the harmonic and unbalance sink capability of grid-forming VSMs, while preserving their performance under normal operating conditions. The experimental validation has been performed focusing on the harmonic and unbalance sink capability of grid-forming VSMs considering zero active power injection. Future works will focus on control strategies to manage the sink capability of VSMs with non-zero active power injection.

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