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Improved Temperature Monitoring and Protection Method of Three-Level NPC Application Based on Half-Bridge IGBT Modules

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ABSTRACT The overheating stress of power devices is the main cause of converter system failures, so real-time temperature acquisition, as well as timely over-temperature protection, under various operating conditions are key to achieving a more reliable energy conversion. In this paper, an improved three-dimensional (3-D) coupled thermal model for insulated gate bipolar transistors (IGBTs) and related heatsink is constructed by considering the thermal coupling effects at both the device- and the module level. Furthermore, the coupled thermal impedance parameters are thereby extracted based on the finite-element method (FEM), so that the dynamic loss and transient temperature distribution under actual working conditions can be obtained based on this electro-thermal coupling model. Meanwhile, to avoid the overheating damage of power devices due to untimely action of the negative temperature coefficient (NTC) thermistor over-temperature protection, this article aims at the idle IGBT device in the three-level neutral-point clamped (NPC) application using IGBT half-bridge modules, combined with the emitter terminal temperature, and finally realizes the multiple over-temperature protection settings. The improved temperature monitoring methods proposed in this paper are realized by the drive and control circuits and verified through simulation and experimental results.

INDEX TERMS Reliability, half-bridge IGBT module, three-level NPC topology, temperature monitoring, over-temperature protection.

I. INTRODUCTION

As the core component, high-power Insulated Gate Bipolar Transistors (IGBTs) have been widely used in large-capacity converter systems, and the junction temperature (T_j) has become the most important factor that determines the reliability of power devices and the safe operation of the entire converter system. Taking the commercial IGBT module, the Infineon FF1400R17IP4, studied in this article as an example, the maximum limit of T_j (T_{j-op}) is 150°C [1]. This is the limit value that the average junction temperature of IGBT/diode chips should not exceed. Some severe fluctuations of T_j under extreme or sudden conditions will also lead to the damage of the IGBT module, such as the short-circuit operation [2].

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At the same time, in the process of device selection and thermal design, if a larger heat capacity is selected, it will cause additional device or heat dissipation costs. Therefore, it is of vital importance to quickly and accurately know the transient temperature distribution of the IGBT module and heatsink under various working conditions, such as rectifier, inverter, rated, overload, etc., as well as make timely and precise over-temperature alarms [3].

At present, some commercial high-power IGBT modules have the negative temperature coefficient (NTC) thermistor placed on the internal substrate, and even some converter manufacturers place a temperature sensor on the heatsink surface for temperature detection. However, the temperature of the NTC thermistor can only represent the temperature of the module substrate edge, and there also exists thermal grease between the substrate and the heatsink surface.

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Therefore, in practical applications, what users or researchers are really interested in is the real T_j of power chips, or how to obtain the transient thermal resistance or temperature difference between the power chip and the measurement reference point.

A. THE PURPOSE OF TEMPERATURE MONITORING

1) FOR OVER-TEMPERATURE PROTECTION

The purpose of temperature monitoring is simply to protect the semiconductors from operating above their thermal limits. The NTC thermistor in IGBT modules is designed for gradually increasing junction temperature situations, such as the increases in ambient temperature or low magnitude/long duration overloads. Therefore, by comparing the NTC temperature with a pre-determined set point at the design stage, the system faults caused by over-temperature can be avoided.

However, to find the reasonable over-temperature protection point of the NTC thermistor, it is necessary to get the real junction temperature of power chips. Because of heat conduction, there exists a temperature difference between the power chip and the NTC thermistor, which is the key to judging whether the IGBT module fails or not. Besides, the junction temperature of power chips may differ widely under different working conditions, which thereby causes great changes in NTC temperature. For example, the temperature of the same IGBT chip will be completely different under rectification and inverter working conditions. Therefore, to avoid the overheating damage of power chips due to untimely NTC protection, simply setting an NTC over-temperature protection point cannot guarantee real-time and effective protection under various working conditions [4].

2) FOR PERFORMANCE OPTIMIZATION

In the process of engineering design, taking the inverter as an example, for the safe and reliable operation of the equipment, the setting of the maximum current protection point is usually based on the most severe working condition and environment. For example, the maximum operating junction temperature is generally left at a 10-15°C safety margin. However, in actual operation, such a severe situation will not occur in most instances, and the resulting "overprotection" limits the maximum current output capacity of the inverter [5].

Taking the inverter for electric vehicles as an example, to achieve rapid start-up acceleration, it needs the inverter to output the maximum current in the start-up phase to provide a large motor torque. But due to the limitation of the maximum current protection point, the maximum output current cannot reach the ideal value. Besides, in most cases, the water-cooled heat dissipation condition of the inverter for electric vehicles is better than the designed heat dissipation requirement of about 65°C. Therefore, if the T_j of power devices can be obtained during the operation of the inverter, the maximum current protection value of the inverter can be thereby flexibly adjusted to achieve the best output performance.

3) FOR CONDITION MONITORING

For intelligent power modules, the current development trend of active gate drive technology is to integrate intelligent condition monitoring technology into the gate drive to assess in real-time the health condition of the converter system [3]. Therefore, obtaining the junction temperature T_j of the power devices can be used for further state monitoring. As a result, preventive maintenance can be performed by detecting the aging of the power devices and the abnormal operation of the converter system.

Take the research object of this article, the three-level NPC inverter based on IGBT modules, as an example [6]. When the inverter is equipped with a motor load for speed regulation, the current is large and the speed is low at startup, which will inevitably cause large junction temperature fluctuations. Therefore, for the frequently-started motor load conditions, it is necessary to monitor the transient junction temperature of the power devices in real-time to avoid excessive fluctuations of T_j during the startup process, which will cause power device failure if it exceeds the critical junction temperature.

4) FOR LIFE EVALUATION

There is an increasing requirement for the operating life and reliability of the converter system composed of power devices [7], especially the intelligent converters in some important applications, such as wind power generation with low output frequency, electric vehicles, elevators and robots with frequent motor acceleration and deceleration, and the servo motor with fast load changes. At present, the emerging trend of converter manufacturers is to study how to integrate the life assessment model into the equipment, so as to know the remaining life of the converter in real-time [8]. There are still many problems to be solved urgently in the practical application of reliability and life assessment models, but the basis and premise are to know the real-time junction temperature of power devices in the converter system.

B. EXISTING TEMPERATURE MONITORING METHODS

Due to the packaging characteristics of IGBT power modules, it is impossible to directly measure the junction temperature of power chips, so certain processing is required for the IGBT power module. There are many ways to obtain the junction temperature, such as the internal NTC thermistor mentioned above. It should be noted that the NTC in the IGBT module is designed for over-temperature detection of long-term overload conditions, but is not suitable for transient failures such as short-circuit. Because the response speed of the internal NTC thermistor in the IGBT module is basically in seconds, while faults like short-circuit usually occur in microseconds [9]. Although the NTC and the power chips are on the same substrate, there is a certain distance between them, so the junction temperature of chips cannot be obtained directly.

At the same time, physical contact measurement method can be adopted to place a thermocouple on the chip surface

after the package of the IGBT module is opened, and the T_j value of power chips can be thereby read through a data acquisition instrument. However, it is inevitable to destroy the module package to place the thermocouple, and the thermocouple wire installed on the chip surface will also affect the heat dissipation path of power chips, causing measurement errors. Besides, to avoid unnecessary personnel and instrument damage, it calls for attention to the potential or galvanic isolation between the data acquisition instrument and the thermocouple during the prototype test.

Some power modules integrate embedded temperature sensing diodes on power chips [10]. By utilizing the approximately linear relationship between the temperature and the forward voltage drop of the diode, the diode can be treated as a temperature sensor to provide an accurate junction temperature of the power chip. However, this method needs to be implemented in the production stage of the power module, which increases the cost and complexity of manufacturing and packaging, and this embedded on-chip temperature measuring diode reduces the overall active area of the junction and requires additional encapsulation ports.

There are two main methods for extracting the junction temperature of power modules that have been studied the most. First is the thermal sensitive electrical parameter (TSEP) method [11]–[13], which does not require intrusive modification of the power module, and directly uses the external electrical characteristics that are easy to measure to obtain the junction temperature. The TSEP method has received extensive attention from academia and industry, but it is hindered by the measurement sensitivity and the decoupling problem of interference terms, such as the aging fault characteristic parameters.

The other is the thermal impedance prediction model used in this article, which requires an accurate power loss model and a thermal impedance network model [14], [15]. By regarding the power device loss as the heat source, the extracted thermal impedance network can reflect the heat conduction between the key nodes, and the junction temperature of power devices can be deduced by thermo-electric coupling. The traditional RC thermal network model is mainly used for temperature estimation of power devices and converters, but it lacks accuracy when it comes to the thermal behaviors of key internal nodes and the thermal coupling between different internal components. At the same time, the finite element method (FEM) is often used to analyze the steady-state temperature distribution of power devices and converters, but the disadvantage is that FEM is not applicable in the analysis of the long-term load profile required for reliability evaluation and thermal optimization design [16]. To conclude, the above temperature acquisition methods are all summarized in Table 1:

Various fresh issues have been considered in current research on the thermal network model, such as thermal coupling effects between different layers inside IGBT module and boundary cooling conditions [17], thermal bonding between the IGBT module and the heatsink [18], and regarding the level information of devices as the same important input variable as the electrical load [19], etc. It is found in [20] that even cyclic junction temperature variations with low amplitude during normal operation may contribute to the aging process of a power module, even if it does not directly initiate a crack, which means that the stress concentration may have an impact on the thermal impedance changes. A multi-input and multi-output thermal network model of a press-pack IGBT device is established in [21] to simplify the calculation of some model parameters, but only the thermal coupling effect between chips is taken into account. To conclude, although various efforts have been made to calculate the junction temperature of the IGBT module and the converter system, there is still room for research in the improved junction temperature estimation method based on a multi-layer coupled thermal impedance model considering the device-level and module-level thermal coupling effects.

TABLE 1. Comparison between different temperature acquisition methods.

Methods	Characteristics	Evaluation (√=good, ×=bad)
Baseplate Sensor (T_{base})	Simple external sensors	√
	Significant error vs. $T_{j\text{-}Chip}$ (>20℃)	×
NTC thermistor (T_{NTC})	Requires module with NTC sensor	×
	Better accuracy than Baseplate	√
Thermocouple on chip surface	Destroyed module package	×
	Best accuracy of all methods	√
Finite Element Method	Requires complex model (full FEM characterization)	×
	Long simulation time and large calculation amount	×
	Better accuracy (approx. 5℃)	√
TSEP method	No intrusive modification	√
	Use the temperature dependencies	√
	Measurement sensitivity and decoupling problem	×
Extracted coupled thermal impedance model from FEM	Based on reference point temperature (T_{base} or T_{NTC})	√
	Maintain accuracy while avoiding slow simulation of FEM (<5℃)	√
	Implemented online without affecting the normal operation	√

The novel contributions of this paper can be summarized as: This article comes from the overheating failures of power devices in an actual converter system. The purpose of this article is to realize real-time temperature acquisition, as well as timely over-temperature protection, under various operating conditions. Most of the related existing literature only carried out independent modeling, instead of taking into account the overall thermal coupling phenomenon of the entire IGBT module and related heatsink system. Therefore, the advancement this article makes is the research in the improved junction temperature estimation method based on a multi-layer coupled thermal impedance model considering the device-level and module-level thermal coupling effects. At the same time, the unique research not found in other

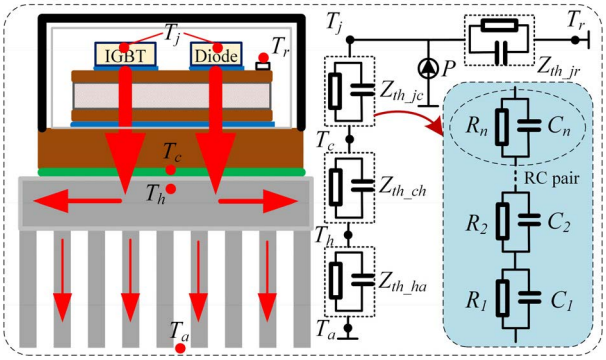

FIGURE 1. Heat conduction, key reference nodes, and multi-layer thermal network model of the IGBT module and related heatsink.

articles is that, combined with the idle IGBT devices in the hottest half-bridge IGBT module of NPC topology, multiple over-temperature protection settings are put forward in this article, which can be implemented online without affecting the normal operation of the equipment. The improved temperature monitoring and protection methods proposed in this paper are key to achieving a more reliable energy conversion.

The rest of this paper is organized as follows. Section II is the basic analysis of multi-layer thermal network and thermal coupling effects at different levels. Then section III builds the overall 3-D coupled thermal impedance network model, and describes how to obtain the coupled thermal impedance parameters, including the parameter extraction between internal chips, thermal grease, and IGBT modules. Simulation and experimental verification are carried out in section IV based on electro-thermal coupling, which proves the accuracy of the improved temperature estimation model. At the same time, the concept of multiple over-temperature protection is put forward and implemented in section V, which aims at the idle IGBT device in three-level NPC application using IGBT half-bridge modules and combined with the emitter terminal temperature. Finally, section VI summarizes the conclusion.

II. ANALYSIS OF MULTI-LAYER COUPLING THERMAL IMPEDANCE MODEL

A. MULTI-LAYER THERMAL NETWORK

The high-power IGBT module is composed of multiple layers of different materials, as shown in Fig. 1, and the IGBT and diode chips are plastic-encapsulated by injecting silica gel. Due to the poor thermal conductivity of silica gel, the heat generated by power chips is mainly conducted downward in the form of heat conduction and finally convection exchanged through the heatsink fins. The physical measurement methods mentioned in the above introduction can only roughly obtain the surface temperature of the IGBT module or the average temperature of the heatsink substrate, and cannot get the accurate T_j values of internal power chips. However, what really matters is the T_j of power chips, which means the PN junction temperature of power semiconductors and can only be obtained by indirect measurement or calculation.

As shown in Fig. 1, the multi-layer thermal network model composed of thermal impedances can simulate the heat conduction process, so using the thermal impedance network model is the most direct method to estimate the junction temperature of key internal nodes in the IGBT module and the heatsink. According to the electro-thermal analogy theory, the thermal resistance and the temperature is analogous to the resistance and the voltage respectively. By monitoring the equivalent thermal impedance network, the corresponding junction temperature information can be effectively obtained. Therefore, to calculate the steady-state and transient junction temperature of the IGBT/diode chips, it is necessary to obtain the thermal impedances between the power chips and the key reference nodes, which refer to the nodes that can directly measure the physical junction temperature, such as the NTC thermistor (T_r), the temperature sensor embedded in the substrate (T_c), and even the ambient temperature (T_a).

This article adopts the Foster thermal network instead of the Cauer model, considering that we are only interested in the temperature difference between set measurement points, without involving the heat transfer temperature difference between different material layers inside the IGBT module, including the thermal grease layer and bond wires. Besides, each layer of the thermal impedance is composed of multi-order RC units, which can be set according to the model needs. Usually, 4th-order RC units can simulate the real heat dissipation process, which is also the order in the datasheet provided by the IGBT module manufacturer. After knowing the power loss distribution, the accurate junction temperature values of the corresponding network nodes can be obtained by utilizing the built thermal impedance model.

B. ANALYSIS OF THERMAL COUPLING EFFECTS

Inside the IGBT module, in addition to IGBT power devices, there also exist freewheeling diodes in anti-parallel, to realize the bidirectional flow of energy. The junction area inside the IGBT/diode chips can be regarded as the heat source, and we consider that it is the equivalent resistance inside the chips that causes most of the power loss. Since the T_j of power chips can be regarded as the superposition of self-heating and the thermal coupling generated by surrounding chips, we cannot ignore the thermal coupling effects between different chips inside the IGBT module.

Fig. 2 (a) illustrates the equivalent device composition of the IGBT half-bridge module, which consists of four devices, namely the upper IGBT unit, the lower IGBT unit, the upper diode unit, the lower diode unit, and the NTC thermistor. Each power device is composed of multiple chips in parallel and distributed evenly on six DCB boards. As shown in Fig. 2 (b), there are four IGBT chips and two diode chips on each DCB, and two parallel IGBT chips can be regarded as an IGBT cell unit, as shown in Fig 2 (c). Therefore, the internal power chips of the IGBT module are divided into four cell units, namely T_1, D_1, T_2, and D_2.

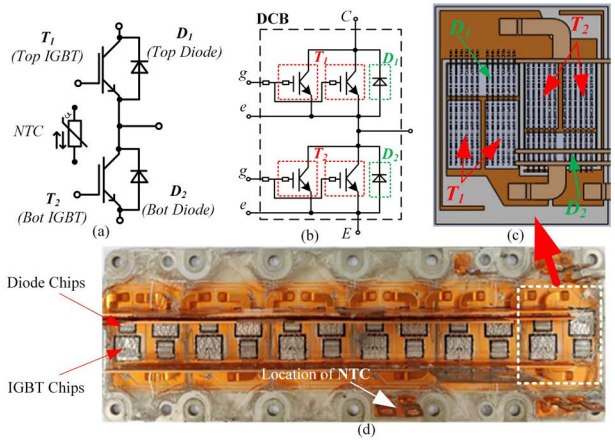

FIGURE 2. Internal structure of IGBT half-bridge module (a) Equivalent devices of IGBT module, (b) Equivalent devices on one DCB, (c) Single DCB structure, (d) Unpacking diagram of the IGBT module.

TABLE 2. Material thermal parameters of IGBT module.

Object	Material	Specific Heat (J/kg • K)	Density (kg/m^3)	Thermal conductivity (W/m • K)
Die	Silicon	705	2330	0/100/200℃ 168/112/82
Baseplate	Copper	384	8960	0/100/200 ℃ 401/391/389
Solder	SnAgCu	230	7400	57
Insulation	Al_2O_3	880	3800	35

The finite element method (FEM) is widely used in the design and reliability analysis of the power module and the heat dissipation system. Therefore, a commercial FEM analysis software (ANSYS Icepak) is used in this article to establish a three-dimensional (3-D) model of the IGBT module and the heat dissipation system, which can intuitively reflect the static and dynamic thermal behaviors. To conclude, this article utilizes the high-power neutral-point clamped (NPC) three-level inverter, which is composed of the common commercial IGBT half-bridge modules (the Infineon FF1400R17IP4) and the specific air-cooled heat dissipation system. By using the FEM method, the thermal impedance parameters can be thereby extracted to verify the accuracy of the established integrated thermal network model.

Aiming at the FF1400R17IP4 IGBT module, the geometric dimensions and thermal parameters of the IGBT module can be easily obtained through the Infineon official website. Therefore, the material thickness and thermal parameters of each layer in the IGBT module are shown in Table 2 [1]. It deserves mentioning that the temperature dependence is considered in the thermal conductivity of Silicon and Copper materials, which exhibit considerably lower conductivity at higher temperatures [17]. Besides, the physical model of the IGBT module established in the FEM software is shown in Fig. 3. It should be noted that the bonding wires

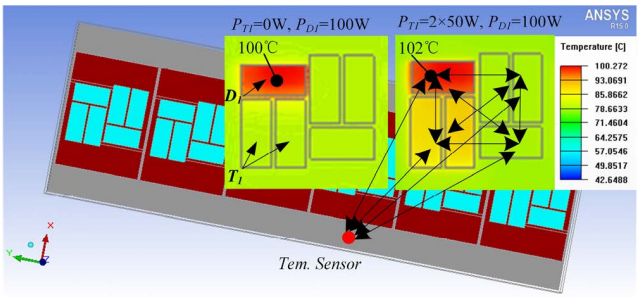

FIGURE 3. Finite element model of the IGBT module illustrating the thermal coupling effect between internal chips and the NTC.

in power modules have an influence on the temperature distribution [22], [23], but for the sake of simplicity and speeding up the FEM simulation, these geometric features are typically ignored. In the FEM software, the IGBT module is thermally simulated by setting different boundary conditions and thermal loads, so that we can obtain the temperature change curves of the power chips inside the IGBT module under different step power inputs.

When it comes to the boundary condition, it refers to the specific heat transfer coefficient for the heatsink. As shown in [22], a convection coefficient of 3000W/m^2·K is defined on the bottom to simulate as forced air cooling [17] and the rest surfaces are defined as 12.5 W/m^2·K in the FEM simulation. This is the boundary setting of merely IGBT module, however, when it comes to the whole FEM model of IGBT module and real heatsink with fans, there is no need to directly give the convection coefficient on the bottom to simulate as forced air cooling.

1) THERMAL COUPLING EFFECT BETWEEN DIFFERENT INTERNAL CHIPS

To begin with, the thermal coupling effect between different internal chips inside the IGBT module is analyzed, as shown in Fig. 3, we use arrows to represent the thermal coupling relationship between the four chip units and the NTC thermistor. To avoid the influence of the thermally conductive silicone grease and the heat dissipation path on the thermal coupling, the substrate temperature is set to a constant 80°C. When only 100W of P_{D1} is applied, the T_j of chip D_1 (T_{D1}) is 100°C, and when additional 2 × 50W of P_{T1} is increased, the T_{D1} becomes 102°C, which means that it is the thermal coupling effect of T_1 on D_1 that leads to the T_{D1} increase of by 2°C. Therefore, this simply and vividly illustrates the existence of the thermal coupling effect between different power chips.

2) THERMAL COUPLING EFFECT BETWEEN DIFFERENT IGBT MODULES

In addition, it is also necessary to take into account the thermal coupling effect between different IGBT modules, because multiple IGBT modules will share one heatsink in the high-power converter system to improve the power

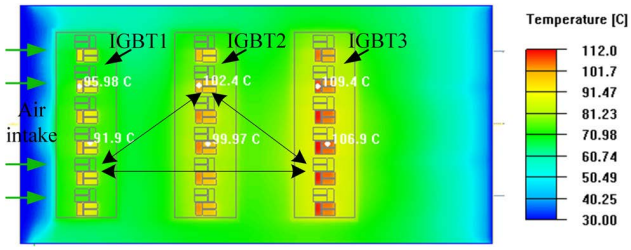

FIGURE 4. Finite element model of single-phase bridge arm illustrating the thermal coupling effect between different IGBT modules.

TABLE 3. Thermal parameters of heatsink and thermal grease.

Object	Material	Size (mm)	Density (kg/m^3)	Thermal conductivity (W/m • K)
Heatsink	Al	460×260×100 (L/W/H)	2800	237
Thermal Grease	Silicone	0.05 (Thickness)	2810	1

density. For example, each phase bridge arm in a three-level inverter consists of three IGBT half-bridge modules, which are all installed on the same heatsink, so there must exist heat transfer in the horizontal direction. This article uses the heatsink structure of the one-phase bridge arm and the installation method of power modules to construct a finite element model, as shown in Fig. 4. When the same thermal loads, 1500W, are applied to the three IGBT modules respectively, it can be seen from the horizontal temperature cloud that the average temperature of the IGBT3 module near the air outlet is the highest, which means that the IGBT3 module is most affected by the thermal coupling between different IGBT modules.

3) THERMAL COUPLING EFFECT BETWEEN DIFFERENT HEATSINKS

Last but not least, the influence of thermal coupling between different heatsinks is also not negligible when the distance between them is too close. Generally, the heat dissipation methods of high-power IGBT converters include water cooling, heat pipe, and forced air cooling, etc. [24]. This article uses the forced air-cooling system, where three low-power axial fans are placed at the air outlet of each phase heatsink. It should be noted that the type of axial flow fans is German EBM3214JH3, whose wind pressure curves can be obtained through the company's official website for thermal simulation analysis. To fully contact the IGBT modules and the heatsink, thermal grease is applied between them and fixed with bolts [25], [26]. The thermal parameters of the heatsink and the thermal grease are shown in Table 3.

Due to the relatively long distance between different heatsinks and the relatively uniform heat dissipation, the thermal coupling effect between different heatsinks is not considered in this article. However, when the heat dissipation method adopted by the IGBT module is more restricted by environmental conditions, such as smaller heat dissipation space, higher power density requirements, etc., the thermal coupling effect between different heat sinks cannot be ignored in those cases.

III. BUILDING OVERALL 3-D COUPLED THERMAL IMPEDANCE NETWORK

Most of the research by other scholars only carried out independent modeling, instead of taking into account the overall thermal coupling phenomenon of the entire IGBT module and related heatsink system. Therefore, studying the thermal coupling effects between different power chips and between different IGBT modules, and establishing a more accurate coupled thermal impedance model for junction temperature calculation will be the focus of this section.

A. MODEL ESTABLISHMENT OF OVERALL COUPLED THERMAL IMPEDANCE NETWORK

Because the IGBT module and the heatsink are analyzed and modeled as a whole in this article, the traditional temperature measurement points are no longer applicable. As long as the continuity of the thermal network model is ensured, the key locations can be determined as temperature measurement points according to actual requirements. Hence, we take the average temperature of the parallel chips inside the IGBT module as the junction temperature of the IGBT/diode chip (T_j), consider the bottom center of the copper substrate as the IGBT module temperature measurement point (T_c), regard the location directly below T_c point and 2mm away from the heatsink surface as the heatsink temperature measurement point (T_h) [26], as well as the NTC thermistor temperature at the substrate edge inside IGBT module (T_r).

1) COUPLED THERMAL IMPEDANCE BETWEEN INTERNAL CHIPS

Formula (1) is for the junction temperature calculation of Chipx ($T_{j(Chipx)}$) based on the real-time substrate temperature ($T_{c(refx)}$), considering the thermal coupling effects between different internal chips.

$$T_{j(Chipx)} = \sum_{y=1}^{4} \left(Z_{th-jc-xy} P_{Chipy}\right) + T_{c(ref\,x)} \tag{1}$$

Similarly, formula (2) is for $T_{j(Chipx)}$ based on the NTC thermistor temperature ($T_{r(refx)}$), as well as considering the thermal coupling effects between internal chips.

$$T_{j(Chipx)} = \sum_{y=1}^{4} \left(Z_{th-jr-xy} P_{Chipy}\right) + T_{r(ref\,x)} \tag{2}$$

where, $Z_{th-jc/r-xy}$ (x, y = 1, 2, 3, 4) represents the thermal coupling resistance of Chipy to Chipx based on different temperature reference points, and when $x = y$, it means the self-heating impedance of Chipx.

Therefore, we can obtain the coupled thermal impedance matrix $\mathbf{Z}_{th-jc/r-coupling}$ between internal chips:

$$\mathbf{Z}_{th-jc/r-coupling} = \begin{bmatrix} Z_{th-jc/r-11} & \cdots & Z_{th-jc/r-14} \\ \vdots & \ddots & \vdots \\ Z_{th-jc/r-41} & \cdots & Z_{th-jc/r-44} \end{bmatrix}$$

2) COUPLED THERMAL IMPEDANCE BETWEEN DIFFERENT IGBT MODULES

Formula (3) is for the temperature measurement point of the heatsink corresponding to the IGBTx module ($T_{h(IGBTx)}$) based on ambient temperature (T_a), considering the thermal coupling effects between different IGBT modules.

$$T_{h(IGBTx)} = \sum_{y=1}^{3} \left(Z_{th-ha-xy} P_{IGBTy}\right) + T_a \tag{3}$$

where, $Z_{th-ha-xy}$ (x, y = 1, 2, 3) represents the coupled thermal resistance of the IGBTy module to the IGBTx module, and when $x = y$, it means the self-heating impedance of IGBTx.

Therefore, we can obtain the coupled thermal impedance matrix $\mathbf{Z}_{th-ha-coupling}$ between IGBT modules:

$$\mathbf{Z}_{th-ha-coupling} = \begin{bmatrix} Z_{th-ha-11} & \cdots & Z_{th-ha-13} \\ \vdots & \ddots & \vdots \\ Z_{th-ha-31} & \cdots & Z_{th-ha-33} \end{bmatrix}$$

3) OVERALL COUPLED THERMAL IMPEDANCE NETWORK

Based on the above analysis, the overall coupled thermal impedance network model of the single-phase bridge arm in the three-level inverter can be established, as shown in Fig. 5. The established model is a 3-D thermal network model, which comprehensively considers various thermal coupling effects, therefore, the temperatures of defined measurement points in the established thermal model can truly reflect the temperature distribution of the whole heat dissipation system.

B. TO OBTAIN THE COUPLED THERMAL IMPEDANCE PARAMETERS

As mentioned earlier, three methods can be used to obtain the T_j of power chips to calculate the thermal impedance, namely the thermocouple, the infrared thermal imager, and the TSEP method, of which the pros and cons have been discussed. At the same time, the FEM as adopted above cannot be ignored, which can get the most direct and accurate temperature distribution. However, many problems do exist with the finite element method, such as the complex modeling and long simulation time. Therefore, to reduce the modeling complexity but ensure certain calculation accuracy at the same time, this article adopts the method of extracting transient thermal impedance curves from the FEM analysis and then obtaining the equivalent RC thermal network parameters through curve fitting.

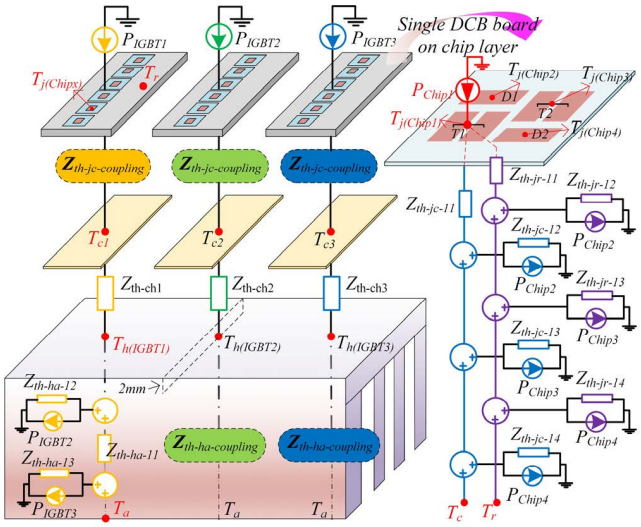

FIGURE 5. Overall coupled thermal impedance network model of the single-phase bridge arm in the three-level inverter.

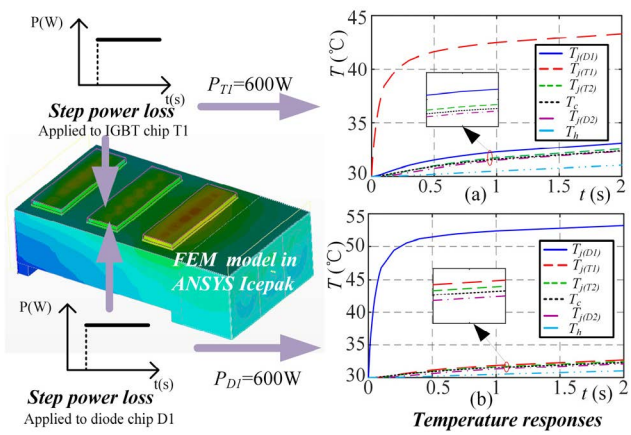

FIGURE 6. Temperature responses of monitoring points in FEM model (a) when P_{T1} = 600W, (b) when P_{D1} = 600W.

1) PARAMETER EXTRACTION OF COUPLED THERMAL IMPEDANCE BETWEEN INTERNAL CHIPS

As analyzed above, the temperature rise of the monitoring point is caused by the superposition of self-heating and the thermal coupling effect of adjacent power chips. Therefore, by separately applying 50W step power to the IGBT chip (T1) in the FEM software, the temperature response curves of monitoring points can be thereby obtained, as shown in Fig. 6 (a), including the self-heating temperature rise of T1 ($T_{j(T1)}$) and the thermal coupling temperature rise of T2, D1, and D2 ($T_{j(T2)}$, $T_{j(D1)}$, and $T_{j(D2)}$), as well as the substrate temperature of IGBT module (T_c), and the heatsink surface temperature (T_h). The ambient temperature is set to 30°C during the simulation. Similarly, when 50W step power is applied to the diode chip (D1) separately, the temperature rise curves of each monitoring point can also be obtained, as shown in Fig. 6(b).

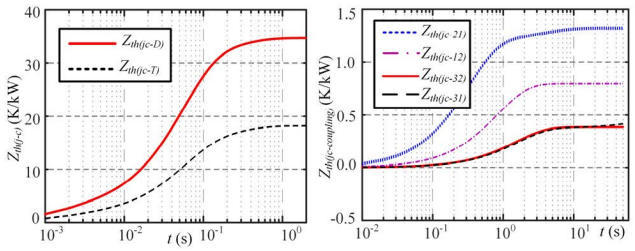

FIGURE 7. The coupled thermal impedance between internal chips (a) the self-heating impedance of D1 and T1 respectively, (b) the coupled thermal impedance arising from D1 and T1.

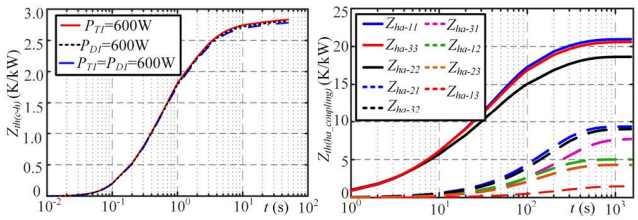

FIGURE 8. (a) The thermal grease impedance, (b) Coupled thermal impedance between different IGBT modules.

It should be noted that to verify the accuracy of the built coupled thermal model based on the datasheet provided by the IGBT module manufacturer, the substrate temperature T_c is used as the reference in this section, instead of the NTC thermistor temperature T_r, because only the $Z_{th(j-c)}$ is given in the datasheet, instead of the $Z_{th(j-r)}$, of which the reason has been explained above. But either way, the parameter extraction process of thermal impedance is consistent [28].

As shown in Fig. 6, the temperature response of the power chip is mainly caused by self-heating, and the thermal coupling between different chips has a relatively small effect but is still not negligible. This is because the power chip acts as a heat source and is closely attached to the substrate, while the distance between different chips is relatively large. As a result, the heat of the power chip is mainly conducted downward to the substrate, resulting in relatively large self-heating and relatively small thermal coupling.

Then, the coupled thermal impedance generated by Chipy can be obtained in (4).

$$Z_{th(jc-xy)}(t) = \left[T_{j(Chipx)}(t) - T_c(t)\right]/P_{Chipy} \tag{4}$$

where, x takes 1, 2, 3, and 4. Meanwhile, y takes 1 and 2, which represents T1 and D1 respectively. When x = y, it is the self-heating impedance of the IGBT chip T1 ($Z_{th(jc-T)}$), and of the diode chip D1 ($Z_{th(jc-D)}$) respectively. According to (5), and combined with the temperature responses in Fig. 6, the coupled thermal impedance curves between internal chips can be thereby obtained as shown in Fig. 7.

It should be noted from Fig. 6 (a) that the thermal coupling temperature rise $T_{j(D2)}$ on D2 generated by T1 turned out to be less than the substrate temperature T_c, which means that the thermal coupling effect between the two chips T1 and D2 can be ignored, that is, the coupled thermal impedance $Z_{th(jc-41)}$ can be set as zero. Similarly, the $T_{j(D2)}$ in Fig. 6 (b) is also less than T_c, so the $Z_{th(jc-42)}$ can also be regarded as zero. The above analysis shows that the thermal coupling effects between internal chips only exist between adjacent chips, and the thermal coupling between two chips in diagonal positions can be ignored. Finally, because of the symmetrical chip distribution on the DCB board, the coupled thermal impedance generated by the chips T2 and D2 can be obtained from the symmetrical relationship of T1 and D1.

As shown in Fig. 7, the self-heating impedance of the diode chip and the IGBT chip reaches steady-state value after about 200ms, respectively 34.4 K/kW and 18.2K/kW, which is similar to the typical value of the junction-case thermal resistance provided in the datasheet, respectively 32.5 K/kW and 15.5 K/kW. This comparison initially verified the accuracy of the extracted thermal impedance parameters.

2) PARAMETER EXTRACTION OF THERMAL GREASE IMPEDANCE

The thermal grease impedance $Z_{th(c-h)}$ between the IGBT module substrate and the heatsink surface is expressed in (5).

$$Z_{th(c-h)}(t) = \left[T_c(t) - T_h(t)\right]/P_{loss} \tag{5}$$

Combined with the temperature responses in Fig. 6, the $Z_{th-(c-h)}$ can be calculated as shown in Fig. 8 (a). We can see that the three thermal grease impedance curves under three different thermal load conditions are approximately coincident, so we believe in this article that $Z_{th(c-h)}$ has nothing to do with the loss distribution in the IGBT module. However, the influence of thermal grease aging on the change of thermal impedance parameters under the long-term mission profile cannot be ignored.

Because with the degradation of the thermal grease caused by the pump-out and dry-out phenomenon, the heat transfer path will be affected, so it is necessary to monitor the change of the thermal grease impedance. As proposed in [25]–[27], by utilizing the time constants of cooling curves, the degradation of thermal impedance can be monitored. It should be noted that this method is based on the Cauer thermal network model. However, this does not apply to this article, because of the Foster thermal network adopted in this article, we only need the measured temperature value of key measurement points, without considering the aging problem of packaging materials.

3) PARAMETER EXTRACTION OF COUPLED THERMAL IMPEDANCE BETWEEN IGBT MODULES

As shown in (6), to obtain the coupled thermal impedance $Z_{th(ha-xy)}$ between IGBT modules, 1200W thermal loads are applied to the three IGBT modules respectively, then the temperature responses ($T_{h(IGBT1)}$, $T_{h(IGBT2)}$, and $T_{h(IGBT3)}$) of the monitoring points (*h1*, *h2*, and *h3*) are recorded, and the heatsink-ambient coupled thermal impedance $Z_{th(ha-xy)}$ can

be thereby obtained, as shown in Fig. 8 (b).

$$Z_{th(ha-xy)}(t) = \left[T_{h(IGBTx)}(t) - T_a(t)\right] / P_{IGBTy} \tag{6}$$

We can see from $Z_{th(ha-xy)}$ curves in Fig. 8 (b) that the thermal impedance size corresponding to different IGBT modules is related to the relative position on the heatsink. When the same thermal loads are applied to the three IGBT modules, the middle IGBT2 module has the smallest thermal impedance, which means the best heat dissipation performance. In addition, the IGBT3 module near the air outlet is most seriously affected by thermal coupling, which is consistent with the previous analysis.

4) PARAMETER EXTRACTION OF FOSTER RC NETWORK

The more accurate transient thermal impedance parameters considering different thermal coupling effects are extracted above based on the finite element model. However, to directly use the thermal impedance to calculate the junction temperature in circuit simulation or practical application, it is necessary to mathematically fit the extracted transient thermal impedance curves of each thermal layer to extract the equivalent Foster RC network. As shown in (7), the n-order RC network can be fitted in the form of the sum of exponential functions [17], [18].

$$Z_{th}(t) = \sum_{i=1}^{n} R_{thi}\left(1 - e^{-t/R_{thi}C_{thi}}\right) \tag{7}$$

where, n represents the RC network order, R_{thi} and C_{thi} are the equivalent thermal resistance and thermal capacity respectively. By utilizing (7) to fit the transient thermal impedance curves of different layers, the required equivalent RC network can be thereby obtained, and the order of the RC network depends on the required fitting accuracy [19].

IV. SIMULATION AND EXPERIMENTAL VERIFICATION BASED ON ELECTRO-THERMAL COUPLING

The coupled thermal impedance matrix, namely the Foster equivalent RC network, extracted in previous sections can be directly used for junction temperature calculation in any circuit simulator, such as PLECS, PSpice, etc., as well as the digital processor of the converter control board. Therefore, by building an NPC three-level inverter model based on the Simulink platform of MATLAB in this section, the coupled thermal network established above can be utilized to estimate the power loss and the junction temperature of power devices. At the same time, the online junction temperature calculation based on the electro-thermal coupling model can also be realized based on practical NPC three-level application [29]. The simulation/experimental parameters are set in Table 4.

A. SIMULATION VERIFICATION

The transient-state and steady-state junction temperature calculation method of the three-level IGBT inverter based on the electro-thermal coupling is shown in Fig. 9, where d_{1-12} are the on-state duty ratios of IGBT devices, and the temperature dependence of power loss calculation has also been taken into account. The loss of power devices consists of conduction loss and switching loss, of which the detailed calculation process can be found in [19]. By inputting the calculated loss values $P_{loss(IGBT)}$ and $P_{loss(diode)}$ into the foster thermal network model extracted above, the estimated junction temperature can be then calculated. Since unit power factor control is used during simulation, that is, only the active current is given, the losses of anti-parallel diodes D1-D4 are all approximately zero. Besides, the actual distribution diagram of power devices on the single-phase bridge arm can be found in Fig. 13.

TABLE 4. Simulation/experimental parameters.

Parameter	Value
Unit power factor control	PF=1
DC bus voltage U_{dc}	1800V
Fundamental frequency	50Hz
Switching frequency	1kHz
DC-side capacitance C	5000μF
Grid-side reactor L_s	0.7mH
Rectifier-side transformer	6kV/1kV
Inverter-side transformer	1140V/6kV
Pulse width modulation strategy	SVPWM
IGBT module	1700V/1400A Infineon (FF1400R17IP4)

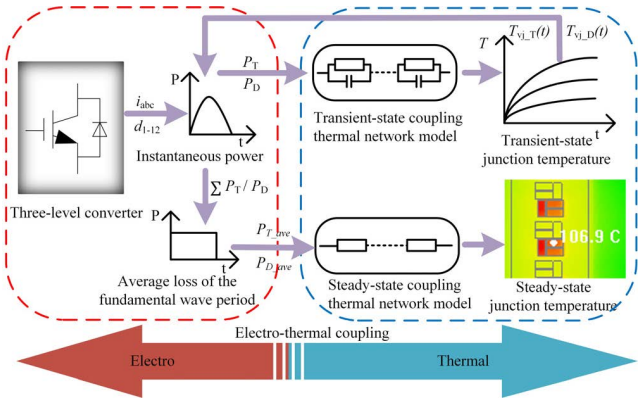

FIGURE 9. The junction temperature calculation method of three-level IGBT inverter based on electro-thermal coupling model.

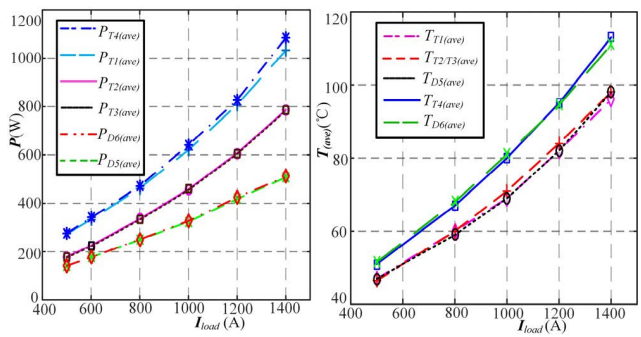

FIGURE 10. (a) The average loss at the fundamental cycle of each power device, (b) The steady-state junction temperature, at different load currents.

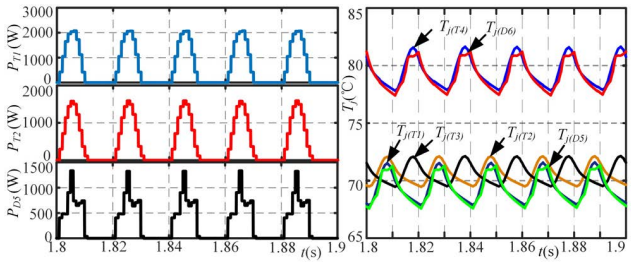

FIGURE 11. (a) The instantaneous power, (b) The resulting junction temperature fluctuation, at the load current I_{load} of 1000A.

We can simulate and obtain the average loss at the fundamental cycle of each power device, as shown in Fig. 10(a), and the steady-state junction temperature, as shown in Fig. 10(b), at different load currents (I_{load}). As can be seen from Fig. 10(a), as the load current increases, the increasing trend of power device loss becomes larger as well. By combining Fig. 10(a) and (b), we can conclude that even if the loss values of T4 and D6 are similar to those of T1 and D5 respectively, the steady-state junction temperature of them are both about 10°C higher. Therefore, due to the thermal coupling effects between IGBT modules, the junction temperatures of T4 and D6 tubes are the highest, and as the load current increases, the thermal coupling effect becomes more obvious.

Regarding the instantaneous power, namely the average loss in a single switching cycle, as shown in Fig. 11 (a), and the resulting transient junction temperature fluctuation, as shown in Fig. 11 (b), we take the load current I_{load} of 1000A as the example. Besides, because the corresponding power device losses of the upper and the lower bridge arms are very similar, we only take the T1, T2, and D5 tubes at the upper bridge arm as the research object. Due to the effect of thermal capacity in the transient thermal network model, it takes a certain time for T_j to reach steady. Therefore, to illustrate the fluctuation of the instantaneous power and the transient junction temperature, we directly select the 5 fundamental wave cycles near the steady-state for display. As can be seen from Fig. 11 that the periodic junction temperature fluctuation range of each device is within ±2.5°C, which arises from the periodic intermittent operation of power devices.

B. EXPERIMENTAL VERIFICATION

To verify the accuracy of the junction temperature estimation method based on electro-thermal coupling, we conduct a joint comparison and verification of Matlab platform simulation, ANSYS finite element model, and experimental measurement. By establishing the three-level inverter simulation model in Matlab, the loss value of each power device can be calculated, and then the loss data can be input into the finite element model in ANSYS Icepak software to obtain the temperature cloud chart, which can be compared and verified with the actual temperature measured by the experiment method.

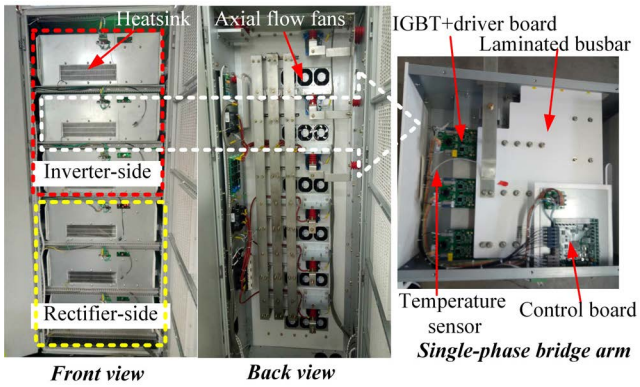

FIGURE 12. Experimental platform (1MW back-to-back three-level inverter).

As shown in Fig. 12, we take a 1MW back-to-back three-level inverter as the experimental platform and adopt the dual three-level mutual-feed experimental method for research. The experimental platform parameters are consistent with the simulation parameters in the previous section. On one hand, the rectifier side adopts double closed-loop vector control, which is mainly used for the DC bus voltage adjustment and the balance control of the neutral-point potential. On the other, the inverter side adopts open-loop control of voltage outer loop, which can test the electro-thermal characteristics of the inverter under different currents by changing the given value of active current on the inverter side.

Since the power devices are packaged in the IGBT module, the IGBT modules are installed on the same heatsink after being connected by the laminated bus bar, and each single-phase bridge arm adopts the pull-out closed structure, as shown in Fig. 12, so it is impossible to directly measure the internal temperature distribution of the converter system. Therefore, the following temperature measurement data at the monitoring points are all obtained through the temperature sensor or the thermal imager.

First of all, by setting the switching frequency f_{sw} to 1500Hz and giving three different active currents (I_{load}, namely 500A, 800A, and 1000A), the temperature at the heatsink fan outlet of the inverter can be captured by a thermal imager, and then compared with the finite element simulation result, as shown in Fig. 13. We can see that in all three cases, the temperature error between the thermal imager and the finite element simulation are all very small, within 2°C. The ambient temperature is set to 30°C in simulation, which is consistent with the actual situation during the experiment.

In addition, according to the location of the temperature monitoring point, the center of the heatsink substrate surface, we compare the measured value by the temperature sensor with the simulation value of the finite element model, which is 61.2°C and 61.85°C respectively, as shown in Fig. 14. The error between the two is also very small, within 1°C, proving the accuracy of the finite element modeling. It should be noted that the measured value by the temperature sensor is

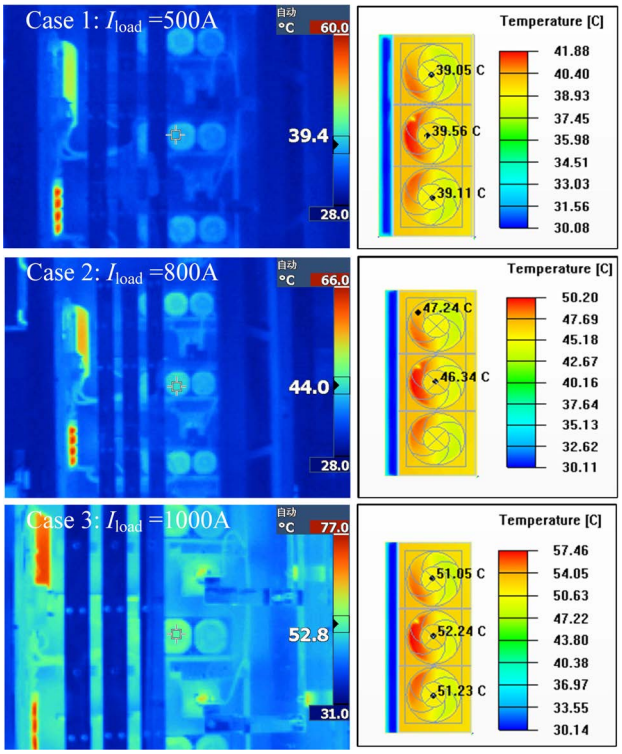

FIGURE 13. Temperature comparison at the heatsink fan outlet (the thermal imager vs. the finite element simulation) at different load currents (I_{load}, namely 500A, 800A, and 1000A).

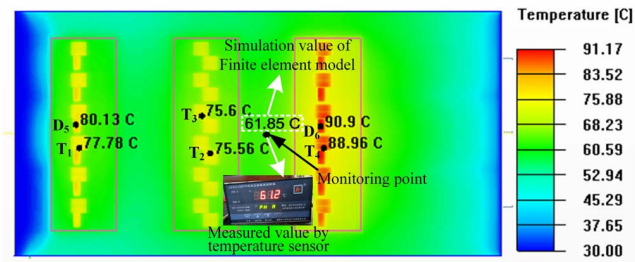

FIGURE 14. Junction temperature comparison at the monitoring point (the temperature sensor vs. the finite element simulation) at the load current I_{load} of 1000A.

directly displayed by an LD-B10-10DP dry-type transformer temperature displayer.

Finally, from Fig. 14, we can also get the junction temperature of each power device from the finite element model. At the same time, we have obtained from Fig. 10 the steady-state Tj values of power devices at I_{load} of 1000A based on extracted thermal impedance parameters. Therefore, we compare the device junction temperatures in Table 5, based on the finite element method and the established electro-thermal coupling model respectively. We can see that the errors between the two methods are around 1°C, which is within an acceptable range [30].

V. MULTIPLE OVER-TEMPERATURE PROTECTION SETTINGS

To avoid the over-temperature damage of the power devices during operation, it is necessary to set a specified maximum

TABLE 5. Comparison of device junction temperature (electro-thermal coupling model vs. finite element results).

Device	Loss/W	Junction Temperature/℃	
		Electro-thermal coupling model	Finite-element model
T_1	729	78.2	77.78
T_2	472	75.2	75.56
D_5	434	79.5	80.13
T_3	468	74.8	75.6
T_4	752	89.8	88.96
D_6	445	91.5	90.9

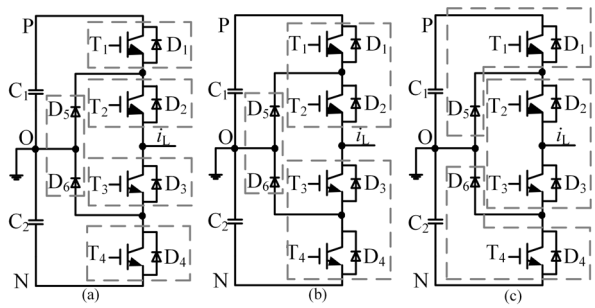

FIGURE 15. Three module combinations of single-phase bridge arm in NPC three-level topology (a) four IGBT discrete modules and one dual-diode module, (b) two IGBT half-bridge modules and one dual-diode module, and (c) two chopper modules and one IGBT half-bridge module.

junction temperature value, the so-called over-temperature protection point. It means that regardless of various operating conditions, the junction temperature of power devices cannot exceed the maximum value. Generally, the existing high-power IGBT modules equipped with NTC thermistor will all set the over-temperature protection point of the thermistor on the drive side. However, due to the distance between the NTC thermistor and the power chips, and the thermal conduction, it is often too late to respond to short-term over-temperature or temperature fluctuations. Therefore, to avoid the situation that power chips have been overheating damaged, whereas the NTC protection is not activated, simply setting an over-temperature protection point of the NTC thermistor cannot guarantee real-time and effective over-temperature protection under various working conditions.

A. DEVICE DISTRIBUTION OF THREE-LEVEL NPC TOPOLOGY USING IGBT MODULES

In the neutral point clamped (NPC) three-level topology using IGBT modules, each phase bridge arm is composed of four switching IGBT devices, four anti-parallel diodes, and two clamping diodes. When the clamping diode works, the phase voltage of that bridge arm is zero, so the phase voltages include three levels of P, O, and N in total. Because of the symmetrical structure of three phases in the three-level inverter, we take the A-phase as an example for analysis. To simplify the labeling, the four IGBTs and six diodes of the A-phase are labeled with T_1-T_4, and D_1-D_6 respectively.

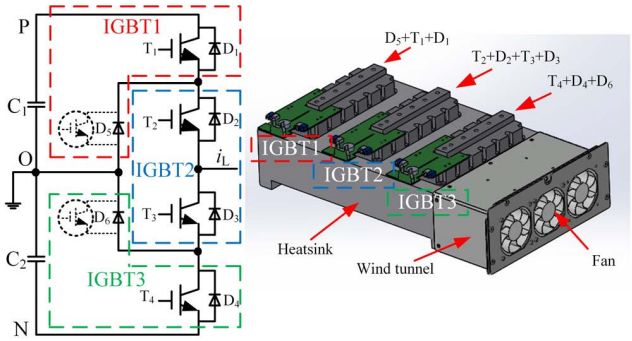

FIGURE 16. The actual distribution diagram of three IGBT half-bridge modules on the A-phase bridge arm in NPC three-level topology.

NPC three-level topology can be designed through different module combinations, and three types of single-phase bridge arm are shown in Fig. 15, including (a) four IGBT discrete modules and one dual-diode module, (b) two IGBT half-bridge modules and one dual-diode module, and (c) two chopper modules and one IGBT half-bridge module. Some emerging applications with low voltage levels, such as UPS and photovoltaic power, even directly use the IGBT full-bridge modules, that is, one module constitutes a single phase and three modules can form a three-level inverter. Its purpose is to reduce the turn-off over-voltage spike caused by stray inductance while simplifying the mechanical design, but the rated current cannot be too large, and the complicated internal circuit and the higher cost can also not be ignored.

In reality, taking into account the assembly convenience, the structure symmetry, and the replaceability of IGBT modules after failure, the medium and high power three-level NPC inverter manufacturers mainly adopt three same IGBT half-bridge modules to form the single-phase bridge arm. Fig. 16 shows the actual distribution diagram of three IGBT half-bridge modules on the A-phase bridge arm in NPC three-level topology, where each IGBT half-bridge module is composed of two IGBT/diode units. As a result, the clamping diodes D_5 and D_6 are replaced by the IGBT/diode units in IGBT1 and IGBT3 modules respectively, leaving two corresponding idle IGBT devices, and causing a waste of hardware resources.

It is worth mentioning that some existing manufacturers may choose to customize specific IGBT modules to avoid the problem of idle devices. Besides, for the three-level topology using IGBT half-bridge modules shown in Fig. 16, the active neutral point clamped (ANPC) topology structure is also a good solution, which has been commercialized by ABB company. However, we cannot ignore the resulting increase of the additional optical fiber channels used for control signal transmission and the increase of control difficulty for the controller. Anyhow, aiming at the widely used three-level NPC topology based on IGBT half-bridge modules, the idle IGBT devices provide the possibility of multiple over-temperature protection methods proposed in this section.

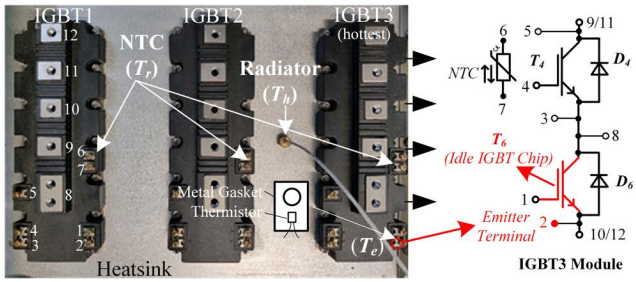

FIGURE 17. The schematic diagram of multiple over-temperature monitoring points and the terminal specification.

B. MULTIPLE OVER-TEMPERATURE PROTECTION

To begin with, the coupled thermal impedance parameters extracted in previous sections can be directly used for real-time T_j estimation of power devices in the digital processor of the control board, which is the basis of the device-level over-temperature protection. Next, according to the previous analysis, the IGBT3 module near the air outlet is most prone to overheating damage, and there exists an idle IGBT device corresponding to the clamping diode D_6 in the IGBT3 module, so we choose the auxiliary emitter terminal temperature of the idle IGBT device in IGBT3 module as a further means of over-temperature monitoring.

We take into account that the emitter terminal temperature of the idle device is only affected by the thermal coupling between different IGBT modules, and the thermal coupling with other power chips is negligible due to no self-heating of the idle IGBT chip and very thin auxiliary emitter bonding wire. As a result, we can achieve a more accurate response to temperature changes on the terminal and surface of the IGBT module. Last but not least, because the idle IGBT device is not working, no control signal flows through the emitter terminal, thereby avoiding problems of signal isolation and insulation withstand voltage of temperature measuring elements.

The schematic diagram of the multiple over-temperature monitoring points on the single-phase bridge arm of NPC three-level topology using half-bridge IGBT modules is shown in Fig. 17, where terminal 2 is the emitter terminal of the idle IGBT device, and the temperature measuring element includes the thermo-sensitive element and the metal gasket. The metal gasket is fixed on the emitter terminal to connect with the IGBT gate driver, and the thermo-sensitive element is fixed on the thin metal gasket, therefore, the temperature of the metal gasket with good thermal and electrical conductivity represents the temperature of the emitter terminal e.

To conclude, we establish the multiple over-temperature protection settings, including the heatsink substrate surface temperature (T_h), the NTC thermistor temperature (T_r), the emitter terminal temperature (T_e) of the idle IGBT device in hottest IGBT module, and the estimated junction temperature of power devices (T_j) based on electro-thermal coupling.

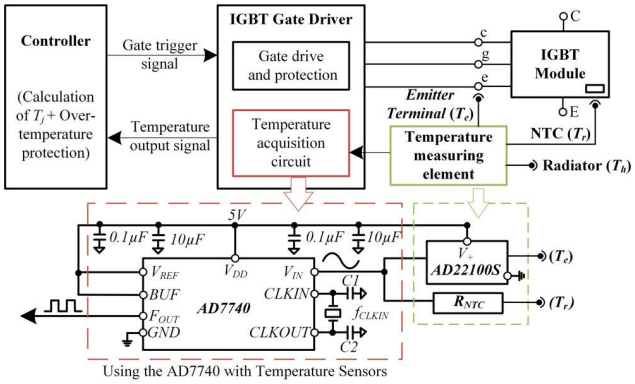

FIGURE 18. The implementation of multiple over-temperature protection.

C. IMPLEMENTATION OF MULTIPLE OVER-TEMPERATURE PROTECTION

The implementation of multiple over-temperature protection methods requires corresponding temperature measurement components, the temperature acquisition circuit integrated into the gate drive circuit, and the main controller, as shown in Fig. 18. The temperature measurement elements are used to measure the temperatures of corresponding reference points, the temperature acquisition circuit is used to collect the temperature signals output by the temperature measuring elements, and the main controller is used to send the gate trigger signal to the gate drive circuit, and at the same time receive the temperature acquisition signal sent by the gate driver, thereby performing junction temperature estimation and logic judgment for over-temperature protection. When the estimated T_j exceeds the set maximum withstand temperature, the controller sends a shutdown signal to the gate driver to realize multiple over-temperature protection functions.

In detail, the typical resistance-temperature characteristics of the NTC thermistor inside the IGBT module can be obtained from the datasheet provided by the manufacturer, so the resistance, namely the temperature value, can be obtained by obtaining the voltage on the NTC thermistor. In addition, the emitter terminal uses the AD22100S temperature sensor to give a digital temperature measurement, and its output voltage is proportional to the temperature multiplied by the power supply voltage (5V). Therefore, by feeding these two voltage outputs to the AD7740 voltage-to-frequency converter (VFC), the temperature value can be converted into the digital pulse train. As shown in Fig. 18, the AD22100S and the AD7740 both use the power supply of 5V (V_{REF}) and are fully decoupled by grounding 0.1μF and 10μF capacitors. For the analog input voltage V_{IN} of 0V-V_{REF}, it can be converted to $0.1f_{CLKIN}$-$0.9f_{CLKIN}$ through the VFC AD7740, which is based on charge balance conversion, and unbuffered mode is selected, so VIN input is from -0.15V to $V_{REF}+0.15$V. At the same time, an external COMS compatible clock, 1MHz crystal SiT8008, is used as the reference clock f_{CLKIN}, and C1 and C2 capacitors are used to ensure that the crystal does not exceed the base frequency over-oscillate. The conversion formula of VFC AD7740 is shown in (8).

$$F_{OUT} = 0.1\, f_{CLKIN} + 0.8\,(V_{IN}/V_{REF})\, f_{CLKIN} \tag{8}$$

As supplementary, among the multiple over-temperature protection methods, the heatsink surface temperature (T_h) is directly output to the display on the inverter shell, as shown in Fig. 14, for the operator's visual judgment. At the same time, the temperature acquisition circuit is easy to integrate into the gate drive circuit, so the collected temperature signal can be uniformly coded with the short-circuit fault signal or can be transmitted in a single channel, and as a result, an additional optical fiber port is needed to transmit the temperature signal. After transmitting the temperature signals to the controller, the T_j of power devices can be calculated based on the RC transient coupled thermal impedances, and at the same time, the logical judgment of over-temperature protection can be also made according to the maximum withstand temperature. It should be noted that the value of the maximum withstand temperature should be determined based on the datasheet of the IGBT module and the actual situation, and to get rid of "overprotection", the safety margin of set temperature protection points can be flexibly adjusted between 5°C and 15°C according to the estimated real-time junction temperature of power devices.

D. THE GENERALITY OF THE PROPOSED METHOD

As described in the introduction part, the overheating stress of power devices is the main focus, so real-time temperature acquisition and timely over-temperature protection are key to reliability for any power electronic device. Therefore, the improved 3-D coupled thermal impedance model for temperature estimation proposed in this paper is of great significance and value. Even if this paper uses the example of a three-phase three-level NPC topology based on half-bridge IGBT modules, the proposed method can be applied to other semiconductors and circuits as well. Though the reference of the built model is the module-integrated temperature sensors, it can also be based on other external sensors (e.g. on the baseplate or heatsink). It means that the generality of the proposed thermal model can be guaranteed as long as the reference measurement points are determined accordingly. What really matters is that the temperature calculation method can be implemented using any digital processor on a converter control board, which applies to any converter system.

At the same time, it deserves mentioning that it's possible to calculate the junction temperature based on the reference measurement points, but the accuracy depends on the characterization level which the designers can undertake during the device design process. Therefore, a detailed coupled thermal model defining transient thermal impedance matrix can be used for dynamic protection, and the timely over-temperature protection can be thereby realized by taking a high safety margin. In all cases, the authors would like to

emphasize that this method proposed in this paper is only valid for a particular converter design, which means that it is necessary to extract related parameters to build the thermal model in advance at the design stage when this model is applied to other applications.

VI. CONCLUSION

In this article, the high-power three-level NPC inverter based on half-bridge IGBT modules with specific heat dissipation structure is taken as the research object, and an improved multilayer 3-D coupled thermal impedance model is established to achieve fast and accurate junction temperature estimation based on electro-thermal coupling. While ensuring accuracy, the transient-state junction temperature distribution under actual working conditions can be quickly obtained and avoids the problems of long simulation time and large calculation amount of the finite element method. At the same time, combined with the idle IGBT devices in the hottest half-bridge IGBT module of NPC topology, multiple over-temperature protection methods are put forward in this article. The temperature acquisition circuit can be integrated into the gate drive circuit, and the over-temperature protection and junction temperature estimation methods can be all implemented online by the controller without affecting the normal operation of the equipment.

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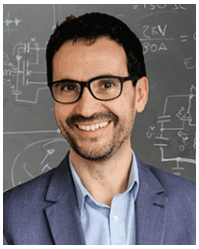

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