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Research Article

About v-i Pinched Hysteresis of Some Non-Memristive Systems

Dalibor Biolek,[1,2] **Zdenek Biolek**,[1,2] **Viera Biolkova**,[1] **Alon Ascoli**,[1,3] **and Ronald Tetzlaff**[1,3]

[1]*Faculty of Electrical Engineering and Communication, Brno University of Technology, Brno, Czech Republic*
[2]*Faculty of Military Technologies, University of Defence, Brno, Czech Republic*
[3]*Faculty of Electrical and Computer Engineering, Technical University Dresden, Germany*

Correspondence should be addressed to Zdenek Biolek; zdenek.biolek@gmail.com

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A special subset of two-terminal elements providing pinched hysteresis loops in the voltage-current plane with the lobe area increasing with the frequency is analysed. These devices are identified as non-memristive systems and the sufficient condition for their hysteresis loop to be pinched at the origin is derived. It turns out that the analysed behaviour can be observed only for just one concrete initial state of the device. This knowledge is conclusive for understanding why such devices cannot be regarded as memristors.

1. Introduction

The hysteresis loop pinched at the v–i (voltage-current) origin is the most widely known fingerprint of the ideal memristor introduced by L. Chua in 1971 [1] and also of the more general memristive systems [2], today referred to as the extended memristors [3].

In [4], L. Chua introduces a frequently cited terse thesis "If it's pinched, it's a memristor". Such a hyperbole reflects the fact that many devices, behaving as a resistor whose resistance depends on the state of associated dynamical networks, comply with the classical definition of the memristive system [2]. Examples are given in [5–7], where the circuits containing conventional nonlinear devices and linear accumulating elements are described which generate pinched hysteresis loops.

On the other hand, the above thesis can be a source of misunderstanding, particularly when insisting on its literal sense. The paper [8] presents a number of models of systems that, even if they are not of memristive nature, generate pinched hysteresis loops. The results from [8] are analysed in [9], claiming that the hysteresis loops of the memristive system must provide pinching at the v–i origin regardless of the parameters of the driving signal and the initial state of the system. It is argued in [9] that since the systems from [8] do not conform to all these conditions, their hysteretic behaviour cannot be interpreted as a manifestation of the memristive effect.

Other examples of non-memristive systems providing pinched hysteresis phenomena are given in [10], namely, the nonlinear inductor with a linear resistor in series and the nonlinear capacitor with a parallel linear resistor. These reactive elements are studied with quadratic nonlinearities and under sinusoidal excitation. It is demonstrated that the hysteresis loops are pinched at the v–i origin for all amplitudes and all frequencies of the driving signal and that their areas increase proportionally with the frequency, which violates the well-known fingerprint of diminishing hysteresis when the frequency tends to infinity [2]. That is why this phenomenon is referred to in [10] as "pinched hysteresis with inverse-memristor frequency characteristics". It is concluded therein that the existence of the pinched hysteresis loop is not the sufficient condition for identifying a memristor and that it is important to clearly identify what exactly the memristor is and in what sense it differs from other nonlinear systems. In the paper [11] the corresponding elements are already called the inverse memristors.

To illustrate the inconsistency of today's understanding of what is/is not a memristor, let us mention that, in contrast to memristors and memristive systems introduced in 1971 [1] and 1974 [2], the current classification of memristors

recognizes ideal, ideal generic, generic, and extended memristors [3]. In addition, the so-called second- or higher-order memristors [15] or the above inverse memristors [11] are also discussed. The possible confusion can be amplified by the frequently used notation of the memristor as the fourth fundamental circuit element [1]. Does it mean that all the above devices called memristors are the fundamental elements?

The question of the so-called new circuit elements, which can be considered as fundamental, is related to Chua's concept of predictive modelling [12]. The term predictive means the model's ability to predict the behaviour of the modelled subject in various modes of its operation. Chua showed that such models can be built from the predictive models of fundamental circuit elements organized in Chua's table [12]. Their models are in the form of unambiguous constitutive relations, which do not depend on the way the element interacts with the surroundings and on the initial state of the element. Each candidate for a "new element" should be put to the test whether it can or cannot be replaced with a combination of existing elements from Chua's table. If yes, then it is surely NOT a new element.

It is well known that the hysteresis loops of memristive systems [2] are also governed by other regularities, which should be taken into account when determining the type of the two-terminal device producing the hysteresis. For example, the ideal memristor driven by a signal modelled by an odd function of time must generate the odd-symmetric loops [16] whereas the loops of the extended memristors can be of both type I and type II (crossing type, CT, and non–crossing type, NCT) with a general order of touching at the v–i origin [17]. All memristive systems without any exceptions exhibit the fingerprint of a gradual [2] or sudden [18] disappearance of the hysteresis if the frequency of applied voltage or current increases above a certain limit, whereas the regularity of this disappearance depends on the concrete characteristics of the memristor [19]. The rule of homothety for ideal memristors, which is published in [20, 21], implies the rule of the quadratic increase in the loop area with increasing frequency if the memristor is driven by a charge or flux waveform of a fixed level.

This study suggests a methodology of identifying the devices exhibiting v-i pinched hysteresis loops that cannot be classified as memristors or memristive systems, or, more generally, as new fundamental circuit elements. In the first step, the classical definitions of the memristor and memristive system are confronted with the current classification of these devices from the point of view of Chua's concept of predictive modelling [12]. This approach will help in clarifying whether the analysed device is a fundamental circuit element. As a demonstration, the devices with the inverse-memristor frequency characteristics are analysed. A more general class of nonlinear inductors and capacitors with the "inverse-memristor pinched hysteresis" than those in [10] is identified. The differences with regard to the loops of the memristive systems are highlighted, and the mechanism explaining why the loop area increases with increasing frequency is revealed. All these new pieces of knowledge can be used for a correct identification of the so-called inverse memristors.

2. Fundamental Elements, Memristors, and Memristive Systems

As follows from a comparison of the original and current classification of memristors and memristive systems in Figures 1(a) and 1(b), the latter is governed by the thesis "If it's pinched, it's a memristor".

Figure 1 illustrates the well-known fact that the notation "memristive system" disappeared in the new classification, and the terms "memristor" and "memristive system" defined in [1, 2] were replaced by "ideal memristor" and "extended memristor". In addition, two new intermediate categories, namely, "ideal generic memristor" and "generic memristor", were introduced [3]. It is important to stress the conflict hidden in the new classification, when some elements are called memristors, but concurrently they are not fundamental elements. Since the ideal generic memristors and ideal memristors introduced in [1] are equivalent in terms of their v-i behaviour [15], they can be considered as the fundamental circuit elements with the (-1, -1) coordinates in Chua's table of Higher-Order Elements [22] or the equivalent storeyed structure [23] in Figures 2(a) and 2(b). However, this is not generally true for the generic and extended memristors. The above conflict may give rise to endeavours to introduce additional new circuit elements and denote them as various kinds of memristor.

It is important to define the memristor as a fundamental circuit element from Chua's table, which contains the elements from the well-known Chua's quadrangle and also from Wang's triangular table [24]. Then the respective conclusions may be acceptable to a wide community of researchers independently of what they prefer, whether Wang's triangle or Chua's quadrangle.

The ideal generic memristors as fundamental elements in Figure 1(b) can be defined via their well-known port and state equations [3].

Current-controlled ideal generic memristor:

$$\begin{aligned} v &= R_M(x)\, i, \\ \frac{dx}{dt} &= f(x)\, i \end{aligned} \tag{1}$$

Voltage-controlled ideal generic memristor:

$$\begin{aligned} i &= G_M(x)\, v, \\ \frac{dx}{dt} &= g(x)\, v \end{aligned} \tag{2}$$

Here v, i, x, R_M, G_M, $f()$, and $g()$ are memristor voltage, current, and state variable, state-dependent memristance and memductance, and generally nonlinear piecewise-differentiable functions.

For $f(x) = 1$ or $g(x) = 1$, the state variable x is the charge or flux for (1) or (2), and the above definitions then model the original memristors from [1], currently classified as ideal memristors:

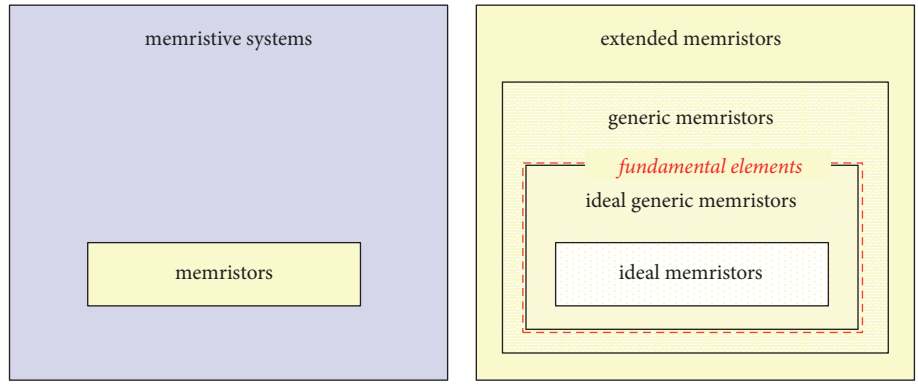

Figure 1: (a) Original classification of memristors as a special case of memristive systems according to [1, 2]; (b) current classification according to [3]: there are no memristive systems, only memristors; however, not all of them are the fundamental elements.

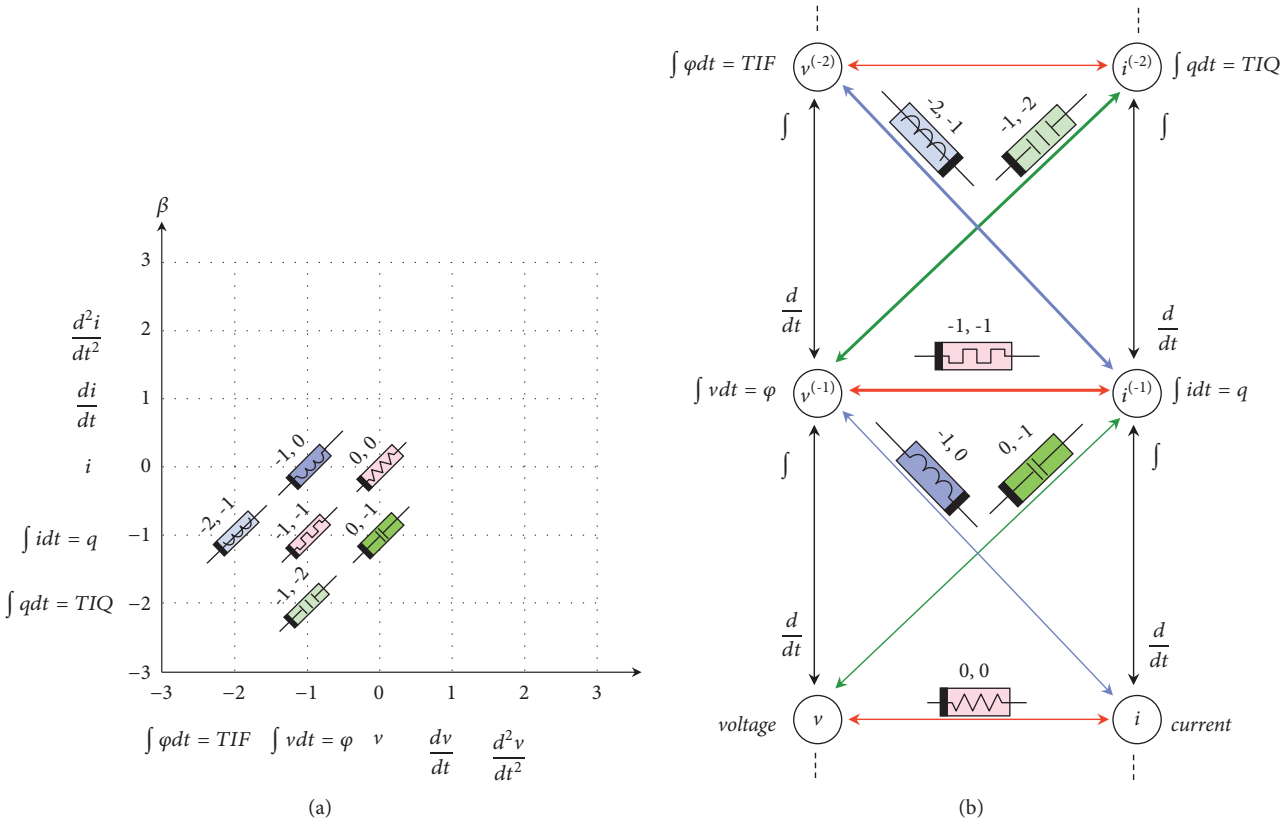

Figure 2: (a) Fragment of Chua's table of fundamental Higher-Order Elements (HOEs) with (α, β) coordinates: (0,0) – resistor, (-1,0) – inductor, (0,-1) – capacitor, (-1,-1) – memristor, (-2,-1) – meminductor, (-1,-2) – memcapacitor; (b) fragment of equivalent storeyed structure. TIF = time integral of flux, TIQ = time integral of charge. For details see [12, 13].

Current-controlled ideal memristor:

$$v = R_M(q)\, i, \qquad \frac{dq}{dt} = i \tag{3}$$

Voltage-controlled ideal memristor:

$$i = G_M(\varphi)\, v, \qquad \frac{d\varphi}{dt} = v \tag{4}$$

It can be concluded that the ideal and ideal generic memristors as fundamental elements can be defined via their memristance or memductance versus state map, where the state can be either the charge, flux, or some other state variable which is linked to the above "natural" state variables as described in [3, 25]. The equivalent well-known characteristics are the charge-flux constitutive relations [3].

Current-controlled ideal or ideal generic memristor:

$$\varphi = \widehat{\varphi}(q) \tag{5}$$

Voltage-controlled ideal or ideal generic memristor:

$$q = \widehat{q}(\varphi) \tag{6}$$

Differentiating (5) and (6) with respect to charge and flux yields the port equations (3) and (4).

All memristive systems from Figure 1(a), which cover all the extended memristors from Figure 1(b) according to the current classification, are modelled as follows [3]:

Current-controlled extended memristor:

$$\begin{aligned} v &= R_M(\mathbf{x}, i)\, i, \\ R_M(\mathbf{x}, 0) &\neq \infty, \\ \frac{d\mathbf{x}}{dt} &= \mathbf{f}(\mathbf{x}, i) \end{aligned} \tag{7}$$

Voltage-controlled extended memristor:

$$\begin{aligned} i &= G_M(\mathbf{x}, v)\, v, \\ G_M(\mathbf{x}, 0) &\neq \infty, \\ \frac{d\mathbf{x}}{dt} &= \mathbf{g}(\mathbf{x}, v) \end{aligned} \tag{8}$$

The bold symbols represent the vector variables or functions; thus the memristance or memductance can be generally modulated by a vector of states.

Definitions (1)–(8) can be conclusive in identifying whether the analysed circuit element is or is not a memristor or memristive system: If the model of this element cannot be written in any of the forms (1)–(8), then it cannot be classified as any memristor from the group in Figure 1(b).

This procedure is definite and thus more conclusive than deducing the type of the element from some limited number of its fingerprints that should hold simultaneously [26].

It is worth noting that the element is surely not a memristor as fundamental element if its model can be built up from models of the fundamental "no- (-1,-1)" elements in Chua's table or the storeyed structure. For example, it is obvious from Figure 2 that the so-called 2nd-order memristor introduced in [15] via a constitutive relation between the integral of flux (TIF) and integral of charge (TIQ) is in fact a (–2, –2) element. Similarly, the 3rd-order memristor, described in [15], is a (–3, –3) element, and other elements defined in [15], namely, the 2nd-order memcapacitor and meminductor, are classical (–2, –3) and (–3, –2) elements [14]. From this point of view, it is not advisable to denote such elements as some kinds of memristors, memcapacitors, or meminductors.

3. Inverse Memristors

Notwithstanding that a different notation is used below than in [10], the current-controlled and voltage-controlled inverse memristors are defined therein via the following equations:

$$v = a_i i + c_i i \frac{di}{dt} \tag{9}$$

$$i = a_v v + c_v v \frac{dv}{dt} \tag{10}$$

Here v, i are the terminal voltage and current, and a_i, c_i, a_v, c_v are real parameters.

It is obvious that the models (1), (2) cannot be arranged to agree with any of the definitions (1)–(8) of memristors.

It is shown in [10] that (9) (or (10)) represents a series connection of a linear resistor and a nonlinear inductor with quadratic flux-current characteristic (or a parallel connection of a linear resistor and a nonlinear capacitor with quadratic charge-voltage characteristic). The proof consists in rewriting (9) and (10) into the forms

$$v = R_i i + \frac{d}{dt}\left(\varphi(i)\right), \quad \varphi(i) = \frac{1}{2} c_i i^2 \tag{11}$$

$$i = G_v v + \frac{d}{dt}\left(q(v)\right), \quad q(v) = \frac{1}{2} c_v v^2 \tag{12}$$

Equations of magnetic flux $\varphi(i)$ and electric charge $q(v)$ describe the constitutive relations, i.e., predictive models of nonlinear inductor and capacitor. According to (11) or (12), the inductor is in series with a linear resistor whose resistance is $R_i = a_i$, or the capacitor is in parallel with a linear resistor whose conductance is $G_i = a_v$. That is why (9) and (10), which define the so-called inverse memristor in [10], do not describe new circuit elements. Because of the unambiguous identification of their subparts as the resistor and inductor (or capacitor) from Chua's table, one cannot denote it as a memristor. Just two problems should be resolved: Why such non-memristive elements can produce v-i pinched hysteretic loops, and why the loop area increases with increasing frequency.

4. Pinched (v, i) Behaviour of Nonlinear Inductors

It is well known that the inductor with a linear current-flux constitutive relation, driven by a sinusoidal voltage or current, generates the (v, i) Lissajous curves as circles (or ellipses), with the drawing point circling around the origin of the coordinates. The nonlinear inductor generates higher harmonic components in the spectrum of the response, which is manifested as a distortion of the Lissajous pattern. The aim is to find a class of such nonlinear characteristics of the inductors that produce patterns passing through the v–i origin.

Consider the current-controlled inductor as fundamental (-1,0) element from Chua's table with a nonlinear flux (φ) – current (i) constitutive relation

$$\varphi = \widehat{\varphi}(i). \tag{13}$$

Since the dual case of the flux–controlled inductor leads to analogous conclusions, it will not be analysed herein.

The terminal voltage of the inductor is

$$v = \frac{d\widehat{\varphi}(i)}{dt} = \frac{d\widehat{\varphi}(i)}{di}\frac{di}{dt} = L^d(i)\frac{di}{dt} \tag{14}$$

where the symbol $L^d(i)$ denotes the differential inductance as a function of current.

Let the inductor be driven via a sinusoidal current source with the amplitude I, repeating period T, and angular frequency $\omega = 2\pi/T$:

$$i(t) = I\sin(\omega t). \tag{15}$$

Then, according to (14), the terminal voltage is

$$v(t) = I\omega L^d[I\sin(\omega t)]\cos(\omega t) \tag{16}$$

As the sufficient condition for the hysteresis loop to be pinched at the origin, the voltage and current waveforms must simultaneously intersect the zero levels at the time instants $t = 0$ and $t = T/2$. Such a condition can, with the help of (16), be expressed in a simple form as

$$L^d(0) = 0. \tag{17}$$

Recall that the condition (17) means that the slope of the constitutive relation (13) at the origin is zero. Such a condition is fulfilled, for example, by the inductor with a quadratic constitutive relation, considered in [10]. The condition (17) of loop pinching at the origin is given explicitly by the nonlinear characteristic of the inductor. This condition does not depend on the parameters of the signal, here on its amplitude and the repeating frequency. It also follows from (15) and (16) that although the current swing is frequency-independent, the voltage swing is directly proportional to the frequency; thus the area of the corresponding v–i hysteresis loop will also increase proportionally with the frequency.

It can be derived from (16) that, regardless of the type of the constitutive relation (13) or the characteristic $L^d(i)$, the voltage must fulfil the following rules:

$$\begin{aligned} v(t) &= -v\left(\frac{T}{2} - t\right), \\ v(T-t) &= -v\left(\frac{T}{2} + t\right), \\ t &\in \left[0, \frac{T}{2}\right]. \end{aligned} \tag{18}$$

It follows from (18) that

$$v\left(\frac{T}{4}\right) = v\left(\frac{3T}{4}\right) = 0. \tag{19}$$

This means that the voltage waveform intersects the zero level also at time instants when the current waveform achieves its local maximum and minimum.

The impact of the symmetry (18) of the response (16) on the v–i hysteresis loop is illustrated in Figure 3. It is obvious that, in contrast to the passive memristor, the lobes of the loop must be located in all four quadrants of the v–i plane. The lobe for $i \geq 0$ (or $i < 0$) is enantiomorphic with respect to the axis of the current, and its shape depends on the nonlinear characteristic of the inductor $\varphi(i)$ for $i \geq 0$ (or $i < 0$). It can also be readily proved that the potential symmetries of this characteristic, namely, $\varphi(-i) = -\varphi(i)$ or $\varphi(-i) = \varphi(i)$, would result in hysteresis loops that would also be symmetric with respect to the vertical axis of the voltage. It is also interesting that both of the above cases would lead to the same loops but of opposite orientations.

An analysis of the type of the loop, i.e., whether it is the (non) crossing type and what is the order of touching the loop arms at the origin, can be done via a methodology from [16], which compares higher-order derivatives of voltages and currents at the time instants 0 and $T/2$, when these signals intersect the zero levels. This analysis reveals that the loops, generated by nonlinear inductors which fulfil the condition (17), can be of both the CT and NCT types and that the order of touching is related to the lowest order of nonzero derivative of the characteristic $\varphi(i)$ with respect to current for $i = 0$. For the "nonsymmetric" characteristics $\varphi(i)$ with possible discontinuous higher-order derivatives for $i = 0$ (see the example in Figure 3), the lobes on the right and on the left of the voltage axis can exhibit different orders of touching.

In order to mimic the definition (1) of current-controlled inverse memristor, Figure 4 demonstrates the superposition of the v–i characteristics of the inductor of type (17) and the linear resistor. It is obvious that if the resistance is high enough, the resulting characteristic of the series connection of these elements will be located only in the first and third quadrants of the v–i space. Then it can resemble the pinched hysteresis loop of the passive memristor. However, there are conclusive signs of non-memristive behaviour: for increasing frequency, however, the vertical (voltage) dimension of the loop in Figure 4(a) increases, and, starting from a certain frequency, the lobes of the loop in Figure 4(b) may also appear in other quadrants. In addition, the loop directions in Figure 4 demonstrate the noncrossing property at the (v, i) origin, which cannot occur in circuits with ideal memristors. As one other difference from the behaviour of ideal memristors, obvious from Figure 3, the pinched hysteresis loop does not provide the odd symmetry if the flux-current characteristic of the inductor is asymmetric.

As follows from Figure 4(b), similar effects can also be obtained via a nonlinear resistor in series with the inductor considered. Then the pinched hysteresis loops may also be asymmetric, resembling the behaviour of general extended memristors.

Figure 5 demonstrates the "inverse-memristor" frequency dependence of the hysteresis studied in Section 6: The lobe area increases with the frequency.

The series connection of a resistor R and the inductor with the nonlinear constitutive relation (13) and with the property (17) can be described by the following relation between terminal voltage and current:

$$v = Ri + \frac{\partial\widehat{\varphi}(i)}{\partial i}\frac{di}{dt} = Ri + L^d(i)\frac{di}{dt} \tag{20}$$

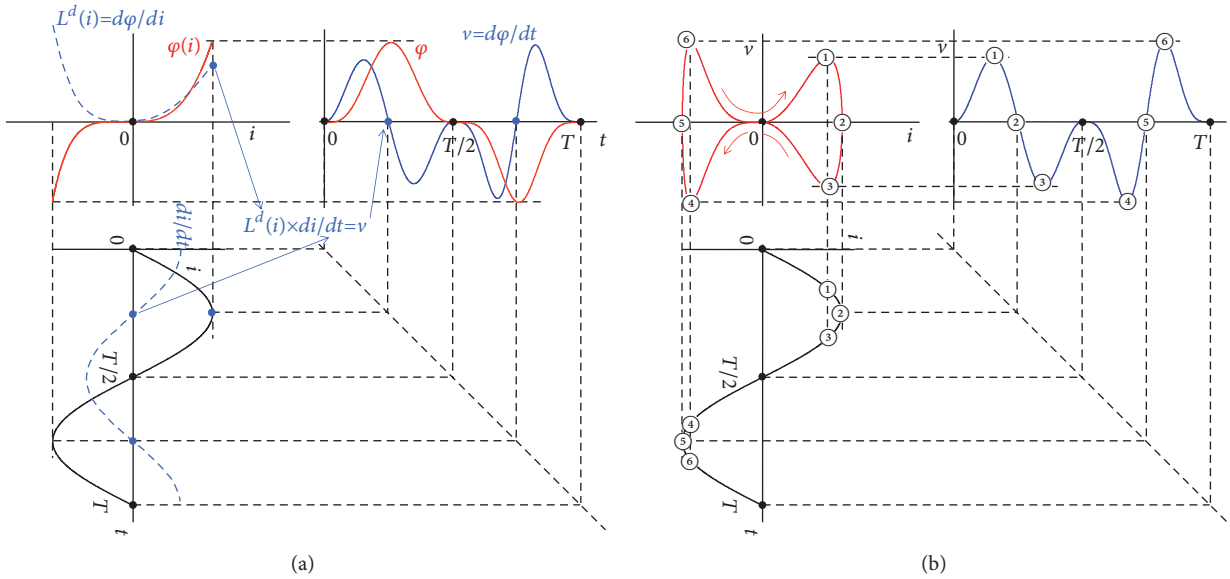

FIGURE 3: Nonlinear inductor with zero differential inductance for $i = 0$ driven by a sinusoidal 1 mA/1kHz current, with the characteristic $\varphi(i) = k_1 i^3$ for $i \geq 0$ and $\varphi(i) = k_2 i^5$ for $i < 0$, $k_1 = 1$ Wb/mA, $k_2 = 1$ Wb/nA. The principle of generating (a) voltage waveform, (b) hysteresis loop pinched at the v–i origin.

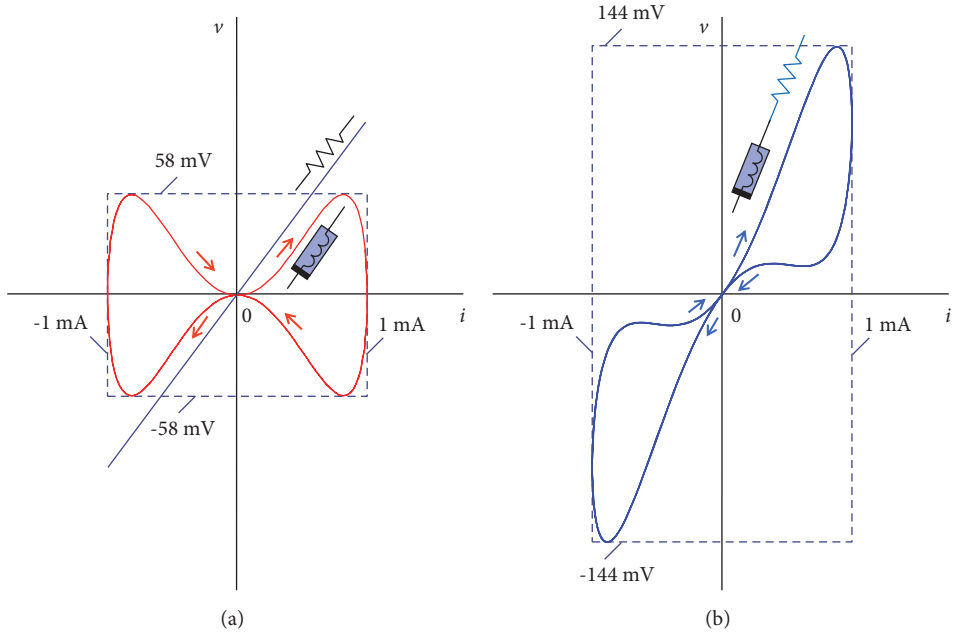

FIGURE 4: Graphical composition of the v–i characteristics of nonlinear inductor with the characteristic $\varphi(i) = ki^3$, $k = 1$ Wb/mA, driven by a sinusoidal 1 mA/1kHz current, and linear 100 Ω resistor (a). The result is a v–i hysteresis loop, which corresponds to the series connection of these elements, reminiscent of the pinched hysteresis loop of a passive memristor (b).

Comparing (20) with the definition of the current-controlled inverse memristor (9) leads to the conclusion that (9) defines a series connection of a linear resistor with the resistance $R = a_i$ and a nonlinear inductor whose differential inductance $L^d = c_i i$ is directly proportional to the inductor current. However, as follows from the above analysis, it is only a special case of a more general R-L circuit (R linear and L nonlinear), which can produce the v–i pinched hysteresis loops.

It is essential to emphasize that the mechanism of generating the pinched hysteresis loops in Figure 3 works only for such an initial state of the inductor which corresponds to the initial position of the operating point on the nonlinear characteristic $\varphi(i)$ with zero differential inductance. For any other initial states, where the condition (17) does not hold, the pinched hysteresis effect does not appear.

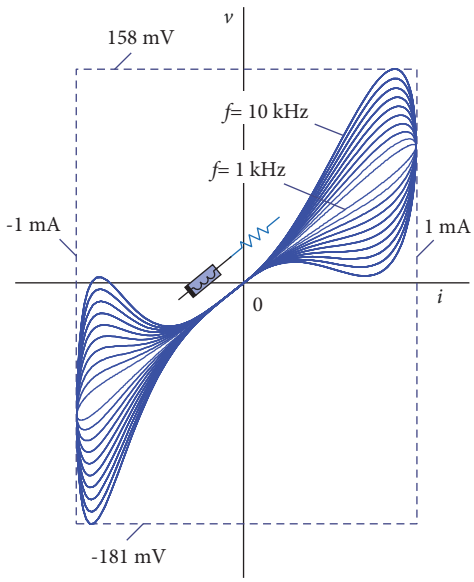

FIGURE 5: Pinched hysteresis loops generated by nonlinear inductor with asymmetric characteristic $\varphi(i) = k_1 i^3$ for $i \geq 0$ and $\varphi(i) = k_2 i^5$ for $i < 0$, $k_1 = 1$ Wb/mA, $k_2 = 1$ Wb/nA in series with 100 Ω resistor, driven by a sinusoidal 1 mA current. The loop area is increasing when the frequency increases from 1 kHz to 10 kHz. For $f = 10$ kHz, the loops occupy 3 quadrants of (v, i) plane, resembling an active memristive system.

5. Pinched (v, i) Behaviour of Nonlinear Capacitors

A similar analysis to that for the inductor from Section 4 can also be done for nonlinear capacitors.

Consider a voltage-controlled capacitor with nonlinear voltage (v) – charge (q) constitutive relation

$$q = \hat{q}(v). \tag{21}$$

Since the current is a derivative of the charge, then

$$i = \frac{d\hat{q}(v)}{dt} = \frac{d\hat{q}(v)}{dv}\frac{dv}{dt} = C^d(v)\frac{dv}{dt} \tag{22}$$

where the symbol $C^d(v)$ denotes the differential capacitance as a function of voltage.

When driving the capacitor by a sinusoidal voltage

$$v(t) = V \sin(\omega t), \tag{23}$$

the current will, according to (22), be

$$i(t) = V\omega C^d [V \sin(\omega t)] \cos(\omega t). \tag{24}$$

The procedure from Section 4 leads to the sufficient condition for the existence of the hysteresis loop pinched at the v–i origin

$$C^d(0) = 0. \tag{25}$$

Since the mathematical models of the hysteretic behaviour of the inductor (13) – (17) and capacitor (21) – (25) are dual, all the conclusions from Section 4 can also be used for the capacitor after a reciprocal v–i replacement. That means, among other things, that the hysteresis loop located in the first and third v–i quadrants (see Figure 4(b)) can be generated via a parallel connection of a nonlinear capacitor with $C^d = c_v v$, which provides the property (25), and a proper resistor with $R = 1/a_v$. This knowledge is in agreement with the conclusion from [10].

6. Pinched Hysteresis with "Inverse-Memristor Frequency Characteristics"

Consider the pinched hysteresis loop generated by nonlinear inductor with differential inductance $L^d(i)$ in series with the linear resistor R in Figure 4(b). Denote the areas enclosed by the loops located in the quadrants for $i > 0$ and $i < 0$ as S_1 and S_2. They can be evaluated as follows [27]:

$$\begin{aligned} S_1 &= \int_0^{T/2} v\frac{di}{dt}dt = -\int_0^{T/2} i\frac{dv}{dt}dt, \\ S_2 &= \int_{T/2}^{T} v\frac{di}{dt}dt = -\int_{T/2}^{T} i\frac{dv}{dt}dt. \end{aligned} \tag{26}$$

After substituting (20) into the formula $v\, di/dt$ in (26) and considering the current excitation (15), the arrangement yields the results

$$\begin{aligned} S_1 &= \omega I^2 \int_0^{\pi} L^d(I \sin\alpha)\cos^2\alpha\, d\alpha, \\ S_2 &= \omega I^2 \int_0^{\pi} L^d(-I \sin\alpha)\cos^2\alpha\, d\alpha \end{aligned} \tag{27}$$

Note that the loop areas do not depend on the resistance R. It confirms the expectable fact that the areas of the hysteresis loops in Figures 4(a) and 4(b) are identical.

It is evident that the loop areas (27) are directly proportional to the frequency ω.

Similar computations can be done for the loops generated by a nonlinear capacitor with differential capacitance $C^d(v)$ in parallel with the linear resistor R, driven by the sinusoidal voltage (23), as discussed in Section 5. The corresponding loop areas are now

$$\begin{aligned} S_1 &= -\omega V^2 \int_0^{\pi} C^d(V \sin\alpha)\cos^2\alpha\, d\alpha, \\ S_2 &= -\omega V^2 \int_0^{\pi} C^d(-V \sin\alpha)\cos^2\alpha\, d\alpha; \end{aligned} \tag{28}$$

thus they also increase with increasing frequency.

Figure 6 illustrates how this rule of frequency dependence of the loop area can be easily deduced from the position of the element in the storeyed structure.

The variables v (voltage), i (current), $v^{(-1)}$ (time integral of voltage = flux φ), and $i^{(-1)}$ (time integral of current = charge q) are four nodal points of a part of the storeyed structure in Figure 6 containing the studied nonlinear inductor and also

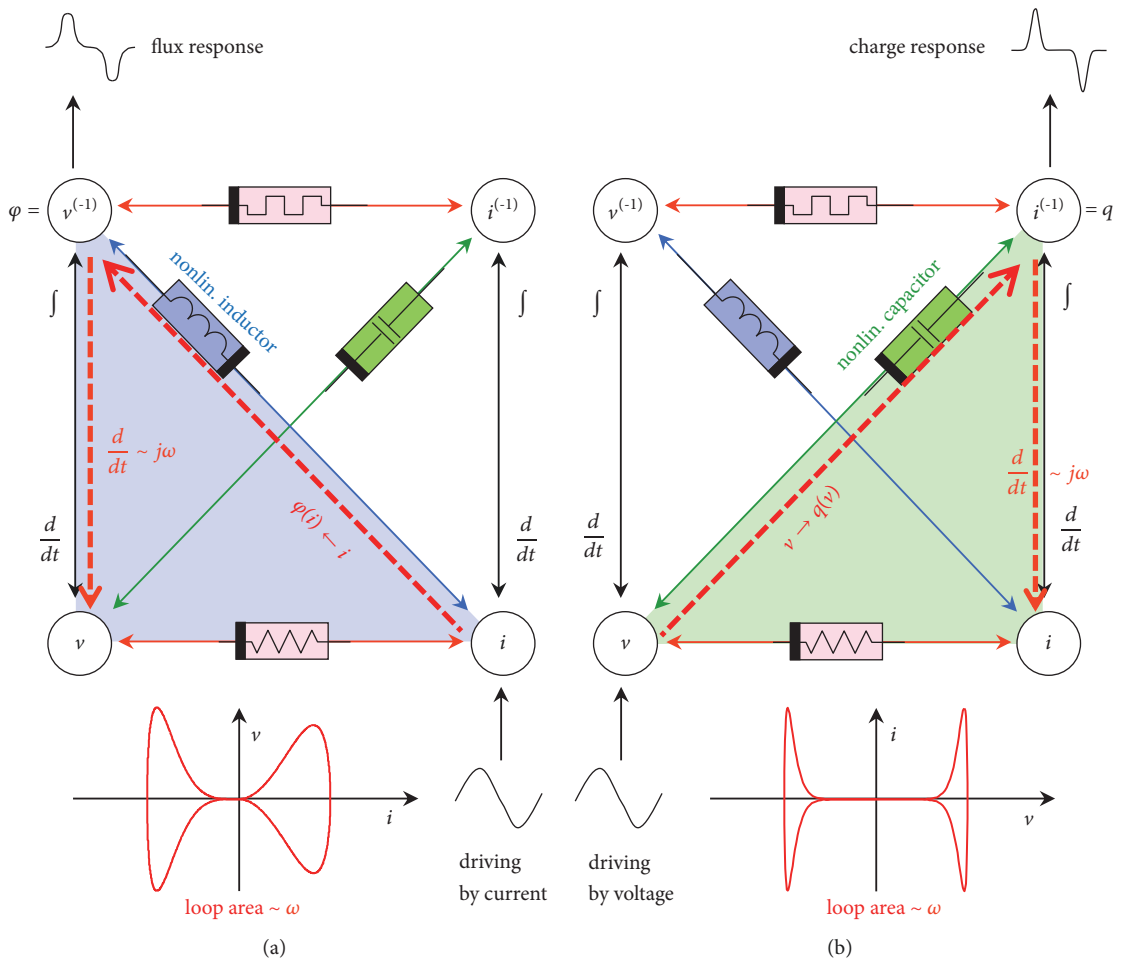

FIGURE 6: Analysis of the frequency dependence of the area of pinched hysteresis loop of the so-called inverse memristor driven by (a) current (the predictive model is a nonlinear inductor) and (b) voltage (the predictive model is a nonlinear capacitor). A similar analysis can be done for the loop area of classical ideal memristor [14].

capacitor. The nonlinear inductor with flux-current constitutive relation, which can produce the pinched hysteresis loops according to Figure 4(a), represents a link between the nodes i and $v^{(-1)}$ (red dashed line in Figure 6(a)). Consider that this inductor is driven by a sinusoidal current as indicated in Figure 6(a). Then, as a consequence of the unambiguous nonlinear flux-current constitutive relation, the inductor flux waveform will be a distorted version of the current waveform. The flux is reflected to the node v via time differentiation (see the red dashed line in Figure 6(a)), which amplifies the signal with the first power ω^1 of the increasing frequency. As a result, if the frequency of the driving current and thus also the flux frequency increase, then the amplitude of the voltage response increases proportionally, and the lobe area of the v-i corresponding pinched hysteresis loop also increases proportionally to the first power of frequency.

A similar analysis can be done for the nonlinear capacitor, which is a part of the voltage-controlled inverse memristor, with the nonlinear constitutive relation between voltage and charge, the latter being the time integral of the current. This element occupies the diagonal between the nodes v and $i^{(-1)}$ in the storeyed structure in Figure 6(b). When driving this capacitor by a sinusoidal voltage, the charge waveform does not keep the sinusoidal form, but its frequency follows the repeating frequency of the excitation, and the current waveform is amplified proportionally to the increasing frequency. As a result, the area of the pinched hysteresis lobe is also directly proportional to the frequency.

7. Conclusions

Observations from this study can be summarized into the following paragraphs. (Only conclusions concerning the current-controlled inductors and voltage-controlled capacitors are given below; dual propositions hold for flux–controlled inductors and charge-controlled capacitors.)

(1) Nonlinear inductors and capacitors with unambiguous constitutive relations (13) and (21) generate ordinary Lissajous v–i curves, which may degenerate into hysteresis loops pinched at the v–i origin under

conditions (17) and (25), i.e., if the characteristics exhibit zero differential inductance/capacitance at the initial point $i = 0$ and $v = 0$.

(2) When driving the inductor and capacitor from Paragraph (1) via a sinusoidal current and voltage, then its voltage and current (i.e., the response) exhibit a special symmetry. As a consequence, the response shows additional zero level crossings at time instants when the driving signal is not zero. From this narrow point of view, the inductor and capacitor from Paragraph (1) manifest themselves as an active memristor ([3], see "coincident zero-crossing memristor fingerprint"), even if it is an accumulating element.

(3) As a consequence of the symmetry of the responses from Paragraph (2), the v–i pinched hysteresis loops are symmetric with respect to the axis of the driving signal, and they are located in all four quadrants. In contrast to the memristor, however, this fact is not related to a potential activity of the elements generating the loops.

(4) The loop symmetry from Paragraph (3) can be violated by adding a resistor in series with the inductor or in parallel to the capacitor from Paragraph (1). Such a resistor does not influence the effect of pinching the loop at the origin and does not modify the loop area. This procedure can place the hysteresis loop into the first and third quadrants. However, this does not say anything about the passivity or activity of the composed element.

(5) The hysteresis loop from Paragraph (3) is proportionally expanding along the axis of the driving signal when the frequency is increasing, and so is the loop area.

(6) The hysteresis loops from Paragraphs (1) and (3) can be of both CT and NCT [17], with various orders of touching at the v–i origin. These parameters are determined by nonlinear constitutive relations of the inductor/capacitor.

(7) The existence of the pinched hysteresis loop of nonlinear inductor and capacitor from Paragraph (1) is subject to exciting the element from the zero initial state $i = 0$ and $v = 0$, where its constitutive relation exhibits zero differential inductance and capacitance. For any other initial state where this condition is not fulfilled the pinched loop according to Paragraphs (1) and (3) will not be observable.

The last paragraph in particular expresses an essential difference in the hysteretic effects of nonlinear inductors and capacitors (the loop is pinched only for concrete initial states) and memristors (the pinched loop is their general fingerprint).

Data Availability

No data were used to support this study.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

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