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Susceptibility to Radio Frequency Interference of eGaN Power Switching Legs

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***Abstract*—Power switching circuits like those used in inverters and DC-DC converters are usually investigated with the purpose of increasing the power efficiency or lowering the electromagnetic emissions. Considered that, the reliability of such modules is also a key aspect, especially in safety critical applications, this work focuses on the susceptibility of such circuits to radio frequency interference. To this purpose, an e-mode GaN power switching leg in a real application environment is considered. A circuit comprising the nominal active and passive components, their stray inductances and capacitances as well as those due to the PCB wiring is presented. The effect of radio frequency interference injected into the output terminal by means of a bulk current injection clamp is analyzed with the purpose of evaluating the risk that such interference propagated through the circuit could induce temporary or permanent failures.**

***Index Terms*—e-mode GaN Power HEMT, Radio Frequency Interference, Isolated Gate Drivers, Integrated Circuit Susceptibility.**

I. Introduction

The safety of modern electric and electronic systems is tightly related with the operation of their power units. Besides common reliability issues, temporary or permanent failures occur also when the system is exposed to the electromagnetic field delivered by radio frequency transmitters such as those used for radio and TV broadcasting or in wireless communication systems. For instance, power cables like those used in electric vehicles to connect the traction inverter to the electric motor or those connecting the power inverter to the battery pack, behave like receiving antennas that collect the disturbances into the power units.

According to [1], the disturbance induced by a plane wave impinging on a cable laid above a metal ground plane can be modeled by a transmission line driven by a set of equivalent voltage sources ($V_{\mathrm{RF-x}}$) at their terminations. The DC inputs are usually protected against such disturbances by an EMI filter, which is present to avoid the switching noise generated inside the power module, to be propagated outside. The AC outputs comprise differential mode filters only, therefore the common mode interference injected into the outputs is allowed to propagate in the power module, especially at high frequency where parasitic elements are effective. Therefore, the AC outputs of common power inverters like that shown in Fig. 1 are affected by the radio frequency voltages and currents induced by the equivalent voltage sources $V_{\mathrm{RF-x}}$. This means that the operation of the power transistors, and that of their respective gate drivers can be affected by such disturbances, causing temporary or permanent failures.

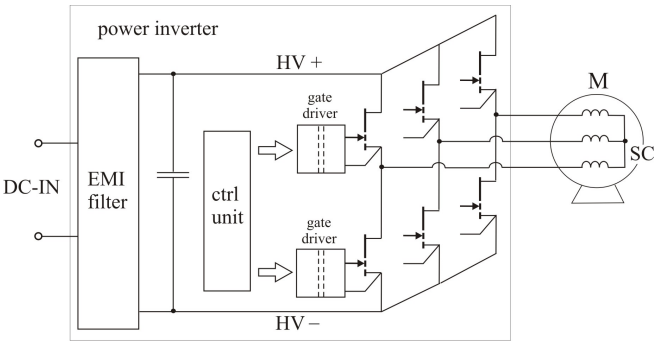

Fig. 1. Three phase traction inverter connected to the battery pack and to the electric motor by cables.

This work investigates how the interference injected into the AC outputs of a power inverter propagates through a power module with the aim to evaluate the level of interference affecting the power transistors and the gate driver signals.

The analysis is carried out referring to a power leg based on e-mode GaN power transistors, which are among the most promising devices in terms of switching speed and power dissipation but also among the most susceptible to the switching noise because of their low threshold voltage.

The paper is organized as follows. Section II introduces the power circuit of interest its main components and features. Section III deepens of the parasitic elements related to the circuits component and its PCB wiring. Section IV shows the circuit considered for simulations and a comprehensive analysis of the simulation results is provided. Some concluding remarks are drawn in Section V.

II. Circuit under Analysis

A common circuit to drive an inductive power load consists of two equal power transistors connected in a stacked fashion as shown in Fig. 2. The switching circuit drives an inductive load at one end (the other is connected to the star center - SC) to module the average current. The high side (HS) transistor T1 provides current to the load in the active phase (T_{on}), the low side (LS) T2 allows the load current to recycle

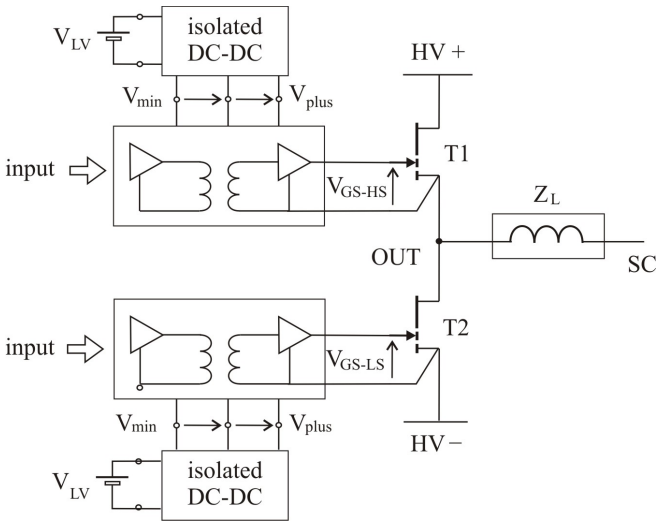

Fig. 2. Single leg schematic view.

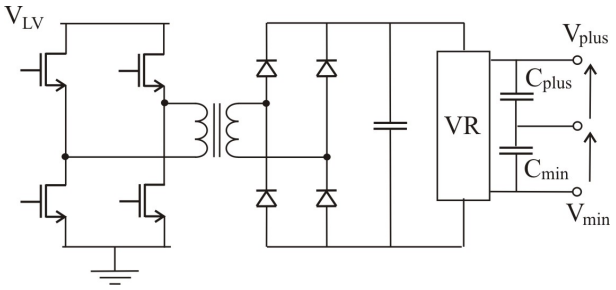

Fig. 3. Gate driver power supply circuit.

in the remainder of the switching time ($T_{\rm off}$). The transition of the output voltage $V_{\rm OUT}$ from high to low (or low to high) is carried out in two steps. The HS, which is initially switched on, is turned off for a small time interval $t_{\rm d}$, the dead time. Therefore, the current flowing in the inductive load drives the LS, which is driven to be switched off, in the reverse conduction mode, thus allowing the free wheeling. At the end of $t_{\rm d}$, the recycling transistor T2 is turned on to reduce its power losses.

As far as high voltage switching legs based on last generation e-mode GaN power transistors are concerned, the switching frequency $f_{\rm sw}$ can take values in the range $100\ {\rm kHz} - 1\ {\rm MHz}$, the rising ($t_{\rm r}$) and the falling ($t_{\rm f}$) times of the switching waveforms is between $2\ {\rm ns}$ and $20\ {\rm ns}$, and the dead time $t_{\rm d}$ is between $50\ {\rm ns}$ and $100\ {\rm ns}$.

The commutation of each power transistor is managed by its gate driver, which output section is isolated from the input one. DC isolation is mandatory for the HS transistor, because its driving voltage $v_{\rm GS-HS}$ is referred to the output node (OUT). Furthermore, the isolation avoids the switching noise generated in the power section to affect the low voltage input signals. To sum up, each transistor is driven by an isolated gate driver, and the circuits providing the power supply to the output section has to be galvanically isolated as well, as it

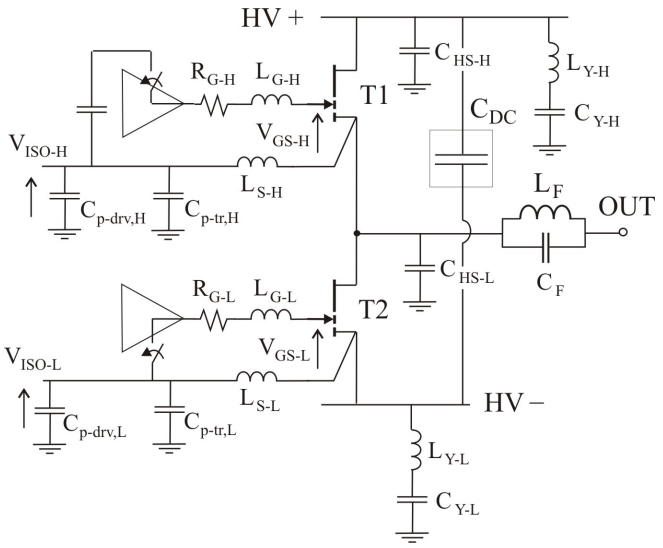

Fig. 4. Schematic view of the power circuit including stray inductances and capacitances.

is shown in Fig. 2. An example of an isolated power supply circuit is provided in Fig. 9. A full bridge drives the primary winding of a transformer, which secondary is loaded by a rectifier and a linear voltage regulator. The latter is needed to avoid the positive and the negative power supply voltage exceeding the maximum and the minimum gate source voltages over which the power transistor can be damaged permanently. The value of the positive power supply $V_{\rm plus}$ is set to the maximum declared by the transistor manufacturer but far enough from its absolute maximum. This allows one to lower the on resistance as much as possible. The negative power supply ($V_{\rm min}$) is needed to avoid self immunity issues, i.e., to keep one of the two transistors switched off while the other is switching on [5]. However, it should be reminded that the lower the minimum voltage ($V_{\rm min}$) , the higher the power dissipation of the power transistor during the dead time. For this reason, in several applications, the negative power supply is zeroed just after the commutation of the other transistor [6]. Finally, it is worth reminding that the switching current needed to turn the power transistors on and off is taken from the decoupling capacitors $C_{\rm plus}$, $C_{\rm min}$. These should be placed as close as possible to the gate driver to the power supply pins to reduce the stray inductances .

III. High frequency model of the power circuit for susceptibility analysis

The magnitude of the continuous wave (CW) interference affecting the components composing the phase leg was investigated referring to the equivalent circuit shown in Fig. 4. It comprises of two eGaN power transistors, their package parasitic elements (not shown), the related gate drivers and the PCB wiring parasitic inductances. In particular, $L_{\rm G-H}$, $L_{\rm S-H}$, $L_{\rm G-L}$, $L_{\rm S-L}$, model the wiring connecting the output of the gate drivers to the power transistor gate-source terminals,

$R_{\mathrm{G-H}}$ and $R_{\mathrm{G-L}}$ represent the resistors that limit the gate currents at the turn on (off). $C_{\mathrm{p-drv,L}}$ and $C_{\mathrm{p-drv,H}}$ model the isolation capacitance of the gate drivers, $C_{\mathrm{p-tr,L}}$ and $C_{\mathrm{p-tr,H}}$ are those of the power supply isolation transformers. The Y capacitors of the EMI filter, which collect the common mode switching noise generated by the power transistors are modeled by $C_{\mathrm{Y-H}}$, $L_{\mathrm{Y-H}}$, and $C_{\mathrm{Y-L}}$, $L_{\mathrm{Y-L}}$, respectively. The capacitive coupling of the LS (HS) drain terminal with the heatsink, thus with the inverter metal case, is modeled by $C_{\mathrm{HS-L}}$ ($C_{\mathrm{HS-H}}$). Furthermore, C_{DC} represents the high frequency impedance of the DC link capacitors, L_{F} and C_{F} that of the output filter inductance.

IV. Interference injection circuit

The bulk current injection method was considered for injecting the interference into the output of the phase leg [2] [3] [4].

For this purpose, the simulation setup shown in Fig. 5 was developed. The interference is injected into the cable connecting the EUT, i.e., the power circuit shown in Fig. 4, to the power load (Z_{L}) by a high frequency transformer (TR). The cable connecting the the EUT to the load is modeled by a uniform transmission line of length L and characteristic impedance Z_0. About the RF source driving the injection clamp (TR), the closed loop method specified in [3] was considered. In the real test setup, the injection clamp is driven by a wide band RF amplifier, which in turn receives the input signal from an RF source. The RF current I_{C}, which flows in the cable harness is monitored by an RF current probe (not shown in Fig. 5). According to the closed loop method, the level of the RF signal driving the amplifier should be increased step by step while monitoring the operation of the EUT as long as a failure takes place, or the maximum current level I_{S} is reached, or the maximum available power delivered by the RF amplifier is reached. The test should be repeated for a set of interference frequency in the range $1\ \mathrm{MHz} - 400\ \mathrm{MHz}$.

Aiming to evaluate the maximum level of disturbance affecting the EUT nominal signals, the equivalent injection circuit shown in Fig. 5 was used. The RF source driving the injection clamp TR is modeled by a current controlled voltage source (CCVS) R_{M} driven by the error current $I_{\mathrm{E}} = I_{\mathrm{S}} - A_{\mathrm{I}} I_{\mathrm{C}}$. I_{S} is the current we want to make flow in the power cable, I_{C} is the current that flows in the cable actually, A_{I} is a gain factor. Wanting to keep the error current I_{E} as low as possible, the simulations were carried out setting $R_{\mathrm{M}} = 100\ \mathrm{k\Omega}$ and $A_{\mathrm{I}} = 1$. The CCVS output resistance R_0, which models the RF amplifier output resistance, was set to $50\ \Omega$.

Finally, the equivalent circuit of the RF injection clamp (TR in Fig. 5) proposed in [9] was used. The circuit is shown in Fig. 6 and its parameters are reporter in Tab. II for convenience.

V. Circuit Analysis

With the purpose of investigating the propagation of continuous wave (CW) interference through the circuit shown in Fig. 4, that in Fig. 5 was analyzed performing frequency domain simulations with the HS switched on and the LS switched off, permanently. Indeed, AC analysis can be carried out only once the bias point of the nonlinear devices are defined. Other bias points were also considered obtaining results similar to those showed below, thus they have not been included in this paper for brevity.

The eGaN transistor considered for the analysis is the GS-66508-B [11]. According to the manufacturer data sheet, its main features are $V_{\mathrm{DS-max}} = 650\ \mathrm{V}$, $R_{\mathrm{ON-typ}} = 50\ \mathrm{m\Omega}$, $V_{\mathrm{GS-TH,typ}} = 1.7\ \mathrm{V}$, $V_{\mathrm{GS-MIN}} = -10\ \mathrm{V}$, $V_{\mathrm{GS-MAX}} = 7\ \mathrm{V}$. The gate driver considered is Si8271 [12]. It shows $R_{\mathrm{OH}} =$

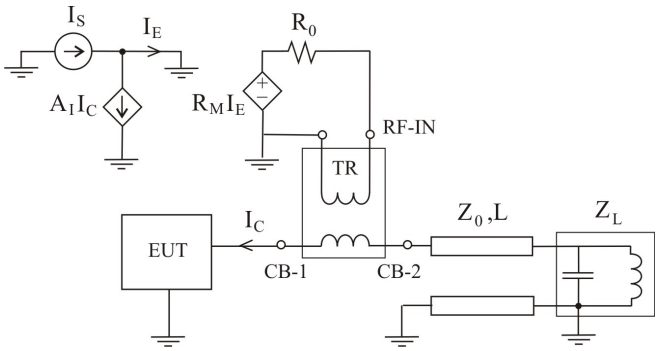

Fig. 5. Simulation set up implementing the closed loop bulk current injection method.

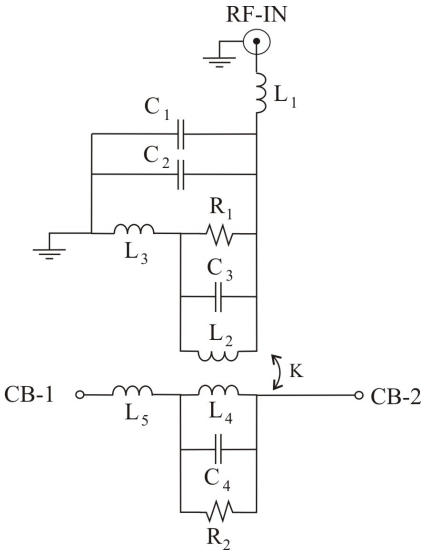

Fig. 6. Model of the bulk current injection clamp.

TABLE I
Parameters of the circuit shown in Fig.6.

Parameter	Value	Parameter	Value
L_1	4 nH	L_3	15 nH
$L_2 = L_4$	2 μH	L_6	30 nH
L_5	15 nH	C_2	7 pF
$C_1 = C_3 = C_4$	2 pF	R_1	700 Ω
R_2	300 Ω	K	0.99

TABLE II
NOMINAL VALUES OF THE COMPONENTS OF THE CIRCUIT SHOWN IN FIG. 4.

Parameter	Value	Parameter	Value
L_{F}	48 μH	C_{F}	12 pF
$C_{\mathrm{Y-H}} = C_{\mathrm{Y-L}}$	1 μF	$L_{\mathrm{Y-H}} = L_{\mathrm{Y-L}}$	38 nH
$L_{\mathrm{G-H}} = L_{\mathrm{G-L}}$	16 nH	$R_{\mathrm{G-H}}$	2 Ω
$L_{\mathrm{S-H}} = L_{\mathrm{S-L}}$	9 nH	$R_{\mathrm{G-L}}$	0 Ω
$C_{\mathrm{p-tr,H}} = C_{\mathrm{p-tr,L}}$	8 pF	$C_{\mathrm{p-drv,H}} = C_{\mathrm{p-drv,L}}$	0.5 pF
$C_{\mathrm{HS-H}}$	41 pF	$C_{\mathrm{HS-L}}$	41 pF

2.7 Ω, $R_{\mathrm{OL}} = 1\ \Omega$, $C_{\mathrm{p-drv}} = 0.5$ pF. The parameters of the passive components as well as those of the stray inductances and capacitances in Fig. 4 are listed in Tab. II.

The nominal values of the passive components resulted from the design specifications of a low power three-phase power inverter. Those of the parasitic elements related to the passive components were derived from the component data sheets. The parasitic inductances of the PCB wiring were obtained from the 3D electromagnetic simulation of the PCB layout. About the DC link capacitors (C_{DC} in Fig. 4), it comprises two capacitors $C_{\mathrm{DC-1}} = 45\ \mu$F each, $C_{\mathrm{DC-2}} = 2.2\ \mu$F, $C_{\mathrm{DC-3}} = 390$ nF. The equivalent circuit was composed including the ESL and ESR of each capacitor provided by the manufacturers.

The simulation results showing the magnitude of the interference affecting each power transistor gate source voltage ($V_{\mathrm{GS-L}}$, $V_{\mathrm{GS-H}}$) and the gate drivers ($V_{\mathrm{ISO-L}}$, $V_{\mathrm{ISO-H}}$) are plotted in Fig. 7 and Fig. 8, respectively.

They were obtained using the closed loop injection method, i.e., referring to the equivalent circuit shown in Fig.5 to set $I_{\mathrm{S}} = 100$ mA.

Moreover, the power cable connecting the eGaN leg output terminal to the load is unshielded and it is assumed to run parallel to the ground plane for $L = 1$ m at distance $h = 50$ mm. Based on this last parameter and being the cable diameter $D = 12$ mm, the characteristic impedance of the equivalent transmission line is $Z_0 = 170\ \Omega$ [7].

According to the simulation results shown in Fig. 7, the gate-source voltages take values comparable to the transistor threshold close to 113 MHz. The HS, which is driven to be switched on, is concerned by lower level of interference (dashed line) and even in the worst case, it cannot be switched off by the interference because the overdrive is always above the maximum interference magnitude. About the LS, which is driven to be switched off, the interference exceeds the threshold for frequencies around 113 MHz as well. This means that the LS transistor can be turned on and off cyclically by the interference although it is driven by the gate driver to be switched off. Therefore, with the HS switched on purposely, the activation of the LS causes unwanted cyclical shoot-through currents that could result in temporary or permanent failures of the power unit.

The operation of the gate drivers can be also affected by the interference injected into the output terminal. A measure of such disturbances is given by the magnitude of the AC

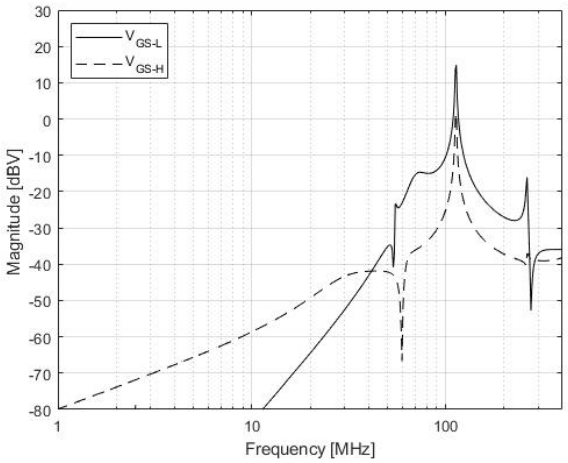

Fig. 7. Magnitude of the interference superimposed onto the gate source voltages $V_{\mathrm{GS-L}}$ (continuous line), $V_{\mathrm{GS-H}}$ (dashed line) vs. frequency.

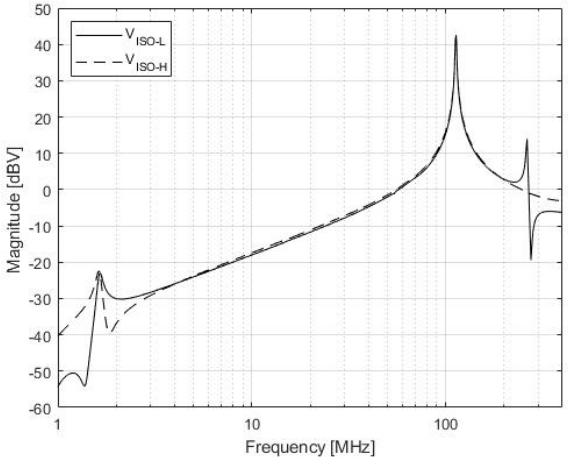

Fig. 8. Simulation results. Magnitude of the interference superimposed onto the gate driver isolation voltages $V_{\mathrm{ISO-L}}$ (continuous line), $V_{\mathrm{ISO-HS}}$ (dashed line) vs. frequency.

isolation voltages $V_{\mathrm{iso-LS}}$, $V_{\mathrm{iso-HS}}$ vs. frequency shown in Fig. 8. Both voltages take the maximum of about 40 dBV at 113 MHz, which is much larger than that taken by the gate source voltage. Furthermore, the interference affecting the isolation voltage is well above the maximum level required by OEMs in the qualification tests of integrated circuits, which is about 33 dBV for global IC pins [10]. This means that, the isolated gate drivers currently on the market, which comply to common immunity specifications [10], could fail the bulk current injection test, or even worse, they could fail in actual application environments. With such a high interference level applied to the DC isolation barrier, the RF communication channel between the low voltage and the high voltage sections [13] could be impaired because of time jittering or false commutations induced by the interference in clock and data signals [14], [15] [16].

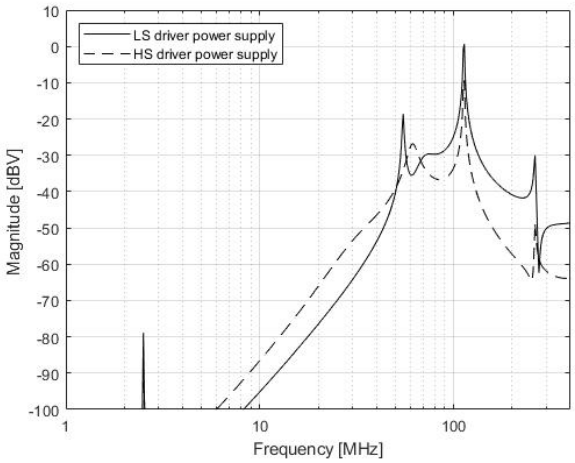

Fig. 9. Magnitude of the interference superimposed onto the gate driver DC power supply vs. frequency.

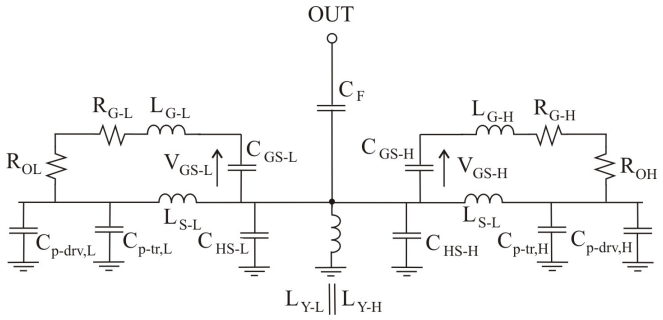

Fig. 10. High frequency equivalent circuit derived from that shown in Fig. 4.

Finally, the interference affecting the power supply voltage of each gate driver (not shown in Fig. 4) was evaluated obtaining the AC plots shown in Fig. 9. Also in this case, the LS gate driver is more affected than the HS one, and the maximum level of about 0 dBV is reached at 113 MHz. The interference superimposed onto the power supply voltage at the chip level can affect subcircuits like the undervoltage lockout (UVLO), i.e., the on chip voltage comparator and the bandgap voltage reference integrated in the gate driver output section [17] [18] [19].

Wanting to understand the reasons of such a high level of interference close to 113 MHz, the circuit in Fig. 4 was simplified obtaining that shown in Fig. 10. In particular, the HS transistor was replaced by a short circuit between drain and source and the transistor gate-source capacitance $C_{\mathrm{GS-HS}}$. Similarly, the LS transistor was replaced by the drain-source capacitance C_{OSS} and the gate-source capacitance $C_{\mathrm{GS-LS}}$. Furthermore, the DC link capacitors (C_{DC}) was replaced by a short circuit and the $C_{\mathrm{Y,x}}$ capacitors by their stray inductances $L_{\mathrm{Y,x}}$.

The AC analysis of the reduced circuit showed that its frequency response is in good agreement with that of the complete one (that shown in Fig. 4) in the range 50 MHz - 200 MHz. Therefore, from inspection, it resulted that the voltage peaks at about 113 MHz deal with the parallel resonance of the $C_{\mathrm{Y,x}}$ stray inductances with the sum of the stray capacitances $C_{\mathrm{p-drv,H}}$, $C_{\mathrm{p-tr,H}}$, $C_{\mathrm{p-drv,L}}$, $C_{\mathrm{p-tr,L}}$, $C_{\mathrm{HS,L}}$, $C_{\mathrm{HS,H}}$. This was also highlighted by the parametric analysis carried out for $C_{\mathrm{p-tr,L}}$ (the power supply transformer stray isolation capacitance), which results are shown in Figs. 11 and 12. Moreover, the reduced circuits highlighted that $V_{\mathrm{GS-LS}}$ and $V_{\mathrm{GS-HS}}$ are affected by the currents flowing through $C_{\mathrm{p-tr,L}}$ and $C_{\mathrm{p-tr,L}}$, which causes the voltage drop across $L_{\mathrm{S,L}}$ and $L_{\mathrm{S,H}}$, respectively.

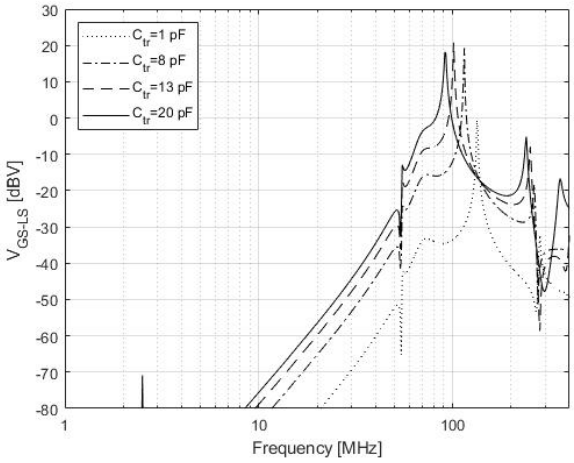

Fig. 11. Magnitude of the interference superimposed onto the LS gate-source voltage , $V_{\mathrm{GS-L}}$ vs. frequency, for $C_{\mathrm{p-tr,L}} = 1, 6, 13, 20\mathrm{pF}$.

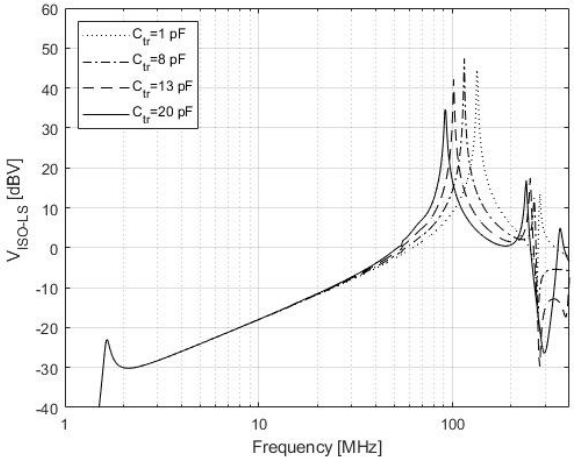

Fig. 12. Magnitude of the interference superimposed onto the LS gate driver isolation voltage , $V_{\mathrm{ISO-LS}}$ vs. frequency, for $C_{\mathrm{p-tr,L}} = 1, 6, 13, 20\mathrm{pF}$.

VI. Conclusions

The susceptibility to the radio frequency interference superimposed onto the AC outputs of switching circuits based on eGaN power transistors was investigated. A high frequency circuit of a switching leg comprising the stray inductances and capacitances of the active and passive components along with those due to intra and inter PCB wiring was defined. The analysis was carried out in the frequency domain referring to the closed loop bulk current injection test method.

The simulations highlighted that an RF current of magnitude $100\ mA$, which is induced in the output cable, affects the gate-source voltage of the HS and LS transistors. Particularly, that of the device driven to be switched off (the LS in the considered case) exceeds the transistor threshold, therefore cyclical commutations of the LS transistor induced by the interference occur. These cause unwanted shoot-through currents that can lead to temporary of permanent failures. Furthermore, it was highlighted that the gate drivers are also concerned by RF voltage across the isolation barrier, because its magnitude can exceed that required for global pins in DPI susceptibility tests.

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