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25 April 2026

Liquid Paste Interconnects on a Silicon Power Diode

Nick Baker, Francesco Iannuzzo, Szymon Bęczkowski

Abstract—**State-of-the-art power semiconductors use solid metal interconnects such as wire-bonding, soldering, and sintering. Thermo-mechanical stress degrades these solid metal interconnects and is the main cause of failure in power semiconductors. This letter demonstrates the use of liquid-metals, which are inherently resistant to thermo-mechanical stress, to package a Silicon power diode. The manufacturing process is performed below 80°C. The thermo-mechanical lifetime is assessed through power cycling and is shown to increase by factor of 3.3x in comparison to SAC305 solder and Aluminium wirebonded diodes. In addition, the thermal resistance of liquid-metal packaged diodes shows a 9% improvement. Corrosion and pump out of the liquid-metal is thought to be the failure mode.**

Index Terms—**Electronics packaging, power semiconductors, liquid-metals.**

I. INTRODUCTION

POWER Semiconductors are one of the fundamental components in electrified transport, electricity generation/distribution, and industrial machinery. According to representatives from the wind, solar, aircraft, automotive, and grid industries, power semiconductors are the component for which reliability is most critical [1].

The dominant stressor on power semiconductors is thermo-mechanical, and the size, weight, and cost of power electronic systems is directly related to this stress. The most vulnerable components within a power semiconductor are the solid metal interconnects [2]. These are most commonly wire-bonding, soldering, or sintering based – solid metals that are physically welded together. Thermal cycling during operation leads to expansion and contraction of these materials and their eventual failure, as shown in Fig. 1. As a result, the semiconductor, and system components (such as capacitors, inductors, and cooling systems) must be oversized to ensure reliability.

Several advanced interconnects have been proposed including Copper (Cu) wire-bonding [3], Cu sintering [4], Bond Buffers [5], Silver Sintering [6], Cu Nanowires [7], and more [8]. However, these technologies are vulnerable to the same inherent weakness as all solid metal interconnects (thermo-mechanical stress). In addition, some of these technologies require a higher temperature and higher-pressure manufacturing process, which reduces yield and increase costs.

Liquid-metals (LMs), on the other hand, are inherently resistant to thermo-mechanical stress. "Liquid-metal" is a term generally used to describe metals that maintain liquid phase at room temperature. Most often, the focus is on Gallium (Ga) and Ga-based alloys for applications ranging from stretchable electronics, soft-sensors, robotics, drug delivery, and thermal interface materials [9].

Fig. 1. Thermo-mechanical failures of state-of-the-art power semiconductor interconnects [3].

Gallium melts at 29.8°C, however it can be combined with other metals to form alloys with melting points down to 10°C. Nevertheless, although Ga experiences supercooling, solidification can still occur if used in automotive, industrial, or military applications, where operation at ambient temperatures down to -55°C may be required.

Considering that the operating range of a power device may reach 200°C (for wide-bandgap devices), the choice of metals that may be liquid in this range can be increased. This would include Indium, Bismuth, and several other metallic alloys.

Therefore, it could be expected that the use of LMs in electronics packaging will require the 'liquid' interconnect to transition back and forth between the solid- and liquid-phase during normal operation of the device. By transitioning from solid- to liquid-phase, either routinely during operation or using a predefined routine (i.e., periodically increasing the junction temperature to the melting point of the metal), an opportunity presents itself to manufacture a device with interconnects that can repair the degradation that forms in solid interconnects.

This article manufactures a 600 V Silicon (Si) diode using a Ga-based LM for die-attach, and an Indium-based LM for the topside connection. The topside connection, therefore, transitions from solid to liquid during normal operation of the diode. The package uses a pressure device made from Silicon rubber to minimize the bondline thickness and contain the LM. In this article, the thermal resistance and power cycling capability of the package is assessed and compared to SAC305 solder and Aluminium (Al) wirebonded diodes.

II. LIQUID METAL INTERCONNECTS

A. Prior Literature

LMs have been widely investigated as thermal interface materials and are now deployed in commercial products such as ASUS ROG laptops and the Sony PlayStation 5. For use as electrical interconnects, investigations are more limited. Pure Gallium and Indium have an electrical conductivity that is approximately 1/8th and 1/5th of Cu, and therefore may be overlooked for use interconnect applications.

In microelectronic applications, [10] investigates the use of Ga-based LM for flip-chip packaging, while [11] uses Ga-based

nanoparticles for Land-Grid-Array packaging. In both cases, a well/socket is used to house the LM.

In power electronic applications, [12] demonstrates the use of Ga-based LM for die-attach of a SiC MOSFET. In this case, a cavity is used in the Cu substrate and the chip floats in the LM. In [13], a Ga-based LM is used for the topside interconnect on a Silicon diode. Again, a cavity is used in the Cu plane to house the LM. Furthermore, the Al surface of the chip is coated with Titanium to prevent reaction with Ga. In [14], an Indium-based LM is used to manufacture a press-pack Si IGBT. Some patents on power devices exist, which again include methods for cavity or encapsulation to constraint the LM [15][16].

B. Liquid Metal Interconnects on a Silicon Power Diode

Fig. 2 displays an LM packaged 600 V Si diode. A Ga-based LM paste is used for the die-attach. The paste contains particles of Ga Oxide and can be manufactured by stirring Ga in air. The manufacturing process is detailed in [17]. For the topside connection, pure Field's Metal (melting point of 62°C) is used to avoid reaction between Ga and Al.

The LMs interface the diode to a Cu clip and an Al Insulated Metal Substrate metallized with 140 µm of bare Cu. Solder mask is present on the substrate; however, this is only used as a guide for diode placement. A35 Silicone rubber presses the diode into the substrate. Since Ga-based pastes have thermal conductivities around 50% less than Solder [17], it is essential to minimize the bondline thickness.

The LMs are contained through a combination of enhanced viscosity (in the case of the Ga-based paste), surface tension, and capillary forces acting on the LM. This is distinct compared to prior literature in Section II.A, which generally use some form of well, cavity, or encapsulation for containment.

C. Manufacturing Process

Only cotton swabs are used to apply the LM materials. The first step is to apply the higher melting temperature LM, Field's Metal, to the contact surfaces of the Cu clip and the diode. The two surfaces are then appended together and solidified. Fig. 3a displays the result. Following this, the Ga-based LM paste can be applied to each contact surface (die-attach side of the diode, and the Cur metal of the substrate). Gentle friction is used to induce wetting of the LM materials [18].

A key theme in LM research is intermetallic formation and wetting properties of the contact surface. Firstly, Al cannot be used near Ga-based LM materials, since the intermetallic formation completely corrodes the Al. For this reason, Field's Metal was chosen for the topside interconnect. The authors found wetting of the Al surface difficult, most likely due to the presence of Al Oxide, and the implications of this are shown in Section III. Other common metals such as Ni, Au, Ti, Cu, are subject of investigation [21][22]. For Cu, a CuGa intermetallic is formed that may have superior wetting properties to bare Cu [23]. The formation of this can take hours or days, and "consumes" the Ga so that the liquid is no longer present. The growth of this intermetallic may however saturate the Cu [22]. Therefore, a pre-aging process of the Cu surfaces was employed in this letter. The process is as follows: 1) Cu is cleaned with Zestron FA+; 2) the LM materials are applied through manual scrubbing; 3) The contact surfaces are placed on a hotplate at 180°C for 12 hours; 4) Excess LM is removed; 5) another layer of LM is applied again through manual scrubbing.

The result of this process after step 4 is shown in Fig. 3b, where intermetallic formation on the Cu pads can be seen.

After the above process, the Ga-based paste contact areas

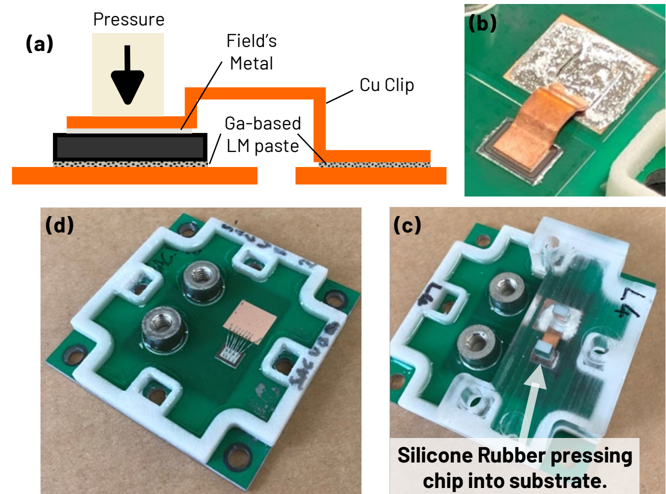

Fig. 2. (a) Cross section schematic (not to scale)
(b) LM packaged Si diode without lid, and (c) with lid
(d) Al wirebond and SAC305 solder packaged Silicon diode.

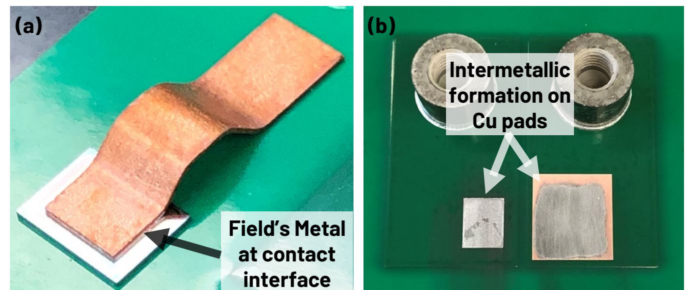

Fig. 3. (a) Diode and Cu clip appended with Field's Metal
(b) Cu metallization pre-aged before assembly. Intermetallic formation can be observed on both pads.

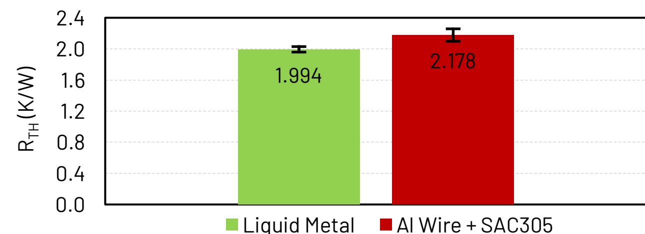

Fig. 4. $R_{TH(J-A)}$ of LM packaged Silicon Diode vs. Aluminium Wirebonded and SAC305 solder packaged Silicon Diode (6 samples each)

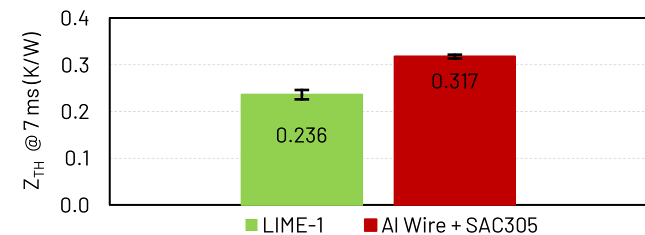

Fig. 5. Z_{TH} at 7-milliseconds measured at 24 A for LM package vs. Al Wirebond and SAC305.

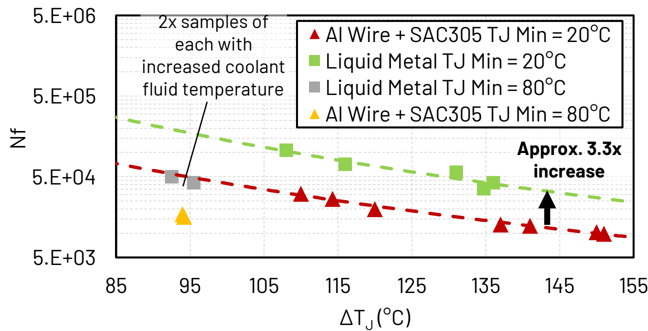

Fig. 6. Power cycling test results for LM packaged diode vs. SAC305 solder and Al Wirebond package.

can be appended. Fig. 2b shows the package at this stage, and the paste-like consistency of the Ga-based paste can be observed. The final step is to place a lid on the package, which contains the Silicone rubber pressure devices, to press the liquid contacts together. This process is also performed manually.

For comparison, a set of Si diodes were also manufactured using SAC305 solder and 8x 250 µm Al wirebonds (Fig. 2d).

III. Thermo-Mechanical Performance

A. Thermal Resistance

Thermal resistance (R_{TH}) was measured at 24 A with a heating and cooling period of 120 s. A Siemens Micred PowerTester 2400A was used, and junction temperature was measured using a sensing current of 50 mA. Fig. 4 displays the results from 6 samples of each group of diodes. LM packaging shows almost a 9% improvement in R_{TH}. In addition, the LM package shows a standard deviation of 0.022 K/W compared to 0.043 K/W. However, with such a small sample size, the variability and optimization of the manufacturing process remains an area for future research.

Additionally, work to locate the time for which the thermal impedance (Z_{TH}) is most dependent on the quality of the die-attach layer (by varying the solder void content) was performed on the same chip and substrate in [19]. This study identified approximately 7 ms after turn-off. Therefore, the Z_{TH} of the samples at 7 ms has been reproduced in Fig. 5 [20]. This shows a 25% improvement with LM packaging. However, in this case the standard deviation increased to 0.02 K/W from 0.008 K/W.

B. Power Cycling Capability

Power cycling was performed with on- and off-periods of 1 s. Cycling currents ranged from 23 A to 28 A, giving a range ΔT_J from 108°C to 151°C. Samples were cycled with constant current and the criteria for failure was either +5% V_{FWD} or +15% ΔT_J. Fig. 6 displays lifetime results. LM packaged diodes were observed to have a lifetime 3.3x higher than SAC305 and Al wirebonded diodes.

C. Failure Mechanism

All wirebonded diodes failed from a 15% increase in ΔT_J. LM packaged diodes on the other hand failed from a combination of +5% V_{FWD} and +15% ΔT_J.

An advantage of the LM packaging is that it enabled easy

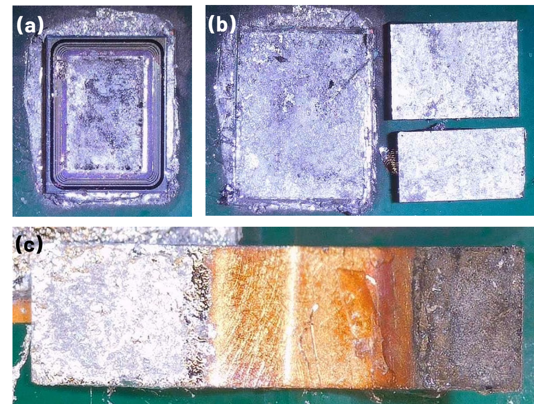

Fig. 7. Separation of LM package after power cycling. (a) Topside of Si diode (Field's metal interface); (b) Die-attach (Ga-based paste interface); (c) Cu clip (both)

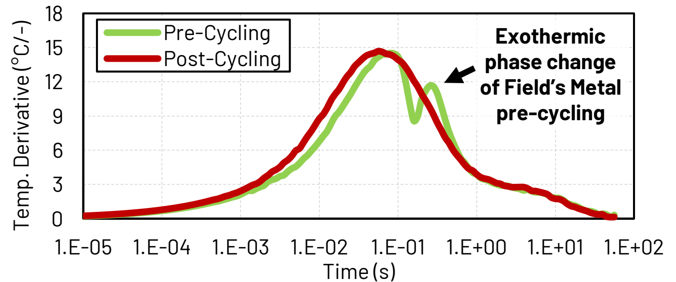

Fig. 8. Cooling rate over time from an $R_{TH(J-A)}$ measurement pre and post power cycling of an LM packaged diode.

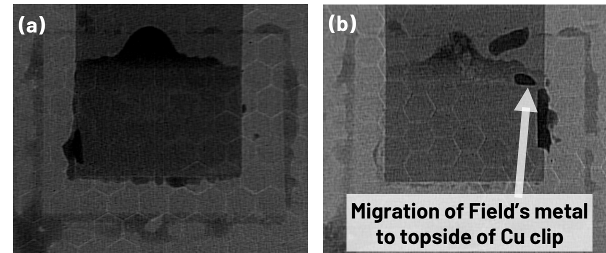

Fig. 9. (a) X-ray image of LM packaged diode before power cycling (b) X-ray image of LM packaged diode after power cycling

separation of parts for visual inspection. Fig. 7 shows images of each LM interface after separation from one sample. From visual inspection, the LM material present at each interface had decreased. For the die-attach, although the die was possible to separate at room temperature, force had to be used such that the chip cracked. This indicates that the pre-aging process of the Cu metal did not saturate the Cu such that intermetallic formation was stabilized. Optimization for such a process (optimum temperature, time, atmospheric conditions, and LM quantity) should be subject of future research, as well as use of other (more favourable) surface metals such as NiAu [21].

The interface between the Cu clip and the Cu pad, however, remained liquid. This interface, nevertheless, was not exposed to the high temperatures of the chip.

Regarding the Field's metal interface on the Cu clip, clear corrosion can be observed, and no liquid metal remained. This is also observed in post-power cycling R_{TH} measurements shown in Fig. 8. Since Field's metal melts at 62°C, it transitions from liquid-to-solid during the cooling process of an R_{TH} measurement. This is an exothermic process and therefore momentarily slows the cooling rate of the device. However,

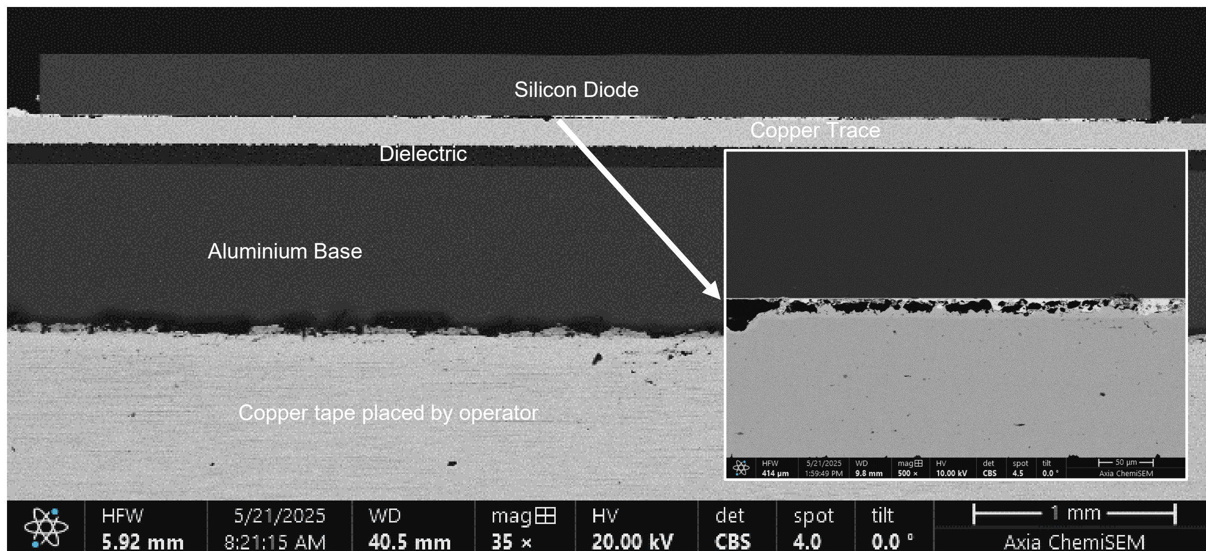

Fig. 10. Cross section of liquid-metal packaged Si diode, with Ga-based paste die-attach. 35x magnification.

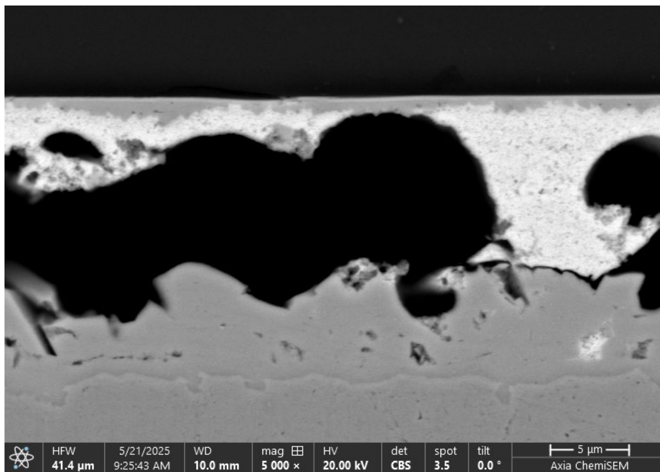

Fig. 11. 5000x magnification cross-section of Ga-based paste bond-line.

this is not present in the post-power cycling R_{TH} measurement.

Furthermore, pump-out of the Field's metal can be observed in X-ray images in Fig. 9. As further support for this, a supplementary video during power cycling is provided [24], which shows that Field's metal has migrated away from the chip surface, against the force of gravity. It is hypothesized that the wetting properties of Cu provide larger adhesive force to the Field's metal than the Al surface of the chip. Therefore, containment of LM is dependent on capillary forces imparted on the LM by the materials at the contact interfaces.

D. Intermetallic Formation in Die-Attach layer

A cross-sectional analysis was performed on one sample in order to estimate the bond-line thickness of the Ga-based die-attach and garner information on intermetallic formations shown in Fig. 3b. This analysis was performed more than 1-year after the conclusion of power cycling and thermal resistance experiments. Additionally, the sample assessed was not subject to high temperature operation. Fig. 10 displays the cross-section. Significant separation between the Si diode and Cu trace can be observed. Overall bond-line thickness is estimated to be between 10 µm to 15 µm.

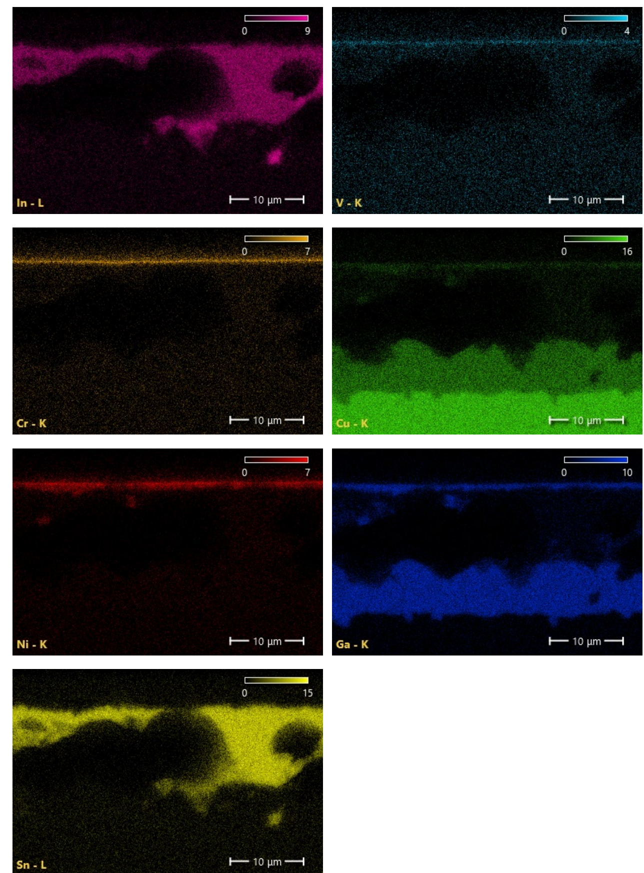

Fig. 12. EDS analysis and X-ray mapping of Ga-based paste bond-line. Correlated to Fig. 11.

Figs. 11 and 12 display the bond-line at higher magnification, as well as EDS analysis with X-ray mapping. The formation of CuGa intermetallic can be observed. The Ga-based paste was manufactured using an alloy including In and Sn. However, it appears from these images that the Ga has separated from the In and Sn. Only the Ga has diffused into the Cu substrate. In addition, the areas rich in Ga are observed only at the surface metals of the Si diode and at the Cu substrate. The In and Sn regions overlap in between the surface metals, and

little or no Ga is present in these areas. CuGa intermetallic formation appears non-uniform and between 5 µm to 8 µm in thickness. As a result, the initial bond-line thickness may have been below 10 µm – nevertheless, more investigation is needed on a larger number of samples. The diffusion of only Ga may also explain the separation and/or void-like structures in the bond-line. Furthermore, this analysis provides an explanation for Fig. 7b, where the chip cracked upon attempting separation: the remaining alloys in the bond-line (CuGa and InSn) are solid at room temperature.

V. Conclusion and Future Work

The thermo-mechanical performance of liquid metal interconnects on Silicon power diodes is assessed. Corrosion and pump-out of the liquid metal are found to be the failure mode. Power cycling using long cycle times, and time-based studies, should be performed to increase the time at high temperature and further assess the corrosion failure mechanism. Additionally, metallization in the liquid metal contact area appears to contribute to pump-out and is an area for future work.

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