POLITECNICO DI TORINO
Repository ISTITUZIONALE

Numerical Model for 32-Bit Magnonic Ripple Carry Adder

Original
Numerical Model for 32-Bit Magnonic Ripple Carry Adder / Garlando, Umberto; Wang, Qi; Dobrovolskiy, Oleksandr V.; Chumak, Andrii V.; Riente, Fabrizio. - In: IEEE TRANSACTIONS ON EMERGING TOPICS IN COMPUTING. - ISSN 2168-6750. - STAMPA. - 11:3(2023), pp. 679-688. [10.1109/TETC.2023.3238581]

Availability:
This version is available at: 11583/2985768 since: 2024-02-07T15:52:46Z

Publisher:
IEEE

Published
DOI:10.1109/TETC.2023.3238581

Terms of use:

This article is made available under terms and conditions as specified in the corresponding bibliographic description in the repository

Publisher copyright

(Article begins on next page)

28 April 2024

Numerical Model for 32-Bit Magnonic Ripple Carry Adder

Umberto Garlando, *Member, IEEE*, Qi Wang, Oleksandr V. Dobrovolskiy, *Senior Member, IEEE*, Andrii V. Chumak, *Senior Member, IEEE*, and Fabrizio Riente, *Member, IEEE*

***Abstract*—In CMOS-based electronics, the most straightforward way to implement a summation operation is to use the ripple carry adder (RCA). Magnonics, the field of science concerned with data processing by spin waves and their quanta magnons, recently proposed a magnonic half-adder that can be considered as the simplest magnonic integrated circuit. Here, we develop a computation model for the magnonic basic blocks to enable the design and simulation of magnonic gates and magnonic circuits of arbitrary complexity and demonstrate its functionality on the example of a 32-bit integrated RCA. It is shown that the RCA requires the utilization of additional regenerators based on magnonic directional couplers with embedded amplifiers to normalize the magnon signals in-between the half-adders. The benchmarking of large-scale magnonic integrated circuits is performed. The energy consumption of 30 nm-based magnonic 32-bit adder can be as low as 961 aJ per operation with taking into account all required amplifiers.**

***Index Terms*—Compact model, magnon, magnonic circuits, spintronics.**

I. Introduction

OVER the last years, spin waves (SWs) and their quanta – magnons – have attracted much attention due to their potential applications as data carriers in future data processing technologies [1]–[7]. Spin waves are propagating disturbances in the spin order of a solid body which occurs without any motion of electrons and, thus, without Joule heating [8]–[11]. Moreover, the phase of spin wave provides additional degrees of freedom (beyond amplitude) to code information, and the features of waves (de/constructive interference, diffraction, etc.) simplify the design structure of wave-based logic gates [6], [12], [13]. Furthermore, the GHz to THz frequency range, the nanoscale wavelength, which is limited downwards only by the lattice constant of the magnetic material used, and the pronounced versatile nonlinear spin-wave phenomena are unique features compared to acoustic waves, and electromagnetic microwaves [14]–[17], which makes them promising for Boolean and unconventional (e.g., neuromorphic) computing as well as for RF applications [1], [18]–[21]. Benchmarking of a recently presented first magnonic integrated circuit in the form of a half adder [6] has shown that magnonic circuits can outperform CMOS devices in terms of energy consumption by up to ten times. A 30-nm-based magnonic half adder has a comparable footprint to a 7-nm-based CMOS half adder but requires 18 ns to process data as opposed to 0.3 ns for CMOS with a 3 GHz clock speed. A further improvement of at least an order of magnitude in all the properties is expected using the recently reported inverse-design magnonics [22], [23]. Nevertheless, the field of magnonics is still positioned primarily in the academic physics domain rather than engineering/manufacturing. Despite its dynamic development (see recent roadmap [21]), several obstacles still have to be overcome. As discussed in this manuscript, the need for efficient transducers to convert spin waves into electrical signals and for highly-efficient low-energy amplifiers is considered the most important challenge.

Several magnonic devices have already been demonstrated at the early stage of single logic gate level, including spin wave logic gates [24], [25], majority gates [13] and magnon transistors [26], [27]. In general, one can define two main approaches for the construction of magnonic circuits: the first one can be named a "converter-based" and relies on the utilization of highly efficient magnon-to-current converters used after each operation with data [20], [28], [29]. The magnonic circuits based on this approach were first introduced and described in [20]. Moreover, the crucial challenges of the realization of fanout and normalization were solved in [30], [31]. The other approach is named "all-magnon" and, although some conversion from magnon to current is still required, aims for the minimization of the converters number via the utilization of natural strongly-pronounced magnonic nonlinear phenomena [26]. Recently, a nanoscale magnonic directional coupler was realized, and its nonlinear functionality was demonstrated experimentally [6], [31]. Furthermore, it was shown numerically that a magnonic half-adder, consisting of an XOR logic gate and AND logic gate, can be realized by combining two directional couplers into a circuit. The half-adder was specially designed to be applicable for further integration after a low-energy amplifier is added [6].

Manuscript received 5 November 2021; revised 19 December 2022; accepted 18 January 2023. Date of publication 26 January 2023; date of current version 6 September 2023. This work was supported by European Research Council (ERC) under the European Union's Horizon 2020 research and innovation programme under Grant 678309. *(Corresponding author: Fabrizio Riente.)*

Umberto Garlando and Fabrizio Riente are with the Department of Electronics and Telecommunications, Politecnico di Torino, 10129 Torino, Italy (e-mail: umberto.garlando@polito.it; fabrizio.riente@polito.it).

Qi Wang, Oleksandr V. Dobrovolskiy, and Andrii V. Chumak are with the Faculty of Physics, University of Vienna, A-1090 Vienna, Austria (e-mail: qi.wang@univie.ac.at; oleksandr.dobrovolskiy@univie.ac.at; andrii.chumak@univie.ac.at).

Digital Object Identifier 10.1109/TETC.2023.3238581

This work is licensed under a Creative Commons Attribution 4.0 License. For more information, see http://creativecommons.org/licenses/by/4.0/

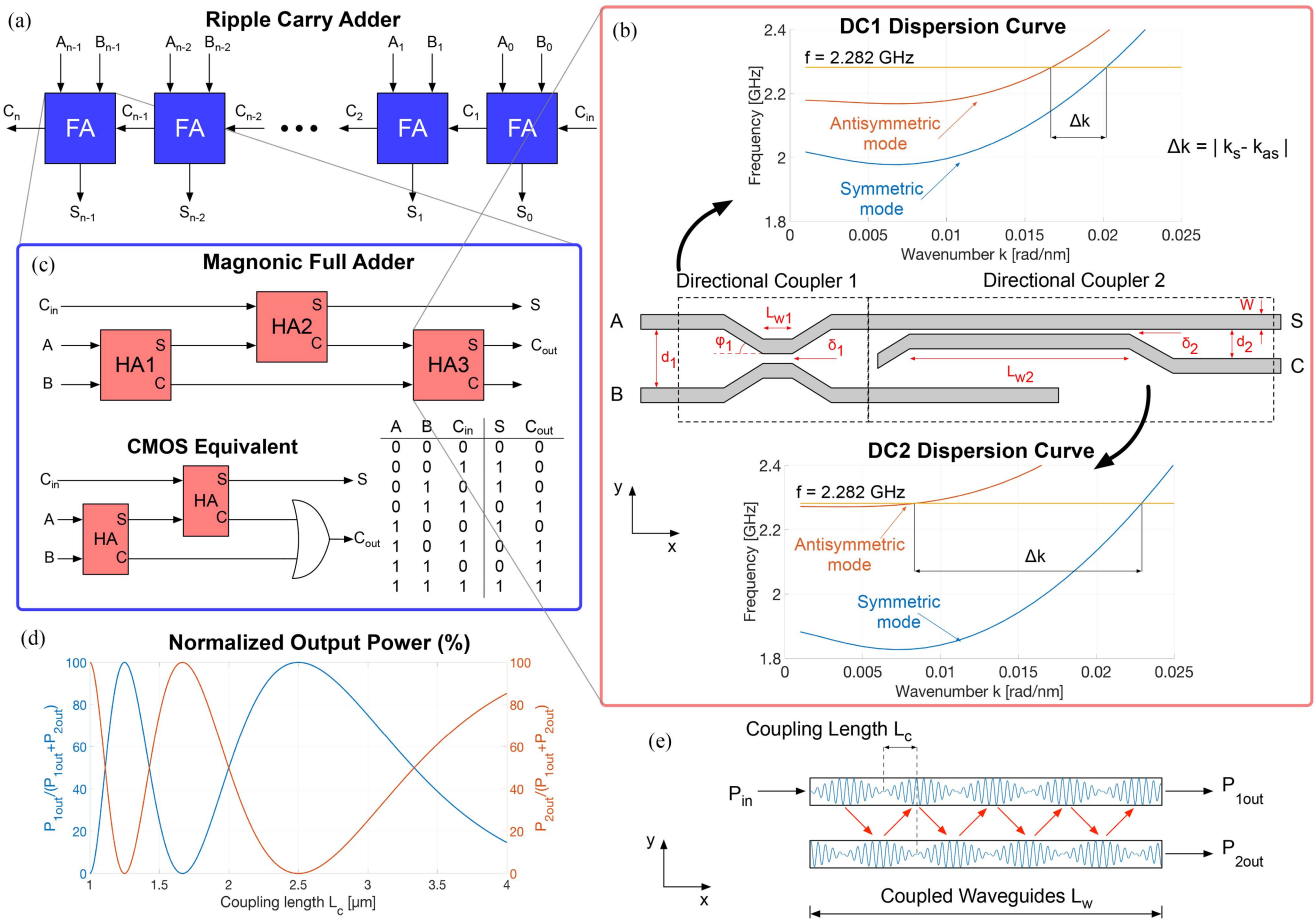


Figure 1. Sketch of the investigated system: a) N-bit ripple carry adder design; b) Zoom of the most important magnonic block, the half adder. The top and bottom graphs depict the dispersion curves of the "symmetric" (s) and "antisymmetric" (as) lowest collective spin wave modes of a pair of coupled waveguides, the DC1 (operating in the linear regime) and the DC2 (operating in the non-linear regime), respectively. The central image depicts the design of the magnonic HA where all the dimensions involved are reported; c) Schematic representation of a magnonic full adder (top) and its CMOS equivalent representation (bottom) with the corresponding truth table; d) Normalized output power as a function of the coupling length L_c for a fixed length of the coupled waveguides $L_w = 4\,\mu$m without damping; e) Schematic representation of the periodic energy exchange between two coupled spin wave waveguides.

Nevertheless, the circuitry which would allow for synchronous operation of many such devices together to perform complex arithmetic operations was far beyond the scope of the previous investigations since such simulations are computationally too expensive and unfeasible. Indeed, increasing the number of elements makes impossible to perform physical simulations in a reasonable amount of time. The high accuracy achievable with that approach has high computational costs and can require a significant amount of time. For those reasons, compact models are fundamental for the exploration of emerging technologies and the same approach is adopted with standard CMOS technologies. Compact model plays a crucial role in designing integrated circuits and serves as a bridge to share the information between technologist/physics and circuit designers. Here, we present a numerical model which allows for the realization of complex all-magnon circuits based on the functional blocks of the previously studied half-adder [6]. The model is demonstrated on the example of a 32-bit integrated ripple carry adder and is made openly available on Github (https://github.com/vlsi-nanocomputing/spinwaves-model). We conclude that complex magnon circuits require the utilization of additional regenerators with embedded amplifiers to restore degraded magnon signals in-between the half-adders. The benchmarking of large-scale magnonic integrated circuits is performed.

II. Magnonic Adder Structure and Operational Principle

Among combinational circuits, the most straightforward way to implement a summation is to use the ripple carry adder (Figure 1(a)). In many computer architectures, adders are used in the arithmetic logic unit and other processor parts.

The fundamental element of such an adder is the full adder (FA). Multiple full adders can be cascaded in parallel to add N-bit operands. As suggested by its name, the carry-out bit is rippled into the next stage in this implementation. The full adder adds binary numbers, particularly it sums three inputs (A_i, B_i, C_{i-1}) and produces two outputs (S_i, C_{i+1}), which represent the sum and the carry-out, respectively. It can be implemented in many ways, and one example is reported in Figure 1(c). The

structure depicted in Figure 1(b) is based on the half adder (HA), which is the most important magnonic building block to perform logic computation [6]. In particular, the design proposed in this paper uses three magnonic half adders. The implemented logic function is reported in (1) and (2), for the sum and carry respectively, where the over brackets represent the operation performed by every HA.

$$S = \overbrace{\overbrace{A \oplus B}^{\text{HA1}} \oplus C_{in}}^{\text{HA2}} \tag{1}$$

$$C_{out} = \overbrace{\overbrace{(A \cdot B)}^{\text{HA1}} + \overbrace{(C_{in} \cdot \overbrace{(A \oplus B)}^{\text{HA1}})}^{\text{HA2}}}^{\text{HA3}} \tag{2}$$

From Figure 1(c) it is possible to observe that the third magnonic HA is used only as OR gate. For the sake of clarity, the CMOS equivalent and its truth table are reported in Figure 1(c).

The magnonic half adder is composed of two directional couplers (DCs), one operating in the linear regime and the other in the non-linear regime [6], they are named DC1 and DC2 respectively (Figure 1(b)). In both cases, the dispersion curve splits into symmetric (s) and antisymmetric modes (as) due to the dipolar interaction between the parallel waveguides, as depicted in both graphs in Figure 1(b). The dispersion relations have been obtained considering $M_s = 1.4 \times 10^5 \mathrm{Am}^{-1}$, exchange stiffness $A = 3.5 \times 10^{-12} \mathrm{J/m}$ and the following geometrical parameters: $L_{w1} = 370\,\mathrm{nm}$, $d_1 = 450\,\mathrm{nm}$, $\varphi_1 = 20\,^\circ$, $\sigma_1 = 50\,\mathrm{nm}$, $L_{w2} = 3\,\mu\mathrm{m}$, $d_2 = 210\,\mathrm{nm}$, $\varphi_2 = 20^\circ$, $\sigma_2 = 10\,\mathrm{nm}$. When the excited spin wave is above the minimum of the antisymmetric mode ($f = 2.282\,\mathrm{GHz}$ in Figure 1(b)) both modes can be excited simultaneously in the coupled waveguides. The two modes have the same frequency but different wavenumber (k_s, k_{as}) that result in a different phase accumulation. The interference of these two modes result in energy exchange between the dipolar coupled waveguides. There is a periodic exchange of energy between the spin waves in one waveguide to the other and vice-versa, which is named coupling length L_c. This phenomenon is schematically represented in Figure 1(e) and can be calculated as:

$$L_c = \frac{\pi}{\Delta k_x} = \frac{\pi}{|k_s - k_{as}|} \tag{3}$$

The coupling length depends on different parameters such as the spin wave wavelength, spin wave power, and geometrical parameter of the waveguide [32]–[34]. The DC1, working in the linear regime, operates as a power splitter, while the DC2, working in the non-linear regime, operates both as AND/XOR gate [6]. Figure 1(d) shows the normalized output power in the coupled waveguides as a function of the coupling length L_c. It can be expressed using the (4).

$$\frac{P_{1out}}{P_{1out} + P_{2out}} = \cos^2\left(\frac{\pi L_w}{2L_c}\right), \tag{4}$$

where L_w represents the length of the coupled region. The normalized output power expression shows that the length of the coupled region and the coupling length play a crucial role in terms of power splitting and the functionality of the directional couplers.

It must be emphasized that in these studies, we do not consider a transducer between electrical and magnonic signals since we assume that a spin wave with the correct amplitude comes from another magnonic unit into the adder under investigations. The "all-magnon approach" assumes that conversion is only required twice at the input and the output of the entire magnonic chip and that the efficiency of such conversion does not play a significant role. Thus, any of the known approaches can be used for the excitation and detection of spin waves [20], [21].

III. Compact Physical Model

The most accurate approach to obtain the dispersion relation of two coupled waveguides is to solve the Landau-Lifshitz equation for the magnetization dynamics [33]. However, this approach is too complex and computationally expensive to be integrated within a tool for circuit-level exploration. On the other hand, the compact physical model presented keeps high accuracy, providing the flexibility to explore magnonic circuits considering their physical properties. It is openly available on Github https://github.com/vlsi-nanocomputing/spinwaves-model.

The model we developed describes the dispersion relation of the DC1 and the DC2 depending on the geometrical characteristics of the couplers and the spin wave amplitude. It considers damping losses and the non-uniform width profile of the fundamental spin wave mode of the waveguide [33], [35], [36]. The effective width (w_{eff}) of the waveguide can be larger than the nominal width (w) when the effective pinning decreases [33]. A change in the dispersion curve results in a variation of the coupling length L_c and, as a consequence, in a different output power partition. The expression for computing the dispersion relation of two coupled waveguides is reported in (5)

$$f^{nl}_{a,as}(k_x, a_k) = f^0_{s,as}(k_x) + T_k |a_k|^2, \tag{5}$$

where $f^0_{s,as}(k_x)$ represents the dispersion relation for the symmetric and antisymmetric spin wave modes in coupled waveguides at linear region, T_k is the nonlinear frequency shift coefficient [37] in the isolated waveguide and a_k is a dimensionless quantity and represents the spin wave amplitude (see Simulation Method).

In general, the directional couplers are the core elements in magnonic circuits consisting of three main regions. Two oblique branches (opening/closing arms) are represented by regions 1 and 3 in Figure 2 and the region 2 shows the coupled region where the waveguides are parallel to each other. Most of the energy exchange between the coupled waveguides is observed in region 2, where the gap σ is very small, 50 nm and 10 nm for the DC1 and DC2 respectively (100 nm technology node). However, there is an additional contribution coming from regions 1 and 3. Starting from the power partition formula reported in (4) it is possible to define the number of jumps along the coupled region 2 as $N = L_w/L_c$. Substituting in (4), the equation can be rewritten as $\cos^2\left(\frac{\pi}{2}N\right)$. The number of jumps from one waveguide to the other is defined by the subsequent constructive

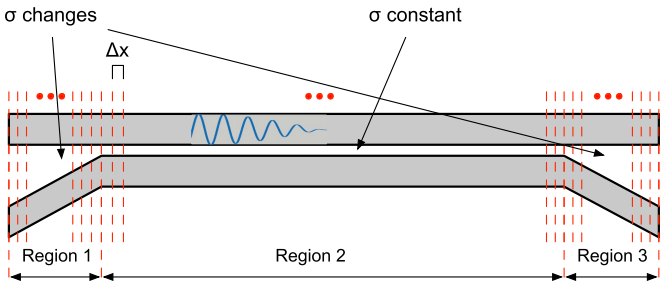


Figure 2. The directional coupler can be divided into three regions: regions 1 and 3 show an increasing/decreasing distance between the two waveguides and region 2 where the gap is constant. The main contribution to the dispersion curve comes from region 2. The introduced discretization along the x axis makes it possible to take into account the additional coupling introduced by the opening/closing arms (region 1 and region 3).

and destructive interference. When the phase difference between the two modes is 180° ($\Delta\varphi = \pi$) all the power is transferred to the other waveguide. Therefore, along the coupled region, the mode can perform a number of jumps equal to N with an overall phase accumulation of πN. Thus, (4) can be rewritten as:

$$\frac{P_{1out}}{P_{1out} + P_{2out}} = cos^2\left(\frac{\Delta\varphi}{2}\right) \tag{6}$$

The coupling length L_c depends on the initial dispersion curve and the nonlinear frequency shift coefficient, which in turn depends on the spin wave power within the directional coupler. If the waveguide considered is not ideal but with losses, the spin wave power is not constant along the propagation direction. In the real case, the spin wave amplitude decreases as an increase of propagation distance according to an exponential decay: $e^{(-|2x|/x_{freepath})}$, where x is distance, $x_{freepath}$ is decay length which can be calculated using the formula 4 in [38]. As a consequence, (4) is not sufficient because it only considers a constant coupling length, while L_c is continuously varying along the waveguide due to the space-dependent spin wave power. The equation is rewritten introducing the concept of average coupling length ($L_{a,avg}$) according to (7),

$$L_{a,avg} = \frac{\pi L_w}{\Delta\varphi} \tag{7}$$

The phase accumulated between the two modes can be obtained by integrating the wavenumber variation along the propagation direction $\Delta\varphi = \int |k_s - k_{as}| dx$. In our model, the directional coupler is discretized along x direction with step size of Δx in a total number of M. As a consequence, the phase accumulated $\Delta\varphi$ can be computed as:

$$\Delta\varphi = \sum_{i=1}^{M} \Delta k_i \Delta x \tag{8}$$

For each subinterval i, the difference between the two wavenumbers is recalculated. Additionally, the model considers the coupling introduced by the opening/closing arms. Thus, regions 1 and 3 are discretized, but here the gap is varying. For those regions, the calculation starts from the unshifted dispersion relation, which depends on the gap σ. In this way, the cumulative phase accumulation makes it possible to correctly estimate the average coupling length and, therefore, the output power partition.

IV. Simulation Method

Dispersion relation

The numerical model developed considers two technology nodes, the 100 nm and the 30 nm, where the node represents the waveguide width. We considered the following parameters for yttrium iron garnet (YIG): the saturation magnetization $M_s = 1.4 \times 10^5 \mathrm{Am}^{-1}$, the damping $\alpha = 2 \times 10^{-4}$ and exchange stiffness $A = 3.5 \times 10^{-12} \mathrm{Jm}^{-1}$. YIG was chosen for its low spin-wave damping [21], but the concept developed here should also be suitable for any other magnetic material. The dispersion relation of the spin wave mode in an isolated waveguide is expressed by (9) according to the work in [33].

$$\begin{aligned} f_0(k_x) &= \frac{1}{2\pi}\{\Omega^{yy}\Omega^{zz}\}^{1/2} \\ &= \frac{1}{2\pi}\Big\{\left(\omega_H + \omega_M(\lambda^2 k_x^2 + F_{k_x}^{yy}(0))\right) \\ &\qquad \left(\omega_H + \omega_M\left(\lambda^2 k_x^2 + F_{k_x}^{zz}(0)\right)\right)\Big\}^{1/2} \end{aligned} \tag{9}$$

where:

- $\Omega^{ii} = \omega_H + \omega_M(\lambda^2 k_x^2 + F_{k_x}^{ii}(0))$, i=y, z.
- $\omega_H = \gamma B_{ext}$, γ is the gyromagnetic ratio, and B_{ext} is external magnetic field.
- $\omega_M = \gamma\, M_s$, M_s is the saturation magnetization.
- $\lambda = \sqrt{2\,A/(\mu_0 M_s^2)}$ is the exchange length, A is the exchange stiffness, and μ_0 is permeability of vacuum.
- $\hat{F}_{k_x}$ is a tensor that describes the dynamical magneto-dipolar interaction.

The tensor $\hat{F}_{k_x}$ calculation developed by Beleggia et al. can be calculated using the Fourier-space approach [39]:

$$\hat{F}_{k_x}(d) = \frac{1}{2\pi}\int_{-l}^{+l} \hat{N}_k e^{ik_y d}\, dk_y \tag{10}$$

$$\hat{N}_k = \frac{|\sigma_k|^2}{\widetilde{w}} \begin{pmatrix} \frac{k_x^2}{k^2} f(kh) & \frac{k_x k_y}{k^2} f(kh) & 0 \\ \frac{k_x k_y}{k^2} f(kh) & \frac{k_y^2}{k^2} f(kh) & 0 \\ 0 & 0 & 1 - f(kh) \end{pmatrix} \tag{11}$$

where:

$$\sigma_k = 2\frac{k_y \cos\left(\frac{\kappa w}{2}\right)\sin\left(\frac{k_y w}{2}\right) - \kappa cos\left(\frac{k_y w}{2}\right)\sin\left(\frac{\kappa w}{2}\right)}{k_y^2 - \kappa^2} \tag{12}$$

$$\widetilde{w} = \frac{w}{2}\left(1 + sinc\left(\kappa w\right)\right) \tag{13}$$

$$f(kh) = 1 - \frac{1 - e^{-kh}}{kh} \tag{14}$$

$$k = \sqrt{k_x^2 + k_y^2} \tag{15}$$

and h is the waveguide thickness, which is equal to 30 nm and 10 nm for the 100 nm and 30 nm technology node respectively.

The tensor $\hat{F}_{k_x}(d)$ represents the self-dipolar interation when $d = 0$ and represents the dipolar interation between waveguides when computed at distance d. In the case of the isolated waveguide, the $d = 0$ and the integral limitation $l = 10$. Note that in the ideal case, l could be infinite. However, the main contributions of this integral are around $l = 0$.

Starting from these considerations, it is possible to obtain the dispersion relation of two coupled waveguides [33]. The split between the symmetric and the antisymmetric mode depends on the dipolar interaction and can be computed according to (16).

$$f_{s,as}(k_x) = \frac{1}{2\pi}\sqrt{(\Omega^{yy} \pm \omega_M F_{kx}^{yy}(d))(\Omega^{zz} \pm \omega_M F_{kx}^{zz}(d))} \tag{16}$$

where:

- $\Omega^{ii} = \omega_H + \omega_M(\lambda^2 k_x^2 + F_{k_x}^{ii}(0))$, i=y, z.
- $d = w + \delta$, w is the width of the waveguides, and δ represents the gap between the two waveguides center to center.
- $F_{k_x}^{ii}(d)$ is calculated according to (10).

In the coupled waveguides, the profile of the spin wave is slightly different compared to the single waveguide [6]. However, the (16) could not take into account the difference. To compensate this error, a solution is to reduce the integral limitation l of (10).

In our case, the integral limitation is changed in the 100 nm technology node, reduced from 10 to 0.53 for DC1 and 0.63 DC2. The simulated and calculated dispersion curves are well matched in this case. This indicates that a slight change in the gap does not dramatically change the spin wave profile The dispersion relation calculation for isolated and coupled waveguides makes it possible to obtain the associated wave number and compute the signal propagating in large circuits.

Geometry: The physical geometries of the diretional couplers depicted in Figure 1(b) are strictly related to the adopted technology node. For the 100 nm YIG the main geometrical quantities for the DC1 are: $L_{w1} = 370$ nm, $d_1 = 450$ nm, $\varphi_1 = 20°$, $\sigma_1 = 50$ nm. The DC2 is based on the following dimensions: $L_{w2} = 3$ μm, $d_2 = 210$ nm, $\varphi_2 = 20°$, $\sigma_2 = 10$ nm. The sizes involved in the DC1 and DC2 when considering the 30 nm YIG are: $L_{w1} = 230$ nm, $d_1 = 50$ nm, $\varphi_1 = 20°$, $\sigma_1 = 20$ nm, $L_{w2} = 2460$ μm, $d_2 = 70$ nm, $\varphi_2 = 20°$, $\sigma_2 = 10$ nm.

Metrics: The compact physical model described to evaluate the signal propagation on every node of the circuit can also be used to extract metrics for analyzing the circuit performance. The model considers the physical geometry of directional couplers, such as the waveguide width and material properties like the gyromagnetic ratio, the damping, the saturation magnetization and the exchange stiffness. The model enables the estimation of the following metrics: occupied area, propagation delay and the energy consumption.

The area occupation can be estimated considering the bounding box that encloses every directional coupler.

$$A_{DC} = w_{DC} * L_{DC} \tag{17}$$

where w_{DC} represents the width of the DC and it is equal to $2\,w + 4 \cdot 5\,h$ (w and h are the width and the thickness respectively) [6]. The quantity $5\,h$ is related to the physical geometry and it is used to compute the minimum distance between two waveguides to have negligible dipolar coupling. The quantity L_{DC} refers to the physical length of coupler and can be computed as $L_w + 2\frac{5h}{sin\varphi}$, where φ is the angle of the opening/closing arms of the waveguide. The same approach is applied for computing the bounding box of the regenerators and therefore estimating the overall area of the circuit.

The input-output delay accumulated by every magnonic element can be estimated considering the entire length of every magnonic block divided by the spin wave group velocity. Being the group velocity dependent on the wave number, the model considers the contribution introduced by the three regions discussed in the Section III. Regions 1 and 3 model the propagation delay as dependent by the spin wave propagating within an isolated waveguide (k_0). On the other end, region 2 considers the propagation of the two modes that have a different delay. In general, the contribution from every zone can be computed as $\tau_{zone_i} = L_{zone_i}/v_{gr_i}$. To evaluate the overall computation time of a single device, all the contributions are summed together considering the largest delay introduced by region 2 (the worst-case scenario):

$$\tau_{DC} = \tau_{zone_1} + \max\{\tau_{zone_2}^{s}, \tau_{zone_2}^{as}\} + \tau_{zone_3} \tag{18}$$

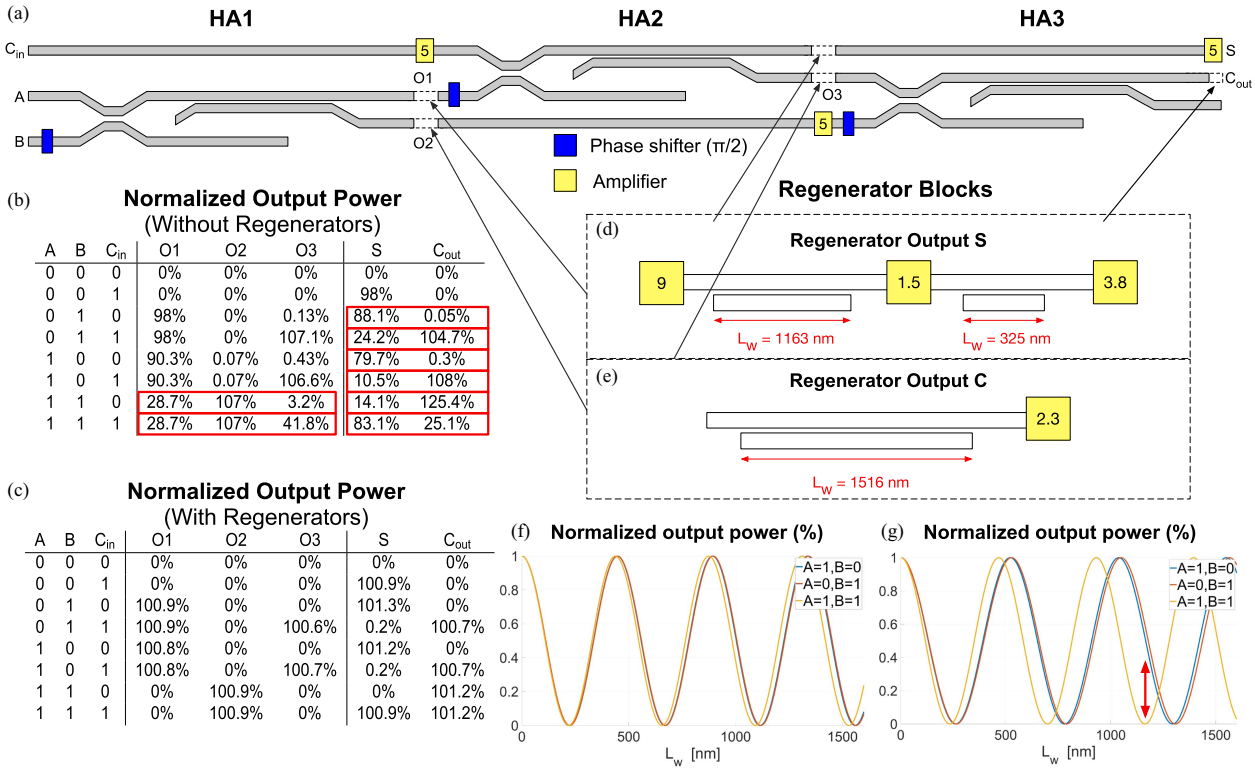
This approach is applied to every directional coupler. For example the HA described in this paper is composed of two directional coupler (DC1 and DC2) and two regenerator blocks, one for the output S and one for the output C. The two regenerators do not have the same length resulting in two different delays:

$$\tau_{HA_S} = \tau_{DC_1} + \tau_{DC_2} + \tau_{reg_S} \tag{19}$$

$$\tau_{HA_C} = \tau_{DC_1} + \tau_{DC_2} + \tau_{reg_C} \tag{20}$$

The delay introduced by the amplifier and phase shifter are considered negligible in this preliminary version of the model. The computed delay is then transferred to the subsequent computing elements up to the output.

The energy consumption is calculated as the sum of the spin wave excitation (E_{SW}) and the VCMA amplifier (E_{amp}). The energy required to excite the spin wave and required by the VCMA amplifier was estimated in [6] (see supplementary information, which can be found on the Computer Society Digital Library at http://doi.ieeecomputersociety.org/10.1109/TETC.2023.3238581) as 12.3 aJ and 3 aJ per operation, respectively. The estimates are performed analytically for CoFeB ultra-thin films with pronounced VCMA efficiency. The amplifiers with the required parameters have not yet been realized, although significant progress towards their development has been reported in [40]. These quantities refer to the 100nm node. Scaling the technology to the 30 nm the energy required to excite the spin wave is reduced to 1.96aJ. When a logic '0' is present at the circuit input, no spin wave is excited, and no power is dissipated. Therefore, the power consumption depends on the probability of the input to assume a logic '1' (excited spin wave). For the HA we considered for simplicity an input probability of



A	B	C_{in}	O1	O2	O3	S	C_{out}
0	0	0	0%	0%	0%	0%	0%
0	0	1	0%	0%	0%	98%	0%
0	1	0	98%	0%	0.13%	88.1%	0.05%
0	1	1	98%	0%	107.1%	24.2%	104.7%
1	0	0	90.3%	0.07%	0.43%	79.7%	0.3%
1	0	1	90.3%	0.07%	106.6%	10.5%	108%
1	1	0	28.7%	107%	3.2%	14.1%	125.4%
1	1	1	28.7%	107%	41.8%	83.1%	25.1%

A	B	C_{in}	O1	O2	O3	S	C_{out}
0	0	0	0%	0%	0%	0%	0%
0	0	1	0%	0%	0%	100.9%	0%
0	1	0	100.9%	0%	0%	101.3%	0%
0	1	1	100.9%	0%	100.6%	0.2%	100.7%
1	0	0	100.8%	0%	0%	101.2%	0%
1	0	1	100.8%	0%	100.7%	0.2%	100.7%
1	1	0	0%	100.9%	0%	0%	101.2%
1	1	1	0%	100.9%	0%	100.9%	101.2%

Figure 3. The layout of the design FA and regenerators: a) Full adder composed of three HA. Blue squares identify the phase-shifter block, while the yellow boxes represent the amplifiers. The numbers inside the yellow boxes represent the amplification factor. The outputs of the single HA are identified with labels; b) and c) Tables with the power distributions at the outputs of the FA and HAs without and with the regenerators. The values equal to 0% refer to the normalized output power lower than 1e-3%. d) and e) Layout and physical dimensions of the designed regenerator blocks with the 100 nm YIG node. The gap σ in all the regenerators is 10 nm; f) and g) Normalized output power as a function of the coupling length of DC2 of an HA for all the input combinations. f shows that it is not possible to find a coupling length that separate the case $A = B = 1$ ($S = 0$) from the other ($S = 1$); g) Presents the same plot after amplification by a factor 9 that increases the separation between the two logic values.

$P(A =' 1') = P(B =' 1') = 0.5$. The energy consumption can be computed as:

$$E_{HA} = P(A =' 1') \cdot E_{SW_A} + P(B =' 1') \cdot E_{SW_B} + \sum_{j}^{S} E_{amp_j}^{HA} \tag{21}$$

where E_{SW_A}, E_{SW_B} are the energy of excited spin wave for input A and B respectively. The last summation considers the contribution of the S amplifiers required by the magnonic HA including the regenerators. The HA is basic building block for construction more complex circuit. Therefore, the (21) can be easily extended to other magnonic circuits with N inputs and M HA as:

$$E_{HA} = \sum_{i}^{N} + P_i(i =' 1') \cdot E_{SW_i} + \sum_{j}^{M} E_{amp_j}^{HA} \tag{22}$$

where E_{SW_i} is the E_{SW} of the ith input with a probability P_i that it assumes a logic '1'.

V. Results

A. Magnonic Full Adder Design With Regenerators

The adoption of the aforementioned simulation model enabled the design of more complex structures. Cascading the HA [6] introduces degradation of the signals, which results in errors in the logical evaluation. The error generation when casting magnetic blocks and the need of output normalization was first mentioned in [31]. In magnonic circuits, the power available at the output identifies the logic values. In particular, a signal below 1/3 of the *Logic 1* power is considered as *Logic 0*. Amplifiers are used to restore the signals. However, after the amplification, some correctly evaluated values are fed to the following block, causing errors. The usage of amplifiers is not enough to guarantee correct information propagation. Figure 3(b) shows the normalized power available at different internal nodes of the FA depicted in Figure 3(a). The values highlighted in red show outputs that can cause errors if directly applied to the following blocks. These errors are because the HA outputs, when amplified and put as input to the following stage reduced the separation among logic values given the extreme non-linearity of DC2. To overcome this limitation, an additional element was introduced in the circuit, the regenerators. Thanks to the non-linearity of specifically designed directional couplers, these blocks increased the logical separation of the outputs. Figure 3(c) shows the output of the same circuit when the regenerators are considered.

The main functionality of the regenerators is to increase the guarantee correct logic values exploiting the magnonic characteristic. As presented in the previous section, the directional

couplers have a strong non-linearity, and they can be used to improve signal integrity. The idea is to design the length of the coupler to reduce the amplitude of the *Logic 0* outputs before the amplifier stage. By selecting the correct physical length, it is possible to attenuate the values close to "0" and amplify the "1". In this way, when the signal is amplified, the "1" is correctly restored to 100% energy, while the "0" is still close to 0% energy. The new DC is similar to DC2, operating in the non-linear regime, but only one output branch is considered. The other is used to dissipate unwanted power. Our approach is different from the one introduced in [31], where weak signals are allowed to propagate, and normalization is performed on signals higher than a certain threshold. Moreover, the "converter-based approach" of magnon computing requires a spin-to-charge conversion repeated with the clock rate of the processor and, thus, the renormalization of the spin-wave amplitude is automatically "embedded" into the conversion mechanism itself [28]. However, realizing such a transducer with the required efficiency is still an open challenge.

The design methodology is presented here using the HA as a case study. The output power available at the output *S* of the HA are named based on the input combination (case A = '0' and B = '0' is not reported since it refers to no input power):

- $S10$: when the HA input combination is A = '1' and B = '0'.
- $S01$: when the HA input combination is A = '0' and B = '1'.
- $S11$: when the HA input combination is A = '1' and B = '1'.

The normalized powers before the amplification are $S10 = 21.5\%$, $S01 = 23.3\%$ and $S11 = 6.8\%$. Figure 3(f) shows the curves for each output power over the length of the DC. The idea is to find the best length to ensure that the regenerator input power (the power of the output S) is entirely conserved for $S10$ and $S01$, but it is completely transferred to the dummy branch of the coupler for $S11$. Since the curves represent the percentage of power at the useful output of the DC, the best point on the curves is where $S10$ is almost 0, and the other powers are maximum. Unfortunately, the three curves are almost completely superposed, and it was not possible to find a suitable length for the new DC implementing the regenerator. An amplifier of value nine was inserted to increase the separation of the curves. In this way, the spin wave powers increase up to $S10 = 193.5\%$, $S01 = 209.9\%$ and $S11 = 61.56\%$. With the new values, it was possible to select a length of 1163 nm that resulted in the complete attenuation of $S11$ as showed in Figure 3. However, the drawback of the inserted DC was that $S10$ and $S01$ became 85% and 105% respectively. An additional DC was inserted to mitigate this difference: an amplifier by factor 1.5, followed by a DC 325 nm long and a final 3.8x amplifier. This final structure resulted in very similar output power for both signals $S10$ and $S01$, around 100%, and zero power for signal $S11$.

The same approach was used to design the regenerator for output C: a single DC with length 1516 nm and an amplifier by factor 2.3 was inserted in this case. Finally, an amplifier was inserted after a long piece of waveguide used to interconnect, for example, *O2* with the input of the last HA. The attenuation of the signal was evaluated using the model and compensated to ensure a correct evaluation of the outputs. Furthermore, a phase shift of $\pi 2$ is needed at one input of each HA [6]. A specifically designed block, which introduces a geometrical restriction of the waveguide [41], [42], was placed in the design to ensure the phase shift. This design shows the need to restore logic 0 and logic 1 to the proper value to ensure the correct signal propagation along the circuit. The propagation of non-restored signals may result in errors in the computation after few elaboration phases.

B. Scaling and Performance Analysis

The model presented was developed considering two technology nodes, the 100 nm and the 30 nm, where the node represents the waveguide width. Figure 4(a) shows the general idea of the developed MatLab model. It takes as input the material parameters and the geometry of the waveguides, the spin wave frequency, phase, and amplitude. Different circuit topologies were already defined inside the model code. After the computation, the normalized output power for every input and area/delay/power metrics are reported. The former is used to evaluate the correct behavior of the selected circuit, while the latter can be used to evaluate the performance of the technology.

Figure 4(b) compares the results of the simulations of the HA using the presented MatLab model and the micromagnetic simulations. Both models result in similar power distributions at the outputs of the DCs. Columns S and C show the normalized output power with respect to the power of the *Logic 1*. The Matlab simulations were performed considering the regenerators, therefore, the output powers are slightly different with respect to the micromagnetic ones. Moreover, the Matlab model makes it possible to reduce considerably the simulation time. The half adder (composed of DC1 and DC2), without regenerators, was simulated running the model on a Windows OS machine, equipped with Intel Core i7-1065G7 and 32 GB of RAM. The simulation of the adder takes about 10.5 seconds on average to be completed. On the contrary, the same circuit simulated on the micromagnetic simulator mumax3 [43], run on a TiTan XP GPU with 12 GB of RAM, with a mesh size of 10x10x30 nm^3 takes about 36min to simulate 300ns of time.

A more complex circuit could not be simulated with the micromagnetic simulator due to the huge computational cost and storage limitation in the computer. Our model provides a simple solution by solving the analytical theory with appropriate approximations. As a case study, we selected a 32-bit ripple carry adder (RCA) even if it is not a high-performance adder. However, the RCA is a simple enough architecture to show the design methodology and to validate the model. Figure 4(c) shows the output power distribution of a 32-bit RCA. The circuit is composed of 32 cascaded FAs resulting in a total of 160 regenerators (96 for output S and 64 for output C), 96 phase shifters, and 736 amplifiers. In the picture, 50 calculations with random inputs are depicted. Each dot represents the output power, normalized with respect to *Logic 1*, of each stage of the RCA (32 sum bit and the final carry out). It can be noticed that a perfect separation between "0" and "1" is obtained. Furthermore,

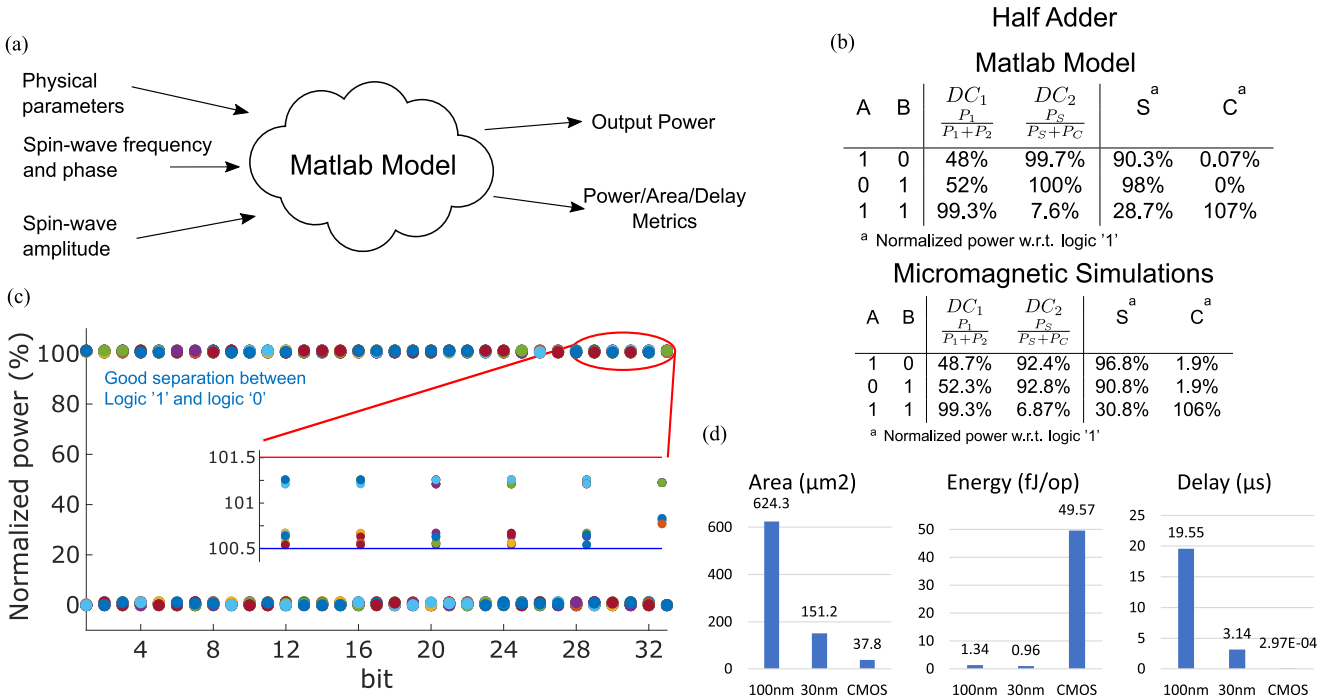


Figure 4. Magnonic circuits metrics and results thanks to the presented model; a) Overview of the model showing required inputs and produced outputs; b) Comparison among the output power distribution obtained with micromagnetic simulations and the proposed Matlab model; c) The output power distribution of a 32-bit RCA repeated 50 times with random inputs. The zoomed portion highlights that thanks to the regenerators, the output evaluated as *Logic 1* are very close to the 100% of the power; d Metrics obtained with the presented model for two technology nodes 100nm and 30nm compared with the 15 nm CMOS technology node.

the zoomed graph highlights that all the outputs evaluated as *Logic 1* are in the $100 \pm 1.5\%$ range, thanks to the introduction and modeling of the regenerator blocks.

Two different magnonic technology nodes were developed and inserted in the model: 100 nm and 30 nm waveguides [6]. Here, the two nodes are compared with a predictive 15 nm FinFET Process Design Kit [44]. The CMOS syntheses were performed with Synopsys Design Compiler, setting the output load capacitance to 10fF and a target frequency of 10ns. The model easily gives the possibility to compare the technologies under various aspects. Figure 4(d) shows the energy consumption, the area, and the delay metrics for the 32-bit RCA in the two technology nodes and CMOS. It is possible to notice that the scaling from 100 nm to 30 nm YIG technology resulted in various benefits. Energy passed from 1343 aJ/op to 961 aJ/ op, meaning that the circuit is more power-efficient. Similarly, area occupation for the RCA dropped from 624.25 μm^2 in the 100 nm to 151.15 μm^2 in YIG 30 nm, resulting in an 76% improvement. Here, the delay is the time needed for the spin wave to propagate from input to output. It resulted in 19.55 μs for the YIG 100 nm and 3.14 μs for the scaled node. The different scaling factors among the energy ($E = P \cdot D$) and delay (D) between the two nodes lead to an increased power dissipation for the 30 nm node. The reason is that the amplifier energy does not scale. Therefore, considering the higher number of amplifiers needed to restore the signals, they significantly impact the total power dissipation. Considering the comparison with a CMOS technology node, it is possible to notice that the area occupation is almost 16 times lower than the 100 nm. This difference is reduced by a factor of four thanks to the scaling, leading to comparable sizes. Similarly, the delay of the CMOS implementation is more than four orders of magnitude smaller than the scaled version of magnonic RCA. However, completely different results are obtained for what concerns energy consumption. In this case, YIG technologies show a 50 times lower energy when compared to the CMOS technology. The presented model allowed for the evaluation of the performance improvement of technological scaling. Furthermore, the design of a complex circuit showed the necessity of restoring the logic signals.

VI. Conclusion

Comparing the works in the literature on spin wave logic devices, it is possible to observe that little effort has been devoted to the development of methodology to study this promising technology at the circuit level.

The aim of this work was to develop a compact model, openly available to the research community (downloadable here), which enables the simulation of large all-magnon circuits, reducing the gap between technologist and architectural designers. The model offers the possibility to design magnonic-based circuits based on two technology nodes, the 100 nm and 30 nm YIG. Moreover, the 32-bit ripple carry adder has been considered as a case study to validate the correctness of the model. The study highlighted the need of regenerators to restore the signal value before feeding the next computing element. In addition, circuit metrics in term area occupation, delay and energy dissipation can be extracted. The proposed methodology could be exploited

to compare all-magnon circuits with state-of-the-art spintronic technologies, i.e., the FA design proposed in [45].

We hope that this model could serve as guide to drive further research activity on magnonics also at circuit level. Metrics extracted with the presented model highlighted that more effort is required in optimizing or using alternative solutions to amplify the spin waves. As a future work, would be interesting to introduce also the coupled circular ring element and introduce the concept of sequential circuits to spin wave computing. Moreover, a dedicated GUI, interacting with the model, would make it possible and easy to circuit designers to easily explore new customized computing elements that at the moment are not part of the set of computing elements. Of course, technological challenges still need to be solved, such as a physical realization of a VCMA amplifier, which is a crucial element for the design of regenerators.

Acknowledgments

The authors would like to thank Huqing Zheng for his support in the development of the model.

References

[1] R. Hertel, W. Wulfhekel, and J. Kirschner, "Domain-wall induced phase shifts in spin waves," *Phys. Rev. Lett.*, vol. 93, 2004, Art. no. 257202.
[2] P. Pirro, V. I. Vasyuchka, A. A. Serga, and B. Hillebrands, "Advances in coherent magnonics," *Nature Rev. Mater.*, vol. 6, pp. 1114–1135, 2021.
[3] T. Ichimura, R. Nakane, G. Tanaka, and A. Hirose, "A numerical exploration of signal detector arrangement in a spin-wave reservoir computing device," *IEEE Access*, vol. 9, pp. 72637–72646, 2021.
[4] Á. Papp, G. Csaba, and W. Porod, "Optically-inspired computing based on spin waves," in *Proc. IEEE Int. Conf. Rebooting Comput.*, 2016, pp. 1–4.
[5] M. Krawczyk and D. Grundler, "Review and prospects of magnonic crystals and devices with reprogrammable band structure," *J. Phys. Condens. Matter*, vol. 26, no. 12, 3 2014, Art. no. 123202.
[6] Q. Wang et al., "A magnonic directional coupler for integrated magnonic half-adders," *Nature Electron.*, vol. 3, no. 12, pp. 765–774, 2020.
[7] A. Mahmoud, F. Vanderveken, F. Ciubotaru, C. Adelmann, S. Hamdioui, and S. Cotofana, "Spin wave based approximate computing," *IEEE Trans. Emerg. Topics Comput.*, vol. 10, no. 4, pp. 1932–1940, Fourth Quarter 2021.
[8] Y. Kajiwara et al., "Transmission of electrical signals by spin-wave interconversion in a magnetic insulator," *Nature*, vol. 464, no. 7286, pp. 262–266, 2010.
[9] M. Collet et al., "Spin-wave propagation in ultra-thin YIG based waveguides," *Appl. Phys. Lett.*, vol. 110, no. 9, 2017, Art. no. 092408.
[10] H. Qin, R. B. Holländer, L. Flajšman, and S. van Dijken, "Low-loss nanoscopic spin-wave guiding in continuous yttrium iron garnet films," *Nano Lett.*, vol. 22, pp. 5294–5300, 2022.
[11] C. Liu et al., "Long-distance propagation of short-wavelength spin waves," *Nature Commun.*, vol. 9, 2018, Art. no. 738.
[12] T. Goto et al., "Three port logic gate using forward volume spin wave interference in a thin yttrium iron garnet film," *Sci. Rep.*, vol. 9, no. 1-11, 2019, Art. no. 16472.
[13] G. Talmelli et al., "Reconfigurable submicrometer spin-wave majority gate with electrical transducers," *Sci. Adv.*, vol. 6, 2020, Art. no. eabb4042.
[14] S. Wintz et al., "Magnetic vortex cores as tunable spin-wave emitters," *Nature Nanotechnol.*, vol. 11, no. 11, pp. 948–953, 2016.
[15] P. Che, K. Baumgaertl, A. Kúkol'ová, C. Dubs, and D. Grundler, "Efficient wavelength conversion of exchange magnons below 100 nm by magnetic coplanar waveguides," *Nature Commun.*, vol. 11, no. 1, 2020, Art. no. 1445.
[16] P. Krivosik and C. E. Patton, "Hamiltonian formulation of nonlinear spin-wave dynamics: Theory and applications," *Phys. Rev. B*, vol. 82, 2010, Art. no. 184428.
[17] R. Verba, V. Tiberkevich, and A. Slavin, "Hamiltonian formalism for nonlinear spin wave dynamics under antisymmetric interactions: Application to Dzyaloshinskii-Moriya interaction," *Phys. Rev. B*, vol. 99, 2019, Art. no. 174431.
[18] T. Brächer and P. Pirro, "An analog magnon adder for all-magnonic neurons," *J. Appl. Phys.*, vol. 124, no. 15, 2018, Art. no. 152119.
[19] G. Csaba, Á. Papp, and W. Porod, "Perspectives of using spin waves for computing and signal processing," *Phys. Lett. A*, vol. 381, no. 17, pp. 1471–1476, 2017.
[20] A. Mahmoud et al., "Introduction to spin wave computing," *J. Appl. Phys.*, vol. 128, no. 16, 2020, Art. no. 161101.
[21] A. V. Chumak et al., "Advances in magnetics roadmap on spin-wave computing," *IEEE Trans. Magn.*, vol. 58, no. 6, pp. 1–72, Jun. 2022.
[22] Q. Wang, A. Chumak, and P. Pirro, "Inverse-design magnonic devices," *Nature Commun.*, vol. 12, no. 1, pp. 1–9, 2021.
[23] A. Papp, W. Porod, and G. Csaba, "Nanoscale neural network using non-linear spin-wave interference," *Nature Commun.*, vol. 12, 2021, Art. no. 6422.
[24] K.-S. Lee and S.-K. Kim, "Conceptual design of spin wave logic gates based on a Mach–Zehnder-type spin wave interferometer for universal logic functions," *J. Appl. Phys.*, vol. 104, no. 5, 2008, Art. no. 053909.
[25] T. Schneider, A. A. Serga, B. Leven, B. Hillebrands, R. L. Stamps, and M. P. Kostylev, "Realization of spin-wave logic gates," *Appl. Phys. Lett.*, vol. 92, no. 2, 2008, Art. no. 022505.
[26] A. V. Chumak, A. A. Serga, and B. Hillebrands, "Magnon transistor for all-magnon data processing," *Nature Commun.*, vol. 5, no. 1, 8 2014, Art. no. 4700.
[27] H. Wu et al., "Magnon valve effect between two magnetic insulators," *Phys. Rev. Lett.*, vol. 120, 2018, Art. no. 097205.
[28] S. Dutta et al., "Non-volatile clocked spin wave interconnect for beyond-CMOS nanomagnet pipelines," *Sci. Rep.*, vol. 5, no. 1, 2015, Art. no. 9861.
[29] E. Egel, C. Meier, G. Csaba, and S. Breitkreutz-von Gamm, "Design of a cmos integrated on-chip oscilloscope for spin wave characterization," *AIP Adv.*, vol. 7, no. 5, 2017, Art. no. 056016.
[30] A. Mahmoud, F. Vanderveken, C. Adelmann, F. Ciubotaru, S. Hamdioui, and S. Cotofana, "Fan-out enabled spin wave majority gate," *AIP Adv.*, vol. 10, no. 3, 2020, Art. no. 035119.
[31] A. N. Mahmoud, F. Vanderveken, C. Adelmann, F. Ciubotaru, S. Cotofana, and S. Hamdioui, "Spin wave normalization toward all magnonic circuits," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 68, no. 1, pp. 536–549, Jan. 2021.
[32] A. V. Sadovnikov et al., "Nonlinear spin wave coupling in adjacent magnonic crystals," *Appl. Phys. Lett.*, vol. 109, no. 4, 2016, Art. no. 042407.
[33] Q. Wang, P. Pirro, R. Verba, A. Slavin, B. Hillebrands, and A. V. Chumak, "Reconfigurable nanoscale spin-wave directional coupler," *Sci. Adv.*, vol. 4, no. 1, 2018, Art. no. e1701517.
[34] A. V. Sadovnikov, S. A. Odintsov, E. N. Beginin, S. E. Sheshukova, Y. P. Sharaevskii, and S. A. Nikitov, "Toward nonlinear magnonics: Intensity-dependent spin-wave switching in insulating side-coupled magnetic stripes," *Phys. Rev. B*, vol. 96, 2017, Art. no. 144428.
[35] K. Y. Guslienko and A. N. Slavin, "Boundary conditions for magnetization in magnetic nanoelements," *Phys. Rev. B*, vol. 72, 2005, Art. no. 014463.
[36] R. Verba, G. Melkov, V. Tiberkevich, and A. Slavin, "Collective spin-wave excitations in a two-dimensional array of coupled magnetic nanodots," *Phys. Rev. B*, vol. 85, 2012, Art. no. 014427.
[37] R. Verba, M. Carpentieri, G. Finocchio, V. Tiberkevich, and A. Slavin, "Excitation of propagating spin waves in ferromagnetic nanowires by microwave voltage-controlled magnetic anisotropy," *Sci. Rep.*, vol. 6, no. 1, 2016, Art. no. 25018.
[38] B. Heinz et al., "Propagation of spin-wave packets in individual nanosized yttrium iron garnet magnonic conduits," *Nano Lett.*, vol. 20, no. 6, pp. 4220–4227, 2020.
[39] M. Beleggia, S. Tandon, Y. Zhu, and M. De Graef, "On the magnetostatic interactions between nanoparticles of arbitrary shape," *J. Magnetism Magn. Mater.*, vol. 278, no. 1, pp. 270–284, 2004.
[40] Y.-J. Chen et al., "Parametric resonance of magnetization excited by electric field," *Nano Lett.*, vol. 17, no. 1, pp. 572–577, 2017.
[41] O. V. Dobrovolskiy et al., "Spin-wave phase inverter upon a single nanodefect," *ACS Appl. Mater. Interfaces*, vol. 11, no. 19, pp. 17654–17662, 2019.
[42] Y. Au, M. Dvornik, O. Dmytriiev, and V. V. Kruglyak, "Nanoscale spin wave valve and phase shifter," *Appl. Phys. Lett.*, vol. 100, no. 17, 2012, Art. no. 172408.

[43] A. Vansteenkiste, J. Leliaert, M. Dvornik, M. Helsen, F. Garcia-Sanchez, and B. Van Waeyenberge, "The design and verification of MuMax3," *AIP Adv.*, vol. 4, no. 10, 2014, Art. no. 107133.
[44] K. Bhanushali and W. R. Davis, "FreePDK15: An open-source predictive process design kit for 15 nm FinFET technology," in *Proc. Symp. Int. Symp. Phys. Des.*, 2015, pp. 165–170.
[45] A. Mahmoud, F. Vanderveken, F. Ciubotaru, C. Adelmann, S. Cotofana, and S. Hamdioui, "Spin wave based full adder," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2021, pp. 1–5.

UMBERTO GARLANDO (Member, IEEE) received the bachelor's and master's degrees in electronic engineering from Politecnico di Torino, in 2013 and 2015, respectively. He is currently working toward the PhD degree in electronic engineering with the VLSILab of Politecnico di Torino, working on CAD and EDA tools for FCN (Field coupled nanocomputing). He worked in the development of the ToPoliNano framework, focusing on the simulation part. In 2020, he joined the MiNES (Micro and Nano Electronic Systems) group as a research associate, where he works on a fast-growing field such as the smart-systems for agri-food technology.

QI WANG received the PhD degree in the physics department from the University of Kaiserslautern, Germany, in 2019. Since 2020, he joined the Nanomagnetism and Magnonics Group with the University of Vienna as a postdoctoral Researcher. His research interests focus on conventional and inverse-design magnonics for data processing.

OLEKSANDR V. DOBROVOLSKIY (Senior Member, IEEE) received the PhD degree from the B. Verkin ILTPE (Kharkiv, Ukraine), in 2009, studying vortices in superconductors. Afterward, he moved to the Physics Institute, Goethe University Frankfurt/M, investigating magneto-transport phenomena and leading the *Nano-Fluxonics Laboratory* (after habilitation in 2016). He received a D.Sci degree in superconductivity (ILTPE, 2016) and was promoted to Professor of Low Temperature Physics. Since 2019, he is with the Faculty of Physics, University of Vienna, leading the *SuperSpin Lab* with Nanomagnetism and Magnonics. His research interests span from magnetism and spin transport phenomena to superconductivity and 3D nanoarchitectures.

ANDRII V. CHUMAK (Senior Member, IEEE) received the PhD degree in the group of Gennadii Melkov, in 2009, studied physics with the Taras Shevchenko National University of Kyiv. After the PostDoc at the group of Burkard Hillebrands with the University of Kaiserslautern, he continued as a Principal Investigator and the Head of ERC Junior Research Group. Andrii Chumak became a full professor and the Head of Nanomagnetism and Magnonics Group with the Faculty of Physics of the University of Vienna, in 2019. His scientific interests include magnetization dynamics and magnonics, nonlinear wave physics, spin-orbit spintronics, unconventional computing, and quantum magnonics.

FABRIZIO RIENTE (Member, IEEE) received the MSc degree (Hons.) (magna cum laude) in electronic engineering and the PhD degree degree from the Politecnico di Torino, in 2012 and 2016, respectively. He was a postdoctoral research associate with the Technical University of Munich, in 2016 and 2019. He is currently an assistant professor with the Politecnico di Torino. His primary research interests are device modeling, circuit design for nanocomputing, with particular interest on spintronic devices. His interests cover also the development of EDA tool for the investigation of beyond-CMOS technologies with the main focus on the physical design and the simulation methods.