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Optimal Zero-Voltage Switching Tracking Approach for Wide-Range Boost Converters Operating in the Boundary Conduction Mode

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ABSTRACT This article introduces a timing optimization approach for wide input voltage range boost converters operating in the Boundary Conduction Mode (BCM). Based on a time-domain analysis of the transient converter waveforms during the deadtime, this work describes the required timing scheme to achieve the optimal Zero Voltage Switching (ZVS) turn on condition for the low-side transistor, in which the driving voltage toggles exactly when the switching node voltage becomes null. The proposed approach consists in optimizing simultaneously the duration of the negative inductor current extension time and the deadtime, so as to achieve optimal ZVS with minimal inductor current ripple. The approach only requires input and output voltage sensors and a Zero-Current Detection (ZCD) circuit, already present in ordinary BCM converters, and is proven to accurately predict the optimal timing parameters. The optimization approach is implemented on a microcontroller, and experimental results on a synchronous boost reveal that the on-line timing adjustment enhances the converter efficiency by up to 1.1 %, and preserves the optimal ZVS operation also in transient conditions. Its simple implementation and performance improvement make this approach suitable for wide-range step-up applications.

INDEX TERMS Boost Converters, Boundary Conduction Mode, Efficiency-oriented Optimization, Timing Optimization, Zero-Voltage Switching.

I. INTRODUCTION

WIDE input/output voltage range DC-DC converters are essential building blocks in a broad spectrum of modern power electronics applications. Relevant examples include photovoltaic (PV) module-level power optimizers, in which the converter must extract maximum power from a PV panel whose terminal voltage varies significantly with irradiance and temperature [1], [2], and power factor correction (PFC) front-ends [3], [4]. In both cases, step-up converters are required to maintain high conversion efficiency not only at the nominal operating point but across the entire input voltage and load range.

Among the available operating modes for non-isolated boost converters, such as the synchronous boost topology shown in Fig. 1, the Boundary Conduction Mode (BCM), also referred to as Critical Conduction Mode (CRM) or Triangular Current Mode (TCM), has gained widespread attention at moderate-to-high switching frequencies, thanks to the inherent possibility to achieve the Zero-Voltage Switching (ZVS) turn-on of both the active devices [5], [6].

The ZVS in BCM is enabled by the resonant interaction between the energy-storage inductor and the parasitic output capacitances of the switching devices, thereby eliminating the turn-on switching loss without any auxiliary resonant circuit [7], [8]. Additional advantages include the absence of reverse-recovery losses in the synchronous rectifier, reduced Electromagnetic Interference (EMI) compared to hard-switching operation, and relaxed magnetic design compared to Continuous Conduction Mode (CCM) [9], [10].

In a BCM synchronous boost converter, ZVS operation is naturally achieved under certain input-output voltage relations [11]: in all the other conditions, the synchronous

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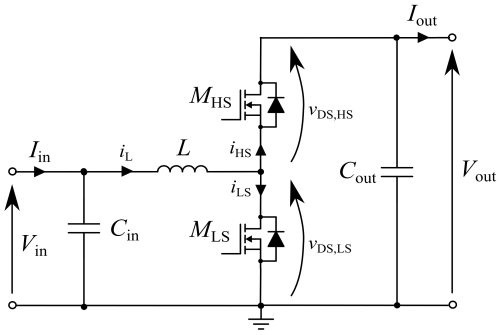


FIGURE 1: Schematic of a synchronous boost converter.

rectifier is kept conducting beyond the natural current zero-crossing, so that the inductor current reverses and discharges the parasitic capacitance of the switching node before the complementary device turns on [7]. The duration of this current-reversal interval, together with the subsequent deadtime, therefore governs the ZVS achievement in BCM-based converters.

Several approaches have been proposed in the literature to determine these intervals across varying operating conditions. In [7], the resonant transition of a non-synchronous CRM boost converter is solved through a piecewise equivalent-capacitance model, and the off-time of the main switch is extended accordingly; without a synchronous rectifier, no current-reversal interval can be controlled. In [11], the extra conduction time of the synchronous rectifier is regulated in closed loop on the switching-node valley voltage, sampled through an auxiliary inductor winding, while the main switch is turned on at the zero derivative of the switching-node voltage. In [12], the synchronous rectifier turn-off instant is tuned cycle by cycle by detecting the body-diode conduction, while the deadtime is computed from a constant-capacitance resonant model. Prediction-based methods replace the zero-current detection (ZCD) circuit with an inductor-current estimate and compute both intervals from analytical resonant expressions [13], [14]. In [15], the current-sensing delay is compensated by shortening the synchronous rectifier extension by a curve-fitted delay, preserving a predefined ZVS margin. Finally, [16] adjusts the switching frequency and the forced-ZVS deadtime of a ZVS quasi-square-wave (QSW) boost converter through multivariate polynomial fits of the sensed voltages and average inductor current, based on a charge-equivalent switching-node capacitance.

Although some of these methods adjust both intervals [12]–[14], [16], they share a common criterion: the negative current is set to the minimum value that brings the switching-node voltage just to zero at the bottom of the resonant transition, possibly with a safety margin [15], and the deadtime follows as the corresponding resonant time, or is replaced by valley detection [11]. However, the two intervals are mutually dependent: the optimal ZVS turn-on, in which the driving voltage toggles exactly when the switching-node voltage becomes null, is obtained by a continuum of current-reversal interval and deadtime pairs. Within this set, the minimum-negative-current solution is not the optimal one: as the initial current approaches its minimum value, the discharge time increases with unbounded slope, so that a slightly larger negative current considerably shortens the deadtime, reduces the overall current ripple, and moves the operating point away from a region of extreme sensitivity to timing errors. Moreover, most closed-form solutions rely on constant or equivalent capacitances [12], [13], [15] and, in the natural ZVS region, neglect the negative current produced by the propagation delay of the detection and driving chain.

This paper proposes a timing optimization framework that jointly determines the current-reversal interval and the deadtime of a BCM synchronous boost converter, as co-dependent degrees of freedom, over a wide voltage range, with three specific advances. First, among all the timing pairs ensuring the optimal ZVS turn-on, the one minimizing a simple, load-independent cost function related to the inductor current ripple is selected, instead of imposing the minimum negative current [11]–[14], [16]. Second, the optimal pair is obtained by numerically solving the resonant transition with the voltage-dependent output capacitance of the adopted transistors, rather than with constant, piecewise or charge-equivalent models [7], [12], [13], [16], and the characterized delay of the sensing, processing and driving chain is embedded in the optimization, so that the delay-induced negative current is exploited also in the natural ZVS region, rather than compensated a posteriori [15]; robustness against tolerances is assessed by Monte Carlo simulations. Third, the optimal profiles are reduced to piecewise analytical functions of the input voltage, evaluated at every update of the voltage regulation loop, so that the optimal ZVS condition is tracked also during load transients. Unlike [16], no average inductor current sensing or low-pass filtered multivariate fits are needed and, unlike [11], [12], no auxiliary winding or switching-node voltage sensing is required.

A key advantage of the proposed approach is that it requires no additional hardware beyond the sensors already present in any practical BCM converter implementation, since the quantities it relies on are already sensed for voltage regulation and ZCD. The optimal timing parameters are computed offline as functions of the converter operating point and applied in real time with no additional sensing or computational overhead.

The remainder of this paper is organized as follows: Section II reviews the operating principles of the BCM synchronous boost converter and introduces the analytical framework used throughout the paper; Section III presents the proposed timing optimization approach; Section IV reports the experimental results to validate the proposed optimal timing approach applied to a synchronous boost converter prototype; finally, Section V concludes the paper.

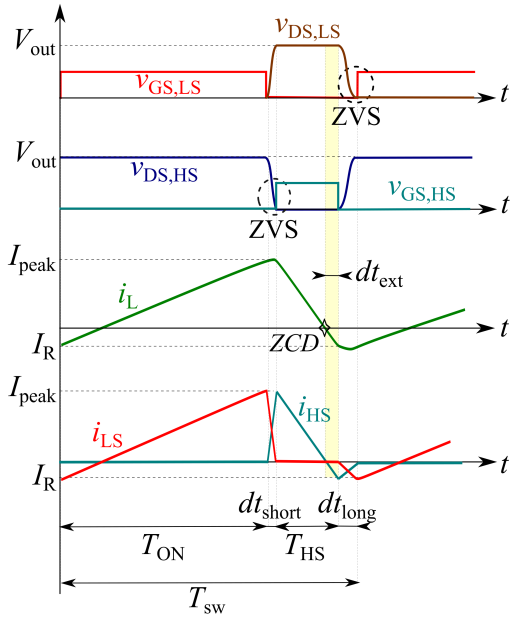


FIGURE 2: Main current and voltage waveforms of a boost converter operating in the BCM during a switching cycle.

II. ANALYSIS OF BCM

The BCM defines the operating condition of an inductor-based switching converter at the boundary between the Discontinuous Conduction Mode (DCM) and the CCM, in which every switching cycle begins exactly when the inductor current reaches zero, irrespective of the specific modulation scheme adopted to generate the driving signals. Equivalently, the switching frequency f_{sw} is adjusted so that the inductance value L always coincides with the critical inductance [17]. For a boost converter, this condition is met when [18]:

$$f_{sw} = \frac{M-1}{M^3}\frac{R}{2L}. \tag{1}$$

where $M = \frac{V_{out}}{V_{in}}$ is the voltage conversion ratio and R is the load resistance. At the steady-state, $M = \frac{1}{1-D}$, where $D = T_{ON} f_{sw}$ is the duty cycle.

Compared to CCM, the BCM ensures an improved power density, as it allows to relax the required inductance value [19], and naturally enables ZVS turn on across a wide operating range [6], [11]. At the same time, compared to DCM, it reduces the current stresses and relaxes the filter capacitance requirements. Overall, as the BCM offers an effective trade-off between power density and electrical stresses [20], it was exploited in PV converters [6], [19], integrated PWM converters [21], but mainly PFC pre-regulators [11], [17], [18], [22]

Before introducing the proposed timing optimization, the steady-state operation of synchronous boost converters (Fig. 1) is briefly recalled. Fig. 2 shows the main current and voltage waveforms of the converter operating in BCM, where the negative current extension, discussed later in this section, is also highlighted. Ideal passive components are assumed for the analysis, while the MOSFETs are considered ideal except for their output parasitic capacitance C_{oss}.

During T_{ON}, the low-side MOSFET M_{LS} conducts the inductor current i_L, which increases linearly with slope $\frac{V_{in}}{L}$. When M_{LS} turns off in a hard-switching condition, the peak current I_{peak} charges the equivalent switching node capacitance, consisting of the parallel C_{oss} of M_{HS} and M_{LS}. As i_L is at its maximum value, L stores enough energy to assist the natural ZVS turn on of M_{HS} after the relatively short deadtime dt_{short}. At the end of dt_{short}, M_{HS} turns on and i_L decreases with slope $\frac{V_{in}-V_{out}}{L}$. In the conventional BCM, as soon as a ZCD circuit captures the zero-crossing of the inductor current, M_{HS} is turned off, and the deadtime dt_{long} begins, during which the residual energy stored in L resonantly discharges the switching node capacitance. This approach ensures the natural ZVS turn on of M_{LS} when $V_{in} \leq \frac{V_{out}}{2}$, provided that dt_{long} is long enough for the complete discharge of the switching node voltage [6], [11]. At the end of dt_{long}, M_{LS} turns on, and a new switching cycle begins.

Since the switching period is set by the zero-crossing of i_L, the conventional BCM described above operates at variable frequency, according to (1), and the inductor current ripple scales with the load power. As an alternative, the constant-frequency BCM was also proposed [6], where the peak and the valley values of the inductor current are adjusted dynamically through a hysteresis band so as to maintain a fixed switching frequency. In this case, however, the inductor current ripple does not scale with the load power, resulting in dominant conduction losses and reduced efficiency at light-load operation.

When $V_{in} > \frac{V_{out}}{2}$, the energy available at the zero-crossing of i_L is no longer sufficient to fully discharge the switching node capacitance, and the natural ZVS turn on of M_{LS} is lost. Under these conditions, the conduction of M_{HS} can be extended beyond the zero-crossing by an interval dt_{ext} [6], [11], [22], allowing i_L to reach a sufficiently negative value I_R to discharge the switching-node capacitance during dt_{long}. The optimal ZVS turn on occurs when the driving voltage $v_{GS,LS}$ toggles exactly when $v_{DS,LS} = 0\,\text{V}$. An earlier commutation results in a hard-switching turn on, while a delayed turn on results in a sub-optimal ZVS, characterized by a temporary conduction of the body diode of M_{LS}. Considering the negative current extension until the target I_R, the switching frequency expressed in (1) decreases by a factor $\alpha = 1 - \frac{I_R}{\overline{I}_L}$, where $\overline{I}_L$ is the average value of inductor current [2].

The main innovative contribution of this work is a systematic and combined optimization of dt_{ext} and dt_{long}. Unlike previous approaches, in which dt_{long} is derived from closed-form resonant expressions assuming a null inductor current at the synchronous rectifier turn-off, dt_{long} is here optimized also in the natural ZVS region ($V_{in} \leq \frac{V_{out}}{2}$), accounting for the delay-induced negative current.

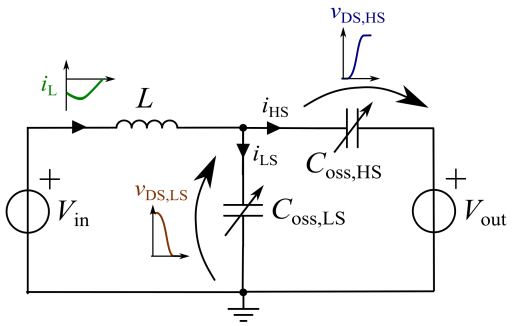


FIGURE 3: Equivalent circuit of the synchronous boost converter during dt_{long}.

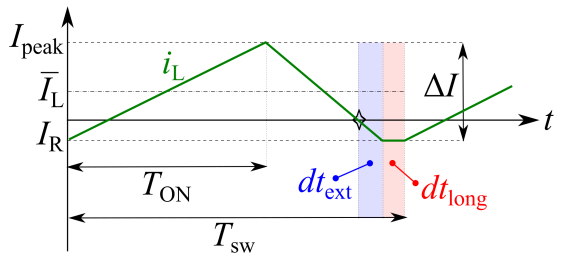


FIGURE 4: Simplified i_{L} waveform considered for the derivation of the optimal $dt_{\text{ext}} - dt_{\text{long}}$ pair.

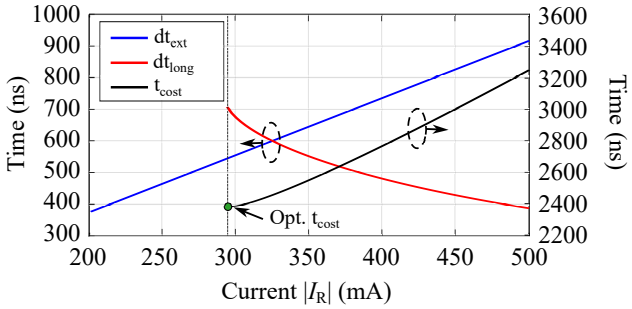


FIGURE 5: Numerical plots of dt_{ext}, dt_{long} and t_{cost} required to achieve the optimal ZVS as functions of $|I_{\text{R}}|$, for $V_{\text{in}} = 32\,\text{V}$ and $V_{\text{out}} = 50\,\text{V}$. The optimal t_{cost} is highlighted in green.

III. PROPOSED TIMING OPTIMIZATION

A. MODELLING OF TRANSIENT DURING THE DEADTIME

In order to compute the required timing scheme to achieve optimal ZVS turn on of M_{LS}, the operation of the converter is analyzed during the dt_{long}. As shown in Fig. 3, during dt_{long}, the inductor L and the non-linear voltage-dependent output capacitances $C_{\text{oss,LS}}$ and $C_{\text{oss,HS}}$ of the MOSFETs resonate, and the transient operation can be described as follows:

$$\begin{cases} \dfrac{di_{\text{L}}(t)}{dt} = \dfrac{V_{\text{in}} - v_{\text{DS,LS}}(t)}{L} \\ \dfrac{dv_{\text{DS,LS}}(t)}{dt} = \dfrac{i_{\text{L}}(t)}{C_{\text{oss,LS}}\big(v_{\text{DS,LS}}(t)\big) + C_{\text{oss,HS}}\big(V_{\text{out}} - v_{\text{DS,LS}}(t)\big)} \end{cases}, \quad (2)$$

with initial conditions $i_{\text{L}}(0^+) = I_{\text{R}}$ and $v_{\text{DS,LS}}(0^+) = V_{\text{out}}$. The complete discharge of the switching node is strongly dependent on the initial conditions of i_{L} and $v_{\text{DS,LS}}$. Since the input and output voltages are independent system parameters linked to the operating point, a properly tuned initial current I_{R} alone determines the possibility of achieving ZVS.

Based on Fig. 2, the target I_{R} can be achieved by properly adjusting dt_{ext}:

$$I_{\text{R}} = \frac{V_{\text{in}} - V_{\text{out}}}{L} \cdot dt_{\text{ext}}\,. \quad (3)$$

Technically speaking, dt_{ext} can be decomposed into two different terms:

$$dt_{\text{ext}} = dt_{\text{ext,HW}} + dt_{\text{ext,SW}}\,, \quad (4)$$

where $dt_{\text{ext,HW}}$ accounts for the hardware-related propagation delays, dependent on the specific ZCD circuit and controller, while $dt_{\text{ext,SW}}$ is the additional time adjusted by the controller according to the specific working point. Based on (3), $dt_{\text{ext,HW}}$ imposes on the system the minimum inductor current at the beginning of the deadtime:

$$I_{\text{R,min}} = \frac{V_{\text{in}} - V_{\text{out}}}{L} \cdot dt_{\text{ext,HW}}\,. \quad (5)$$

At low voltage gains, the extension time $dt_{\text{ext,SW}}$ can be controlled to tune the initial current $I_{\text{R}} < I_{\text{R,min}}$ to meet the ZVS condition. Notably, when the voltage gain exceeds 2 [11], the natural hardware propagation delay is sufficient to guarantee ZVS without extending the high-side MOSFET conduction time: in these cases, the controller imposes $dt_{\text{ext,SW}} = 0\,\text{ns}$. It must be emphasized, however, that this exact minimum gain is highly dependent on the total hardware delay of the given architecture.

B. TIMING OPTIMIZATION

To meet the optimal ZVS condition $v_{\text{DS,LS}}(dt_{\text{long}}) = 0\,\text{V}$, the duration of the output capacitance discharge must be rigorously evaluated. This enables the low-side MOSFET to be turned on immediately after the complete discharge of $v_{\text{DS,LS}}$, thus avoiding the conduction of its body diode. By numerically solving (2) with parametric initial condition I_{R} given by (3) and the interpolated Lookup Table (LUT) data of C_{oss} for the specific transistors, the optimal ZVS condition can be met by multiple pairs of $dt_{\text{ext,SW}}$ and dt_{long}. For instance, to ensure a very fast discharge of the switching node capacitance (reduced dt_{long}), I_{R} should be increased through an extended $dt_{\text{ext,SW}}$, resulting in increased ripple current and conduction losses. On the other hand, reducing $dt_{\text{ext,SW}}$ may result in a considerably longer deadtime to accommodate the full discharge of $v_{\text{DS,LS}}$. In other terms, both $dt_{\text{ext,SW}}$ and dt_{long} can be expressed as functions of the initial current I_{R}.

Since multiple pairs of the two timing parameters are available, an additional criterion is required to identify a unique optimum. The adopted criterion aims at minimizing

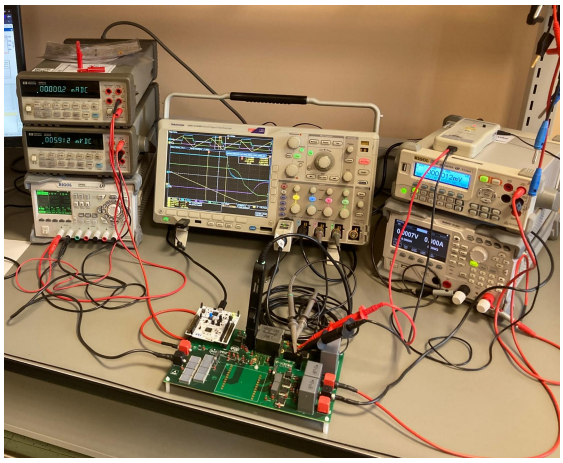


FIGURE 6: Laboratory setup.

the conduction losses in the inductor and transistors of the synchronous boost. As proved in [2], the RMS current stresses in all the boost components depend on the peak-to-peak inductor current ripple ΔI: therefore, for a given operating power, a pair of timing parameters that increases ΔI is expected to deteriorate the conversion efficiency due to the higher conduction losses. Based on this consideration, the optimal pair of dt_{ext} and dt_{long} among all the available combinations is the one minimizing ΔI.

To express this criterion in an analytical form, the simplified i_{L} waveform in Fig. 4 is considered, where $dt_{\text{short}} \approx 0$ and $i_{\text{L}} = I_{\text{R}}$ during dt_{long}. By imposing the average inductor current equal to $\frac{V_{\text{out}}^2}{RV_{\text{in}}}$, the following second-order equation is obtained:

$$\Delta I^2 \frac{M}{M-1}\frac{L}{2V_{\text{in}}} - \Delta I \cdot M\left(dt_{\text{ext}} + \frac{M^2}{M-1}\frac{L}{R}\right) - dt_{\text{long}}\frac{V_{\text{in}}(M-1)}{L}\left(dt_{\text{ext}} + \frac{M^2}{M-1}\frac{L}{R}\right) = 0\,. \quad (6)$$

The explicit solution of (6) exhibits a non-linear dependence on both dt_{ext} and dt_{long}. However, for sufficiently small timing parameters, a first-order two-variable Taylor approximation can be performed, leading to a simple and linear expression of ΔI:

$$\Delta I \approx \frac{M-1}{M}\frac{V_{\text{in}}}{L}\left(\frac{2M^3}{M-1}\frac{L}{R} + 2M dt_{\text{ext}} + dt_{\text{long}}\right). \quad (7)$$

The mathematical details of the derivation of (6) from the simplified current waveform of Fig. 4, and the validity range of the linear solution (7) can be found in Appendix A. Based on (7), for a given operating point (constant M, V_{in}, and R), the minimization of the current ripple is obtained by minimizing the load-independent and linear cost function t_{cost}:

$$t_{\text{cost}} = 2M dt_{\text{ext}} + dt_{\text{long}}\,. \quad (8)$$

Fig. 5 plots, for a specific voltage gain condition ($\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{50\,\text{V}}{32\,\text{V}}$), the pairs of dt_{ext} (blue curve) and dt_{long} (red curve) ensuring optimal ZVS condition, and the behaviour of t_{cost} for different values of I_{R}. For the considered operating point, t_{cost} is minimized for the pair of timing parameters associated to $I_{\text{R}} \approx -295\,\text{mA}$.

TABLE 1: Bill of materials of the tested boost prototype.

Component	Part number	Value
MOSFETs $M_{\text{HS-LS}}$	STB45N30M5	37 mΩ (typ.)
Inductor L	AGP4233-333ME	33 µH
Output capacitor C_{out}	R75MW51004030J	10 µF
Input capacitor C_{in}	8x CB182D0475JBC	37.6 µF
Current sensor	CT431-HSWF20MR	N/A
Comparator	TS3011ILT	N/A
Microcontroller	STM32G474RE	N/A
Gate driver	STGAP2DM	N/A

TABLE 2: Delay contributions of the acquisition chain.

Device	**Delay contribution [ns]**
CT431 (current sensor)	264.0
TS3011 (comparator)	19.4
STm32g474 (MCU)	32.0
STGAP2D (gate driver)	76.6
Total:	**392.0**

IV. EXPERIMENTAL VALIDATION

The developed optimization approach was applied to a specific case study, a wide-range synchronous boost converter for single-module PV applications [23], whose bill of materials is reported in Table 1. The boost converter was originally designed for the wide 15 V–45 V input voltage range and a rated 100 W power. The details of the converter design can be found in [23]. More specifically, the power MOSFETs were designed according to the worst-case voltage and current stresses, while the input and output capacitors C_{in}–C_{out} were designed to limit the voltage ripples below the desired values. The inductance value $L = 33\,\mu\text{H}$ was designed to bound the switching frequency of the BCM boost within 20 kHz and 200 kHz for most of the target PV panel operating points [2]. Fig. 6 shows the test setup, including a DC voltage supply and programmable DC electronic load, digital multimeters for the characterization of input and output powers, and a digital oscilloscope to verify the correct time-domain operation and the achievement of the optimal ZVS condition.

A. EXPERIMENTAL CHARACTERIZATION OF HARDWARE AND FIRMWARE DELAYS

According to (5), the optimal timing for the achievement of the ZVS condition is inherently affected by the propagation delays associated with the acquisition and processing of the current zero-crossing, $dt_{\text{ext,HW}}$. As a consequence, the various delay contributions of the acquisition chain were

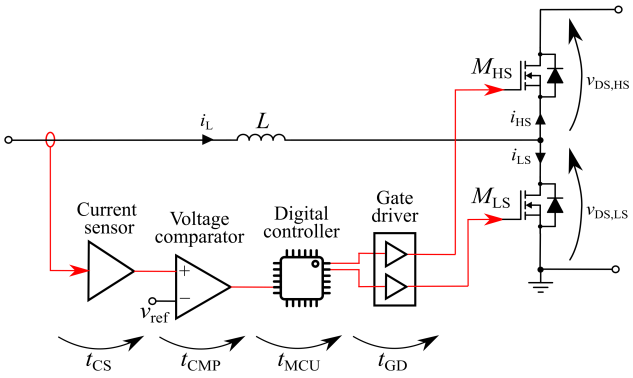


FIGURE 7: Block diagram of the different HW delay contributions affecting the BCM operation.

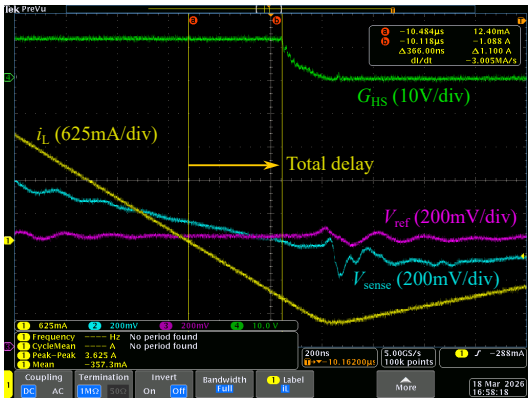


FIGURE 8: Characterization of total propagation delay between the zero-crossing of current probe signal i_L and the turn-off of the high side gate G_{HS}. V_{sense} and V_{ref} are the analog output voltage and reference voltage of the current sensor, respectively.

experimentally characterized to tune the optimization algorithm. For the adopted setup, a block diagram of the various delay contributions is presented in Fig. 7. The total propagation delay between the zero-crossing of i_L and the turn-off of M_{HS} is the summation of the delays of the current sensor t_{CS} (due to the bandwidth limitations of the analog sensor), the propagation delay of the high-speed comparator t_{CMP}, the time required by the digital controller to process the external event and toggle the digital control signal t_{MCU}, and the propagation delay of the gate driver t_{GD}:

$$dt_{ext,HW} = t_{CS} + t_{CMP} + t_{MCU} + t_{GD}\,. \tag{9}$$

Every delay contribution was individually characterized, and the averaged results on 50 acquisitions are listed in Table 2. According to the characterization, the current sensor accounts for the largest fraction of the total delay ($\approx 67\,\%$), followed by the gate driver ($\approx 19\,\%$). Fig. 8 shows a picture of the main relevant waveforms used to characterize the total delay, defined between the zero-crossing of i_L and the 90 % of the high-side gate-source driving voltage G_{HS}. V_{sense} and V_{ref} are the analog output and reference voltages of the current sensor, which are connected to the non-inverting and inverting inputs of the comparator, respectively. Therefore, the output of the comparator represents the polarity of i_L, whose transition from positive to negative triggers the microcontroller to update the control signals.

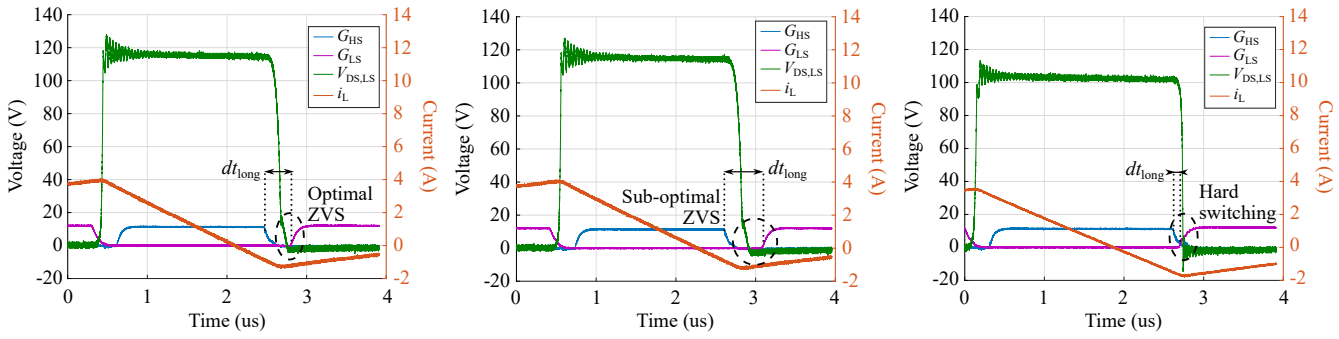
B. OPTIMAL TIMING COMPUTATION AND OPEN-LOOP VALIDATION

After characterizing the hardware delay constraints, the proposed timing optimization was implemented on an STM32G474RE microcontroller to validate its effectiveness in tracking the optimal ZVS condition and characterize the efficiency enhancement compared to the cases in which fixed dt_{ext} and dt_{long} are employed.

Fig. 9 shows some experimental waveforms with $V_{in} = 20\,\text{V}$, $R = 500\,\Omega$, $T_{ON} = 12\,\mu\text{s}$, resulting in $V_{out} = 115\,\text{V}$ and 25 W load power. In more detail, Fig. 9a was obtained with the optimal timing parameters found by solving (2) and selecting the minimum t_{cost}. As it can be seen, the numerically evaluated $dt_{ext}, SW = 0\,\text{ns}$ and $dt_{long} = 350\,\text{ns}$ ensure the optimal ZVS turn on condition of M_{LS}. When a larger $dt_{long} = 500\,\text{ns}$ is used (Fig. 9b), the switching node voltage falls to 0 V too early compared to the G_{LS} toggling, resulting in a temporary conduction of the body diode ($\approx$100 ns) and in a sub-optimal ZVS condition. On the other hand, the smaller $dt_{long} = 100\,\text{ns}$ does not ensure the full discharge of the switching node voltage, and the resulting hard switching causes additional losses and worse EMI performance (Fig. 9c).

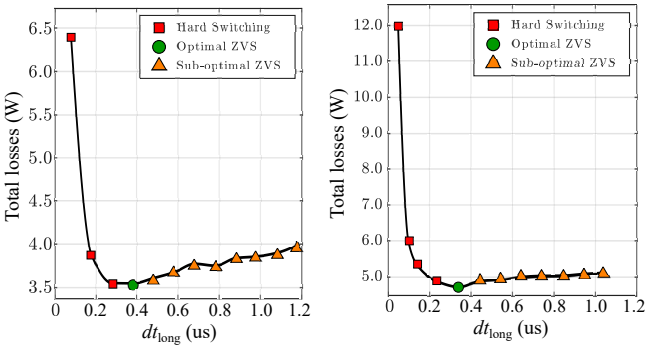
To quantify the performance drop when the timing parameters deviate from the optimal ones, the converter losses were measured in two specific operating points ($V_{in} = 20\,\text{V}$ / $R = 500\,\Omega$ / $T_{ON} = 9\,\mu\text{s}$ and $V_{in} = 20\,\text{V}$ / $R = 500\,\Omega$ / $T_{ON} = 12\,\mu\text{s}$) by sweeping dt_{long}. The resulting loss profiles are shown in Figs. 10a and 10b, respectively. Both plots show that the optimal dt_{long}, computed off-line and highlighted with a green circle, minimizes the total converter losses, thanks to the optimal ZVS condition. For lower values of dt_{long}, the losses steeply increase due to the hard switching condition. On the other hand, the almost linear increase of losses for higher dt_{long} can be explained by the increasing dissipation in the M_{LS} body diode, due to the sub-optimal ZVS condition.

Monte Carlo simulations were run to evaluate the impact of tolerances on the optimal timing values. Considering all the delay contributions of the acquisition chain as individual and independent Gaussian distributions, the whole hardware propagation delay can be modeled as a Gaussian distribution itself. The optimal timing parameters results, extracted over 5000 iterations, can be fitted by gaussian profiles, as shown in Fig. 11, referred to the operating condition $V_{in} = 32\,\text{V}$ and $V_{out} = 50\,\text{V}$, and assuming 20 % tolerance on all the delay contributions, on L and C_{oss}. Based on (3) and (4), as $dt_{ext,SW}$ depends linearly on the



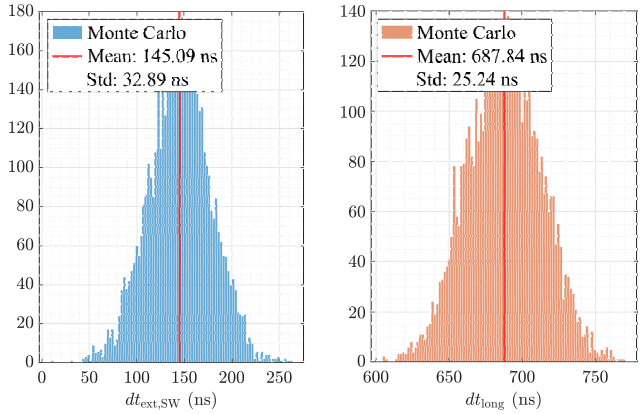
(a) (b) (c)

FIGURE 9: Detail of the main converter waveforms (switching node voltage $V_{\mathrm{DS,LS}}$, driving voltages G_{LS} / G_{HS}, inductor current i_{L}) at $V_{\mathrm{in}} = 20\,\mathrm{V}$, $R = 500\,\Omega$, $T_{\mathrm{ON}} = 12\,\mu\mathrm{s}$, for different values of dt_{long}: (a) $dt_{\mathrm{long}} = 350\,\mathrm{ns}$ (optimal ZVS); (b) $dt_{\mathrm{long}} = 500\,\mathrm{ns}$ (sub-optimal ZVS); (c) $dt_{\mathrm{long}} = 100\,\mathrm{ns}$ (hard-switching).



(a) (b)

FIGURE 10: Total converter dissipation as a function of dt_{long}, for V_{in}=20 V and R=500 Ω. The green circle identifies the numerically computed optimal timing for the ZVS condition: (a) T_{ON}=9 µs; (b) T_{ON}=12 µs.



(a) (b)

FIGURE 11: Distribution of optimal timing parameters in a Monte Carlo simulation: (a) $dt_{\mathrm{ext,SW}}$; (b) dt_{long}.

inductance L and the hardware-related propagation delay $dt_{\mathrm{ext,WH}}$, their tolerances propagate directly to the optimal $dt_{\mathrm{ext,SW}}$. On the other hand, as the optimal dt_{long} depends on the resonant interaction between L and the strongly nonlinear C_{oss}, the quantitative propagation of the uncertainty of C_{oss} is harder to perform. Specific temperature-dependent propagation delays in the acquisition chain and layout-related parasitic capacitances should be evaluated case by case. Nevertheless, the 20 % tolerances adopted for the Monte Carlo simulations are expected to provide a conservative estimate of the unavoidable deviations from the nominal parameters. Figs. 10a and 10b show, for two different operating conditions, the behaviour of the total converter losses when dt_{long} deviates from the optimal value, computed with the proposed approach.

C. CLOSED-LOOP VALIDATION

After validating the efficiency enhancement by the offline timing optimization, the algorithm was implemented in the microcontroller firmware to update $dt_{\mathrm{ext,SW}}$ and dt_{long} online in closed-loop operation, based on the controller block diagram shown in Fig. 12. A Proportional-Integral (PI) compensator was designed empirically to regulate $V_{\mathrm{out}} = 50\,\mathrm{V}$ over the 12 V–40 V input voltage range and the 5 W–50 W load power range. The optimal timing parameters, whose profiles are shown in Fig. 13, were computed offline, fitted by piecewise linear-parabolic analytical functions of V_{in}, and implemented in the firmware. At every acquisition of V_{in} and V_{out}, the controller updates the control variable T_{ON} to regulate V_{out}, and concurrently adjusts $dt_{\mathrm{ext,SW}}$ and dt_{long} to maintain optimal ZVS operation. The BCM and optimal ZVS tracking were implemented on a STM32G474RE microcontroller. As schematically shown in Fig. 12, the BCM timer exploits a High-Resolution Timer, configured as a Finite State Machine (FSM): the driving signals for M_{LS} and M_{HS} are toggled upon the occurrence of matching events between a free-running counter and various threshold values, while the counter is reset in correspondence of the ZCD event. The update of both the control variable T_{ON} and of

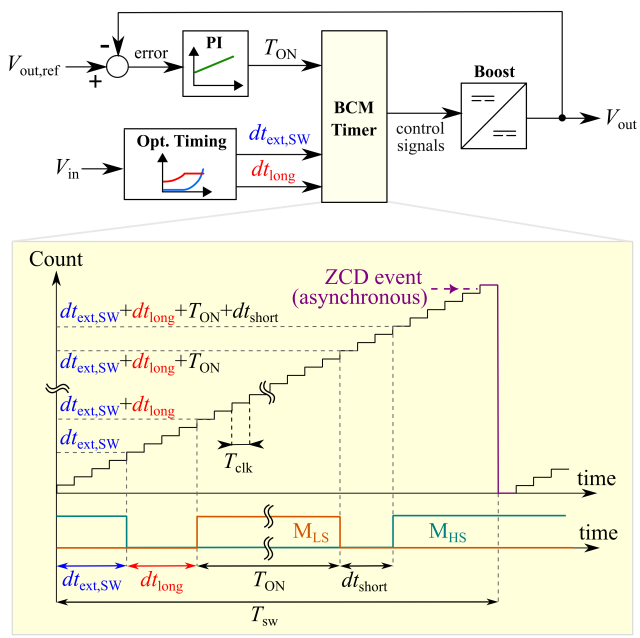


FIGURE 12: Block diagram of the implemented closed-loop control and simplified timing diagram of the operation of the BCM timer.

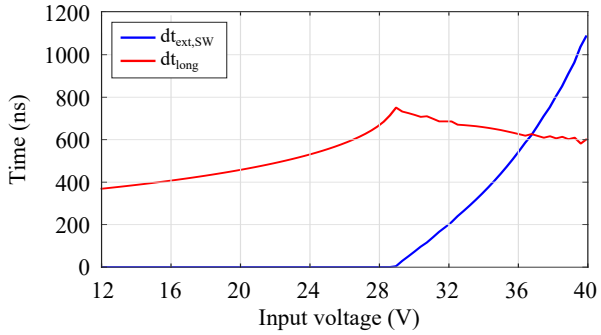
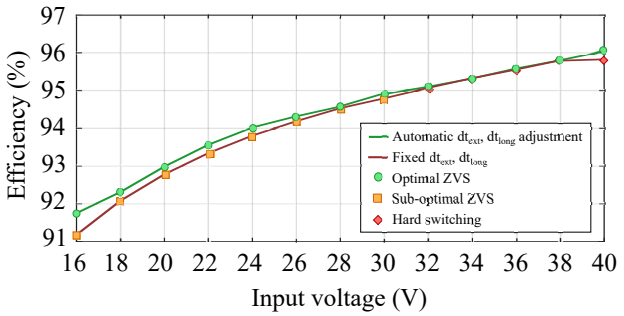
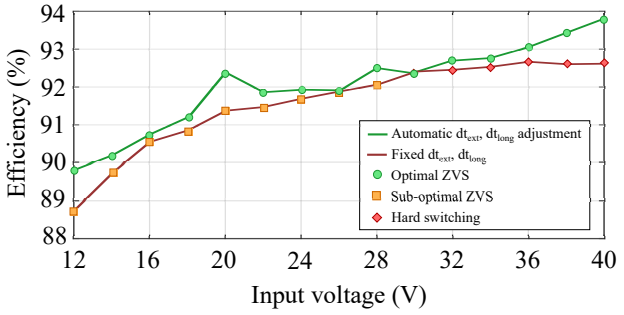


FIGURE 13: Optimal timing parameters computed in the defined input range and $V_{\text{out}} = 50\,\text{V}$, considering the effect of the hardware propagation delay.



(a)



(b)

FIGURE 14: Converter efficiency VS input voltage in closed-loop operation (regulated $V_{\text{out}} = 50\,\text{V}$), with and without online timing optimization: (a) $R = 50\,\Omega$; (b) $R = 100\,\Omega$.

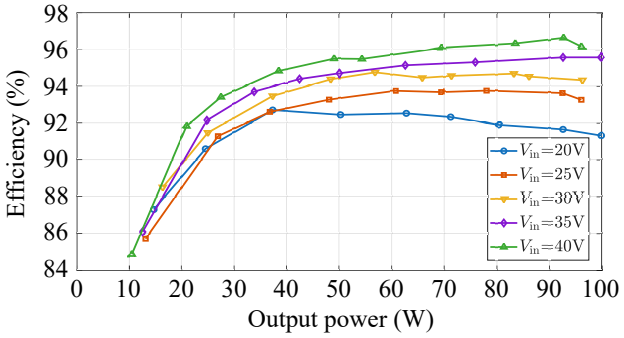


FIGURE 15: Converter efficiency VS load power at different input voltages, with the optimal timing parameters.

the optimal timing parameters is handled by an Interrupt Service Routine (ISR): thanks to the simple piecewise linear-parabolic interpolation of $dt_{\text{ext,SW}}$ and dt_{long}, the maximum required computation time of the ISR is just $1.56\,\mu\text{s}$, enabling update rates beyond $600\,\text{kHz}$. The memory requirements of the developed algorithm are $2.27\,\text{kB}$ of RAM and $22.36\,\text{kB}$ of Flash memory.

Figs. 14a) and 14b plots the converter efficiency characterized at different input voltages and two load conditions, namely $R = 50\,\Omega$ ($50\,\text{W}$) and and $R = 100\,\Omega$ ($25\,\text{W}$), respectively. The green curves represent the converter efficiency profiles adopting the online timing optimization, while the yellow / red curves refer to the cases in which fixed non-optimal $dt_{\text{ext,SW}}$ and dt_{long} were used, resulting sometimes in hard-switching conditions and sometimes in sub-optimal ZVS conditions. In the tested conditions, the proposed approach achieves up to $+0.7\,\%$ efficiency at $50\,\text{W}$ load power, and up to $+1.1\,\%$ efficiency at $25\,\text{W}$. Thanks to the minimal current ripple and optimal ZVS condition, the online optimization improves the efficiency in the whole voltage range.

Fig. 15 shows multiple converter efficiency profiles as functions of the load power and at different input voltage conditions, for a constant $50\,\text{V}$ regulated output. For each V_{in} condition, the same pair of dt_{ext} and dt_{long} was kept constant

along the swept power, as the optimal timing parameters are load-independent. The peak measured efficiency is 96.6 %, obtained at 93 W power and $V_{\text{in}} = 40\,\text{V}$. As expected, for a given output power, the efficiency increases at higher input voltages, thanks to the reduced conduction losses in all the boost components.

Finally, to prove that the proposed approach maintains the optimal ZVS conditions during transient operation, Fig. 16 presents relevant experimental waveforms during a load current step from $I_{\text{out}} = 500\,\text{mA}$ to $I_{\text{out}} = 100\,\text{mA}$. In more detail, Fig. 16a shows the complete acquired 10 ms time window, while Figs. 16b, 16c and 16d present zoomed views of the converter waveforms at steady state before the load step, in correspondence with the peak V_{out} overshoot, and when the converter approaches the new steady-state operation, respectively. In all three cases, the optimal ZVS condition is preserved, ensuring reliable and efficient operation of the converter also during transient conditions.

V. CONCLUSION

This article has presented a timing optimization approach to achieve the optimal ZVS condition of the low-side transistor in boost converters operating in the BCM with negative current extension. The approach is based on the numerical solution of the transient waveforms during the deadtime, imposing that the output voltage falls to 0 V right at the end of the deadtime. The algorithm simultaneously optimizes the negative current extension time dt_{ext} and the deadtime dt_{long} to ensure minimal inductor current ripple, also considering the non-linear behaviour of the transistors' output capacitance and the impact of hardware and firmware delays.

The optimal timing profiles can be computed offline and implemented in a digital controller firmware as Look-Up Tables (LUT) or analytical piecewise functions. The algorithm was implemented on a microcontroller and experimentally proved to track the optimal ZVS condition on a wide input voltage range, resulting in lower measured converter losses and efficiency enhancements up to $+1.1\,\%$ compared to fixed timing parameters. Closed-loop tests prove that the optimal ZVS condition is still preserved during load steps.

The proposed approach is only based on the acquisition of the input and output voltages and the polarity of the inductor current, and is generally applicable, provided that the parameters of the optimization algorithm are adapted to the specific experimental setup. Thanks to its inherent features, the proposed approach represents a simple and effective solution to optimize the performance of wide-range step-up converters without requiring additional sensors.

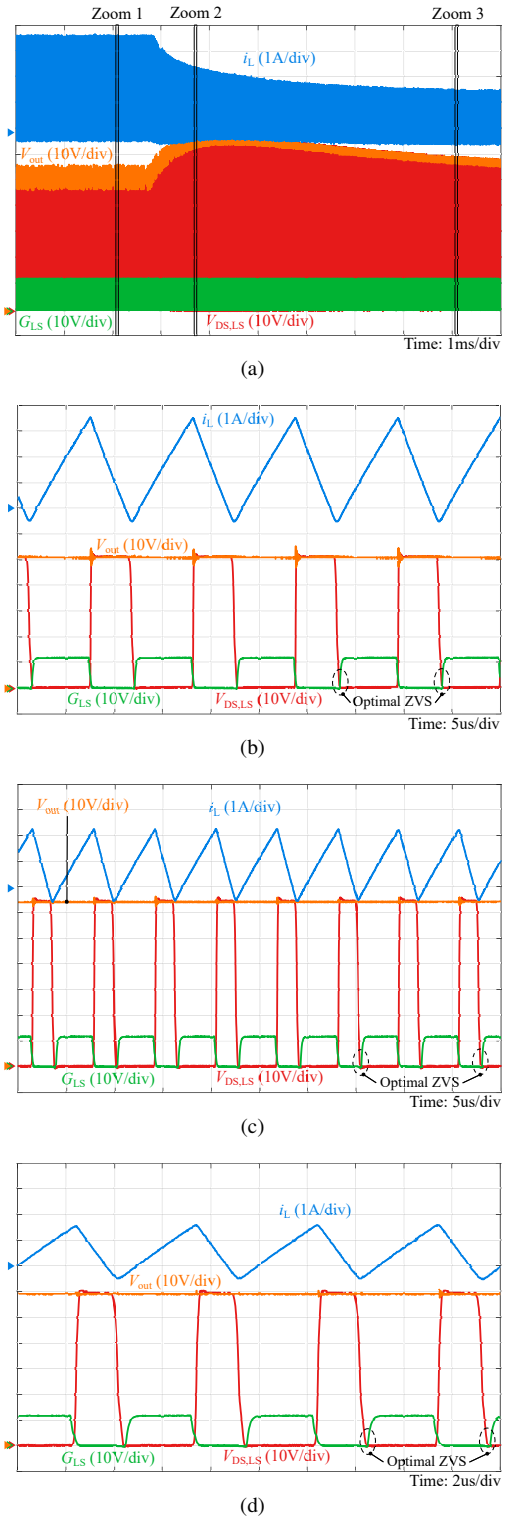


FIGURE 16: Closed-loop transient converter waveforms (output voltage V_{out}, low-side MOSFET driving voltage G_{LS}, switching node voltage $V_{\text{DS,LS}}$, inductor current i_{L}) for a load current step from 500 mA to 100 mA: (a) Complete time window; (b) Zoom 1; (c) Zoom 2; (d) Zoom 3.

Appendix A
DERIVATION OF COST-FUNCTION FOR THE MINIMIZATION OF THE INDUCTOR CURRENT RIPPLE

In this Appendix, a more detailed derivation of (6) and its first-order solution (7) are proposed. The analytical derivation of (6) follows from geometrical considerations on the

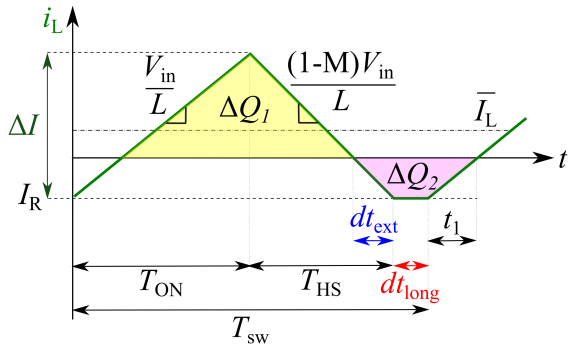


FIGURE 17: Simplified i_L waveform considered for the analytical derivation of (6).

inductor current waveform i_L. The main relevant quantities involved in the derivation are reported in Fig. 17, in which, as in Fig. 4, i_L is assumed to be constant during dt_{long}.

By averaging i_L on a switching cycle T_{sw}:

$$\int_0^{T_{sw}} i_L dt = \overline{I}_L \cdot T_{sw} = \Delta Q_1 + \Delta Q_2 \,, \tag{10}$$

where $\Delta Q_1 (> 0)$ and $\Delta Q_2 (< 0)$, expressed in (11) and (12), respectively, are the positive and negative quantities of electrical charge supplied by the input source during a switching period.

$$\Delta Q_1 = \frac{1}{2} \left(T_{ON} + T_{HS} - t_1 - dt_{ext} \right) \left(\Delta I + I_R \right) \tag{11}$$

$$\Delta Q_2 = \frac{1}{2} \left(2dt_{long} + dt_{ext} + t_1 \right) I_R \,. \tag{12}$$

Starting from (10), the goal is to derive an analytical expression relating the current ripple ΔI to dt_{ext} and dt_{long}, treating the remaining quantities (V_{in}, L, I_R etc.) as parameters. Exploiting the current slopes of i_L during the conduction periods of M_{LS} and M_{HS}, T_{ON}, T_{HS} and t_1 can be expressed in terms of ΔI as:

$$T_{ON} = \frac{L}{V_{in}} \Delta I \tag{13}$$

$$T_{HS} = \frac{L}{V_{in} \left(M - 1 \right)} \Delta I \tag{14}$$

$$t_1 = -\frac{L}{V_{in}} I_R \,. \tag{15}$$

Finally, assuming a lossless conversion ($\eta \approx 100\,\%$), the average input current can be expressed as:

$$V_{in} \overline{I}_L = \frac{V_{out}^2}{R} = \frac{M^2 V_{in}^2}{R} \longrightarrow \overline{I}_L = M^2 \frac{V_{in}}{R} \tag{16}$$

By substituting (11), (12), (13), (14), (15) and (16) in (10) and performing some algebraic manipulations, the second-order equation (6) is obtained.

The explicit solution of (6) can be expressed in the form $\Delta I = \frac{-B \pm \sqrt{\Delta}}{2A}$, where $\sqrt{\Delta}$ reveals a non-linear dependence on both dt_{ext} and dt_{long}. However, for sufficiently small dt_{ext} and dt_{long}, the term $\sqrt{\Delta}$ can be rearranged to enable the first-order Taylor approximation $\sqrt{1+x} \approx 1 + \frac{x}{2}$:

$$\begin{aligned} \sqrt{\Delta} &= \frac{M^3 L}{(M-1)R} \Bigg[1 + \frac{2(M-1)R}{M^2 L} dt_{ext} + \frac{2(M-1)R}{M^3 L} dt_{long} \\ &\quad + \left(\frac{(M-1)R}{M^3 L} dt_{ext} \right)^2 + \frac{2(M-1)^2 R^2}{M^7 L^2} dt_{long} dt_{ext} \Bigg]^{\frac{1}{2}} \\ &= \frac{M^3 L}{(M-1)R} + M dt_{ext} + dt_{long} + \mathcal{O}(dt_{ext}^2 + dt_{long}^2) \end{aligned} \tag{17}$$

Eq. (17) is valid only if $dt_{ext} \ll \frac{M^2 L}{2(M-1)R}$ and $dt_{long} \ll \frac{M^3 L}{2(M-1)R}$ simultaneously, conditions that are more easily met at higher voltage gain and heavier load operation. Based on (17), the linear approximated solution of (6) becomes:

$$\begin{aligned} \Delta I = \frac{(M-1)V_{in}}{ML} \Bigg[&\frac{2M^3 L}{(M-1)R} + 2M dt_{ext} \\ &+ dt_{long} + \mathcal{O}(dt_{ext}^2 + dt_{long}^2) \Bigg] \,, \end{aligned} \tag{18}$$

from which the cost function $t_{cost} = 2M dt_{ext} + dt_{long}$ is defined.

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