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(36^{th}cycle)

Switching Power Converters

Advanced Design Methodologies and Control Techniques

By

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2024

Declaration

I hereby declare that the contents and organization of this dissertation constitute my own original work and do not compromise in any way the rights of third parties, including those relating to the security of personal data.

Andrea Celentano
2024

* This dissertation is presented in partial fulfillment of the requirements for **Ph.D. degree** in the Graduate School of Politecnico di Torino (ScuDo).

I would like to dedicate this thesis to my loving parents

Abstract

This doctoral research extensively explores advanced techniques in the design and control of switching power converters, aiming to address current challenges in the state of the art. These challenges include the impact of approximated (i.e., non-analytical) design on converter characteristics and the inherent issues deriving from the choice of control strategies. A particular focus is also on low-coupling in isolated converters (i.e., Wireless Power Transfer systems) addressing communication and control considerations for compact low-power systems (e.g., biomedical implants). Additional attention is then given to high-frequency optimization challenges related to electromagnetic interference through the use of Spread Spectrum.

This work begins with the design of class-E resonant DC-DC converters, building upon the design methodology proposed by Professors F. Pareschi and G. Setti. Their approach offers a dimensionless and exact solution to the system of differential equations governing the circuit behavior. My contribution involves a twofold improvement: alternative modeling for devices like transformers to enhance flexibility and generality, and a new normalization revealing a 2D design workspace, simplifying conditions representation and facilitating exploration of converter properties.

Building upon refined converter design techniques, a novel dual-frequency control method is developed, overcoming the limitations of on-off control. As in the standard on-off and dual-frequency control, the approach is based on the ability of the converter to alternately operate in a high- and low-power state. The proposed solution has a twofold advantage: on the one hand, soft-switching capabilities are preserved in both operating states; on the other hand, it is possible to eliminate any transient when switching from one state to the other one. The direct consequence is the possibility of increasing the frequency at which the two operating states are switched up to the same order of magnitude as the converter main switching frequency. In this way, the additional ripple introduced by the proposed dual-frequency

control can be decreased to a negligible value. The approach has been validated by measurements on a prototype operating between 4 and 8 MHz in which the control frequency has been tuned up to 500 kHz.

Recent work explores communication capabilities in isolated class-E converters, using low-coupling transformers for high-speed (one bit per clock period) bidirectional data transmission. Reviewed assumptions, considering an increased operating frequency and coreless transformers (i.e., low loss but low coupling factor), improve converter efficiency (92% at 6.78 MHz) at the expense of reduced communication speed (one bit every four clock cycles).

The proposed analytical design advances Wireless Power Transfer (WPT) systems using isolated class-E DC-DC converters. A comparative analysis of class-E-based WPT methodologies is presented. Then, by addressing the challenge of nominal design, this research i) thoroughly reviews the available methodologies for measuring mutual inductance (i.e., the coupling factor); ii) highlights the issues that may arise, and iii) identifies the most suitable technique for a common yet challenging frequency of 6.78 MHz.

In low-power WPT applications, where simplicity and compactness of the system are crucial, a unique primary side control is investigated. It is therefore possible to regulate the power delivered to the load at the desired level by only sensing and modifying quantities available at the primary side. By adding a power regulator at the secondary side, the Desired Operating Point corresponding to the regulator is barely ON (and so dissipating negligible energy) while still providing the correct power to the load is easily detectable at the primary side. The main novelty of the proposed approach is the capability of working without advanced modeling of the system or its parameters estimation. The theoretically developed model is verified by measurements on a 60-mW-class-E-based WPT prototype working at 6.78 MHz and by simulations, only, on state-of-the-art WPT systems, both capacitively and inductively coupled.

The final phase explores Spread Spectrum (SS) capabilities in switching power converters, addressing limited coverage for three-phase circuits. The research demonstrates SS effectiveness in three-phase inverters and tackles high-frequency optimization challenges, specifically, harmonics overlap. Additionally, the study fills a literature gap in Talkative Power Converters, proposing SS guidelines to address EMI issues.

Preface

This text originates from the research conducted during my doctoral studies in Electrical Electronics and Communication Engineering at Politecnico di Torino. While various topics were explored, the primary focus revolved around switching power converters. Collaborations with companies such as Marelli Europe and STMicroelectronics, other universities like TU Delft and CAU Kiel, research institutes like INRIM as well as the DENERG Department of Politecnico di Torino, have enriched this work.

My research path commenced with the design of class-E resonant DC-DC converters, a subject hugely investigated by my supervisors Prof. Fabio Pareschi and Prof. Gianluca Setti, together with Nicola Bertoni, a former Ph.D. student. Their groundwork, resulting in numerous publications to overcome the state-of-the-art techniques limitations, served me as a starting point. Part I of this thesis is devoted to class-E resonant converters.

My first contribution involved comprehensive study, refinement, and consolidation of the existing material related to this class of converters. Finally, a unified methodology was formulated [1] and an open-source framework [2] was developed and shared in order to simplify the class-E converter design. This study led us to a publication in IEEE Access and the analysis is included in Chapter 1.

Upon refining the converter design techniques, a novel control method was developed in [3] to overcome the limitations of the usual on-off control and to achieve better performance. In particular, the switching between two operating points at different frequencies, along with the proper design of the converter, allows the achievement of virtually zero transient and dramatically increases the converter control frequency. This analysis led to a publication in IEEE Transactions on Power Electronics and the details are available in Chapter 2.

Accordingly, this converter also enables communication between the primary and secondary sides taking advantage of the low-coupling factor of the transformer involved. As a matter of fact, the low coupling fosters communication across the barrier, eliminating the need for an extra link or an extra communication block. This application [4] was presented at the IEEE International Symposium on Circuits and Systems (ISCAS) and it is the focus of Chapter 3.

The proposed analytical design has allowed, not only the overcoming of the strongly simplifying assumptions adopted in the state-of-the-art methodologies but also a better design of Wireless Power Transfer (WPT) systems that adopt isolated class-E DC-DC converters. Part II of this work is devoted to WPT systems. By focusing on the several design methodologies available for WPT class-E DC-DC converters, a comparative analysis has been presented at the 2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS) [5] and analyzed in Chapter 4.

An inherent challenge in the nominal design of isolated Class-E converters for WPT systems lies in the determination of the nominal coupling factor and in the way of performing accurate coupling factor measurements. This aspect was thoroughly explored in [6] in collaboration with Luca Callegaro, a researcher at INRIM, and a detailed discussion is available in Chapter 5. This study led to the publication of a tutorial brief published in IEEE Transactions on Circuits and Systems-II.

Given the frequent application of these circuits in biomedical implants (or in general in low-power WPT systems), where the simplicity and the compactness of the implanted part are crucial, a primary-side control (i.e., a control made exclusively at the non-implanted part) was investigated together with the Bioelectronics Section of the TU-Delft, headed by W.A. Serdijn. Preliminary findings were presented at the 2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS) and can be found in [7]. A comprehensive analysis that details the methodology, by generalizing the approach to every WPT circuit topology, is drafted in [8] and explained in Chapter 6. The application of the methodology to available state-of-the-art WPT topologies has been presented at the 2023 IEEE 66th International Midwest Symposium on Circuits and Systems (MWSCAS) and it is included in Chapter 7.

In the concluding phase of the PhD, the focus has shifted to the exploration of the Spread Spectrum (SS) capabilities in switching power converters. Part III is devoted to this.

The SS as a software technique to reduce the ElectroMagnetic Interference (EMI) has been extensively investigated by my supervisors during their research years. Despite the SS being a well-known technique, due to the increasing employment of wide bandgap devices in power electronics and the capability of increasing the converter switching frequency, some unaddressed issues in the state of the art, have been investigated. Among these, the high-frequency optimization that includes the harmonics overlap, usually neglected in the literature, has been the result of a partnership with Marelli Europe, together with the DENERG department, and in particular with the group headed by Prof. Radu Bojoi. Preliminary results are shown in Chapter 8.

In the last four months of the doctoral program, the attention was devoted to the EMI issues in Talkative Power Converters (TPC). The principles of SS were employed in the TPC domain to suppress harmonic contents causing disturbances. This work has mainly been conducted at the Power Electronic Chair of CAU Kiel, headed by Marco Liserre, and the details together with preliminary measurements are shown in Chapter 9.

Contents

Part I

Class-E Resonant DC-DC Converters

Introduction

This part dives into the realm of cutting-edge advancements in the design and control of resonant DC-DC converters. In this part, we delve into three distinct chapters, each unveiling innovations that push the boundaries of conventional methodologies.

In Chapter 1, a dimensionless analytical approach for class-E resonant DC-DC converters takes center stage. Pioneered in recent papers, this design methodology not only challenges the established norms of design but also extends its applicability across various class-E converter topologies. Its peculiarity is to be dimensionless and based on the exact solution of the system of differential equations regulating the behavior of the circuit, ensuring very high precision and reliability with respect to all methodologies previously proposed by the state of the art and based on the so-called sinusoidal approximation. Here, we review this methodology and improve it in a twofold way. On the one hand, we propose alternative modeling for some devices (in particular the transformer), increasing both flexibility and generality, with the possibility of extending the application to more topologies and more operating points. On the other hand, a new normalization is proposed, showing that the actual dimension of the design workspace is 2, and not 3 as assumed in the previous works. This has important consequences. As an example, the solution existence condition can be represented on a simple 2D plot, with the possibility to immediately check whether the optimal class-E condition can be ensured or not. Furthermore, we can completely and conveniently explore the entire design space to investigate properties such as the stress on the switching devices or the root-mean-square currents, allowing further optimization of the converter design.

Moving on to Chapter 2, a dual-frequency control method designed to regulate the output power in class-E resonant DC-DC converters is introduced. As in the standard ON-OFF control or other recently proposed dual-frequency controls, the approach is based on the ability of the converter to alternately operate in a high-

and low-power state. The proposed solution, based on the design described in the previous chapter, has a twofold advantage: on the one hand, soft-switching capabilities (i.e., zero-voltage and zero-voltage-derivative switching) are preserved in both operating states; on the other hand, it is possible to reduce to zero the transient time required to switch from one state to the other one. The most straightforward consequence is the possibility of increasing to very large values the frequency at which the two operating states are switched, up to the same order of magnitude as the main switching frequency of the converter. In this way, the additional ripple introduced by the proposed dual-frequency control can be decreased to a negligible value. The approach has been validated by measurements on a prototype operating between 4 and 8 MHz in which it has been possible to increase the control frequency up to 500 kHz.

Chapter 3 explores a through-the-barrier communication technique tailored for isolated resonant converters. The approach is capable of sending data bi-directionally at high speed (one bit for each converter clock period) without the need for any additional isolating device other than the transformer necessary for the power transfer and has been demonstrated by means of a proof-of-concept low-frequency prototype. In this chapter, we review that work under the assumption of increasing the operating frequency by using a coreless transformer presenting low losses, but also a low coupling factor k. This allows to increase the converter efficiency to a very high value (92% in the proposed design working at 6.78 MHz), but the communication speed has to be reduced (one bit every four clock cycles).

Chapter 1

Class-E DC-DC Converter Design

1.1 Introduction

Resonant dc-dc converters have been introduced to operate at high switching frequencies and so increase system power density [9–16], with advantages also in terms of dynamic performance [10] and EMI [16, 17]. Frequencies up to the VHF range $30-300\,\text{MHz}$ are possible [14, 15] by lowering switching losses thanks to techniques used in radio-frequency (RF) power amplifiers [9, 10, 18], thus overcoming the main drawback of conventional switching topologies given by the frequency-dependent losses. We focus here on the class-E approach [10, 13], featuring the so-called *soft-switching* technique in opposition to the *hard-switching* of class-D converters. It was first proposed by Sokal *et al.* in [9] to improve performance in RF amplifiers. In details, we refer to *Zero-Voltage Switching* (ZVS) if the reactive components reshape the voltage on a switch, either controlled (e.g., a power MOS) or non-controlled (a rectifying diode) in a way that it slowly goes to zero before the turn-on instant, and gradually increases from zero after the turn-off. We refer to *Zero-Voltage-Derivative Switching* (ZVDS) if it approaches zero also with zero-time-derivative. Alternatively, one may focus on the current flowing into the switch devices; this is referred to as *Zero-Current Switching* (ZCS) and *Zero-Current-Derivative Switching* (ZCDS)[1]. If both the zero-level and the zero-derivative conditions (either for voltages or currents) are satisfied, we achieve the *optimal* class-E operation. We refer to the achievement

[1]Note that with ZVS/ZVDS and ZCS/ZCDS we refer both to the controlled and non-controlled switches. However, some authors prefer to reserve these terms for the controlled switches only, and use the expression *low* dv/dt and *low* di/dt [19, 20, 16] for diodes.

of the zero-level condition only (i.e., without zero-derivative) as *suboptimal* class-E operation [21–23]. It is a common practice to consider resonant dc-dc converters as composed of the cascade of an inverter and a rectifier stage. While in some cases [11, 12, 16] a dc-dc converter is considered belonging to class-E when the inverter only is designed according to the class-E methodology and the rectifier is non-resonant, the converters we consider in this chapter are composed of both a class-E inverter and a class-E rectifier [24, 16]. Note that they are sometimes called class-E^2 converters [25–27] to distinguish them from converters where the inverter only relies on the class-E approach. Furthermore, we also focus on the voltage waveforms (i.e., ZVS and ZVDS) that, due to better performance [28, 16], is the technique considered in all recent papers.

Since the first proposal in [10], many papers have appeared in the Literature proposing improvements in the class-E dc-dc converter state of the art, even in recent years [29–36]. Many works are focused on the efficiency improvement or device stress reduction [37, 38]; others aim at improving the converter control [39, 33, 35, 36] or the design methodology [37, 39, 40, 31, 27, 34] in already known topologies. Recently, the class-E converters have received attention also for the possibility of relying on them the design of a wireless power system [41–45], and of embedding also data transfer in isolated converters without the need of additional isolating devices [46].

In this chapter, we follow up the works in [31, 34], and improve the normalized semi-analytical design methodology proposed there. In particular:

- the methodology is extended to cover more converter topologies and more operating regions (such as different duty-cycles for the switching clock, or different sequences of on and off configuration of the switches);
- we are able to reduce any considered converter, with any combination of input and output voltages, output power and switching frequency, to a 1 V-to-1 V, 1 W normalized converter operating at 1 rad/s.

Even if, apparently, these improvements are only minor ones, the second point is actually of a *paramount importance*, since it allows to reduce the dimension of the design workspace to 2, whereas 3 was assumed in [31, 34] (ignoring in both cases the additional design parameter given by the clock duty-cycle). This paves the way to the *exploration of the entire design space*. One can either look for an in-depth

converter optimization or explore the many trade-offs of the converter. In this chapter we are able to investigate, at the same time, properties such as the existence of the optimal or sub-optimal condition, the stress on the switching devices, the converter efficiency, the robustness to parameter variation, and the uniqueness of the optimal solution, and to evaluate which trade-off may represents the optimal point according to designer specifications. Such an exhaustive analysis was not possible with any other design approach presented so far in the Literature. An example can be found at the end of this chapter.

The chapter is organized to be self-consistent, and we choose on purpose to restate the description of the design problem from the start. In this way, we can avoid systematically referring [31] or [34], with increased readability. For a better organization, many details have been moved to the appendix, so that the reader can first focus on the exploration of the converter design space.

In detail, Section 1.2 presents a brief overview of the state of the art in the class-E dc-dc converters design. In Section 1.3 the normalized converter is introduced, whereas the exact analysis and the semi-analytical approach for its optimal design are postponed in Appendices A and B. In Section 1.4 we show how to denormalize the proposed converter into many real class-E topologies. Then, in Section 1.5 we investigate the converter design space and many properties such as the existence and uniqueness of the optimal class-E condition, the stress of the devices, the robustness of the operating point to parameter variations, and the converter efficiency. In Section 1.6 a design example taking into account all the considered issues is presented, and in Section 1.7 we compare the proposed improved approach with that introduced in [31]. Finally, we draw the conclusion.

1.2 State of the art in class-E converter design

The design of a class-E dc-dc converter is not an easy task, mainly due to the combination of non-linearities and of reactive elements in the circuit, which does not allow an exact symbolic solution of the circuit evolution. So, the design procedure has to be based on some approximated approach.

Historically, the most common approach is the well-known sinusoidal (also known as *first harmonic*) approximation originally used in RF circuits design [10, 11].

In detail, the design procedure is separated into the two steps concerning the design of the inverter stage (providing a dc/ac conversion with angular frequency $\omega_s = 2\pi f_s$) and of the rectifier stage (providing the final ac/dc conversion). First, the rectifier circuit is linearized and averaged by computing its input impedance, under the assumption that the input voltage is a sinusoidal tone at ω_s. Then, the design of the inverter is obtained assuming that it is a class-E power amplifier loaded by the equivalent rectifier impedance. Since the reflected rectifier impedance does not generally lead to the optimal primary load, which ensures both ZVS and ZVDS at the primary side, a matching network is interposed between the RF power amplifier and the rectifier to ensure the optimal class-E working condition. The first harmonic of the waveform on the equivalent rectifier impedance has to match (both in amplitude and phase) the sinusoidal tone assumed at the inverter input. An example of design relying on this approach can be found in [13].

It is clear that, with this approach, only approximated solutions can be achieved, and a subsequent refinement by means of additional, time-consuming SPICE simulations is often required. Furthermore, the approach is effective only if the sinusoidal assumption is verified. To support this assumption, a (high loaded quality factor) LC filter is sometimes added between the inverter and the rectifier, thus increasing converter size and cost. Furthermore, also large RF choke inductors can be added (typically, at the converter input and/or output node) to ensure the additional assumption of a constant current, and so to further simplify the converter analysis.

The recent years' Literature focuses on improving the standard design methodology with the main aim of removing (or, at least, replacing with smaller, resonant counterparts) bulky elements such as the input RF choke inductor or the high-Q LC filter. More complex design procedures have been proposed since, without the aforementioned structure, a meaningful difference between expected and actual waveforms would be observed.

We consider the state of the art in the design of a class-E converter as given by [31] and [34]. Bertoni *et al.* in [31] analyze the converter of Figure 1.1(a). The converter is isolated, and the distinction between the inverter stage (the primary side, that includes a MOS as a controlled switch) and the rectifier stage (secondary side, that includes a diode as a non-controlled switch) is clearly visible. The inverter and the rectifier stages are connected by means of the isolation transformer only and do not feature any additional LC filter or large RF choke inductor.

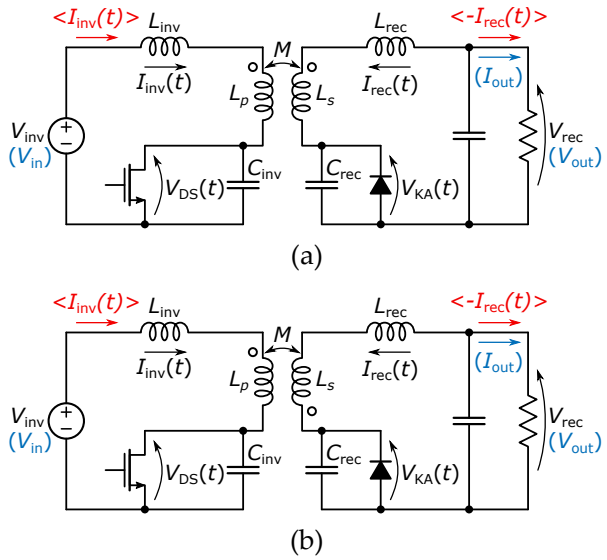


Fig. 1.1 Canonical isolated class-E converter schematics. (a) In-phase (direct) coupling. (b) 180° out-of-phase (inverse) coupling.

For this circuit, a semi-analytic design approach based on the exact solution of the system of differential equations regulating the converter evolution is proposed. The approach relies on the exact symbolic evolution of the converter, and only minor and negligible approximations are introduced; however it requires some coefficients whose numerical computation is necessary, hence it has to be considered semi-analytic.

This approach, differently from many others proposed in the Literature and based on ideal devices only, is also capable of taking into account the main circuit sources

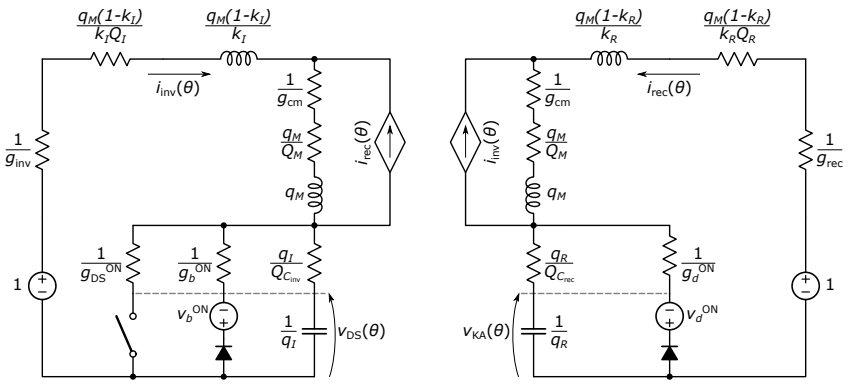


Fig. 1.2 Schematic of the normalized (1 V-to-1 V, 1 W, 1 rad/s) isolated class-E converter considered.

of losses. For the sake of generality, it is dimensionless, and based on the design of a normalized converter (1 V output voltage, 1 W output power, 1 rad/s angular frequency), that is then denormalized to deal with any output voltage, output power, and operating frequency. The only constraint is that the ratio between input and output voltages has to be equal to the design parameter $V_{\text{in}}/V_{\text{out}} = \mu$, and each value of μ identifies a different converter family.

In [34] Pareschi *et al.* extend the semi-analytic design approach to the circuit of Figure 1.1(b). The converter is identical to that of Figure 1.1(a), except that the transformer features an inverse coupling (i.e., 180° out-of-phase) instead of a direct (in-phase) one. Then, the authors show that these two converters are equivalent to many other non-isolated class-E dc-dc converters appeared in the recent Literature, and that the proposed design approach can be extended *as is* to all of them.

Here we further improve the design approach developed in [31, 34]. We are able to show that the parameter μ is not actually necessary, lowering to 2 the size of the design space and paving the way to an in-depth converter optimization through a comprehensive design space analysis. Note that, in this chapter, we focus on the theoretical model only. Adherence of the model both to low-level circuit simulations and to measurements from prototype has been already extensively proven in [31] and in [34], and are out of the scope of this work. This choice has been preferred to allow a more concise discussion.

Note that a class-E converter is typically designed for a given operating condition, which could be the one ensuring the nominal or the maximum output power. To cope with different output power, a control methodology among the many presented in the Literature may be applied. In this chapter we consider any control methodology to be applied to the designed converter out of scope and, referring to the notation of Figure 1.1, we will always assume that quantities that may actually exhibit variations such as V_{in} or I_{out} are a-priori known and fixed. As a matter of fact, a limitation of *all* resonant converters is that their behavior depends also on these quantities, and a designer can ensure ZVS and ZVDS *for a given operating condition only*, i.e., for a well-defined value of V_{in} and I_{out}. Control methodology such as frequency control [10, 33] or ON-OFF control [47, 39] ensure the correct output power even with a variable load or a non-precisely known V_{in}, but typically, at the cost of a perfect ZVS or ZVDS. To cite a simple example, we can consider the design in [13], where the optimal behavior is observed at the maximum output power only; at a lighter load,

the converter is regulated by increasing the switching frequency, but in this way, the system features *suboptimum* class-E condition only: a diode connected in antiparallel to the MOS switch (we refer to this as the *body diode* since, in most of the cases, it is just the parasitic diode present in any discrete MOS, not been depicted in the schematics of Figure 1.1 for the sake of simplicity) turns ON earlier than the MOS turn-on instant, thus ensuring ZVS operation, but not ZVDS. We refer the reader to the aforementioned works for possible ways to control the converter.

1.3 Dimensionless circuit analysis and design

Let us consider the schematic of Figure 1.2, depicting a class-E converter very similar to that of Figure 1.1, and designed to work as a 1 V-to-1 V converter clocked at 1 rad/s with a 1 W output power. Ideal devices only are considered, with many of them introduced to model the main sources of losses in non-ideal converters. To allow a simpler analysis, the output network (i.e., the filter capacitor and the load) is replaced with a 1 V voltage generator.

The actual inductors L_{inv} and L_{rec} are replaced with two inductances $q_M(1-k_I)/k_I$ and $q_M(1-k_R)/k_R$, and the two series resistances $q_M(1-k_I)/k_I/Q_I$ and $q_M(1-k_R)/k_R/Q_R$, respectively, whereas the transformer with the inductance q_M and the series resistance q_M/Q_M, as well as with two controlled current generators to model the interaction between the primary and the secondary side. The actual capacitors C_{inv} and C_{rec} are replaced with capacitances $1/q_I$ and $1/q_R$, with series resistances $q_I/Q_{C_{\text{inv}}}$ and $q_R/Q_{C_{\text{rec}}}$. The rectifying diode is ideal, with a series resistance $1/g_d^{\text{ON}}$ and a voltage drop v_d^{ON}. The MOS is an ideal switch with a series resistance $1/g_{\text{DS}}^{\text{ON}}$; its body diode has also been considered as an ideal diode with series resistance $1/g_b^{\text{ON}}$ and a voltage drop v_b^{ON}. Finally, three additional resistances $1/g_{\text{inv}}$, $1/g_{\text{rec}}$ and $1/g_{\text{cm}}$ have been introduced to model additional losses in the inverter loop, in the rectifying loop, or in both.

This circuit is described by the five main dimensionless parameters (circuit design parameters)

$$q_I, q_R, q_M, k_I, k_R \tag{1.1}$$

and by the many secondary dimensionless parameters related to circuit losses (lossy parameters)

$$\begin{gathered} v_d^{\mathrm{ON}}, v_b^{\mathrm{ON}}, Q_I, Q_R, Q_M, Q_{C_{\mathrm{inv}}}, Q_{C_{\mathrm{rec}}}, \\ g_{\mathrm{inv}}, g_{\mathrm{DS}}^{\mathrm{ON}}, g_b^{\mathrm{ON}}, g_{\mathrm{cm}}, g_d^{\mathrm{ON}}, g_{\mathrm{rec}} \end{gathered} \tag{1.2}$$

that can be set to 0 (in the case of v_b^{ON} and v_d^{ON}) or to infinity (all other ones) in case of an ideal associated device (lossless analysis).

The circuit of Figure 1.2 has been introduced with no actual physical meaning, but with the only aim of supporting a mathematical model of a class-E converter. Values of inductances and resistances, in fact, can be either positive or negative. Furthermore, we have considered a normalized time variable θ, so that the main switch is driven by a clock with 2π period and duty cycle D. This circuit:

- can be used to describe both converters of Figure 1.1 (and also many others) by means of a simple change of variables, as detailed in Section 1.4;
- can be analytically solved through a step-wise analysis similar to that proposed in [31], and based on the assumptions that the evolution of the converter relies on the succession of many different *configurations* (Z_1, Z_2, Z_3, Z_{3a}, Z_4, Z_{4a}, as described in Appendix A) according to the on/off state of its three non-linear devices (i.e., the MOS switch and the two diodes);

The circuit solution, detailed in Appendix A, leads to the definition of the mathematical expressions for the four (normalized) state variables of the circuit, i.e., $i_{\mathrm{inv}}(\theta)$, $i_{\mathrm{rec}}(\theta)$, $v_{\mathrm{DS}}(\theta)$, and $v_{\mathrm{KA}}(\theta)$ (lower case to indicate electrical quantities of the normalized circuit). These are expressed as functions of the circuit parameters, and of the circuital initial conditions $i_{\mathrm{inv}}(0) = i_{\mathrm{inv}}^{(0)}$, $i_{\mathrm{rec}}(0) = i_{\mathrm{rec}}^{(0)}$, $v_{\mathrm{KA}}(0) = v_{\mathrm{KA}}^{(0)}$, but independently of $v_{\mathrm{DS}}(0)$ thanks to the particular choice of the reference time $\theta = 0$. The Matlab software developed, along with all the software used in this thesis, is freely distributed in [2].

As an example, in Figure 1.3(a) we have shown the evolution analytically computed in the normalized time $0 \leq \theta \leq 4\pi$ (two consecutive periods) for a lossless system, with $D = 50\%$ and assuming the parameters $i_{\mathrm{inv}}^{(0)} = 0$, $i_{\mathrm{rec}}^{(0)} = 0.463$, $v_{\mathrm{KA}}^{(0)} = 2.156$, $q_I = 2.193$, $q_R = 1.586$, $q_M = 3.04$, $k_I = 0.8$, $k_R = 0.8$. The evolution starts at $\theta = 0$ with the rectifying diode off, and shows in the first period the configuration sequence

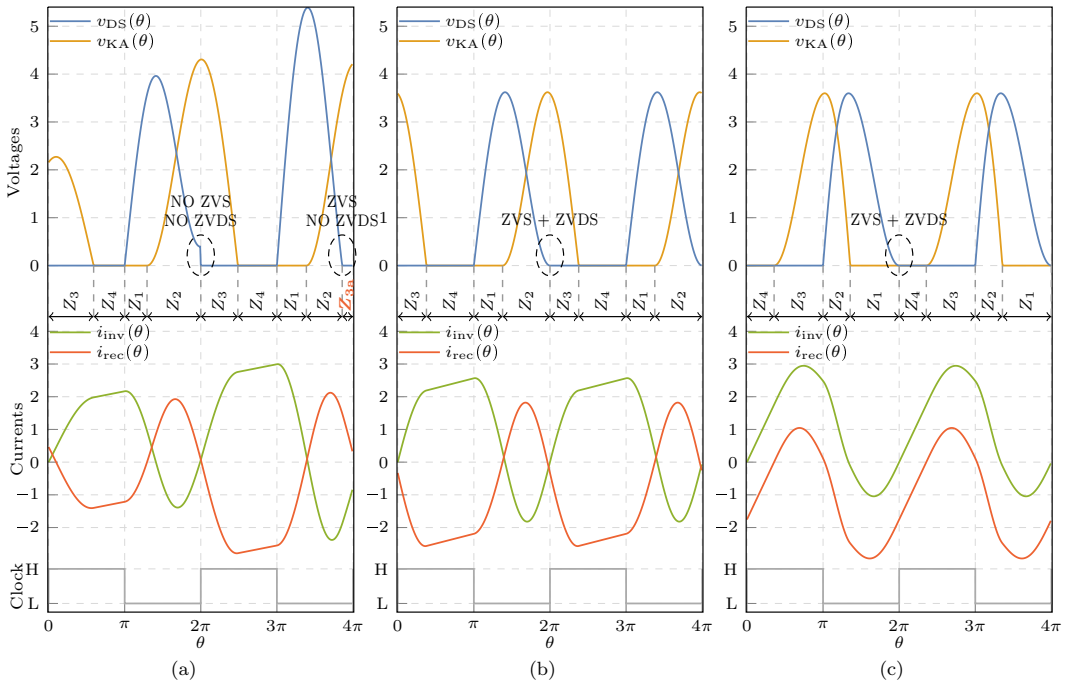


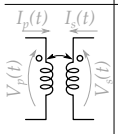
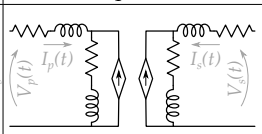
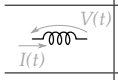
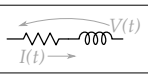
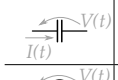
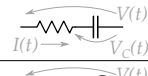
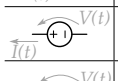
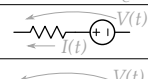
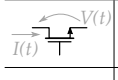
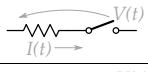
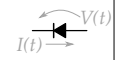
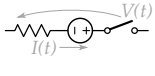
Fig. 1.3 Evolution of the normalized lossless converter for $0 \leq \theta \leq 4\pi$: (a) random values of the parameters; (b) optimal class-E condition, achieved for $k_I = 0.8$ and $k_R = 0.8$; (c) optimal class-E condition, achieved for $k_I = -0.8$ and $k_R = -0.8$.

$Z_3Z_4Z_1Z_2$, with $v_{DS}(2\pi^-) = 0.398 > 0$, i.e., ZVS is not achieved. In the second period the observed sequence is $Z_3Z_4Z_1Z_2Z_{3a}$, and actually features ZVS since the body diode turns on at $\theta = 3.86\pi < 4\pi$ and $v_{DS}(4\pi^-) = -v_b^{ON} = 0$, but not ZVDS.

Note that the achieved evolution is exactly what we could get from any circuital simulator. However, in this case it is achieved by means of exact mathematical functions, that can be used for any further mathematical optimization instead of time-consuming transient circuital simulations. Our aim is to exploit these functions to describe ZVS and ZVDS in terms of mathematical constraints, and use a numerical optimization software to manipulate the circuit parameters so that the evolution of the converter actually features optimal class-E condition at stationary regime.

This approach leads to the set of constraints (B.1a)–(B.1g), whose detailed explanation can be found in Appendix A. Now, let us assume that D is known an fixed, that all design parameters in (1.1), as well as initial conditions, are free design variables, and that lossy parameters in (1.2) are given (constrained, for example, by technological limits). According to this point of view, (B.1a)–(B.1g) can be considered as a system of seven equations to be solved in the eight unknowns

Table 1.1 Real device models used for the lossy converter analysis.

Device	Eq. sch.	Mathematical model
		$\begin{pmatrix} V_P(t) \\ V_S(t) \end{pmatrix} = \begin{pmatrix} L_P & \pm M \\ \pm M & L_S \end{pmatrix} \frac{d}{dt} \begin{pmatrix} I_P(t) \\ I_S(t) \end{pmatrix} + + \omega_s \begin{pmatrix} L_P/Q_{L_P} & \pm M/Q_M \\ \pm M/Q_M & L_S/Q_{L_S} \end{pmatrix} \begin{pmatrix} I_P(t) \\ I_S(t) \end{pmatrix}$
		$V(t) = L\frac{dI(t)}{dt} + L\frac{\omega_s}{Q_L} I(t)$
		$V(t) = V_C(t) + \frac{1}{\omega_s C Q_C} I(t), \quad I(t) = C\frac{dV_C(t)}{dt}$
		$V(t) = V_S - R_S I_S(t)$
		$V(t) = R_{\mathrm{DS}}^{\mathrm{ON}} I(t) \quad (m^{\mathrm{ON}} = 1)$ $I(t) = 0 \quad (m^{\mathrm{ON}} = 0)$
		$V(t) = -V_d^{\mathrm{ON}} + R_d^{\mathrm{ON}} I(t),\ I(t) < 0 \quad (d^{\mathrm{ON}} = 1)$ $V(t) > 0,\ I(t) = 0 \quad (d^{\mathrm{ON}} = 0)$

$i_{\mathrm{inv}}^{(0)}$, $i_{\mathrm{rec}}^{(0)}$, $v_{\mathrm{KA}}^{(0)}$, q_I, q_R, q_M, k_I and k_R, i.e., in the set including all initial conditions and all design parameters. However, being the system strongly non-linear (all the expressions of the evolution of the state variable are non-linear), properties such as the existence and the number of solutions cannot be a-priori determined by only looking at the number of equations and of unknowns.

Anyway, the system is under-determined. Empirically, two degrees of freedom exist, and once they are set, a single solution can be found for almost all combinations of the degrees of freedom. For example, assuming $D = 50\%$ and by imposing $k_I = 0.8$ and $k_R = 0.8$, the solution of the above mathematical problem is ensured by $i_{\mathrm{inv}}^{(0)} = 0$, $i_{\mathrm{rec}}^{(0)} = -0.331$, $v_{\mathrm{KA}}^{(0)} = 3.593$, $q_I = 1.687$, $q_R = 1.687$, $q_M = 2.338$. The evolution of the converter when using these parameters is depicted in Figure 1.3(b), showing that the stationary condition, the ZVS, and the ZVDS are perfectly achieved. The observed sequence of configurations is $Z_3Z_4Z_1Z_2$.

Interestingly, the mathematical problem has solutions also for negatives values of k_I, k_R and q_M. By imposing $k_I = -0.8$ and $k_R = -0.8$, we get a solution for $i_{\mathrm{inv}}^{(0)} = 0$, $i_{\mathrm{rec}}^{(0)} = -1.755$, $v_{\mathrm{KA}}^{(0)} = 0$, $q_I = 2.581$, $q_R = 2.581$, $q_M = -2.55$, and the corresponding evolution has been plotted in Figure 1.3(c). The sequence of configurations is different from the previous case, and given by $Z_4Z_3Z_2Z_1$.

Note that, in both cases, we have $i_{\mathrm{inv}}^{(0)} = 0$. This is actually a constraint when asking for ZVDS, as observed in Appendix B. Note also that in the normalized converter, by indicating with the notation $\langle f(\theta) \rangle$ the average value of $f(\theta)$ over one

period, we have that the output delivered power is $1 \cdot \langle -i_{\text{rec}}(\theta) \rangle = 1$, and the input power $1 \cdot \langle i_{\text{inv}}(\theta) \rangle \geq 1$. The efficiency of the converter is $\eta = 1/\langle i_{\text{inv}}(\theta) \rangle \leq 1$.

1.4 Denomalization of the normalized converter

By introducing simple changes of variables, as detailed in the following, both schematics of Figure 1.1 can be reduced to the normalized converter of Figure 1.2.

First, for both topologies, let us consider the output network replaced by a (real) voltage source V_{out}. Let the design rely on the state variable $I_{\text{inv}}(t)$, $I_{\text{rec}}(t)$, $V_{\text{DS}}(t)$, $V_{\text{KA}}(t)$ (upper case to indicate electrical quantities at the real circuit) as a function of the time t. Let us also define the design meta-variable $\langle I_{\text{inv}}(t) \rangle$ and $\langle -I_{\text{rec}}(t) \rangle$ as the average values of $I_{\text{inv}}(t)$ and $-I_{\text{rec}}(t)$ over one converter period $T_s = 1/f_s$, and V_{inv} and V_{rec}, defined as, for both schematics[2]

$$\begin{aligned} V_{\text{inv}} = V_{\text{in}},\ V_{\text{rec}} = V_{\text{out}}, \\ \langle I_{\text{inv}}(t) \rangle = I_{\text{in}},\ \langle -I_{\text{rec}}(t) \rangle = I_{\text{out}}. \end{aligned} \tag{1.3}$$

With this, the inverter and the rectifier loop are similar, with a voltage generator (V_{inv} and V_{rec}), an inductor (L_{inv} and L_{rec}), one side of the transformer, and one capacitor (C_{inv} and C_{rec}) in parallel with a switching device.

Then, let us replace all devices according to Table 1.1 in order to include the main sources of losses, so that both schematics can be described by the main parameters (circuit design parameters)

$$L_{\text{inv}}, L_{\text{rec}}, M, L_p, L_s, C_{\text{inv}}, C_{\text{rec}}$$

and the secondary parameters (lossy parameters)

[2]The reason for introducing these meta-variables is to allow the analysis also when considering non-isolated converter topologies, where the relation between V_{in} and V_{out} with the introduced V_{inv} and V_{rec}, and between I_{in} and I_{out} with $\langle I_{\text{inv}}(t) \rangle$ and $\langle -I_{\text{rec}}(t) \rangle$, is not straightforward as in this case. The choice of $\langle -I_{\text{rec}}(t) \rangle$ as meta-variable is due to the advantage of dealing with positive value variables only.

$$V_d^{\mathrm{ON}}, V_b^{\mathrm{ON}}, Q_{L_{\mathrm{inv}}}, Q_{L_{\mathrm{rec}}}, Q_M, Q_{L_p}, Q_{L_s}, Q_{C_{\mathrm{inv}}}, Q_{C_{\mathrm{rec}}},$$
$$R_{\mathrm{in}}, R_{\mathrm{out}}, R_{\mathrm{DS}}^{\mathrm{ON}}, R_d^{\mathrm{ON}}, R_b^{\mathrm{ON}}$$

where R_d^{ON} and V_d^{ON} refer to the rectifying diode, R_b^{ON} and V_b^{ON} refer to the MOS body diode, $Q_{L_{\mathrm{inv}}}$ and $Q_{L_{\mathrm{rec}}}$ are the quality factors of L_{inv} and L_{rec}, Q_M, Q_{L_p} and Q_{L_s} indicate the losses of the transformer, $Q_{C_{\mathrm{inv}}}$ and $Q_{C_{\mathrm{rec}}}$ are the quality factor of C_{inv} and C_{rec}, and the R_{in} and R_{out} are the series resistances of the real generators (Thevenin equivalent) used to replace the input source and the output network, respectively.

Now, let us write down the equations regulating the evolution of the converters following the same procedure used for the normalized converter in Appendix A, and leading to (A.1). We can get exact equivalence between all systems by imposing

$$\begin{gathered} I_{\mathrm{inv}}(t) = \frac{V_{\mathrm{rec}}\langle -I_{\mathrm{rec}}(t)\rangle}{V_{\mathrm{inv}}} i_{\mathrm{inv}}(\theta), \quad I_{\mathrm{rec}}(t) = \langle -I_{\mathrm{rec}}(t)\rangle \, i_{\mathrm{rec}}(\theta), \\ V_{\mathrm{DS}}(t) = V_{\mathrm{inv}} v_{\mathrm{DS}}(\theta), \quad V_{\mathrm{KA}}(t) = V_{\mathrm{rec}} v_{\mathrm{KA}}(\theta), \quad \theta = \omega_s t \end{gathered} \tag{1.4}$$

and, for the in-phase coupling case

$$\begin{gathered} q_I = \frac{V_{\mathrm{rec}}\langle -I_{\mathrm{rec}}(t)\rangle}{V_{\mathrm{inv}}^2} \frac{1}{\omega_s C_{\mathrm{inv}}}, \; q_R = \frac{\langle -I_{\mathrm{rec}}(t)\rangle}{V_{\mathrm{rec}}} \frac{1}{\omega_s C_{\mathrm{rec}}}, \\ q_M = \frac{\langle -I_{\mathrm{rec}}(t)\rangle}{V_{\mathrm{inv}}} \omega_s M, \qquad , \\ k_I = \frac{V_{\mathrm{inv}}}{V_{\mathrm{rec}}} \frac{M}{L_{\mathrm{inv}} + L_p}, \; k_R = \frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}} \frac{M}{L_{\mathrm{rec}} + L_s} \end{gathered} \tag{1.5}$$

whereas for the 180° out-of-phase coupling

$$\begin{gathered} q_I = \frac{V_{\mathrm{rec}}\langle -I_{\mathrm{rec}}(t)\rangle}{V_{\mathrm{inv}}^2} \frac{1}{\omega_s C_{\mathrm{inv}}}, \; q_R = \frac{\langle -I_{\mathrm{rec}}(t)\rangle}{V_{\mathrm{rec}}} \frac{1}{\omega_s C_{\mathrm{rec}}}, \\ q_M = -\frac{\langle -I_{\mathrm{rec}}(t)\rangle}{V_{\mathrm{inv}}} \omega_s M, \qquad . \\ k_I = -\frac{V_{\mathrm{inv}}}{V_{\mathrm{rec}}} \frac{M}{L_{\mathrm{inv}} + L_p}, \; k_R = -\frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}} \frac{M}{L_{\mathrm{rec}} + L_s} \end{gathered} \tag{1.6}$$

Transformation rules for the lossy parameters are postponed to Appendix C.

The main difference between the in-phase and the 180° out-of-phase coupling is that in the former we have $q_M > 0$, $k_I > 0$ and $k_R > 0$, whereas in the latter

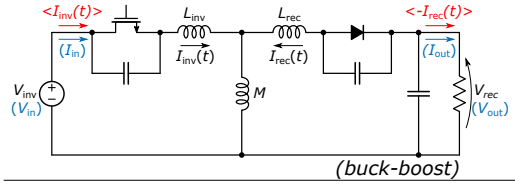
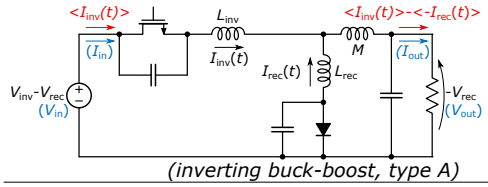
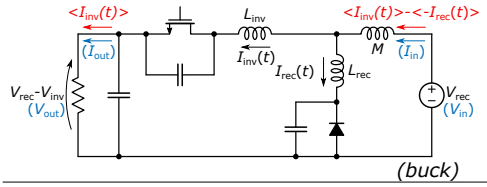
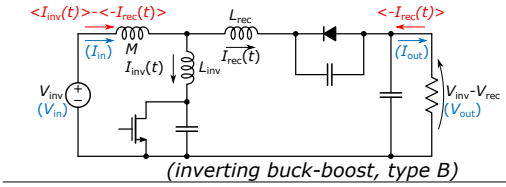
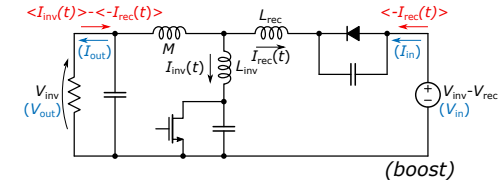
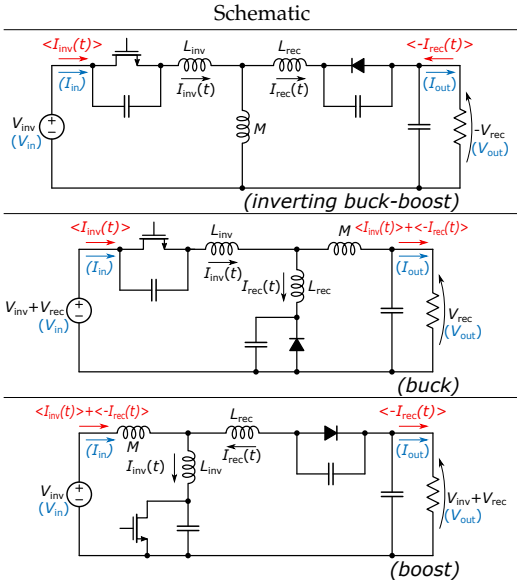
Schematic	Denormalization
	*same as* (5), (6) *and* (7) $\eta = \dfrac{1}{\langle i_{\mathrm{inv}}(\theta)\rangle}$
	$V_{\mathrm{in}} = V_{\mathrm{inv}} - V_{\mathrm{rec}},\ V_{\mathrm{out}} = -V_{\mathrm{rec}} < 0$ $I_{\mathrm{out}} = \langle I_{\mathrm{inv}}(t)\rangle - \langle -I_{\mathrm{rec}}(t)\rangle < 0$ $\eta = \dfrac{1}{\langle i_{\mathrm{inv}}(\theta)\rangle}\dfrac{1 - \langle i_{\mathrm{inv}}(\theta)\rangle\frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}}}{1 - \frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}}} < \dfrac{1}{\langle i_{\mathrm{inv}}(\theta)\rangle} \quad \left(\dfrac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}} < \dfrac{1}{\langle i_{\mathrm{inv}}(\theta)\rangle}\right)$
	$V_{\mathrm{in}} = V_{\mathrm{rec}},\ V_{\mathrm{out}} = V_{\mathrm{rec}} - V_{\mathrm{inv}}$ $I_{\mathrm{in}} = \langle I_{\mathrm{inv}}(t)\rangle - \langle -I_{\mathrm{rec}}(t)\rangle,\ I_{\mathrm{out}} = \langle I_{\mathrm{inv}}(t)\rangle$ $\eta = \langle i_{\mathrm{inv}}(\theta)\rangle\dfrac{\frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}} - 1}{\langle i_{\mathrm{inv}}(\theta)\rangle\frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}} - 1} \quad \left(\dfrac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}} > 1\right)$
	$V_{\mathrm{out}} = V_{\mathrm{inv}} - V_{\mathrm{rec}} < 0$ $I_{\mathrm{in}} = \langle I_{\mathrm{inv}}(t)\rangle - \langle -I_{\mathrm{rec}}(t)\rangle,\ I_{\mathrm{out}} = -\langle -I_{\mathrm{rec}}(t)\rangle < 0$ $\eta = \dfrac{\frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}} - 1}{\langle i_{\mathrm{inv}}(\theta)\rangle\frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}} - 1} < \dfrac{1}{\langle i_{\mathrm{inv}}(\theta)\rangle} \quad \left(\dfrac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}} > 1\right)$
	$V_{\mathrm{in}} = V_{\mathrm{inv}} - V_{\mathrm{rec}},\ V_{\mathrm{out}} = V_{\mathrm{inv}}$ $I_{\mathrm{in}} = \langle I_{\mathrm{rec}}(t)\rangle,\ I_{\mathrm{out}} = \langle -I_{\mathrm{rec}}(t)\rangle - \langle I_{\mathrm{inv}}(t)\rangle$ $\eta = \dfrac{1 - \langle i_{\mathrm{inv}}(\theta)\rangle\frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}}}{1 - \frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}}} \quad \left(\dfrac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}} < \dfrac{1}{\langle i_{\mathrm{inv}}(\theta)\rangle}\right)$

Fig. 1.4 Schematic of non-isolated class-E converter topologies derived from the in-phase coupling isolated converter, and denormalization rules for perfect equivalence for the normalized converter of Figure 1.2. Only differences with respect to (1.3), (1.4) and (1.5) are shown. Rules for the lossy parameters can be found in Appendix C.



$$V_{\text{out}} = -V_{\text{rec}} < 0,\ I_{\text{out}} = -\langle I_{\text{rec}}(t)\rangle < 0 \qquad \eta = \frac{1}{\langle i_{\text{inv}}(\theta)\rangle}$$

$$V_{\text{in}} = V_{\text{inv}} + V_{\text{rec}},\ I_{\text{out}} = \langle I_{\text{inv}}(t)\rangle + \langle -I_{\text{rec}}(t)\rangle \qquad \eta = \frac{1}{\langle i_{\text{inv}}(\theta)\rangle}\frac{1+\langle i_{\text{inv}}(\theta)\rangle\frac{V_{\text{rec}}}{V_{\text{inv}}}}{1+\frac{V_{\text{rec}}}{V_{\text{inv}}}} > \frac{1}{\langle i_{\text{inv}}(\theta)\rangle}$$

$$V_{\text{out}} = V_{\text{inv}} + V_{\text{rec}},\ I_{\text{in}} = \langle I_{\text{inv}}(t)\rangle + \langle -I_{\text{rec}}(t)\rangle \qquad \eta = \frac{1+\frac{V_{\text{rec}}}{V_{\text{inv}}}}{1+\langle i_{\text{inv}}(\theta)\rangle\frac{V_{\text{rec}}}{V_{\text{inv}}}} > \frac{1}{\langle i_{\text{inv}}(\theta)\rangle}$$

Fig. 1.5 Schematic of non-isolated class-E converter topologies derived from the 180° out-of-phase coupling isolated converter, and denormalization rules for perfect equivalence for the normalized converter of Figure 1.2. Only differences with respect to (1.3), (1.4) and (1.6) are shown. Rules for the lossy parameters can be found in Appendix C.

$q_M < 0$, $k_I < 0$ and $k_R < 0$. In both cases, the efficiency of the converter is given by $\eta = V_{\text{rec}}\langle -I_{\text{rec}}(t)\rangle / V_{\text{inv}} / \langle I_{\text{inv}}(t)\rangle = 1/\langle i_{\text{inv}}(\theta)\rangle$.

Interestingly, we may note that a designer may be not interested in an isolated topology. In this case, the transformer can be replaced by a real single inductance with $L_p = L_s = M$ and $Q_{L_p} = Q_{L_s} = Q_M$. The two schematics of Figures 1.1(a) and 1.1(b) can be modified to get all schematics of Figures 1.4 and 1.5, respectively. All of them are simply obtained from the isolated converters by rearranging elements in the inverter or in the rectifier loop in order to obtain a ground-referred V_{out}. As for the isolated converters, it is possible to show equivalence between these schematics and the normalized one of Figure 1.2. The changes of variables required are similar to that in (1.3), (1.4) and (1.5) for all schematics of Figure 1.4, and to that in (1.3), (1.4) and (1.6) for all schematics of Figure 1.5. The exact relations, when different from the reference isolated converter cases, are reported next to each specific schematic. As in the previous case, transformation rules for the lossy parameters are postponed to Appendix C.

The main differences with respect to the already considered cases involve how V_{in}, V_{out}, I_{in} and I_{out} are related to the meta-variables V_{inv}, V_{rec}, $\langle I_{\text{inv}}(t)\rangle$ and $\langle -I_{\text{rec}}(t)\rangle$, and the definition of $1/g_{\text{in}}$, $1/g_{\text{cm}}$ and $1/g_{\text{out}}$.

Note that the equivalence between the canonical isolated converter with 180° out-of-phase coupling and the schematics of Figure 1.5 was already observed in [34]. This includes the class-E buck converter [48–50] and the class-E boost converter [51–53, 39, 54], well known in the Literature. Conversely, almost all schematics of Figure 1.4 are new and have been obtained using the same circuital transformation as that used for the obtained schematic of Figure 1.5.

Note also that in the schematics derived from the 180° out-of-phase coupling, in the definitions of input or output voltages and currents, the terms $V_{\text{inv}} + V_{\text{rec}}$ and $\langle I_{\text{inv}}(t)\rangle + \langle -I_{\text{inv}}(t)\rangle$ appear. These are always positive quantities. Instead, in some schematics derived from the in-phase coupling, we can identify the terms $V_{\text{inv}} - V_{\text{rec}}$ and $\langle I_{\text{inv}}(t)\rangle - \langle -I_{\text{rec}}(t)\rangle$, that can be either positive or negative.

Interestingly, for the feasibility of the converter, these two terms must feature opposite signs. This happens either for $V_{\text{inv}}/V_{\text{rec}} < 1/\langle i_{\text{inv}}(\theta)\rangle < 1$, or $V_{\text{inv}}/V_{\text{rec}} > 1$. According to which one among these two assumptions is verified, we deal with two different schematics, where in one of them the roles of source and load of energy are exchanged with respect to what we have seen up to now (i.e., V_{rec} plays the role of source voltage and $\langle I_{\text{inv}}(t)\rangle >$ of load current, or V_{inv} the role of load voltage and $\langle -I_{\text{rec}}(t)\rangle$ of source current). The case $1/\langle i_{\text{inv}}(\theta)\rangle < V_{\text{inv}}/V_{\text{rec}} < 1$ is not interesting, since it leads to converters where both sides act as sources of energy, that is entirely dissipated by the converter losses.

Finally, the converter efficiency as a function of $\langle i_{\text{inv}}(\theta)\rangle$ has been computed for all considered schematics, and can be equal, smaller, or even larger, with respect to the reference value $1/\langle i_{\text{inv}}(\theta)\rangle$.

In conclusion, to analyze the behavior of the real converter, it is enough to get a solution of the normalized one, and convert it by using the proposed denormalization rules using the value of ω_s, V_{inv}, V_{rec} and $\langle -I_{\text{rec}}(t)\rangle$ only. The approach is not different from that proposed in [34], but the design parameter μ, defined both in [31] and in [34] as $\mu = V_{\text{in}}/V_{\text{out}}$, is not necessary anymore.

From the designer's point of view, this is indeed a very important advantage. Referring to the normalized system, the number of degrees of freedom is two. In

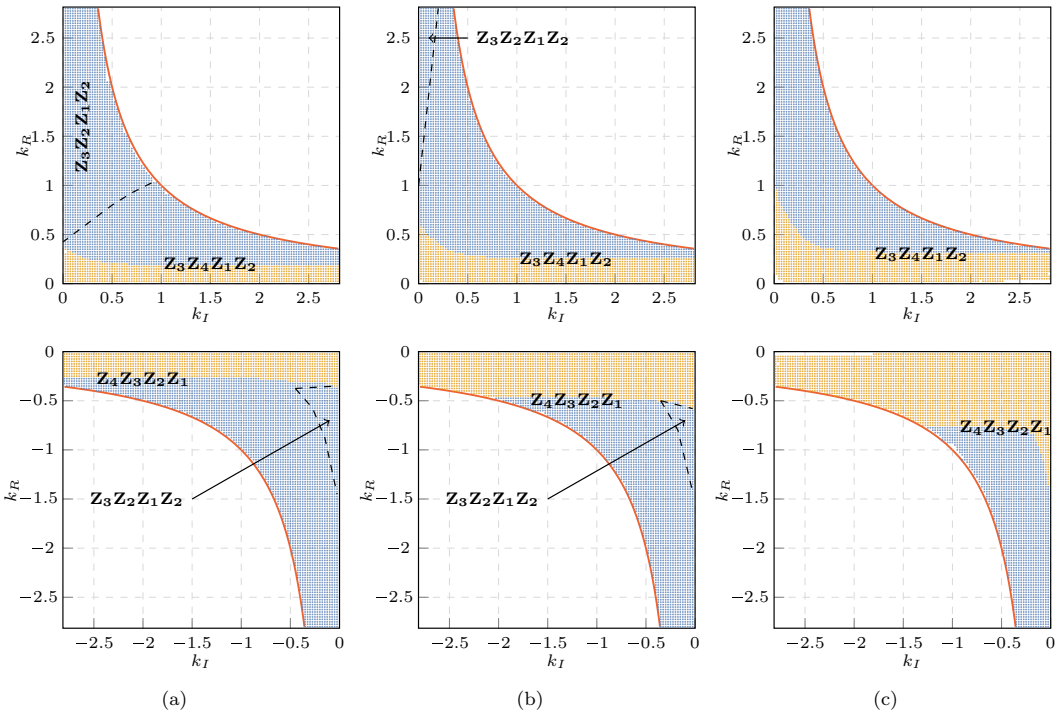


Fig. 1.6 Existence of the solution of the class-E design problem in the lossless normalized system for different values of the duty cycles D, assuming k_I and k_R as free variables. Blue points refer to the optimal (ZVS + ZVDS) class-E solution, whereas orange points to a sub-optimal solution (ZVS only). (a) $D = 30\%$. (b) $D = 40\%$. (c) $D = 50\%$.

other words, it is possible to set two among the parameters in (1.1) and find all the others by solving the mathematical problem imposed by the optimal class-E condition. The space of the solution can be plotted in a 2-D graph, and it is possible to identify areas of the solution space where the choice of the degrees of freedom allows a solution of the design problem, and others where no solutions exist. Another advantage of this approach is given by the normalization with respect to both the input and output voltages (the converter of Figure 1.2 is 1 V-to-1 V). This allows the fair comparison of performance in terms of quantities related both to the primary side and to the secondary side. As an example, one of the most important stress conditions for the MOS device is given by the maximum value of the $V_{\mathrm{DS}}(t)$ in the off state. In the proposed approach is possible to study this problem by looking at the normalized $v_{\mathrm{DS}}(\theta)$ waveform only, since its denormalization depends on the input voltage only, and not on the output voltage.

1.5 Design state space exploration for the normalized converter

As already anticipated, the design optimization problem of Section 1.3 for the normalized converter, and that can be applied also to all converters of Section 1.4, has two degrees of freedom. We focus on k_I and k_R as free design variables for many reasons, all of them inferred from (1.5) and (1.6).

The first practical reason is that k_I and k_R fix the ratio of the inductors in the circuit. Since the selection of the inductors is typically the most constrained problem in circuit design, we prefer to give to a designer the choice of k_I and k_R. Furthermore, as already observed in [34], a designer can opt to set either $L_{\text{inv}} = 0$ or $L_{\text{rec}} = 0$ in the aim of simplifying the circuit design. This option can be enabled by setting the proper value of k_I or k_R.

As a second reason, let us consider to model the transformer according to the coupling factor k and the turns ratio n_p/n_s as in [31]. Since $k = M/\sqrt{L_p L_s}$ and $n_p/n_s = \sqrt{L_p/L_s}$, it is possible to rewrite the definition of k_I and k_R as

$$\begin{aligned} k_I &= \pm k \frac{L_p}{L_{\text{inv}} + L_p} \frac{n_s}{n_p} \frac{V_{\text{inv}}}{V_{\text{rec}}}, \\ k_R &= \pm k \frac{L_s}{L_{\text{rec}} + L_s} \frac{n_p}{n_s} \frac{V_{\text{rec}}}{V_{\text{inv}}} \end{aligned} \tag{1.7}$$

i.e., k_I and k_R can be considered the extension (at the inverter and the rectifier side, respectively) of the coupling factor k of the transformer, which is a parameter quite difficult to control.

A final mathematical reason is that the values of k_I and k_R are constrained. Since $L_{\text{inv}} \geq 0$, $L_{\text{rec}} \geq 0$ and $0 < k \leq 1$, we have

$$|k_I| \leq k_I^{(\text{lim})} = \frac{n_s}{n_p} \frac{V_{\text{inv}}}{V_{\text{rec}}}, \quad |k_R| \leq k_R^{(\text{lim})} = \frac{n_p}{n_s} \frac{V_{\text{rec}}}{V_{\text{inv}}}, \quad k_I k_R \leq 1 \tag{1.8}$$

i.e., k_I and k_R are both independently constrained (where the bound is known only once $V_{\text{inv}}/V_{\text{rec}}$ and n_p/n_s are set) and also mutually constrained, i.e., $k_I k_R < 1$ independently of all other parameters.

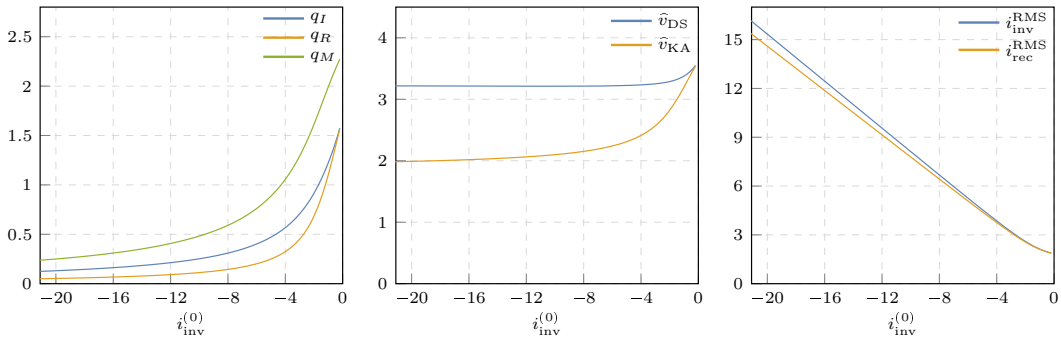


Fig. 1.7 Component and stress analysis for relaxed design solutions for $k_I = 0.8$ and $k_R = 0.8$, with $D = 50\%$. (a) values of q_I, q_R and q_M, that are proportional to the capacitances and inductances values; (b) voltage peak value across the MOS and the rectifying diode, respectively; (c) RMS value of the $i_{\mathrm{inv}}(\theta)$ and $I_{\mathrm{rec}}(\theta)$ currents.

1.5.1 Existence of an optimal solution

Once the degrees of freedom k_I and k_R have been selected, one may wonder if this choice effectively allows a solution.

In Figure 1.6 we have plotted, using blue dots, all points for which we were able to find a solution to the optimal class-E design problem, i.e., ensuring ZVS and ZVDS. The figure refers to the lossless system, i.e., with $v_d^{\mathrm{ON}} = v_b^{\mathrm{ON}} = 0$ and all quality factors to infinity. All the datasets are included in [2]. In our intention, these plots have to be used as a proxy for checking the existence of the solution in a real lossy system, under the assumption that the results may slightly change once the lossy parameters are considered, and actual existence has to be verified. The figure, also, refers both to the in-phase coupling (i.e., $k_I > 0$ and $k_R > 0$) and the 180° out-of-phase coupling (i.e., $k_I < 0$ and $k_R < 0$), and for the cases $D = 30\%$, $D = 40\%$ and $D = 50\%$ (i.e., $\theta_2 = 0.6\pi$, $\theta_2 = 0.8\pi$ and $\theta_2 = \pi$). Larger values of the duty-cycle are characterized by a much smaller area, and we consider these cases not interesting.

The values of q_I, q_R and q_M associated to each point can be found in the datasets provided in [2]. Interestingly, q_I and q_R do not feature a large spread of their value but are indeed limited from a few tenths to a few units. Conversely, both for the in-phase and the 180° out-of-phase coupling the absolute value of q_M goes to infinity when the considered point approaches the existence boundary condition $k_I k_R = 1$, plotted as a red line in the figure. Since $|q_M|$ is proportional to the value of all

inductors, it is not suggested to set a working point next to the existence boundary condition.

In the figure, we have also indicated the configuration sequence observed. In the large majority of the cases, the observed sequence is $Z_3Z_4Z_1Z_2$ for the in-phase coupling, and $Z_4Z_3Z_2Z_1$ for the 180° out-of-phase coupling, exactly as in the examples of Figure 1.3. Indeed, in some cases, and especially for low values of D, we observe that the rectifying diode is always off when the MOS switch is on, and the Z_4 configuration is missing. In these cases, the sequence is $Z_3Z_2Z_1Z_2$, either for the in-phase coupling or the 180° out-of-phase coupling.

1.5.2 Existence of sub-optimal solutions

Sometimes it is possible to *relax* the requirements for a class-E converter, asking for a ZVS condition only. This case is addressed as sub-optimal. In terms of the mathematical problem discussed in Appendix B, it is enough to remove the constraint identified by (B.1g).

As a matter of fact, a sub-optimal solution is not unique since the value of $dv_{\mathrm{DS}}(\theta)/d\theta$ at the MOS turn-on instant is not constrained to 0, so an additional degree of freedom is introduced. Instead of looking at the derivative of $v_{\mathrm{DS}}(\theta)$, we prefer to focus at the value of the parameter $i_{\mathrm{inv}}^{(0)}$, that is indeed proportional to it when ZVS is ensured. As already observed, $i_{\mathrm{inv}}^{(0)} = 0$ leads to ZVDS; otherwise it is $i_{\mathrm{inv}}^{(0)} < 0$.

As an example, let us consider for the sake of simplicity the case $k_I = 0.8$, $k_R = 0.8$, with $D = 50\%$, that allows an optimal solution already plotted in Figure 1.3b. It also allows a family of relaxed solutions associated to $-21.1 < i_{\mathrm{inv}}^{(0)} < 0$. To show how these relaxed solutions differ from the optimal one, we have plotted in Figure 1.7 the obtained values of the parameters q_I, q_R, and q_M as a function of $i_{\mathrm{inv}}^{(0)}$, along with the peak values of $v_{\mathrm{DS}}(\theta)$ and $v_{\mathrm{KA}}(\theta)$, and the root-mean-square (RMS) value of the $i_{\mathrm{inv}}(\theta)$ and $i_{\mathrm{rec}}(\theta)$.

The more we deviate from the ZVDS, i.e., the larger the value of $\left|i_{\mathrm{inv}}^{(0)}\right|$, the smaller the values of q_I, q_R, and q_M. This leads to a denormalized system with smaller inductance values and larger capacitor values, according both to (1.5) and (1.6). This is indeed a positive outcome: smaller inductors are always welcome, with a reduction in the size of the converter. Conversely, capacitors for which size is

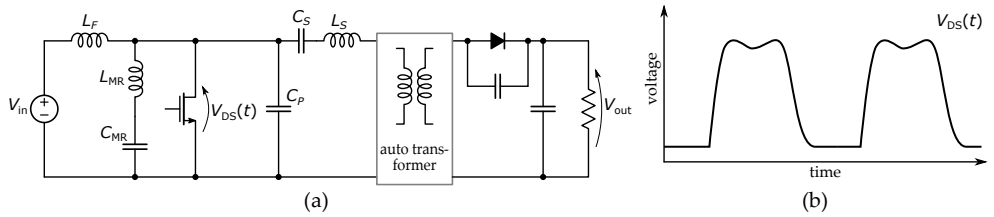


Fig. 1.8 The class-E boost converter based on the Φ_2 inverter. (a) Simplified schematic; (b) Desired shape for the $V_{\mathrm{DS}}(t)$ waveform.

typically not a problem, should be as large as possible to be able to mask the parasitic of the semiconductors.

Furthermore, deviating from the optimal solutions allows also an advantage (even if quite limited) in terms of reduction of the peak value of both $v_{\mathrm{DS}}(\theta)$ and $v_{\mathrm{KA}}(\theta)$. The topic will be discussed in Section 1.5.3.

However, the RMS values of the currents are increased. This topic will be deeply discussed further in Section 1.5.4, and leads to a reduction of the converter efficiency. According to this point of view, the optimal solution (under the assumption that the values of inductors and capacitors make the design feasible) has to be preferred.

As a final comment, allowing a sub-optimal solution expands the solution space with respect to what observed in Section 1.5.1. The orange area of the plots in Figure 1.6 includes all points (k_I, k_R) for which the solution of the design problem can only be found by relaxing the system of equations. Also, these datasets are included in [2], where the considered point is that ensuring the smallest value of $i_{\mathrm{inv}}^{(0)}$.

1.5.3 Device stress analysis

One of the main problems of resonant converters is the high peak level of both $V_{\mathrm{DS}}(t)$ and $V_{\mathrm{KA}}(t)$ voltages. Particular attention is given to the $V_{\mathrm{DS}}(t)$, which should be limited to avoid stress on the MOS switch that could cause a breakdown in the device. This voltage stress can, in fact, reach over four times the input voltage.

This problem has been considered many times in Literature. As an example, Rivas *et al.* proposed in [37] a boost class-E converter, whose schematic is very similar to the boost topology of Figure 1.5, but where the inverter is based on the Φ_2 topology [52, 55]. Basically, an additional *LC* resonator (in details, L_{MR} and C_{MR}) is added in parallel to the MOS, as depicted in Figure 1.8(a), in order to tune the $V_{\mathrm{DS}}(t)$

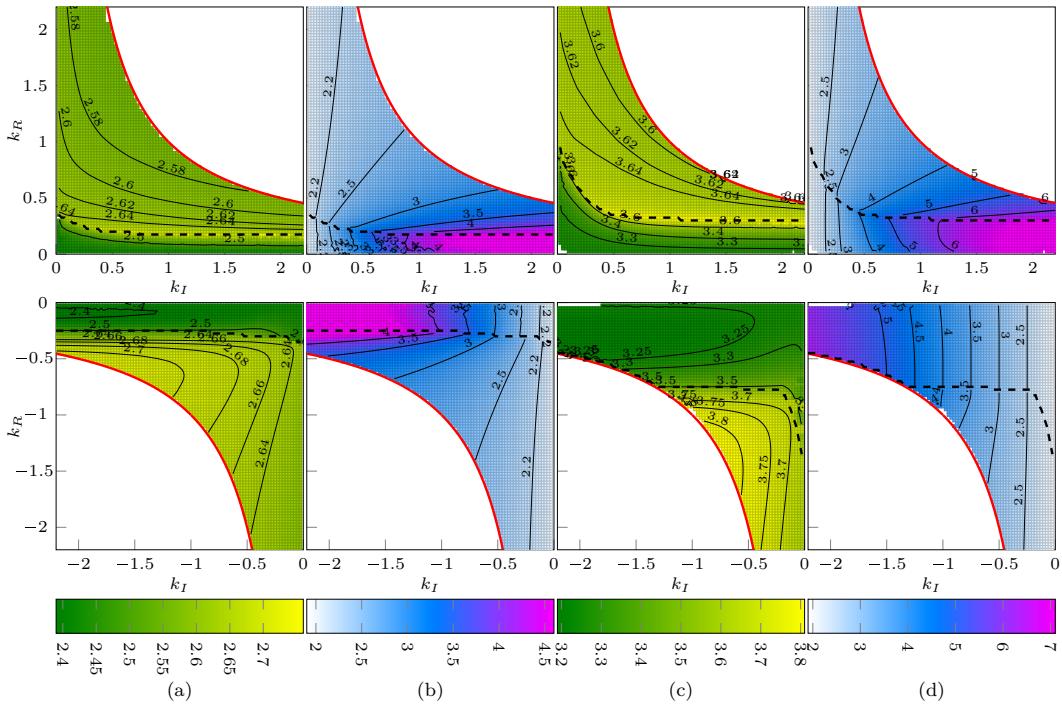


Fig. 1.9 Contour plots of the stress on the switching devices according to the design point for the normalized converter. The black dashed line indicates the separation of the optimal from the sub-optimal solutions, and the red solid lines the existence boundary condition $k_I k_R = 1$. (a) $\widehat{v}_{\mathrm{DS}}$, $D = 30\%$; (b) $\widehat{v}_{\mathrm{KA}}$, $D = 30\%$; (c) $\widehat{v}_{\mathrm{DS}}$, $D = 50\%$; (d) $\widehat{v}_{\mathrm{KA}}$, $D = 50\%$;

waveform on the third harmonic of the clock, and obtain a trapezoidal-like shape similar to that in Figure 1.8(b), with a reduced peak value. The converter proposed in [37] is operated at fixed switching frequency $f_s = 30\,\mathrm{MHz}$ and duty ratio $D = 30\%$, and the obtained peak drain-source voltage to input voltage ratio is ≈ 2.35.

Interestingly, the normalized proposed circuit allows one to estimate the peak drain-source voltage to input voltage ratio simply by looking, for almost all class-E topologies considered[3], at the peak value $\widehat{v}_{\mathrm{DS}}$ of $v_{\mathrm{DS}}(\theta)$. In a similar way, we can also look at the peak cathode-anode voltage to output voltage ratio simply by looking at the peak value $\widehat{v}_{\mathrm{KA}}$ of $v_{\mathrm{KA}}(\theta)$.

We have computed these two peak values for all points in the solution space (both optional and sub-optimal solutions have been considered). Results are shown in the contour plots of Figure 1.9.

[3] More precisely, to all topologies for which $V_{\mathrm{inv}} = V_{\mathrm{in}}$.

Interestingly, the $\widehat{v}_{\mathrm{KA}}$ has important variations across the solution space, and it can be lowered by using low values of $|k_I|$. Conversely, $\widehat{v}_{\mathrm{DS}}$ is almost constant, and apparently is mainly depending on D, and ranging from about 2.6 for $D = 30\%$, up to about 3.7 for $D = 50\%$. From a mathematical point of view, this is reasonable. Let us consider the schematic of Figure 1.2, and let us assume that lossy elements are negligible. The KVL at the inverter loop imposes $v_{\mathrm{DS}}(\theta) + v_{q_M}(\theta) + v_{k_I}(\theta) = 1$, where $v_{q_M}(\theta)$ and $v_{k_I}(\theta)$ are the voltages across the two inductances q_M and $q_M(1-k_I)/k_I$. By integrating over one full period, we have

$$\begin{aligned} \int_0^{2\pi} v_{\mathrm{DS}}(\theta)d\theta + \int_0^{2\pi} v_{q_M}(\theta)d\theta + \int_0^{2\pi} v_{k_I}(\theta)d\theta = \\ = \int_{\theta_D}^{2\pi} v_{\mathrm{DS}}(\theta)d\theta = 2\pi \end{aligned} \tag{1.9}$$

where the first integral term can be computed over a limited interval since $v_{\mathrm{DS}}(\theta) = 0$, $0 < \theta < \theta_D$, with $\theta_D = 2\pi D$, and where the second and third ones are zero assuming to be in the stationary condition. So, the integral of the $v_{\mathrm{DS}}(\theta)$ has a constant value, and the larger the integration interval $2\pi - \theta_D$, the smaller the expected $v_{\mathrm{DS}}(\theta)$ peak value. Since $v_{\mathrm{DS}}(\theta_D) = v_{\mathrm{DS}}(2\pi) = 0$ and assuming a half sine-wave shape, the first integral terms can be approximated as $2\widehat{v}_{\mathrm{DS}}(2\pi - \theta_D)/\pi$, that leads to $\widehat{v}_{\mathrm{DS}} = \pi^2/(2\pi - \theta_D) = \pi/2/(1-D)$. Observed values are very similar to those obtained with these very simple and approximated models.

According to the plots, the value of $\widehat{v}_{\mathrm{DS}}$ is slightly reduced for relaxed solutions, as already observed in Figure 1.7(b). Empirically, the peak value is also further reduced when introducing losses in the converter. This can be easily explained by considering that any lossy circuital elements in the inverter loop will add a positive contribution to the first term in (1.9), whereas the second term is constant.

In light of this, it appears that the best option when designing a resonant converter is to keep the value of D as low as possible to reduce the stress on the main switch. Furthermore, it also appears that the reduction in the peak drain-source voltage to the input voltage ratio observed in the Φ_2 converter in [37] is mainly due to the low value of D.

With a similar analysis, we can say that the value of $\widehat{v}_{\mathrm{KA}}$ can be reduced by reducing the duty cycle of the rectifying diode. According to the figure, this is obtained by setting low values of $|k_I|$.

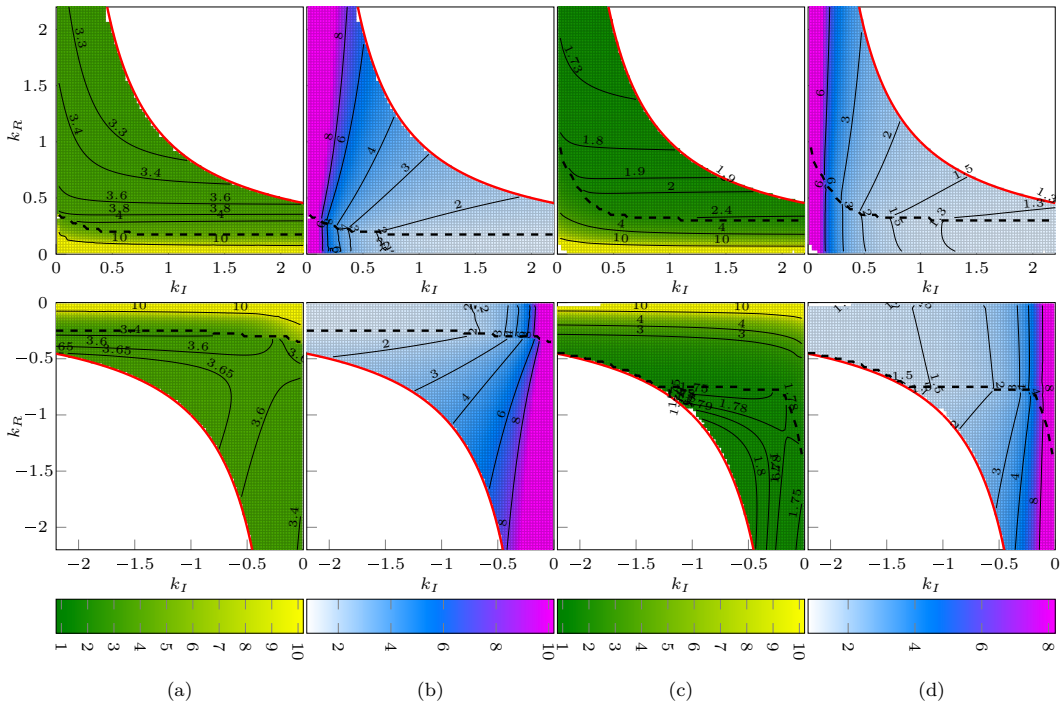


Fig. 1.10 Contour plots of the inverter and rectifier loops RMS currents according to the design point for the normalized converter. The black dashed line indicates the separation of the optimal from the sub-optimal solutions, and the red solid lines the existence boundary condition $k_I k_R = 1$. (a) i_{inv}^{RMS}, $D = 30\%$; (b) i_{rec}^{RMS}, $D = 30\%$; (c) i_{inv}^{RMS}, $D = 50\%$; (d) i_{rec}^{RMS}, $D = 50\%$;

1.5.4 Converter efficiency

In Section 1.4 we were able to express the converter efficiency η, for all considered topologies, as a function of $\langle i_{\text{inv}}(\theta)\rangle$. The aim of this section is to investigate if all points in the existence solution space are equivalent in terms of efficiency, or if some of them are instead capable to ensure a higher efficiency with respect to others.

Note that a comprehensive investigation relying on the computation of $\langle i_{\text{inv}}(\theta)\rangle$ would require the exact knowledge of all lossy parameters, and would be of no general validity; for this reason, we propose high-level consideration only using the behavior of the lossless converter as a proxy for that of any lossy converter.

When investigating the sources of loss on a real converter, we may note that switching losses on the MOS are already been limited by soft switching techniques. Furthermore the average power P_D dissipated on the rectifying diode, being $I_K(t)$

and $I_{C_{\text{rec}}}(t)$ the currents on the diode and on the C_{rec} with $I_{\text{rec}}(t) = I_K(t) + I_{C_{\text{rec}}}(t)$, can be approximated with

$$\begin{aligned} P_D \approx -\frac{1}{T_S}\int_0^{T_S} V_D^{\text{ON}} I_K(t)dt = -\frac{1}{T_S}\int_0^{T_S} V_D^{\text{ON}} I_{\text{rec}}(t)dt + \\ +\frac{1}{T_S}\int_0^{T_S} V_D^{\text{ON}} I_{C_{\text{rec}}}(t)dt = V_D^{\text{ON}}\langle -I_{\text{rec}}(t)\rangle \end{aligned} \tag{1.10}$$

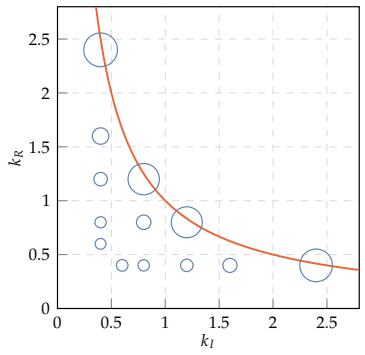
where the last equality holds due to stationary condition on the C_{rec}. In other terms, rectifying diode losses are dependent on the $\langle -I_{\text{rec}}(t)\rangle$ (i.e., according to Section 1.4, on the I_{out}), but do not depend on the converter operating point.

Conversely, all ohmic losses such as that due to the non-infinite quality factor of the reactive elements of the circuit or to the $R_{\text{DS}}^{\text{ON}}$, depend on the RMS value of the current flowing through the corresponding element. In this section we consider these kinds of losses, and we focus on the RMS values $I_{\text{inv}}^{\text{RMS}}$ and $I_{\text{rec}}^{\text{RMS}}$ of the inverter and rectifier loop currents only, assuming that these two currents can be considered a good proxy for all RMS current flowing into any circuit devices.

In detail, let us consider the ratios $I_{\text{inv}}^{\text{RMS}}/\langle I_{\text{inv(t)}}\rangle$ and $I_{\text{rec}}^{\text{RMS}}/\langle I_{\text{rec(t)}}\rangle$, equal to the normalized currents RMS values $i_{\text{inv}}^{\text{RMS}}$ and $i_{\text{rec}}^{\text{RMS}}$, respectively. These quantities are interesting since the average current values set the lower bound for losses, whereas actual losses are given by the RMS current values, that in a resonant converter can be much higher than the average value.

In the contour plots of Figure 1.10 we have shown how $i_{\text{inv}}^{\text{RMS}}$ and $i_{\text{rec}}^{\text{RMS}}$ depend on the values of k_I and k_R for the cases $D = 30\%$ and $D = 50\%$. Independently of D, for small values of $|k_R|$, the $i_{\text{inv}}^{\text{RMS}}$ quickly increases, also increasing the converter losses at the inverter side. Conversely, small values of $|k_I|$ generate solutions with a large $i_{\text{rec}}^{\text{RMS}}$, thus increasing losses at the rectifier side. In conclusion, in order to not increase ohmic losses, a designer should set a point where both k_I and k_R are not too small.

Note that the proposed analysis does not aim to be exhaustive, for many reasons. First, an exhaustive analysis would require the computation of the RMS current for all ohmic device considered, and the single computation of $i_{\text{inv}}^{\text{RMS}}$ and $i_{\text{rec}}^{\text{RMS}}$ has to be considered just a proxy. Then, the choice of the optimal values of $i_{\text{inv}}^{\text{RMS}}$ and $i_{\text{rec}}^{\text{RMS}}$ involves many tradeoffs. As an example, focusing on the losses of the inductors, changing the values of k_I and k_R will not result in a change of i_{inv}^{RMS} and $i_{\text{rec}}^{\text{RMS}}$ only,



(a)

Design point	σ_{q_I}	σ_{q_R}	σ_{q_M}	σ_{k_I}	σ_{k_R}
$k_I = 0.4,\ k_R = 2.4$	0.57%	1.65%	4.21%	44.08%	47.80%
$k_I = 0.8,\ k_R = 1.2$	0.67%	0.71%	3.05%	42.68%	37.70%
$k_I = 1.2,\ k_R = 0.8$	0.72%	0.36%	2.84%	39.34%	39.43%
$k_I = 2.4,\ k_R = 0.4$	0.82%	0.05%	2.61%	44.44%	44.20%
$k_I = 0.4,\ k_R = 1.6$	0.59%	1.22%	3.68%	8.88%	9.06%
$k_I = 0.8,\ k_R = 0.8$	0.77%	0.40%	2.92%	7.36%	6.61%
$k_I = 1.6,\ k_R = 0.4$	0.90%	0.03%	2.56%	7.13%	6.55%
$k_I = 0.4,\ k_R = 1.2$	0.62%	0.87%	3.53%	5.37%	5.52%
$k_I = 1.2,\ k_R = 0.4$	0.97%	0.14%	2.61%	5.64%	3.95%
$k_I = 0.4,\ k_R = 0.8$	0.75%	0.27%	2.77%	3.84%	3.24%
$k_I = 0.8,\ k_R = 0.4$	1.25%	0.48%	2.57%	4.58%	2.26%
$k_I = 0.4,\ k_R = 0.6$	1.05%	0.42%	2.59%	4.07%	1.95%
$k_I = 0.6,\ k_R = 0.4$	1.53%	1.10%	2.65%	5.44%	1.02%

(b)

Fig. 1.11 Robustness of the optimal solutions to parameters variation in the case $D = 50\%$, in-phase coupling ($k_I > 0$, $k_R > 0$), when parameters are perturbed with a $\pm 3\%$ error. Data refer to the observed variation of the output power. (a) Design points considered. The area of the circle representing each point is proportional to the average value of the observed statistical deviation of the output power, and the red solid line is the boundary existence condition $k_I k_R = 1$. (b) Statistical deviation observed when only one parameter is perturbed.

but also in the change of the value of the inductors, and so in their parasitic resistance. An example can be proposed by considering Figure 1.7. The more the converter is working far from the ZVDS condition, the higher $i_{\text{inv}}^{\text{RMS}}$ and $i_{\text{rec}}^{\text{RMS}}$, but also the lower the q_M, i.e., the smaller the inductances, and this effect should also be taken into account. Note however that losses increase linearly with the inductance size, but quadratically with the RMS currents, so that a working point with low RMS currents is typically preferable.

1.5.5 Robustness of the solution to parameter variation

In any effective implementation, we have to cope with an unavoidable tolerance of the values of capacitors and inductors, which is reflected in a variation of the dimensionless parameters from the desired value. As a result, the actual operating point is not the expected, optimal one. The aim of this section is to investigate if some points of the design space feature higher robustness to these variations.

As a first step, we observe how a variation in a circuit element may change the value of a dimensionless parameter. According to (1.5) and (1.6), a variation in the value of C_{inv}, C_{rec} and M implies a variation of the same relative amount in q_I, q_R

and q_M, respectively. Conversely, to estimate the effect of a variation in L_{inv} and L_{rec} it is simpler to look at (1.7). Under the reasonable assumptions that n_p/n_s is fixed, and that k shows very limited variations only, the relative deviation of k_I and k_R is always a fraction of the relative variation of L_{inv} and L_{rec}. In particular, by approximating the derivative of k_I and k_R by means of their finite difference, we can write

$$\left|\frac{\Delta k_I}{k_I}\right| \approx \left(1 - k_I \frac{1}{k}\frac{n_p}{n_s}\frac{V_{\text{rec}}}{V_{\text{inv}}}\right)\left|\frac{\Delta L_{\text{inv}}}{L_{\text{inv}}}\right| = \\ = \left(1 - \frac{k_I}{k_I^{(\text{lim})}}\right)\left|\frac{\Delta L_{\text{inv}}}{L_{\text{inv}}}\right|$$

$$\left|\frac{\Delta k_R}{k_R}\right| \approx \left(1 - k_R \frac{1}{k}\frac{n_s}{n_p}\frac{V_{\text{inv}}}{V_{\text{rec}}}\right)\left|\frac{\Delta L_{\text{rec}}}{L_{\text{rec}}}\right| = \\ = \left(1 - \frac{k_R}{k_R^{(\text{lim})}}\right)\left|\frac{\Delta L_{\text{rec}}}{L_{\text{rec}}}\right|$$

where $k_I^{(\text{lim})}$ and $k_R^{(\text{lim})}$ have been defined in (1.8), and are such that $0 \leq 1 - k_I/k_I^{(\text{lim})} \leq 1$ and $0 \leq 1 - k_R/k_R^{(\text{lim})} \leq 1$. In other words, the relative variations of k_I and k_R are always fractions of the variation of L_{inv} and L_{rec}.

Then, in Figure 1.11 we have considered a small subset of points associated to an optimal solution for the in-phase coupling case (i.e., $k_I > 0$, $k_R > 0$) with $D = 50\%$. We consider this particular case representative for any other cases with different coupling type or duty cycle, since all of them lead to very similar results. For each point, we have introduced a variation of one parameter among q_I, q_R, q_M, k_I, k_R uniformly distributed in the $\pm 3\%$ range with respect to its nominal value ensuring the optimal class-E condition. We have evaluated the perturbation of the system by measuring the variation of the output delivered power. In the table of Figure 1.11(b), with the term σ_{q_I} we indicate the standard deviation of the observed output power in a Montecarlo simulation of 100 runs when the perturbed parameter is q_I, and a similar notation is used when perturbing the other parameters. The considered points have also been highlighted in the k_I-k_R space plotted in Figure 1.11(a). The area of the circle indicating the position of each point is proportional to the average value of the standard deviation observed. We focus on the standard deviation only since variations in the average value of the delivered power, even if present, are much smaller.

Interestingly, the converter is quite robust to variations of q_I and q_R, but may be extremely sensitive to variations of k_I and k_R. The parameter q_M plays an intermediate

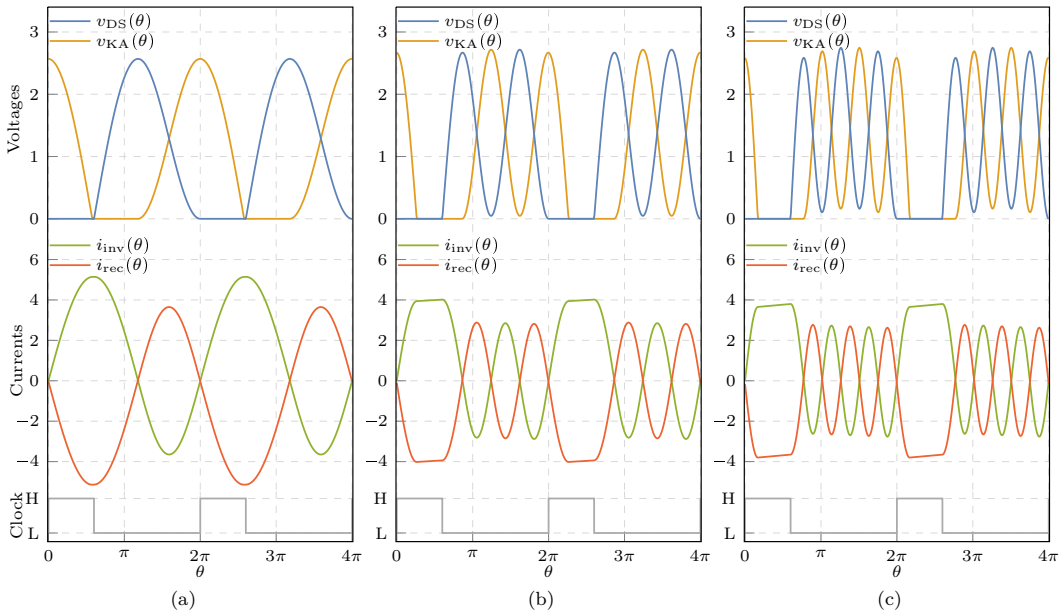


Fig. 1.12 Multiple solutions observed for $D = 30\%$, $k_I = 0.975$, $k_R = 0.975$ of the normalized lossless converter for $0 \leq \theta \leq 4\pi$. (a) first harmonic solution; (b) second harmonic solution; (c) third harmonic solution.

role. In particular, it is strongly suggested to set a working point that is as far as possible to the boundary existence condition $k_I k_R = 1$, plotted as a red line in Figure 1.11(a). In this area, in fact, even small variations of k_I and k_R may lead to a completely different converter behaviour. Even if, as observed above, the relative variations of k_I and k_R are always a fraction of the variations of L_{inv} and L_{rec}, the sensitivity to these parameters in this area may lead to unreliable implementations.

1.5.6 Uniqueness of the optimal solution

In the previous sections we have implicitly assumed that, even if the normalized system may present an infinite number of solutions to the relaxed design problem, it always has (if existing) a unique solution.

This assumption is actually not correct. The existence of multiple solutions has been observed in [56], where authors addressed additional solutions as *higher harmonic solutions* since currents and voltages waveforms present more than one oscillation in a clock period. The name reflects the common approach to tune an RF amplifier on the second or higher harmonic to increase its operating frequency.

According to [56], tuning the design of a converter on the second harmonic may lead to two advantages: *i*) the reduction of either the size of the magnetic elements or the clock frequency; and *ii*) a small but non-negligible increase in the converter efficiency. Therefore, this approach deserves investigation.

As an example, in Figure 1.12 we are able to plot many different solutions one can find for $D = 30\%$, $k_I = 0.975$, $k_R = 0.975$. The case of Figure 1.12(a) is the standard (first harmonic) solution, with $i_{\text{inv}}^{(0)} = 0$, $i_{\text{rec}}^{(0)} = -0.033$, $v_{\text{KA}}^{(0)} = 2.568$, $q_I = 0.429$, $q_R = 0.429$, $q_M = 11.256$. This solution is characterized by $\widehat{v}_{\text{DS}} \approx \widehat{v}_{\text{KA}} \approx 2.57$ and $i_{\text{inv}}^{\text{RMS}} \approx i_{\text{rec}}^{\text{RMS}} \approx 3.26$. The second harmonic solution has been plotted in Figure 1.12(b). This case is characterized by $i_{\text{inv}}^{(0)} = 0$, $i_{\text{rec}}^{(0)} = -0.095$, $v_{\text{KA}}^{(0)} = 2.668$, $q_I = 1.240$, $q_R = 1.240$, $q_M = 6.898$, and leads to $\widehat{v}_{\text{DS}} \approx \widehat{v}_{\text{KA}} \approx 2.71$ and $i_{\text{inv}}^{\text{RMS}} \approx i_{\text{rec}}^{\text{RMS}} \approx 2.65$. For this point it is also possible to find a third harmonic solution, that is depicted in Figure 1.12(c), obtained for $i_{\text{inv}}^{(0)} = 0$, $i_{\text{rec}}^{(0)} = -0.168$, $v_{\text{KA}}^{(0)} = 2.582$, $q_I = 1.954$, $q_R = 1.954$, $q_M = 4.585$. In this case, we have $\widehat{v}_{\text{DS}} \approx \widehat{v}_{\text{KA}} \approx 2.75$ and $i_{\text{inv}}^{\text{RMS}} \approx i_{\text{rec}}^{\text{RMS}} \approx 2.53$. All three solutions are characterized by the sequence $Z_3Z_4Z_1Z_2$.

The example confirms that higher harmonic solutions feature a smaller q_M, i.e., either a smaller magnetic size or a lower operating frequency, and lower RMS currents, with an expected higher efficiency. Conversely, we can observe an increase in the stress on the switch devices.

However, the exhaustive analysis of higher harmonic solutions is quite a complex topic. Despite the fact that the convergence of a standard solution is quite easy, finding a higher harmonic solution is not easy and requires some guidance of the design optimization algorithm. Many higher harmonic solutions are proposed in the datasets provided in [2], but it is not possible for us to show either a solution existence space as that of Figure 1.6, or a stress and efficiency analysis.

1.6 Design Example

In the previous section, thanks to the proposed normalization approach that reduces the degrees of freedom to k_I, k_R and D, we were able to propose the exhaustive analysis of many properties of class-E converters according to the selected design point. Here, we propose an example of how to take into account the developed guidelines in the design of a real converter. Note that, as already observed, the

focus of this chapter is on the theoretical model and on the possibilities given by the reduction of the design space dimension. Adherence of the analytical model both to low-level circuital simulations and to measurements from the prototype has been already extensively proven in [31] and in [34]. For this reason, we limit ourselves to provide the design of the converter.

Let us consider a 500 mW isolated dc-dc converter (i.e., according to one of the canonical schematic in Figure 1.1), with $V_{\text{in}} = 12\,\text{V}$ and $V_{\text{out}} = 5\,\text{V}$ (so $I_{\text{out}} = 100\,\text{mA}$) operating at the frequency $f_s = 5\,\text{MHz}$. Let us focus on possible solutions that allow optimal class-E condition with $L_{\text{inv}} = 0$. Let us also assume a non-ideal transformer with a coupling factor $k = 0.98$, and that all magnetics have a quality factor $Q_M = Q_{L_p} = Q_{L_s} = Q_{L_{\text{rec}}} = 100$ at the operating frequency $f_s = 5\,\text{MHz}$. Conversely, we assume ideal capacitors ($Q_{C_{\text{inv}}} = Q_{C_{\text{inv}}} \to \infty$) as it is known that ceramic capacitors with high-quality dielectric (such as C0G) have high a quality factor (typically, $Q > 1000$) with negligible series resistance. Diodes have been modeled with a voltage drop $V_d^{\text{ON}} = 0.7\,\text{V}$ and a series resistance $R_d^{\text{ON}} = 0.1\,\Omega$, and the MOS transistor reckons with its series resistance $R_{\text{DS}}^{\text{ON}} = 0.1\,\Omega$ when turned ON. The converter model is then completed with two additional resistors $R_{\text{in}} = R_{\text{out}} = 0.25\,\Omega$ to take into account other non-idealities, or simply to consider current sensing resistors.

As a first step, we may investigate possible candidate operating points assuming a lossless system employing an ideal transformer with turns ratio $n_p/n_s = 1$. With the above specs, for both coupling, we have $V_{\text{inv}} = 12\,\text{V}$, $V_{\text{rec}} = 5\,\text{V}$ and $\langle -I_{\text{inv}}(t) \rangle = 100\,\text{mA}$. Accordingly, equation (1.7) leads to $|k_I| = 2.4$ and $|k_R| \leq 0.41$.

The existence of the optimal solutions at the constrained k_I and for different duty cycle choice, as according to Figure 1.6, allows values of k_R approximately in the range $0.2 \leq k_R \leq 0.4$, $0.275 \leq k_R \leq 0.41$ and $0.325 \leq k_R \leq 0.41$ for the in-phase coupling at $D = 30\%$, $D = 40\%$, $D = 50\%$, respectively, and $-0.41 \leq k_R \leq -0.275$ for the 180° out-of-phase coupling with $D = 30\%$. No solutions exist for $D = 40\%$ and $D = 50\%$ with 180° out-of-phase coupling.

Among all these possibilities, we limit ourselves to $D = 30\%$. The reason is twofold. Fist, a lower value of D leads to a larger k_R range, with additional optimization possibilities. Then, this value of D allows a reduction of the stress across the main switch.

Then, k_R may be selected by taking into account its effects on the other design parameters. In the in-phase coupling, with k_I from 0.175 to 0.41, the parameter q_I

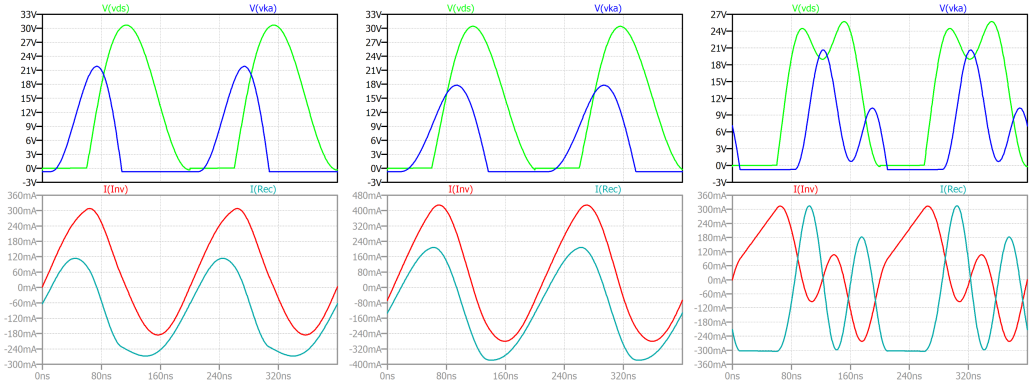


Fig. 1.13 Spice simulation results for the three design examples proposed in Section 1.6. (a) Optimal design (ZVS + ZVDS) based on the 180° out-of-phase coupling; (b) sub-optimal design (ZVS only) based on the 180° out-of-phase coupling, with a 25% reduction in the magnetic size; (c) optimal design (ZVS + ZVDS) based on the in-phase coupling and a second-harmonic solution.

ranges from 0.28 to 0.35, q_R from 4.11 down to 2.12, q_M from 1.62 up to infinity at the existence boundary condition. In the 180° out-of-phase coupling, with k_I from -0.41 to -0.25, the parameter q_I ranges from 0.40 to 0.44, q_R from 2.63 to 9.27, q_M grows from minus infinity at the existence boundary condition up to -2.49. According to these values, q_I (whose value sets C_{inv}) has only minor variations, whereas q_R (whose value sets C_{rec}) has larger variations, but we may assume that no value in the range gives rise to any problem. Conversely, q_M parameter is critical due to its very large variation, and a solution far from the existence boundary condition $k_I k_R = 1$ (where the value of q_M is actually slowly changing) is required in order to minimize inductance values. A solution far from the existence boundary condition also ensures higher robustness to parameter variations in an actual implementation.

However, the exact value of k_R has to be set according to other trade-offs. For example, across the k_R interval, as observed in Section 1.5, values of $\widehat{v}_{\text{DS}}$ and $\widehat{v}_{\text{KA}}$ have opposite trends. The same is observed for $i_{\text{inv}}^{\text{RMS}}$ and $i_{\text{rec}}^{\text{RMS}}$.

The solution we propose is to look at the $\langle i_{\text{inv}}(\theta)\rangle$, that is inversely proportional to the converter efficiency and can be computed since the converter specs are given, leading to $|k_I| = 2.352$, $v_d^{\text{ON}} = 0.14$, $Q_I = Q_R = 100$, $g_{\text{DS}}^{\text{ON}} = 2880$, $g_d^{\text{ON}} = 500$, $g_{\text{inv}} = 1152$, $g_{\text{cm}} \to \infty$, $g_{\text{rec}} = 200$. When considering the lossy parameters, the solution space is slightly enlarged for all considered cases. For the in-phase coupling, it is $0.15 \leq k_R \leq 0.42$, and the minimum observed average inverter current is $\langle i_{\text{inv}}(\theta)\rangle =$

1.267 for $k_R = 0.25$. For the 180° out-of-phase coupling, the solution space is enlarged to $-0.42 \leq k_R \leq -0.2$, and the average inverter current is minimized for $k_R = -0.2$, with $\langle i_{\text{inv}}(\theta)\rangle = 1.304$.

Another possibility is to configure the transformer with a turns ratio $n_p/n_s = 2$. This gives rise to $|k_I| = 1.2$ for the associated ideal system, and $|k_I| = 1.176$ when considered the non-ideal transformer, and allows a much broader range of solutions for any value of D. With the same considerations as in the previous case, we limit to $D = 30\%$ and to the lossy system, we have solutions for $0.175 \leq k_R \leq 0.85$ for the in-phase coupling, with the optimum point at $k_R = 0.25$ with $\langle i_{\text{inv}}(\theta)\rangle = 1.262$, and $-0.88 \leq k_R \leq -0.22$ for the 180° out-of-phase coupling, with the optimum point at $k_R = -0.22$ with $\langle i_{\text{inv}}(\theta)\rangle = 1.256$. The latter represents the point with the maximum efficiency, with $\eta = 79.6\%$, $\widehat{v}_{\text{DS}} = 2.53$, $\widehat{v}_{\text{KA}} = 4.33$. This solution is given by $q_I = 0.338$, $q_R = 3.102$, $q_M = -0.396$ and it is denormalized to

$$L_p = 3.08\,\mu\text{H}\ (L_s = 771\,\text{nH})\,,\ L_{\text{rec}} = 2.09\,\mu\text{H},$$
$$C_{\text{inv}} = 327\,\text{pF},\ C_{\text{rec}} = 205\,\text{pF}$$

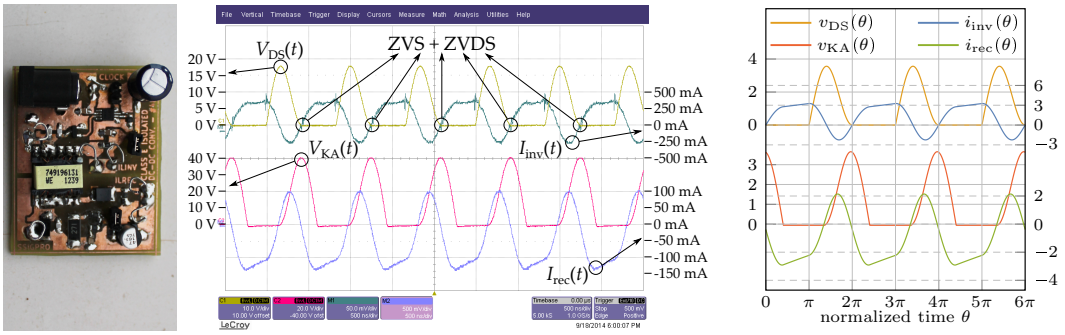
that gives rise to a converter whose spice simulation is depicted in Figure 1.13(a).

Assuming that magnetic values of this solution are too large for an actual implementation, it is possible to relax the requirements in terms of soft switching and look for a sub-optimal solution. By considering the previous design, and imposing a derivative of $V_{\text{DS}}(t)$ at the MOS turn-on time such that $i_{\text{rec}}^{(0)} = -1.6$, we have a solution given by $q_I = 0.338$, $q_R = 3.102$, $q_M = -0.396$, that leads to

$$L_p = 2.35\,\mu\text{H}\ (L_s = 588\,\text{nH})\,,\ L_{\text{rec}} = 1.59\,\mu\text{H},$$
$$C_{\text{inv}} = 537\,\text{pF},\ C_{\text{rec}} = 536\,\text{pF}$$

with $\langle i_{\text{inv}}(\theta)\rangle = 1.298$, $\widehat{v}_{\text{DS}} = 2.51$, $\widehat{v}_{\text{KA}} = 3.54$. Magnetics are reduced in size by 25%, but the efficiency is decreased to $\eta = 77\%$. The spice simulation of this converter is depicted in Figure 1.13(b).

Another possibility is to investigate the existence of higher harmonics solutions. Interestingly, considering the lossy system with $D = 30\%$ and $n_p/n_S = 2$, i.e., $|k_I| = 1.176$, we have a second-harmonic optimal solution for $0.425 \leq k_R \leq 0.85$ (in-phase coupling only). An interesting point is given by $k_R = 0.6$ ($q_I = 0.633$, $q_R = 1.54$, $q_M = 0.708$), characterized by $\langle i_{\text{inv}}(\theta)\rangle = 1.215$, $\widehat{v}_{\text{DS}} = 2.38$, $\widehat{v}_{\text{KA}} = 3.56$, that is



(a) (b) (c)

Fig. 1.14 Class-E converter prototype proposed in [31]. (a) Prototype photograph. (b) Measurements from the prototype showing $V_{DS}(t)$ (top, left axis), $V_{KA}(t)$ (bottom, left axis), $I_{inv}(t)$ (top, right axis), $I_{rec}(t)$ (bottom, right axis). (c) Normalized waveforms obtained from the analytical model proposed in this chapter, scaled to approximately match the resolution of the measurement plot. Voltages $v_{DS}(\theta)$ and $v_{KA}(\theta)$ are referred to the left axis, currents $i_{inv}(\theta)$ and $i_{rec}(\theta)$ to the right one.

more convenient than previously considered solutions both in terms of efficiency ($\eta = 82.3\%$) and peak voltage stress. This solution leads to

$$L_p = 2.77\,\mu\text{H}\ \ (L_s = 693\,\text{nH})\,,\ L_{\text{rec}} = 439\,\text{nH},$$
$$C_{\text{inv}} = 300\,\text{pF},\ C_{\text{rec}} = 357\,\text{pF}$$

The spice simulation of this converter is depicted in Figure 1.13(c).

1.7 Comparison

In [31], a 5 V-to-12 V, 1.25 MHz, $D = 50\%$, 500 mW class-E prototype based on the in-phase coupling schematic of Figure 1.1(a) has been presented. The prototype, whose photograph is proposed in Figure 1.14(a), features a very good adherence between theoretically expected waveforms and actual measurements. In this section we show that, by using the procedure proposed here, the design of the prototype is much easier than what proposed in [31], and leads to the same result. Furthermore, other converter features such as stress devices can be well predicted in advance.

The class-E dc-dc converter in [31] relies on a WE-FLEX commercial transformer by Würth Elektronik, in $n_p/n_s = 1/2$ configuration, with coupling coefficient $k \approx 0.98$, $L_p = 10.9\,\mu\text{H}$ (so, $L_s = 43.6\,\mu\text{H}$ and $M \approx 21.4\,\mu\text{H}$) and quality factor $Q_{L_p} =$

$Q_M = Q_{L_s} \approx 45$. Furthermore, $L_{\text{inv}} = 0$ and $L_{\text{rec}} = 33\,\mu\text{H}$, with $Q_{L_{\text{rec}}} \approx 47$. According to the procedure in [31], the design is achieved by considering an equivalent 5 V-to-6 V, where all the elements at the secondary side are referred to the primary side. So, the equivalent voltage conversion ratio is $\mu = 1.2$, and the equivalent rectifier inductance is 8.25 µH. Once the design is achieved, all the equivalent elements at the primary side are referred back to the secondary.

Indeed, with the new approach, one can use (1.5) to immediately compute $k_I \approx 0.817$ and $k_R \approx 0.670$. This is enough to allow us to extrapolate many results from the ideal lossless model: *i*) according to Figure 1.6, the optimum class-E condition can be ensured using these magnetics; *ii*) the $1/2$ choice of the transformer ratio is good, since it leads to a solution point that is quite distant from the existing boundary condition $k_I k_R = 1$; *iii*) since $D = 50\%$, we expect (see Figure 1.9) a quite high peak voltage, in particular for the inverter circuit, with $\widehat{v}_{\text{DS}} \approx 3.63$ (i.e., $\widehat{V}_{\text{DS}} \approx 18.2\,\text{V}$) and $\widehat{v}_{\text{KA}} \approx 3.82$ (i.e., $\widehat{V}_{\text{KA}} \approx 45.8\,\text{V}$). Furthermore (from Figure 1.10) we expect $i_{\text{inv}}^{\text{RMS}} \approx 1.9$ and $i_{\text{rec}}^{\text{RMS}} \approx 1.8$.

Then, referring to [31] for the complete modeling of the circuit elements, we consider C_{inv} and C_{rec} ideal, we ignore the bulk diode parameters since it is never turned on, and we compute the other lossy parameters as $v_d^{\text{ON}} \approx 0.058$, $Q_I \approx 45$, $Q_R \approx 47.6$, $g_{\text{inv}} \approx 500$, $g_{\text{DS}}^{\text{ON}} \approx 1850$, $g_{\text{cm}} \to \infty$, $g_d^{\text{ON}} \approx 96$ and $g_{\text{rec}} \approx 56$. The optimal class-E design problem solution is $q_I = 1.305$, $q_R = 1.337$ and $q_M = 1.391$, that given $f_s = 1.25\,\text{MHz}$ leads to

$$L_p = 10.8\,\mu\text{H}\ \left(L_s = 43.3\,\mu\text{H}\right),\ L_{\text{rec}} = 32.8\,\mu\text{H},$$
$$C_{\text{inv}} = 1.95\,\text{nF},\ C_{\text{rec}} = 330\,\text{pF}$$

that is exactly the design proposed in [31]. The measurements from the prototype are shown in Figure 1.14(b), and can be compared with the waveforms expected from the theoretical model, depicted in Figure 1.14(c). From the measurement, we get $\widehat{V}_{\text{DS}} \approx 17.8\,\text{V}$ and $\widehat{V}_{\text{KA}} \approx 40.6\,\text{V}$, quite similar to the predicted values. Furthermore, $I_{\text{inv}}^{\text{RMS}} / \langle I_{\text{inv}}(t) \rangle \approx 2.0$ and $I_{\text{rec}}^{\text{RMS}} / \langle I_{\text{rec}}(t) \rangle \approx 2.2$. All these values have been well predicted just by using the lossless system as a proxy, and can even better approximated when considering the lossy model of the converter, with $\widehat{v}_{\text{DS}} \approx 3.56$, $\widehat{v}_{\text{KA}} \approx 3.63$ (i.e., $\widehat{V}_{\text{DS}} \approx 17.8\,\text{V}$ and $\widehat{V}_{\text{KA}} \approx 43.5\,\text{V}$), $i_{\text{inv}}^{\text{RMS}} \approx 2.3$ and $i_{\text{rec}}^{\text{RMS}} \approx 2.1$. The theoretically computed efficiency is $\eta = 1/\langle i_{\text{inv}}(\theta) \rangle = 77\%$, and approximates quite well the measured one (75%).

Table A.1 Possible different configurations of the circuit of Figure 1.2 according to the state of the MOS and the diodes.

Config.	MOS and diodes state	state variables	constrained variables
Z_1	$m^{\mathrm{ON}}=0,\ b^{\mathrm{ON}}=0,\ d^{\mathrm{ON}}=1$	$i_{\mathrm{inv}}(\theta),\ i_{\mathrm{rec}}(\theta),\ v_{\mathrm{DS}}(\theta)$	$v_{\mathrm{KA}}(\theta)=-v_b^{\mathrm{ON}}$
Z_2	$m^{\mathrm{ON}}=0,\ b^{\mathrm{ON}}=0,\ d^{\mathrm{ON}}=0$	$i_{\mathrm{inv}}(\theta),\ i_{\mathrm{rec}}(\theta),\ v_{\mathrm{DS}}(\theta),\ v_{\mathrm{KA}}(\theta)$	–
Z_3	$m^{\mathrm{ON}}=1,\ b^{\mathrm{ON}}=0,\ d^{\mathrm{ON}}=0$	$i_{\mathrm{inv}}(\theta),\ i_{\mathrm{rec}}(\theta),\ v_{\mathrm{KA}}(\theta)$	$v_{\mathrm{DS}}(\theta)=0$
Z_{3a}	$m^{\mathrm{ON}}=0,\ b^{\mathrm{ON}}=1,\ d^{\mathrm{ON}}=0$	$i_{\mathrm{inv}}(\theta),\ i_{\mathrm{rec}}(\theta),\ v_{\mathrm{KA}}(\theta)$	$v_{\mathrm{DS}}(\theta)=-v_b^{\mathrm{ON}}$
Z_4	$m^{\mathrm{ON}}=1,\ b^{\mathrm{ON}}=0,\ d^{\mathrm{ON}}=1$	$i_{\mathrm{inv}}(\theta),\ i_{\mathrm{rec}}(\theta)$	$v_{\mathrm{DS}}=0,\ v_{\mathrm{KA}}(\theta)=-v_d^{\mathrm{ON}}$
Z_{4a}	$m^{\mathrm{ON}}=0,\ b^{\mathrm{ON}}=1,\ d^{\mathrm{ON}}=1$	$i_{\mathrm{inv}}(\theta),\ i_{\mathrm{rec}}(\theta)$	$v_{\mathrm{DS}}=-v_b^{\mathrm{ON}},\ v_{\mathrm{KA}}(\theta)=-v_d^{\mathrm{ON}}$

1.8 Conclusion

In this chapter, we have considered an analytical approach for the design of Class-E dc-dc converters recently appeared in the literature and improved it mainly by observing that the design space dimension, neglecting the clock duty-cycle ratio, is only two and not three as assumed in previous works. The most important consequence is that this reduction allows us an exhaustive analysis of all the design space, with the possibility to investigate the optimal design according to the design requirements. For the sake of clarity, an example of a possible optimization is then provided.

Chapter 2

A Zero Transient Dual Frequency Control in Class-E DC-DC Converters

2.1 Introduction

Resonant DC-DC converters have been introduced to allow operations at high switching frequencies with many advantages in terms of power density [14–16], EMI [16, 17, 57] and dynamic performances [58, 59]. They usually take advantage of techniques commonly used in Radio-Frequency power amplifiers [9, 10, 18, 60] to reduce switching losses and overcome the drawback of hard-switching converters [61, 62], where losses increase with the operating frequency. As such, resonant converters are capable of operating in the frequency range from a few MHz to hundreds of MHz.

In this chapter, we focus on *class-E* resonant converters that feature the well-known soft-switching technique, in opposition to the hard-switching one that characterizes the *class-D* family [1] [10, 13, 63]. More specifically, we refer to Zero-Voltage Switching (ZVS) if the reactive components, used in the converter, reshape the voltage across a switch –either a controlled (e.g., a power MOS) or non-controlled one (e.g., a rectifying diode)– in a way that it slowly goes to zero before turn-on, and gradually moves from zero after turn-off. Additionally, we refer to Zero-Voltage-Derivative Switching (ZVDS) if the zero voltage level is approached with zero time derivative, too. If both ZVS and ZVDS are satisfied, the class-E converter is said to

operate under *optimum* condition. If only ZVS is satisfied, the class-E converter is said to operate under *sub-optimum* condition.

The critical aspect of all resonant topologies, including the class-E one, is that the optimum or sub-optimum behavior can be ensured for a given operating point only (e.g., the one that guarantees the nominal output power). As a consequence, in order to cope with different output power levels, several control methodologies have been presented so far in the literature [64–73].

In this chapter, the aim is to significantly progress in this direction by introducing an optimized dual-frequency control method. The core idea is to allow the converter to alternatively operate between a high-power and a low-power state so that the average output power can be regulated by changing the relative duration of the two states. Two important advantages characterize this approach when compared to existing methods: *i*) the optimal ZVS-ZVDS conditions are *preserved* in both operating states, thus maximizing converter efficiency; and *ii*) the transient response, i.e., the time required for switching between the two states, can be reduced to zero, allowing to increase the control frequency to a value of almost the same order of magnitude as the main switching frequency. This is fundamental to reduce the additional output ripple introduced by the control strategy to a negligible level. Our approach relies its theoretical background on the exact class-E design approach proposed in [1].

This chapter is organized as follows. In Section 2.2 we present an overview of the state of the art of class-E control methodologies. In Section 2.3 we show the basic principle and the optimization of the proposed technique. In Section 2.4, measurements results from a suitably implemented prototype are presented. Finally, we draw the conclusion.

2.2 State of the art in class-E output power regulation

Control methodologies that ensure the correct output power even when the load is variable or when the input voltage is not precisely known are desirable but they typically violate ZVS and/or ZVDS. The most common control techniques adopted in the regulation of resonant DC-DC converters are: Pulse Frequency Modulation (PFM), Pulse Width Modulation (PWM), and ON-OFF control.

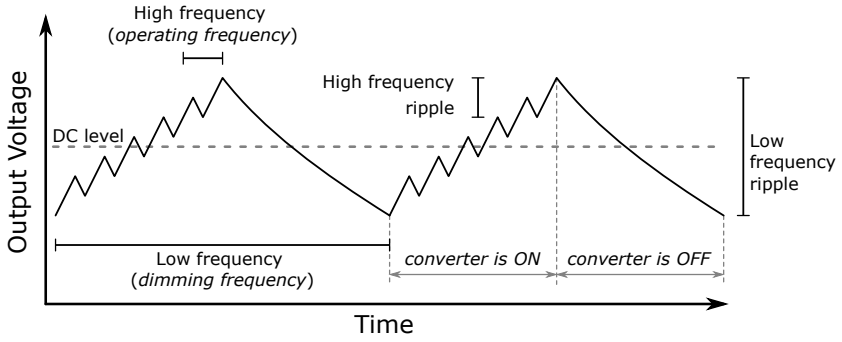


Fig. 2.1 High-frequency and low-frequency components in the output voltage ripple of an ON-OFF controlled converter.

PFM output power regulation basically relies on the variation of the converter switching frequency according to the desired output power. The side effect is the loss of soft-switching properties, achievable at the resonant frequency only. As an example, in [13] a class-E converter in which the optimum behavior is achieved at the maximum output power only is designed. At a lighter load, the converter is regulated by increasing the switching frequency, but the system is not able to maintain the optimum class-E condition anymore. Most recently, in [66] an asymmetric pulse frequency modulation is proposed, characterized by constant on time for series resonant converter in high-voltage and high-power applications.

In PWM control, the converter operates at constant switching frequency while the pulse width of the waveform, which controls the turn-on and turn-off of the power switch, is suitably modified. The main issue is that soft switching can be maintained at the nominal duty cycle only since, by varying the pulse width, the instant at which the power switch turns on may not be equivalent to the instant at which the voltage across it vanishes. In [67], a PWM controller is used together with a look-up table for a DC-DC class-E buck-boost converter in which the pulse width changes according to the load. In [68], an FPGA-based dynamic duty cycle controller is built to modulate the duty cycle and the frequency of the gate driving signal, so that ZVS and ZVDS are always achieved for a different level of input voltage while the output voltage is regulated via ON-OFF control.

The ON-OFF control has proven to be one of the most popular techniques in the MHz-range applications [69, 71–73]. Its basic principle is a low-frequency *dimming* of the output power: the converter is turned on and off at the frequency f_d. When the

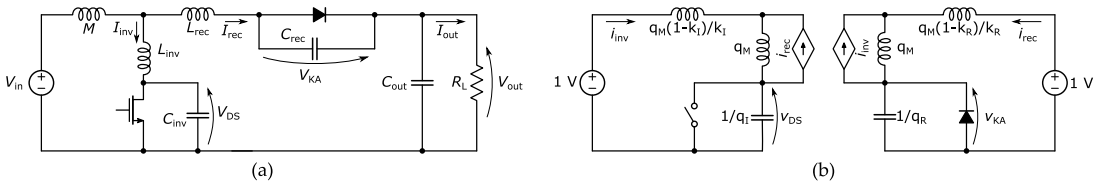


Fig. 2.2 (a) Basic schematic of the standard class-E boost converter considered in this chapter. (b) Schematic of the normalized $1\,\mathrm{V}-1\,\mathrm{V}$, $1\,\mathrm{W}$ $1\,\mathrm{rad/s}$ equivalent class-E converter considered in [1] for the design of the converter in Figure 2.2(a).

converter is on, it is working at the nominal average power P_{nom}, whereas when off, the power decreases to zero. Indicating with D the dimming ratio (i.e., the fraction of the period in which the converter is on, with $0 \leq D \leq 1$), and assuming an output low-pass filter that delivers to the load the *average* power generated by the converter only, we get

$$P_{\mathrm{out}} = P_{\mathrm{nom}} \cdot D. \tag{2.2.1}$$

A detailed analysis of a 20 MHz class-E DC-DC converter with ON-OFF control over a wide input voltage range is provided in [70]. Similarly, the design and control of a 10 MHz class-E DC-DC converter employing the ON-OFF control technique are reported in [73], where the possibility to reduce the voltage stress across the main switch at lighter load is analyzed.

However, one of the major problems of the ON-OFF control is the very long transient time characterizing the start-up/shut-down of each ON-OFF cycle [69], which sets an upper bound on the dimming frequency f_d.

The consequence is an increase in the output voltage ripple, as sketched in Figure 2.1. When the converter is off, the load is powered by drawing energy from the output filter. By reducing the energy accumulated in the filter, the output voltage reduces, and an additional (low frequency) ripple superimposed to the standard (high-frequency) ripple of the converter is observed. Typically, the low-frequency ripple is the dominant one.

A simple analysis, assuming the output voltage almost constant, the high-frequency ripple negligible with respect to the low-frequency one, and a capacitance

C_{out} as output filter, easily leads to estimate the output ripple as

$$\Delta V = \frac{P_{\text{nom}}}{V_{\text{out}}} \frac{1}{f_d C_{\text{out}}} D(1-D). \tag{2.2.2}$$

A direct consequence of the above result is that f_d must be set to the largest possible value to either reduce ΔV given C_{out}, or reduce C_{out} given ΔV.

Furthermore, the existence of long turn-on and turn-off transients in which there is no sufficient time for the converter to reach its steady-state condition, and thus ZVS-ZVDS cannot be ensured, leads to significant energy losses at each ON-OFF cycle. This affects the overall power converter efficiency, especially at higher f_d values. In other words, contrarily to (2.2.2), which suggests that a sufficiently high dimming frequency should be used to reduce ΔV, the efficiency constraint sets a competing constraint in terms of an upper bound for it.

Note that ensuring a sufficiently large f_d will also have beneficial effects in terms of ElectroMagnetic Interference (EMI) reduction. Even if an exact and rigorous analysis is out of the scope of this chapter, we can say that, in converters of this class, the most important contribution to EMI is the conducted emission generated by the converter input current propagating through the power-supply wires. The expected spectrum includes components at f_d and its harmonics, at the main switching frequency and its harmonics, and at all the intermodulation frequencies. It yields that by increasing f_d, the low-frequency components are moved higher in the interference spectrum, making it easier for an input EMI filter to attenuate them.

The frequency issue can be further highlighted by considering some of the results recently presented in the literature when a resonant converter enjoys ON-OFF control. As two noteworthy examples, in [70], measurements on a prototype working at the operating frequency of 20 MHz show a dimming frequency which is about $1000\times$ smaller, i.e. $f_d = 30\,\text{kHz}$ with $D = 50\%$. In [73], the authors use a variable f_d. In the provided example, with $D = 17\%$, one can estimate from measurements a value of $f_d \approx 150\,\text{kHz}$, which is almost $100\times$ smaller than the operating frequency.

In settings similar to the ones above, the low-frequency ripple dominates. This is the reason why many works can be found in the literature trying to solve the transient time issue. Some solutions use a second-order harmonic filter [52] or reduce the input inductance value [39]. However, due to the difficulties in achieving ZVS during both start-up and shut-down transient response, extra snubbing elements, as

the ones generally adopted to mitigate the effects of the hard switching, are used to ensure soft-switching at every cycle. As an example along this line, in [69] an additional Zero Voltage Transient (ZVT) cell is proposed to be added to the converter to speed up the turn-off time. The paper shows measurement results from a 3 MHz quasi-resonant boost converter with the additional ZVT cell, which uses an ON-OFF control at $f_d = 300\,\text{kHz}$. Furthermore, in [71] an extra control is added to the latter boost converter to manage the first switching period of each power pulse, in order to reduce the transient power losses of the ON-OFF control.

More recent works replace the ON-OFF control with a *dual-frequency control*, in which the converter is not switched between an ON- and an OFF-state, but between a higher power $P_{\text{nom}}^{(1)}$- and a lower power $P_{\text{nom}}^{(2)}$-state, typically by modifying the main clock signal. Indicating, as in the standard ON-OFF case, with f_d the dimming frequency and with D the dimming ratio, defined as the ratio of time in which the converter operates at $P_{\text{nom}}^{(1)}$, (2.2.1) is replaced by

$$P_{\text{out}} = P_{\text{nom}}^{(1)} \cdot D + P_{\text{nom}}^{(2)} \cdot (1 - D) \tag{2.2.3}$$

and a condition similar to (2.2.2) holds for the ripple. The advantage of this solution is that, since the converter is never turned off, transient times are substantially reduced. Yet, the additional problem of ensuring optimal or suboptimal condition is still present and must be addressed to prevent unacceptable drops in the efficiency.

As an example, the authors of [72] implement a class-E DC-DC converter designed to operate at multiple switching frequencies (more precisely, at the two frequencies $f_s^{(1)} = 20.5\,\text{MHz}$ and $f_s^{(2)} = 22.5\,\text{MHz}$) in order to deal with multiple input power levels. In the provided example, the dimming frequency is set to $f_d = 17.9\,\text{kHz}$ with $D \simeq 0.7$ (estimated from the figure in the paper). Therefore, f_d results to be about $1200\times$ smaller than $f_s^{(2)}$. The main issue is that the converter topology remains unchanged when switching from $f_s^{(1)}$ to $f_s^{(2)}$, which results in the converter being able to operate only at suboptimal condition and just in the neighborhood of the designed working frequency of $f_s = 20\,\text{MHz}$.

From the above considerations and examples, one can readily conclude that the issues that arise from the ON-OFF control, are only partially solved in the classic dual-frequency designs. The main reason for this is that the achieved transient time, which has indeed been considerably reduced, has still an appreciable negative effect

on the converter efficiency drop so further improvements are needed in this respect. Additionally, the proposed state-of-the-art dual-frequency techniques either introduce extra control elements, as in [70], or they are not able to ensure soft-switching during frequency transition, as in [72].

In this work, a dual-frequency control method, simply based on the modification of the value of two capacitances, is applied to a resonant class-E converter. The method is *capable of mitigating both problems* of the standard dual-frequency approach. More precisely, we will show that for the proposed solution:

- the circuit operates under *optimum soft-switching condition* in both high- and low-power states;
- it is possible to optimize the converter and *achieve a zero transient time* when switching from one state to the other.

Despite the apparent similarity, the proposed control technique must not be confused with works such as [74–76], in which the circuit is dynamically tuned to achieve impedance matching in order to compensate for environmental effects or component tolerances that may alter the desired operating point (and in particular the resonant frequency). As a matter of fact, the key idea of this work is to intentionally (and dynamically) change the converter operating point to allow a dimming between two frequencies in order to modulate the output power and overcome the ON-OFF control issues.

2.3 Theoretical Analysis

The basic schematic of the converter topology considered in this work is shown in Figure 2.2(a). This topology is known as the *boost* class-E converter [1] [13, 16, 19, 77, 34, 78], since it ensures $V_{\text{out}} > V_{\text{in}}$, and includes five resonant elements, i.e., according to the naming system of the figure, the inductances L_{inv}, L_{rec} and M, and the capacitances C_{inv} and C_{rec}. Capacitance C_{out}, instead, is simply used as output filter capacitance. For the sake of simplicity, a resistive load R_L is considered.

2.3.1 Single-Frequency Class-E Converter Design

The converter design relies on the results reported in [1]. Instead of considering the standard sinusoidal approach, this work bases the design of the converter on the exact and semi-analytical design methodology first proposed in [31], introducing a few improvements and analyzing many trade-offs. The analysis is limited to the scheme of Figure 2.2(b), which is however shown to be equivalent to many class-E converter topologies, including the one in Figure 2.2(a). In the proposed analysis, the five resonant elements are replaced by expressions of the corresponding five dimensionless parameters k_I, k_R, q_M, q_I, and q_R. The procedure is however very complex and, even if based on exact and analytic equations, requires many numerically computed constants. For this reason, it is not possible to report here simple equations capable of computing the optimal values of the parameters. Indeed, [1] provides tools for the easy computation of them.

The main advantages of the approach proposed in [1][31], with respect to the many others proposed so far, can be summarized as follows:

i) the main sources of losses for all active and passive devices can be taken into account;

ii) a normalized converter, i.e., a 1 W, 1 V-to-1 V converter, whose main switch is operating at 1 rad/s with any desired duty cycle. The converter parameters are then de-normalized to fit the desired input/output voltage combination, operating frequency, and output power;

iii) in the most general case, two among the five dimensionless parameters are degrees of freedom. In all examples provided in [1], k_I and k_R are selected by the designer, whereas q_M, q_I and q_R are computed accordingly to ensure the optimal class-E condition.

The point i) above is of paramount importance to ensure adherence between the design model and the real converter behavior. As such, we will always implicitly consider lossy models in our converter design; yet, to keep the discussion as simple as possible, we will not consider lossy terms in the rest of this section. The interested reader is referred to [1] for a more detailed discussion.

Roughly speaking, once the duty cycle has been selected, the normalized procedure in [1] is used to get a set of dimensionless parameters k_I, k_R, q_M, q_I and q_R

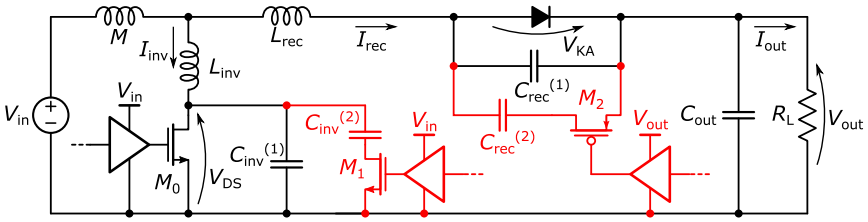


Fig. 2.3 Schematic of the boost resonant class-E converter allowing dual-frequency control. The additional cost with respect to the standard ON-OFF control in terms of hardware devices is highlighted in red.

ensuring the optimal class-E condition. Then, given the desired values of input and output voltages V_{in} and V_{out}, of the output current I_{out} and of the operating frequency f_s, the values of the inductors L_p, L_s, M and the capacitors C_{inv}, C_{rec} can be computed as

$$\begin{aligned} C_{\text{inv}} &= \frac{V_{\text{out}} I_{\text{out}}}{V_{\text{in}}^2} \frac{1}{2\pi f_s q_I}, \; C_{\text{rec}} = \frac{I_{\text{out}}}{V_{\text{out}} - V_{\text{in}}} \frac{1}{2\pi f_s q_R}, \\ M &= -\frac{q_M V_{\text{in}}}{2\pi f_s I_{\text{out}}}, \; L_{\text{inv}} = -M\left(\frac{V_{\text{in}}}{V_{\text{out}} - V_{\text{in}}} \frac{1}{k_I} + 1\right), \\ L_{\text{rec}} &= -M\left(\frac{V_{\text{out}} - V_{\text{in}}}{V_{\text{in}}} \frac{1}{k_R} + 1\right). \end{aligned} \tag{2.3.4}$$

Note that, according to (2.3.4), values of k_I, k_R, and q_M are expected to be negative in order to deal with a feasible converter (i.e., whose components have positive values).

2.3.2 Dual-Frequency Class-E Converter Design

The dual-frequency control technique we propose is a direct consequence of the multiple possible ways in which (2.3.4) can be de-normalized starting from the same dimensionless solution $\{k_I, k_R, q_M, q_I, q_R\}$.

In more details, let us assume that, given V_{in}, V_{out}, I_{out}, f_s and the solution $\{k_I, k_R, q_M, q_I, q_R\}$, one obtains from (2.3.4) the corresponding values for the circuit components M, L_{inv}, L_{rec}, C_{inv} and C_{rec}. Let us also assume that, with V_{in} and V_{out} remaining constant, the desired output power must be decreased by a factor $\alpha < 1$,

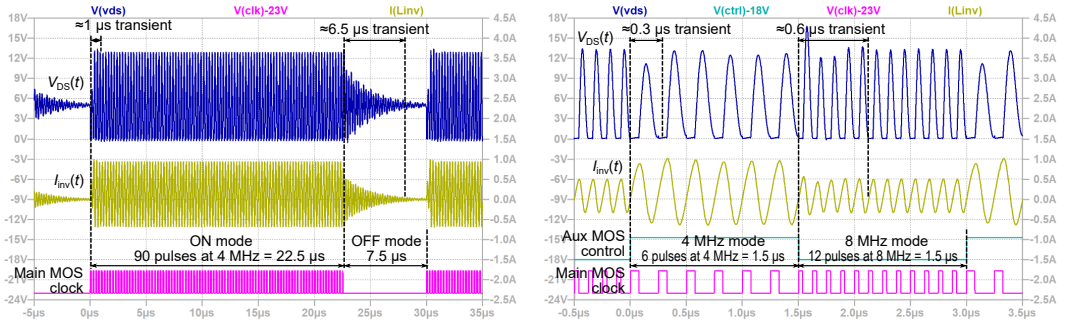


Fig. 2.4 Drain-to-source voltage $V_{\rm DS}$ and inverter current $I_{\rm inv}$ in a simulation of a controlled class-E boost converter. (a) The time required to turn-off the converter under the ON-OFF control is extremely long, setting the upper bound on the dimming frequency f_d; (b) transients in the proposed dual-frequency control are extremely short, allowing a much higher f_d.

so that the output current has to be set to $\alpha I_{\rm out}$. According to (2.3.4), we have a few possibilities to satisfy the new constraint:

- the most intuitive one is to maintain f_s constant. In this case, (2.3.4) is still satisfied by adopting M/α, $L_{\rm inv}/\alpha$, $L_{\rm rec}/\alpha$, $\alpha C_{\rm inv}$ and $\alpha C_{\rm rec}$ for the values of the circuit components;
- another possibility is to increase the switching frequency to f_s/α. In this case, (2.3.4) is satisfied if one chooses the same values of M, $L_{\rm inv}$ and $L_{\rm rec}$ as in the original solution, and decreases the resonant capacitances to $\alpha^2 C_{\rm inv}$ and $\alpha^2 C_{\rm rec}$.

The latter approach is extremely interesting from a hardware point of view as it shows that, to decrease the output power, it is enough to *i*) increase the oscillating frequency; and *ii*) decrease the values of the resonant capacitances (e.g., by simply disconnecting part of them from the circuit –assuming, for instance, that they are obtained by more capacitors connected in parallel– via an auxiliary switch). Noticeably, no changes are required to the magnetic elements.

In other words, in a real circuit implementation, we may change the output current by adopting the very simple schematic of Figure 2.3. The circuit is designed to work at an operating frequency $f_s = f_s^{(1)}$ with resonant capacitances $C_{\rm inv} = C_{\rm inv}^{(1)} + C_{\rm inv}^{(2)}$ and $C_{\rm rec} = C_{\rm rec}^{(1)} + C_{\rm rec}^{(2)}$, delivering $I_{\rm nom}^{(1)} = I_{\rm out}$. When the output current has to be decreased to $I_{\rm nom}^{(2)} = \alpha I_{\rm out}$, the switching frequency is increased to $f_s/\alpha = f_s^{(2)}$, and

the two extra capacitors $C_{\text{inv}}^{(2)}$ and $C_{\text{rec}}^{(2)}$ are disconnected from the circuit, so that $C_{\text{inv}} = C_{\text{inv}}^{(1)}$ and $C_{\text{rec}} = C_{\text{rec}}^{(1)}$. Since both solutions correspond to the same optimal dimensionless solution $\{k_I, k_R, q_M, q_I, q_R\}$, they both feature ZVS and ZVDS.

The only critical point from the hardware point of view is the design of the auxiliary switches. Our suggestion is to design the switch connecting $C_{\text{inv}}^{(2)}$ as an NMOS (M_1 in the figure), driven by a gate driver whose supply voltage is V_{in}. The switch connecting $C_{\text{rec}}^{(2)}$ can be a PMOS (M_2 in the figure) driven by a gate driver whose supply voltage is V_{out}. This solution, based on the observation that the voltage at the drain of M_1 is always positive, and that the one at the drain of M_2 is always lower than V_{out}, allows both switches to correctly turn off when required.

The dual solution based on a switched inductor approach could also be adopted. Assuming to decrease the output current to αI_{out}, it is possible to rely on the same normalized solution by decreasing the switching frequency to αf_s and increasing magnetics to M/α^2, L_{inv}/α^2 and L_{rec}/α^2, while keeping capacitances constant. The value of the inductance can be changed assuming to implement the inductors as a series of multiple devices, and by shorting some of them when required. Even if possible, this solution is not suggested, as it would be far more complex from the hardware point of view with respect to the switched-capacitor case. First of all, three switches are required instead of two. Then, the implementation of the switches by means of MOS devices would be difficult as it is not possible to identify a configuration where the source terminal voltage is at a constant level, as in the switched capacitor case.

The idea grounding this work is to introduce a dimming mechanism, similar to what happens in the standard ON-OFF approach, based on the architecture of Figure 2.3. Instead of alternating the converter in an ON-mode (output current I_{nom}, for a fraction of time D) and an OFF-mode (output current 0, for a fraction of time $1-D$), we alternate two converter configurations at different frequencies. In the first one the converter is operating, for a ratio of time D, at $f_s^{(1)}$, and the two extra capacitors are connected to the circuit, so that a current $I_{\text{nom}}^{(1)}$ is delivered to the load. In the second one, for a fraction of time $1-D$, the oscillation frequency is $f_s^{(2)}$, the extra capacitors are disconnected, and the current delivered to the load is $I_{\text{nom}}^{(2)}$. By *dynamically* alternating the two modes, only the weighted average of the two currents is delivered to the output, so that (2.2.3) holds. In other words, it is possible to regulate, with the advantages detailed below, the output current in

the range $[I_{\text{nom}}^{(1)}, I_{\text{nom}}^{(2)}]$. Lower values are still obtainable with the standard ON-OFF approach, if needed.

The additional hardware cost with respect to the ON-OFF approach has been highlighted in Figure 2.3, in red. Neglecting the control unit (that is required also with the ON-OFF methodology, and whose design is out of the scope of this work), two additional capacitors and two MOS switches only, are required. This is a fairly low cost in terms of hardware devices. Beyond that, even the increase in terms of required energy, or additional losses, is expected to be limited. Some details on this are provided in Section 2.4.

To show the advantages of our approach, a 5 V-to-10 V converter with dual-frequency control capabilities and $\alpha = 0.5$ has been designed, assuming that $P_{\text{nom}}^{(1)} = 1\,\text{W}$ ($I_{\text{nom}}^{(1)} = 100\,\text{mA}$) at $f_s^{(1)} = 4\,\text{MHz}$, and $P_{\text{nom}}^{(2)} = 0.5\,\text{W}$ ($I_{\text{nom}}^{(2)} = 50\,\text{mA}$) at $f_s^{(2)} = 8\,\text{MHz}$.

In the corresponding simulation, we used a model of the NMOS IRLM0030TRPBF by Infineon as main switch M_0, and of a Nexperia PMEG6030ELP Schottky barrier diode as rectifier diode D_0. An additional instance of an IRLM0030TRPBF is used as M_1, whereas a PMOS BSS315PH6327XT by Infineon is used as M_2.

Resonating capacitors are considered ideal, whereas inductors have been considered lossy, with quality factors $Q = 55$ at 4 MHz and $Q = 75$ at 8 MHz. Furthermore, three additional $0.1\,\Omega$ series resistances have been added to emulate current sensing resistors for M, L_{inv} and L_{rec}.

The design has been obtained by following the many trade-offs suggested in [1]. The duty cycle of the main clock is set to 30%, as this value ensures reduced stress on the main switch. The two degrees of freedom k_I and k_R of the dimensionless system should be sufficiently far from 0, to reduce the RMS value of the currents in the circuit, and so increase the efficiency. At the same time, the product $k_I k_R$ should be sufficiently lower than 1 to ensure robustness to parameter variations in a real circuit implementation. The operating point $k_I = -0.75$ and $k_R = -0.75$ appears to be a good choice. The optimum class-E condition is obtained for $q_I = 0.23$, $q_R = 0.21$, $q_M = -0.51$. The dimensionless solution leads to $L_{\text{inv}} = L_{\text{rec}} = 336\,\text{nF}$ $M = 1.01\,\mu\text{H}$, $C_{\text{inv}}^{1)} = 605\,\text{pF}$, $C_{\text{rec}}^{(1)} = 648\,\text{pF}$ and $C_{\text{inv}}^{(2)} = 2.71\,\text{nF}$, $C_{\text{rec}}^{(2)} = 2.83\,\text{nF}$. These values, with respect to the straightforward conversion given by (2.3.4), have been modified to keep into account devices non-idealities. In particular, capacitor values have been slightly decreased to compensate the parasitic capacitances of the IRLM0030TRPBF,

the PMEG6030ELP and the BSS315PH6327XT, evaluated to be 125 pF, 180 pF and 100 pF, respectively.

Simulation results, showing the profile of the drain-to-source voltage V_{DS} and the L_{inv} current I_{inv}, are plotted in Figure 2.4. Part (a) refers to a standard ON-OFF control for the converter operating at $f_s^{(1)} = 4\,\mathrm{MHz}$, with dimming ratio $D = 75\%$ to achieve an expected $I_{\mathrm{out}} = 75\,\mathrm{mA}$. Part (b) refers to the proposed dual-frequency approach with dimming ratio $D = 50\%$, to get the same expected $I_{\mathrm{out}} = 75\,\mathrm{mA}$. Both cases feature almost perfect ZVS and ZVDS conditions once transient from one state to the other one is completed.

The most impressive difference is that, in the ON-OFF approach, the turn-off transient time is extremely long. This is indeed expected. Roughly speaking, transients are observed since there is an abrupt change in some parameters of the system or in the control function (in this case, the clock), that implies a change in the steady-periodic solution of the system. Switching instantaneously from one steady-periodic solution to another one is generally not possible, as this would imply a discontinuity in the system state variables. To ensure continuity between the old and the new steady-state solution, a transient response is generated. The length of the transient depends both on the entity of the aforementioned discontinuity, and on the capability of the system to dissipate energy, associated with resistive elements of the circuit (mainly the load, but also all parasitic resistances).

By considering this simple model, the complexity of the transient length computation is clear. Hence, it is difficult even to provide an estimation of it; however, we can intuitively say that, in order to turn the converter off, all inductor currents should be instantaneously set to zero. Being this not possible, a transient is generated. Furthermore, since in the OFF-mode the load is not powered anymore by the converter, there are no resistive elements (besides the parasitics ones) capable of quickly dissipating the energy associated with the residual oscillations. This slows down the transient.

Since the transient time should be at least shorter, if not negligible, with respect to the converter ON and OFF times, this sets a very low upper bound to the dimming frequency f_d. The consequence, according to (2.2.2), is an important low-frequency output ripple or the need for a very large output filter capacitor. Conversely, transient times are much shorter in the dual-frequency example since the load is always receiving energy from the converter, both in the $f_s^{(1)}$-mode and $f_s^{(2)}$-mode, and can

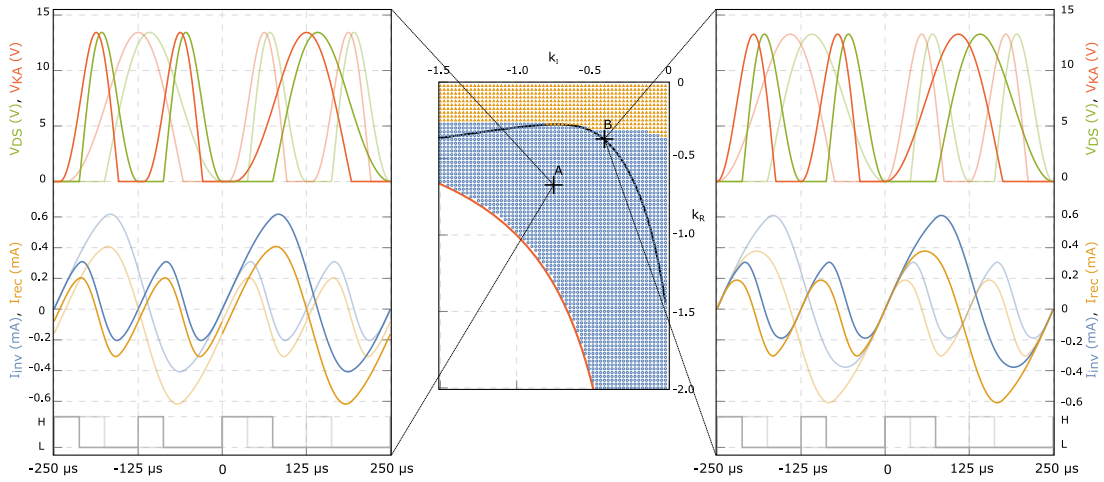


Fig. 2.5 Space of the solutions of the class-E design problem in the lossless normalized system for main clock duty cycle 30%. Blue points refer to the optimal (ZVS + ZVDS) class-E solution, and orange points to a sub-optimal solution (ZVS only). The points laying on the black line indicate solutions featuring Zero-Transient (ZT). Two examples of waveforms are also shown, one (on the left) not featuring ZT, and one (on the right) featuring ZT.

therefore dissipate the energy associated to the transient response. It implies that a much higher f_d is allowed in this case.

2.3.3 Dual-Frequency Class-E Converter Optimization

One important point to be noted in the previous design example is that the two degrees of freedom k_I and k_R were (somehow arbitrarily) set following suggestions in [1] with the only aim of ensuring the good behavior of the converter. No attempt was made to use these degrees of freedom with the aim of optimizing the performance of the converter when working in the dual-frequency mode.

One significant way to do so is to choose k_I and k_R to minimize the transient time from one state to another one, as this would maximize the dimming frequency, and either minimize the output ripple or relax constraints on the output filter capacitance.

To this aim, let us consider the scatter plot in the middle of Figure 2.5, which is the normalized solution state space for the degrees of freedom k_I–k_R taken from [1] for the (ideal version) of the converter topology under investigation. Here, a point in the scattered blue area represents a choice of the two degrees of freedom that allows an optimal behavior (both ZVS and ZVDS), whereas orange points correspond to

solutions where only the ZVS sub-optimal behavior can be achieved. The red line sets the feasibility condition limit in a real system.

The point $(-0.75, -0.75)$, highlighted as "A", is the one considered in the previous example. The evolution of the optimal converter given this choice of the degrees of freedom is plotted on the left, where one shows the voltages V_{DS} and V_{KA}, and the currents I_{inv} and I_{rec}, both for the $f_s^{(1)} = 4\,\mathrm{MHz}$ and the $f_s^{(2)} = 8\,\mathrm{MHz}$ systems. For $t < 0$, we have reported the waveforms for the 8 MHz configuration, and for $t > 0$ those for the 4 MHz configuration. For the sake of thoroughness, the dual transition, i.e. 4 MHz-to-8 MHz, is shown with transparent lines.

The highlighted waveforms are not continuous at $t = 0$ due to a step in I_{rec} (see the yellow line in the left plot of Figure 2.5). Indeed, this is the expected discontinuity that, according to the simple model proposed above, generates a transient response: the larger the discontinuity, the longer the transient.

Yet, the transient time can be shortened by reducing this discontinuity. Ideally, it can be completely removed by decreasing the discontinuity to zero, i.e., by imposing waveform *continuity* at the switching instant $t = 0$. This happens if and only if $I_{\mathrm{rec}}(0) = 0$[1] If we are able to ensure this condition, we can expect a Zero Transient (ZT) response.

It is interesting to wonder whether there are points, among the space of solutions, capable of ensuring a ZT response. Indeed, many points exist, and they have been highlighted with the black line of the center scatter plot in Figure 2.5. Regrettably, the computation of all these points has the same complexity and the same drawbacks as the computation of the optimal solution of the normalized class-E converter according to the procedure in [1]. Due to this, it is not possible to provide here a closed-form equation able to identify them, and the easiest way to compute them is by using the tools provided in [1].

As an example, the point $(-0.4, -0.4)$, highlighted as "B", belongs to the ZT locus of the points. The observed behavior for the design of the ideal converter using these values of the degrees of freedom is shown on the right, and the waveforms

[1] It has been shown in [1] that the I_{rec} waveforms, for the $f_s^{(1)}$ and the $f_s^{(2)}$ cases, are obtained from their dimensionless counterpart i_{rec} multiplied by two different scaling factors. Accordingly, the only way to ensure the continuity at $t = 0$ is to have $i_{\mathrm{rec}}(0) = 0$, so that $I_{\mathrm{rec}}(0) = 0$ independently of the scaling factor.

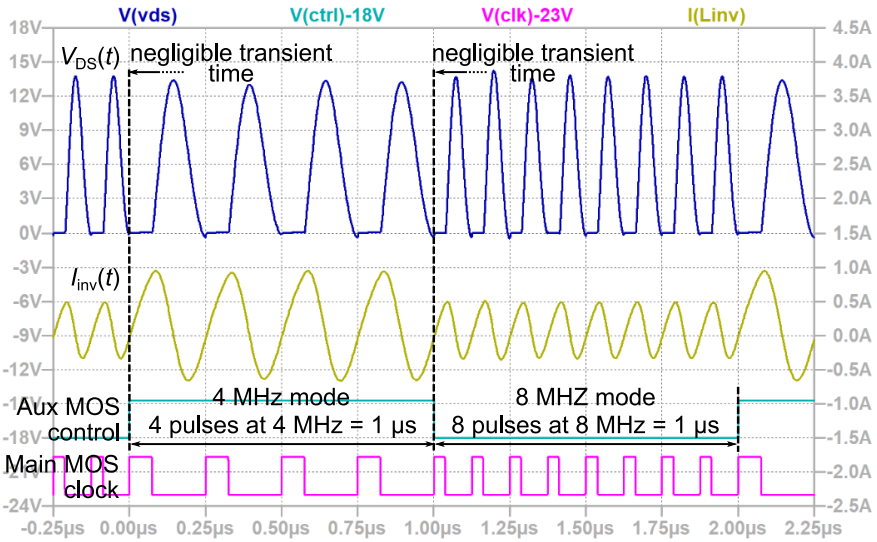


Fig. 2.6 Simulation of the dual-frequency converter designed to work in a ZT point. Waveforms clearly show no settling time when switching from one state to the other one. Furthermore, ZVS and ZVDS are clearly preserved in both states.

of the 8 MHz configuration and that of the 4 MHz one join with no discontinuity at $t = 0$.

With the aim of exploiting ZT in a converter where non-ideal components are employed, we consider here a second design with the same specifications as the first one described so far and corresponding to $k_I = -0.4$ and $k_R = -0.4$ in the ideal setting. Indeed, when introducing losses parameters, the ZT line is slightly modified with respect to the one shown in Figure 2.5, but we can still approximate k_I and k_R with -0.4, so that optimum soft-switching condition is ensured for $q_I = 0.24$, $q_R = 0.22$, $q_M = -0.11$.

This dimensionless solution leads to real components given by $L_{\text{inv}} = L_{\text{rec}} = 332\,\text{nF}$ $M = 221\,\text{nH}$, $C_{\text{inv}}^{(1)} = 558\,\text{pF}$, $C_{\text{rec}}^{(1)} = 645\,\text{pF}$ and $C_{\text{inv}}^{(2)} = 2.56\,\text{nF}$, $C_{\text{rec}}^{(2)} = 2.77\,\text{nF}$.

Simulation results are plotted in Figure 2.6 and show, as expected, a ZT response, with no visible transient when switching to the 4 MHz configuration to the 8 MHz one, and vice-versa.

This condition is clearly the optimal one for a dimming-based control, as it allows to push the dimming frequency f_d to extremely high values, that can be of almost the same order of magnitude as $f_s^{(1)}$ and $f_s^{(2)}$. More precisely, the upper bound of

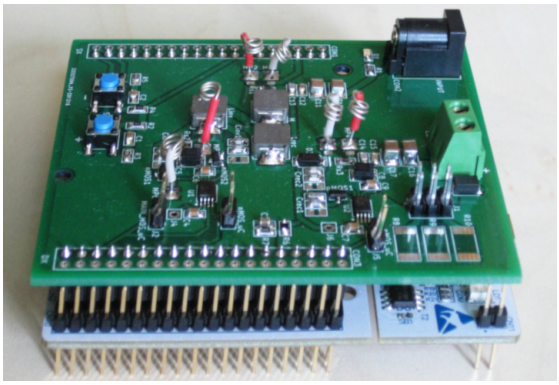


Fig. 2.7 A picture of the designed prototype that fits on top of the NUCLEO-F334R8 board.

the dimming frequency can be calculated by considering one only high-frequency and one low-frequency period so that $f_d = 1/(1/f_s^{(1)} + 1/f_s^{(2)})$.

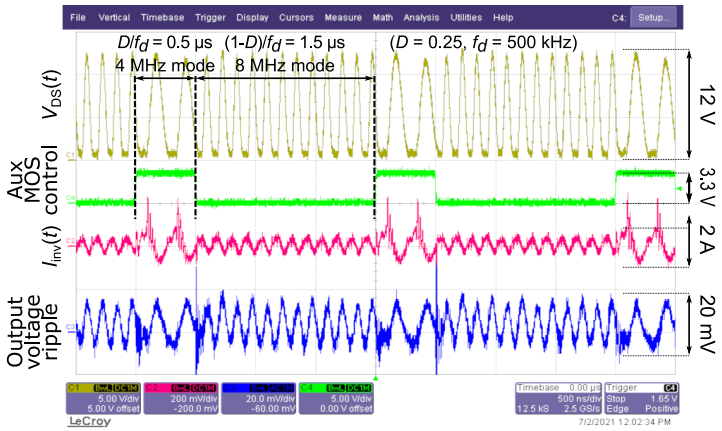
2.4 Experimental Results

A prototype of the 5-to-10 V class-E boost converter capable of dual-frequency control and optimized for ZT, described in the previous section, has been assembled and tested.

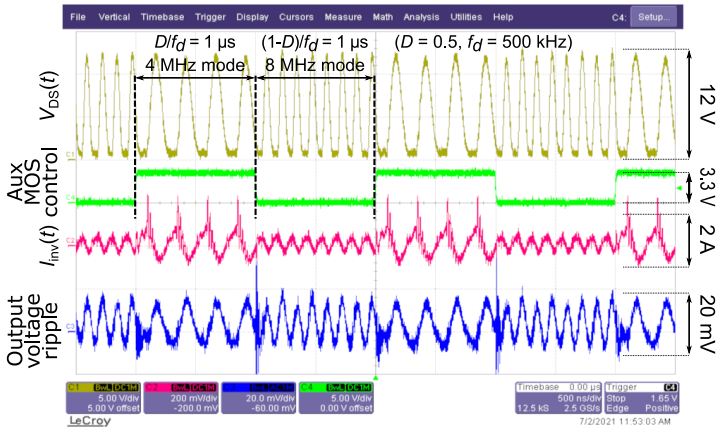
The values of inductances and capacitances have been approximated to fit values easily achievable with commercial devices. More precisely, $L_{\text{inv}} = L_{\text{rec}} = 330\,\text{nH}$, $M = 220\,\text{nH}$ and $C_{\text{inv}}^{(1)} = 550\,\text{pF}$, $C_{\text{rec}}^{(1)} = 660\,\text{pF}$ and $C_{\text{inv}}^{(2)} = 2.5\,\text{nF}$, $C_{\text{rec}}^{(2)} = 2.8\,\text{nF}$. The output filter capacitance has been set to 20 µF.

Ceramic capacitors with a high-quality dielectric (e.g., C0G) have been used for the resonant capacitances to support the assumption of ideality, as they are known to have very high-quality factors ($Q > 1000$). Inductors have been selected as commercial shielded molded inductors from the IHLP-2525CZ-01 series by Vishay Dale. Their quality factors have been measured as $Q_{L_{\text{inv}}} \approx Q_{L_{\text{rec}}} \approx 43$ and $Q_M \approx 42$ at 8 MHz and $Q_{L_{\text{inv}}} \approx Q_{L_{\text{rec}}} \approx 60$ and $Q_M = 58$ at 4 MHz. Finally, all MOS transistors are driven by means of an ISL5510IVZ, a high-speed MOS gate driver by Renesas.

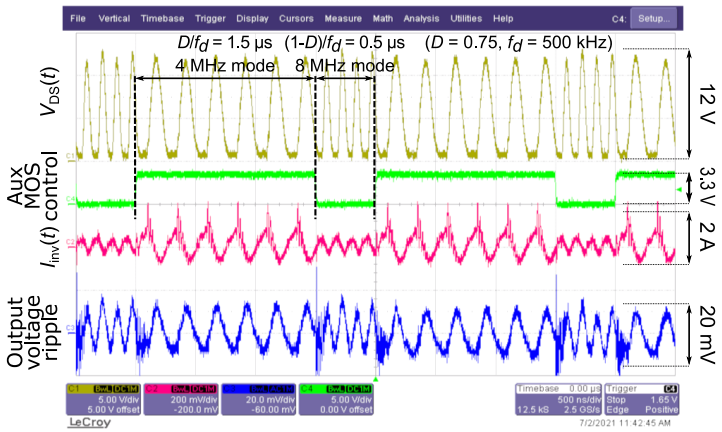
The prototype, which can be seen in Figure 2.7, has been designed to fit on top of a Nucleo-F334R8 by STMicroelectronics, used to provide all timing signals. This board is a mainstream 32-bit MCU, based on an ARM micro-controller embedding a high-resolution timer module, used to generate both the main clock signals and



(a)



(b)



(c)

Fig. 2.8 Measurements from the designed prototype. From top to bottom: Drain-to-source voltage V_{DS}; additional MOS control signal; inverter current I_{inv}; output voltage ripple. (a) Dimming ratio 25%. (a) Dimming ratio 50%. (a) Dimming ratio 75%.

the additional MOS control signal. The ARM microcontroller also embeds a very simple feedback loop; however, we consider the design of this feedback, including the stability analysis and bandwidth, out of the scope of this work. In any case, any control specifically designed for the ON-OFF approach is expected to correctly work in dual-frequency one, too.

Measurements are shown in Figure 2.8. When the output voltage is regulated at $V_{\text{out}} = 10\,\text{V}$, the system clearly features optimum soft-switching condition (both when operating at 4 MHz and at 8 MHz) and zero transient, in agreement with the developed model and with circuit simulation. In our prototype we were able to rise the dimming frequency to $f_d = 500\,\text{kHz}$, that is a very high value with respect to other solutions in the Literature, in particular when compared to the 4 MHz–8 MHz operating frequencies. In fact, the ratio between the operating frequency and the dimming frequency is, in our case, as low as 16–8[2]. The proposed prototype works with a dimming frequency 16× smaller than the higher available switching frequency (i.e., $f_d = 500\,\text{kHz}$ and $f_s^{(2)} = 8\,\text{MHz}$) that is an excellent result with respect to the state-of-the-art examples [72, 70, 73] mentioned in Section 2.2, and in which f_d is between 100× and 1200× smaller than the switching frequency. With such a high value of f_d, the low-frequency component of the output ripple is negligible, and in the figure, the observed output ripple has indeed a high-frequency component only. This is an important result, especially considering that the output filter capacitance is as low as 20 µF.

The measured efficiency of the converter (considering the converter alone, i.e., neglecting the Nucleo board and the gate drivers), depends obviously on the output current (and so on the dimming ratio) and ranges from 70% in the high-power, 4 MHz state (it results in $I_{\text{in}} = 270\,\text{mA}$ and $I_{\text{out}} = 95\,\text{mA}$), to 73% in the low-power, 8 MHz state (it results in $I_{\text{in}} = 126\,\text{mA}$ and $I_{\text{out}} = 47\,\text{mA}$) and it is aligned with the expected efficiency given the values of the lossy parameters. By means of a SPICE simulation, it is also possible to investigate how conduction losses are distributed. The main observed contribution is given by the finite-Q of the inductors and by the current sensing resistors, required in our prototype for the verification of the correct behaviour of the circuit. Then, as in the majority of DC-DC converters, the other large source of losses is the rectifying diode (slightly smaller than 20%). A similar amount of power is cumulatively dissipated by the main MOS ($\approx 5\%$) and the two

[2] i.e., a number of high-frequency periods between 8 and 16 is observed in a dimming period

auxiliary ones ($\approx 15\%$). The analysis based on the measured current waveforms of Figure 2.8 and the estimation of the main circuit parasitics confirm this distribution.

It is worth stressing that only a negligible increase in the conduction losses can be expected when the proposed dual-frequency technique is employed instead of the standard ON-OFF methodology. To show this, we considered the simulations of the two converters with the same design specifications and the same circuit elements, except for the additional switches and capacitors that are only needed for the dual-frequency control. In order to ensure the same output power, the converter employing the ON-OFF control operates at 4 MHz with a dimming ratio $D = 0.75$ to achieve the expected output current of 75 mA. On the other hand, the converter employing the Zero Transient Dual Frequency control alternates between 4 MHz and 8 MHz with $D = 0.5$ to get the same output current. In both cases, the power required to drive all MOS devices is not taken into account but, being f_d one order of magnitude lower than the oscillation frequency, driving losses are certainly dominated by the main switch, present in both implementations. Conduction losses are the same for corresponding elements in the two circuits and therefore the only additional contribution to losses for the dual frequency control is given by the two auxiliary MOS devices. This is just a small fraction of the overall conduction losses, evaluated in the proposed prototype to be $\approx 15\%$ of the total value.

2.5 Conclusion

In this chapter, a new dual-frequency control for Class-E DC-DC resonant converters has been proposed. The main advantage with respect to the state of the art is that the proposed control allows reaching zero transient response when the converter is switched from the state in which it is operating at the first frequency, to the state in which it is operating at the other one. This allows to extremely increase the dimming frequency f_d at which the two states are switched while preserving the class-E optimum condition during all converter operations. As a proof of concept, we presented a DC-DC converter prototype capable of alternatively working either at 4 MHz or 8 MHz and controlled with f_d of almost the same order of magnitude. The prototype operates with $f_d = 500$ kHz, that is $16\times$ smaller than the higher available switching frequency. This is an excellent result compared to the mentioned state-of-the-art examples, where the observed reduction of f_d with respect to the operating

frequency is between 100× and 1200×, with evident advantages in terms of output voltage ripple. The measurements confirm an almost perfect matching with the expected results by always guaranteeing both the optimal class-E converter behavior and the zero transient time when switching from one frequency to other.

Chapter 3

"Through-The-Barrier" Communication in Isolated Class-E Converters Embedding a Low-K Transformer

3.1 Introduction

Due to safety or grounding purposes, galvanic isolation from the main power supply is in many cases useful or even mandatory. Applications requiring such a feature range from safety-critical devices, such as medical equipment, to the most different scenarios [79–83].

To achieve this target, special approaches are required both for transferring the energy trough the isolation barrier, and for allowing the two isolated parts to communicate with the each other. The adoption of an isolation transformer is the classical solution almost always adopted for transferring energy; conversely, many different approaches can be found for creating an electrically isolated communication channel. Common solutions include extra pulse transformers, optocouplers, or high-voltage capacitors. Yet, these solutions pose several limitations in the realization of miniaturized or even fully integrated systems, as all these devices are typically the most cumbersome and difficult to integrate parts.

In the effort of moving towards miniaturized solutions, some recent approaches proposed to use a single isolation transformers both for energy and data transfer. Even if they strongly differ in methodology and application, the underlying idea is to use the data signal to modulate the power signal. Efficiency, effectiveness and complexity of the decoding depend on the particular case [84–86].

In this chapter we focus on the methodology proposed in [46] that applies to a resonant class-E dc-dc converters. Briefly, the principle is based on the modification of a circuit parameter (in detail, the value of a capacitance by connecting in parallel or disconnecting an additional one) that, due to the properties of the resonant architecture, generates detectable changes in all circuit waveforms. The approach allows a bidirectional (half-duplex) fast communication, since a binary symbol (either backward, i.e., from the secondary to the primary side, or forward, i.e., from the primary to the secondary side) can be transmitted at each converter clock cycle. In [46] a 1 MHz prototype capable of delivering up to 1.2 W is presented as a proof-of-concept. We review here the methodology, considering the case where a coreless transformer with a low coupling factor k is adopted to increase the converter working frequency. Communication is still possible; indeed, due to the lower coupling, the transmission of one bit requires more than one clock cycle, with a slightly different sensing strategy.

This chapter is organized as follows. In Sec. 3.2 we review the methodology proposed in [46], highlighting the problems that may arise when k is too small. In Sec. 3.3 we propose a modification in the communication strategy to solve the identified problems, and in Sec. 3.4 we validate this strategy by means of realistic circuit-level simulations of a case study. Finally, we draw the conclusion.

3.2 System design and considerations

The schematic of the circuit proposed in [46] is depicted in Fig. 3.1. Basically, it is a class-E dc-dc converter [10, 11, 16] operating at frequency $f_s = 1/T$, and featuring zero-voltage switching (ZVS), i.e., a resonant converter where reactive elements are designed to ensure that $V_{\mathrm{DS}}(t)$, when the main MOS is off, oscillates and reaches exactly zero level at the same instant when the MOS has to be turned on. This alleviates the turn-on transient problems, reduces the power consumption and allows higher speed operation [9, 18].

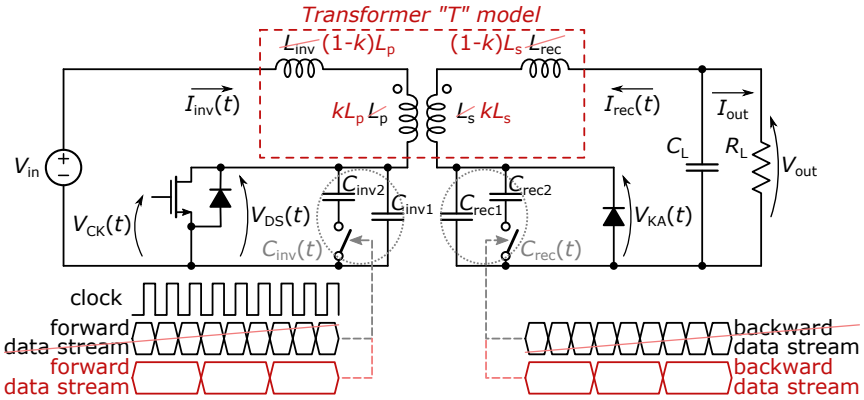


Fig. 3.1 Schematic and working principle (black color) of the class-E converter with bidirectional communication capability proposed in [46], and modification (red color) proposed when using a low-k transformer.

The strategy used to introduce communication relies on the semi-analytic design approach proposed in [31] and improved in [34]. Basically, it is enough to add two additional capacitances C_{inv2} and C_{rec2} in parallel to the already existing ones C_{inv1} and C_{rec1}, respectively, thus giving rise to the two time-varying capacitances $C_{\text{inv}}(t)$ and $C_{\text{rec}}(t)$, whose value is modulated by the symbol to be transmitted, as sketched in Fig. 3.1. When communicating backward we set

$$C_{\text{inv}}(t) = C_{\text{inv1}} + C_{\text{inv2}}$$
$$C_{\text{rec}}(t) = \begin{cases} C_{\text{rec1}} & \text{when transmitting '0'}_b \\ C_{\text{rec1}} + C_{\text{rec2}} & \text{when transmitting '1'}_b \end{cases}$$

and when communicating forward

$$C_{\text{inv}}(t) = \begin{cases} C_{\text{inv1}} & \text{when transmitting '0'}_f \\ C_{\text{inv1}} + C_{\text{inv2}} & \text{when transmitting '1'}_f \end{cases}$$
$$C_{\text{rec}}(t) = C_{\text{rec1}} + C_{\text{rec2}}$$

where the notation 's'$_b$ or 's'$_f$ stands for a symbol or a sequence s transmitted backward or forward, respectively.

In this way, the perfect ZVS property is lost and replaced by a (perfectly tolerable) quasi-ZVS, where the $V_{\text{DS}}(t)$ at the MOS turn-on time is *almost* zero, with the advantage to enable communication between the two sides of the transformers.

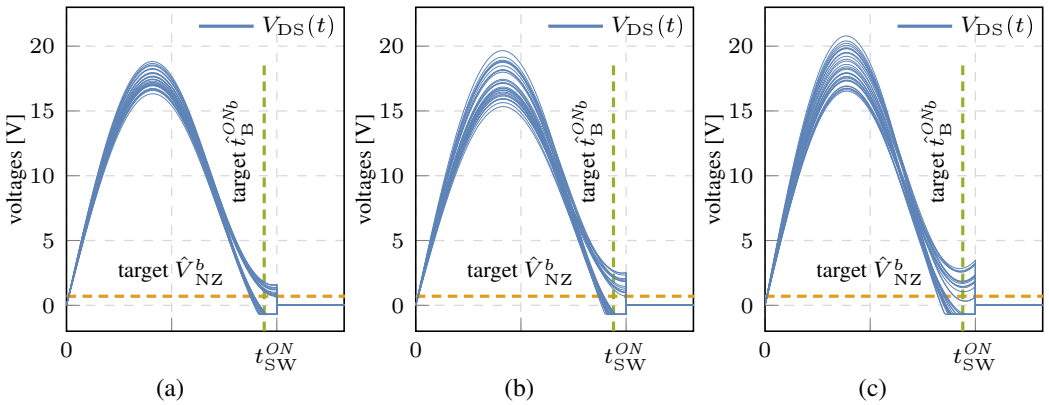


Fig. 3.2 Eye-diagram of the $V_{DS}(t)$ in backward communication mode according to the theoretical model developed in [46] using a transformer with coupling factor: (a): $k = 0.98$; (b): $k = 0.9$; and (c): $k = 0.8$.

In backward communication mode, decoding is achieved by sensing $V_{DS}(t)$ as illustrated in Fig. 3.2(a). When sending '1'$_b$, the body diode of the MOS turns on at a time $t_B^{ON_b} < t_{SW}^{ON}$, whereas when sending '0'$_b$, at the MOS turn-on instant t_{SW}^{ON}, it is $V_{DS}(t_{SW}^{ON}) = V_{NZ}^b > 0$. Without entering into details that can be found in [46], two main problems arise in the converter behavior. First, the power transferred to the load depends on the transmitted symbol. This issue can be solved by adopting a coding strategy where '1'$_b$ and '0'$_b$ are balanced, so that the actual transferred power is the average we get in the two cases independently of the transmitted sequence. Second, there is a *memory effect*. Mathematically, the behavior of the converter in one clock period can be schematized as depending both on $C_{inv}(t)$ and $C_{rec}(t)$, and on the converter state that can be summarized with the two initial currents $\{I_{inv}(0), I_{rec}(0)\}$. The latter however depends on all previously transmitted symbols, and the same happens for V_{NZ}^b and $t_B^{ON_b}$. According to [46], the dependence is weak, and it is possible to design a system according to its *worst-case*: designers should consider $\hat{t}_B^{ON_b}$, defined as the *latest value* of $t_B^{ON_b}$ when transmitting '0'$_b$, and $\hat{V}_{NZ}^b$, defined as the *lowest value* of V_{NZ}^b when sending '0'$_b$.

In backward communication, the suggested decoding strategy is differential and based on the sensing of $V_{KA}(t)$. Being T_D^f the time between two consecutive rectifying diode turn-on instants, when the transmitted symbol is the same as the previous one, it is $T_D^f \approx T$. When transmitting a symbol '1'$_f$ after a '0'$_f$, it is $T_D^f \approx T - \Delta\bar{t}_D^{ON_f}$, and when transmitting a symbol '0'$_f$ after a '1'$_f$, it is $T_D^f \approx T + \Delta\bar{t}_D^{ON_f}$ with $T_D^f \approx T$.

The methodology was experimentally verified on a prototype operating at $f_s = 1\,\text{MHz}$ using a WE-FLEX transformer by Würth Elektronik, with a coupling factor $k \approx 0.98$. As almost all commercial devices, it is built using ferro-magnetic core that ensures a very high coupling factor, but losses are rapidly decaying when increasing the frequency. As an example, in the considered transformer, the quality factor drops to 4 at a frequency of 10 MHz. Such a low value unfortunately prevents any useful application.

A possible workaround for high-frequency designs is to use coreless transformers, that may ensure at the same time a high operating frequency and low losses. This however comes at the cost of a lower coupling factor k, due to the lack of the ferromagnetic core that concentrates the magnetic flux.

Indeed, using a transformer with a low k requires to modify the described communication technique. In Fig. 3.2 we have shown the eye-diagram of $V_{\text{DS}}(t)$ when re-designing the circuit proposed in [46] using a transformer where k has been reduced from $k = 0.98$ to $k = 0.9$ and to $k = 0.8$. The obtained eye-diagrams are compared with the target values of $\hat{t}_{\text{B}}^{ON_b}$ and $\hat{V}_{\text{NZ}}^{b}$, superimposed to the figure. Is it clear that, as k decreases, the spread between all possible waveforms increases. Furthermore, for $k = 0.8$, desired values are only approximately reached. For lower values of k, the convergence of the mathematical script was not reached, and we were not able to find a design with the given constraints.

Intuitively speaking, a possible explanation is the following one. When the coupling between the primary and the secondary side decreases, it is reasonable to assume that a larger variation in parameters at the secondary side (i.e., of $C_{\text{rec}}(t)$) is necessary to get the same change in the waveform at the primary side. This however implies a larger spread of the system state $\{I_{\text{inv}}(jT), I_{\text{rec}}(jT)\}$ at the j-th clock cycle, and as a consequence, a stronger memory effect, with a growing difficulty in ensuring a good converter behavior for any possible transmitted sequence.

3.3 Converter design with a low k transformer

In this chapter, we consider the design of a system using a transformer made of two printed circuit board (PCB) inductors of Fig. 3.3. The coils have been designed to operate at the ISM band centered at 6.78 MHz in a wireless power transfer system,

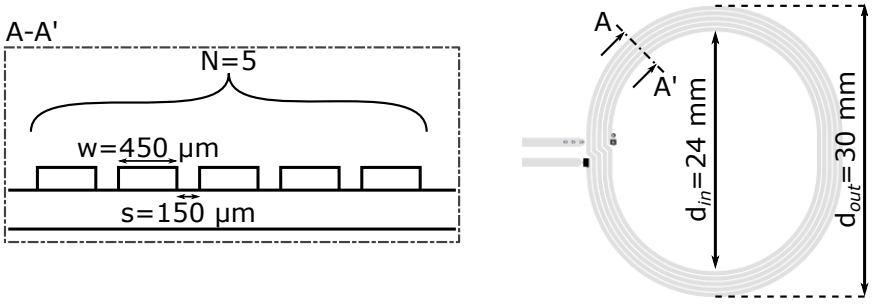


Fig. 3.3 Layout of the PCB inductor used both as primary and secondary coil in the coreless transformer.

and their inductance is equal to 1.47 µH. The transformer is obtained by using two of these coils, one on the top side of the PCB used a primary coil, and one on the bottom side of the PCB used a secondary one. The structure behaves as a 1:1 transformer, with a measured coupling factor $k = 0.52$ and a quality factor of about 200 when implemented over a standard 1.6 mm board with FR4 dielectric when working at 6.78 MHz.

To enable communication between primary and secondary side, we propose two modifications with respect to the original technique proposed in [46].

First, the schematic can be simplified. When considering the classic "T" model for a transformer, with coupling factor k and a total inductance L_p at the primary side (and L_s at the secondary side, with $L_\mathrm{p}/L_\mathrm{s} = (n_s/n_p)^2$, being n_s/n_p the transformer turns ratio), we have two large leakage inductors $(1-k)L_\mathrm{p}$ and $(1-k)L_\mathrm{s}$ that can be used instead of the original resonance ones L_inv and L_rec, along with a perfectly coupled transformer with inductance kL_p at the primary side and kL_s at the secondary side[1]. This has been illustrated in Fig. 3.1.

Second, it is mandatory to mitigate the catastrophic consequences of the stronger memory effect. The solution we propose is to repeat the transmission of any symbol for a number R of consecutive clock periods. The intuitive effect on the system state $\{I_\mathrm{inv}(jT), I_\mathrm{rec}(jT)\}$ of allowing the converter to work in the same configuration (i.e., with the same value of $C_\mathrm{inv}(t)$ and $C_\mathrm{rec}(t)$) for many consecutive clock periods is illustrated in Fig. 3.4: independently of the initial condition, the converter is moving towards a stable state that does not depend anymore on previous transmitted symbols.

[1]Note that $L_\mathrm{inv} = 0$ was assumed in [46] to work with a simpler schematic.

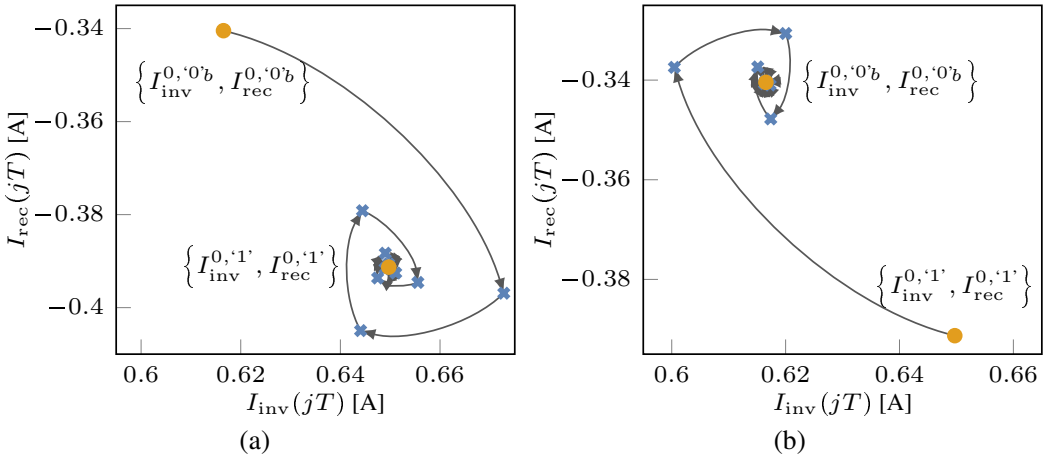


Fig. 3.4 Example of transitions to the two stable states during backward communication.

In other words, for large R, the converter is always moving towards one of the three *stable* states:

- $\left\{I_{\mathrm{inv}}^{0,\text{`1'}}, I_{\mathrm{rec}}^{0,\text{`1'}}\right\}$ when transmitting either '1'$_b$ or '1'$_f$ (i.e., $C_{\mathrm{inv}}(t) = C_{\mathrm{inv1}} + C_{\mathrm{inv2}}$ and $C_{\mathrm{rec}}(t) = C_{\mathrm{rec1}} + C_{\mathrm{rec2}}$);
- $\left\{I_{\mathrm{inv}}^{0,\text{`0'}_b}, I_{\mathrm{rec}}^{0,\text{`0'}_b}\right\}$ when transmitting '0'$_b$ (i.e., $C_{\mathrm{inv}}(t) = C_{\mathrm{inv1}} + C_{\mathrm{inv2}}$ and $C_{\mathrm{rec}}(t) = C_{\mathrm{rec1}}$);
- $\left\{I_{\mathrm{inv}}^{0,\text{`0'}_f}, I_{\mathrm{rec}}^{0,\text{`0'}_f}\right\}$ when transmitting '0'$_f$ (i.e., $C_{\mathrm{inv}}(t) = C_{\mathrm{inv1}}$ and $C_{\mathrm{rec}}(t) = C_{\mathrm{rec1}} + C_{\mathrm{rec2}}$).

The transition from $\left\{I_{\mathrm{inv}}^{0,\text{`0'}_b}, I_{\mathrm{rec}}^{0,\text{`0'}_b}\right\}$ to $\left\{I_{\mathrm{inv}}^{0,\text{`1'}}, I_{\mathrm{rec}}^{0,\text{`1'}}\right\}$ is shown in Fig. 3.4(a), and the transition from $\left\{I_{\mathrm{inv}}^{0,\text{`1'}}, I_{\mathrm{rec}}^{0,\text{`1'}}\right\}$ to $\left\{I_{\mathrm{inv}}^{0,\text{`0'}_b}, I_{\mathrm{rec}}^{0,\text{`0'}_b}\right\}$ is shown in Fig. 3.4(b).

Of course, using a limited value for R will only produce an attenuation, and not a complete cancellation, of the memory effect. Yet, according to the figure, a value of R slightly larger than 3 is enough to ensure that the converter, when sending a new symbol, is in a state that is almost superimposed with one of the three above identified stable points.

The repetition of the transmitted bits imposes an update of the decoding strategy with respect to the original scheme proposed in [46]. In backward communication the detection is related to the way in which $V_{\mathrm{DS}}(t)$ reaches the zero level. To let such a feature correctly show up, it is suggested to look at the last among the R clock cycles, where the dependence of previously transmitted symbol is attenuated.

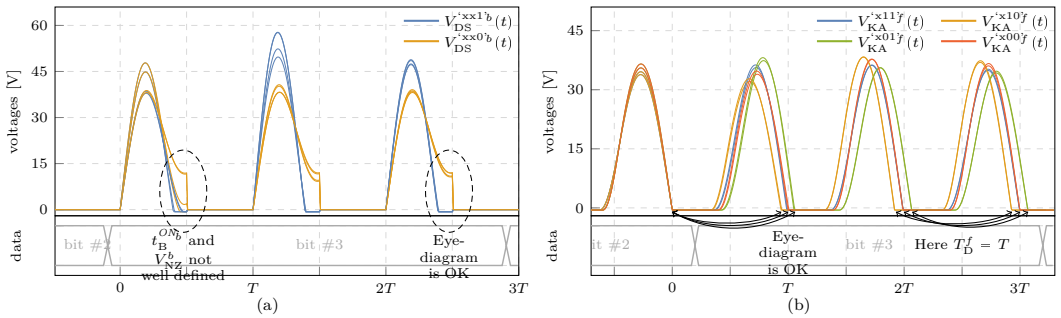


Fig. 3.5 Basic working principle of the decoding. (a) Backward communication. (b) Forward communication.

In forward communication, the decoding is on the $V_{KA}(t)$ and is differential; in this case, it is mandatory to observe the transition between the last clock cycles of the transmission of a symbol, and the first clock cycle in the transmission of the successive symbol.

An example for the backward communication mode is sketched in 3.5(a). The case $R = 3$ is assumed. Any possible combination of three symbols is transmitted from the same initial condition, and only the final part of $V_{DS}(t)$ is shown. The reference time $t = 0$ is set to the rising edge of the clock cycle associated to the first transmission of the third symbol. We refer to waveforms associated to the transmission of sequences ending with symbol '1' with $V_{DS}^{\text{`xx1'}_b}(t)$, and to waveforms associated to sequence ending with '0' with $V_{DS}^{\text{`xx0'}_b}(t)$. From the figure it is clear that the two decoding quantities $t_B^{ON_b}$ and V_{NZ}^b are not well defined in the first clock period (i.e., $t \in [0,T]$ in the figure) of the transmitted bit. Instead, they converge to two well-defined values as the time increases.

The forward communication is considered in 3.5(b). As in the previous case, the transmission of all combination of three symbols is considered. Here the $V_{KA}(t)$ is plotted and the reference time $t = 0$ is set to the rectifying diode turn-on time during the last clock cycle of the second transmitted bit, thus simplifying the evaluation of T_D^f as the first rectifying diode turn-on instant. Using a notation similar to the previous case, it is clear that all $V_{KA}^{\text{`x11'}_f}(t)$ and $V_{KA}^{\text{`x00'}_f}(t)$ are characterized by $T_D^f \approx T$, whereas we have $T_D^f \approx T - \Delta\bar{t}_D^{ON_f}$ for all waveforms $V_{KA}^{\text{`x10'}_f}(t)$, and $T_D^f \approx T + \Delta\bar{t}_D^{ON_f}$) for all $V_{KA}^{\text{`x01'}_f}(t)$. Conversely, even if the choice of the reference time does not allow an immediate evaluation, it easy to see that measuring T_D^f in the following clock cycles brings no information. The reason is that the converter is moving toward a stable state, where $T_D^f = T$. Note that, even if the decoding is performed at the first

clock cycle, waiting R cycles before transmitting a new symbol is fundamental to reset the memory effect, and to allow a successful decoding of the new symbol.

3.4 Proof of concept: design example at high frequency

In this section, we consider the design of a 12 V-to-12 V class-E isolated converter (V_{in} = 12 V, $V_{\text{out}} = 12\,\text{V}$) with bidirectional communication capabilities and an output current $I_{\text{out}} = 175\,\text{mA}$. The resonant converter is designed to operate at a 6.78 MHz frequency, using the transformer made with two inductors illustrated in Fig. 3.3, with quality factor 198, turns ratio 1:1, total inductance $L_{\text{p}} = L_{\text{s}} = 1.47\,\mu\text{H}$. The main MOS switch is a Si2392ADS from Vishay (modeled with a on resistance of $0.1\,\Omega$, and considering $V_{\text{B}}^{ON} = 0.7\,\text{V}$ for its body diode) and the rectifying diode is a Nexperia PMEG6030ELP Schottky barrier (modeled with $V_{\text{D}}^{ON} = 0.55\,\text{V}$ and an ON resistance of $0.1\,\Omega$). The additional MOS used for attaching/detaching C_{inv2} and C_{rec2} is a standard small signal 2N7002. This solution allows to limit the parasitic introduced into the circuit. Capacitors are considered ideal, and by setting $R = 4$, we get the values $C_{\text{inv1}} = 142\,\text{pF}$, $C_{\text{inv2}} = 64\,\text{pF}$, $C_{\text{rec1}} = 178\,\text{pF}$, and $C_{\text{rec2}} = 71\,\text{pF}$. With respect to the straightforward solution of the system, these values have been reduced to take into account the parasitic capacitances added to the circuit by the Si2392ADS, the PMEG6030ELP and the 2N7002, that have been evaluated as 112 pF, 127 pF and 6 pF, respectively. By setting $R = 4$, the communication speed is set to about 1.7 Mbit/s.

The design of the system has been achieved under the assumption that $R = 4$ is enough to reset the memory effect, i.e., that the converter when sending a new symbol is always in one of the three stable states identified above. This simplifying assumption allows us to compute the design quantities as:

1. $t_{\text{B}}^{ON_b}$ and V_{NZ}^{b} the body diode turn-on time and as $V_{\text{DS}}(t_{\text{SW}}^{ON})$ in a system transmitting '1'$_b$ and '0'$_b$, respectively;
2. $\Delta\bar{t}_{\text{D}}^{ON_f}$ is the best fit for the two assumptions: *i*- the time passed between the two rectifying diode turn-on instants (as according to the decoding strategy described in the previous section) when transmitting '01'$_f$ is $T + \Delta\bar{t}_{\text{D}}^{ON_f}$; and

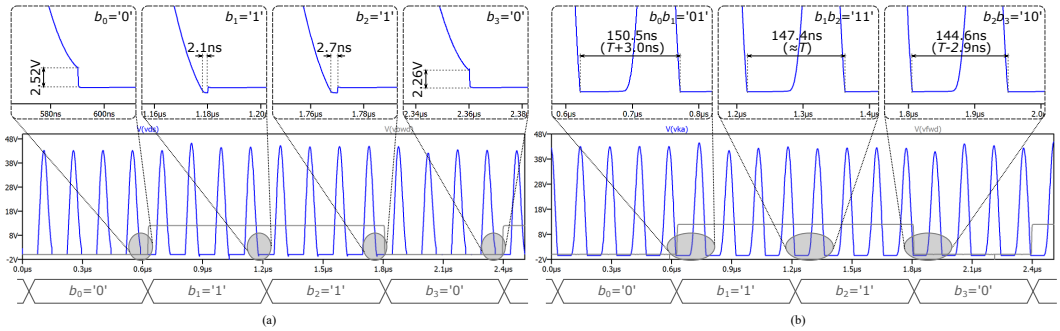


Fig. 3.6 Spice simulation of the proposed design. (a) Backward communication, showing the $V_{\mathrm{DS}}(t)$ and the transmitted symbol. (b) Forward communication, showing the $V_{\mathrm{KA}}(t)$ and the transmitted symbol.

ii- the time passed between the two rectifying diode turn-on instants when transmitting '10'$_f$ is $T - \Delta\bar{t}_{\mathrm{D}}^{ON_f}$;

3. the converter output power (in backward communication mode) is the average value of: *i*- the output power when transmitting '1'$_b$; *ii*- the output power when transmitting '0'$_b$; *iii*- the output power when sending '0'$_b$ for R clock cycle starting from the initial condition $\left\{I_{\mathrm{inv}}^{0,\text{'1'}}, I_{\mathrm{rec}}^{0,\text{'1'}}\right\}$; and *iv*- the output power when sending '1'$_b$ for R clock cycle condition starting from the initial condition $\left\{I_{\mathrm{inv}}^{0,\text{'0'}_b}, I_{\mathrm{rec}}^{0,\text{'0'}_b}\right\}$. In forward communication mode, the converter output power is computed in a similar mode, considering $\left\{I_{\mathrm{inv}}^{0,\text{'0'}_f}, I_{\mathrm{rec}}^{0,\text{'0'}_f}\right\}$ as initial condition in the last case.

While the first two conditions are quite easy to understand, we would like to give more details on the last one. We have implicitly assumed that all four combinations of two symbols '11', '10' '01' and '00' are equiprobable. The transmission of two symbols requires $2R$ clock cycles; we focus here on the power transferred during the last R clock cycle. When sending '00', and recalling the simplifying assumption that the system is capable to reach a stable state point in R clock cycles, the transferred power is given by the quantity at the item *i*. Similarly, the quantity at the item *ii* is the power transferred in the last R clock cycles when sending '11', the quantity at the item *iii* the power when sending '10', and the quantity at the item *iv* the power when sending '01'. The average value of these four quantities is the average power of the converter.

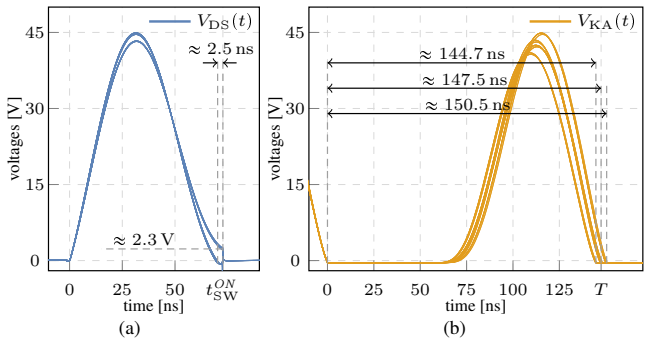


Fig. 3.7 Eye diagrams extracted from a spice simulation. (a) Backward communication. (b) Forward communication.

The proposed design has been obtained by imposing

$$V_{\mathrm{NZ}}^{b} = 2.5\,\mathrm{V},\ t_{\mathrm{B}}^{ON_b} = 3\,\mathrm{ns},\ \Delta\bar{t}_{\mathrm{D}}^{ON_f} = 3\,\mathrm{ns},\ I_{\mathrm{out}} = 175\,\mathrm{mA}$$

The screenshots from a SPICE simulation using realistic models developed by the manufacturer for all active devices is depicted in Fig. 3.6. In both cases of backward and forward communication, we have transmitted a pseudo-random sequence given by the maximum-length linear-feedback shift register (LSFR) of width $\ell = 7$, whose periodicity is $n = 2^{\ell} - 1 = 127$ bits. The figure shows only a portion of the simulation, where the transmitted bits are '0110'. The simulation of the transmission of the entire pseudorandom sequence shows a correct decoding both for backward and forward transmission. The average output current is evaluated in 176.6 mA for the backward communication, and 174.8 mA for the forward communication. Converter efficiency is 92.3% and 91.8%, respectively. As already noted in [46], the efficiency in the forward communication is lower due to higher losses on the MOS body diode.

The eye-diagrams for backward and forward communication extracted from the SPICE simulations are plotted in Fig. 3.7(a) and 3.7(b), respectively. For the backward communication we have considered only the R-th clock cycle in each bit transmission. From the figure, we have $V_{\mathrm{NZ}}^{b} \approx 2.2\,\mathrm{V}$ and $t_{\mathrm{B}}^{ON_b} \approx 2.3\,\mathrm{ns}$ as worst-case conditions. For the forward communication, we have considered the transition between the two clock cycles immediately before and immediately after the change of the transmitted bit. The worst-case condition is $\Delta\bar{t}_{\mathrm{D}}^{ON_f} \approx 2.4\,\mathrm{ns}$. All observed values are very similar to that imposed by using the approximated design procedure described.

3.5 Conclusion

We have reviewed a through-the-barrier communication strategy recently proposed in the literature, that allows the two sides of an isolated class-E resonant converter to communicate with each other by a simple modulation of the energy signal across the main power transformer, and without the need of any other additional isolating devices. In this chapter the case of using a low-k coreless transformer as isolating device is considered, and the effect of the low coupling on the communication is analyzed. With a few modifications with respect to the original work it is still possible to establish a communication channel. Realistic circuit-level simulations of a case study show the possibility to design an isolated converter operating at 6.78 MHz with an additional isolated data channel with almost 2 Mbit/s capacity, and an efficiency of about 92%.

Part II

Wireless Power Transfer

Introduction

This part embarks on a journey through four chapters, each exploring the critical aspects of the design and control of Wireless Power Transfer (WPT) systems. In particular, in Chapter 4 the design of WPT systems based on inductive links is considered and the focus is on recent works where the whole WPT system (i.e. both energy transmitter and energy receiver) is designed as an isolated resonant class-E DC-DC converter characterized by a loosely-coupled transformer. This chapter aims to compare the classic WPT design approach, based on class-E converters, with a new one, based on the class-E design described in part I, that aims to achieve comparable performance with fewer reactive components, thereby reducing system complexity, size, and cost. Notably, this reduction in reactive components enhances performance robustness against variations in the inductive link coupling factor. Its nominal value is of great importance for the design and its measurement results tricky.

Therefore, Chapter 5 focuses on the problem of the experimental measurement of the mutual inductance (or, equivalently, of the coupling factor) of two coupled coils designed for WPT systems. Although many instruments and techniques are available for this purpose, in the literature, no clear guidelines defining the most reliable technique exist, and the vast majority of papers propose ad-hoc measurement approaches without clearly explaining the pros and cons of each specific choice. The contribution of this work is to fill this gap by i) reviewing the available methodologies that can be used to measure the mutual inductance, ii) highlighting the issues that may arise, and iii) identifying the most suitable technique for a particular use case. More specifically, to increase the impact of our analysis, we focus on the case of a couple of WPT coils for biomedical applications designed to work at 6.78 MHz, which is a setting both very common and quite tricky for the direct measurement.

In Chapter 6, the focus is moved to the control of a WPT system, and the primary-side control capability is deeply investigated. In particular, with primary-side control, the possibility to regulate the power delivered to the load at the desired level by only sensing and modifying quantities available at the primary side is defined. It is possible to observe that, when adding a power regulator at the secondary side, the Desired Operating Point, corresponding to the regulator barely ON (and so dissipating negligible energy) while still providing the correct power to the load, is easily detectable at the primary side. The most important novelty of the proposed approach is that it is capable of working without the need for any advanced system modeling and without any estimation of system parameters. The theoretically developed model is verified by measurements on a prototype built upon a 60 mW-class-E-based WPT link working at 6.78 MHz.

Finally, in Chapter 7, the proposed approach has been applied to different state-of-art WPT systems, either inductively or capacitively coupled, in order to improve the generality of the adopted control methodology and to extend its validity beyond the class-E circuit topology considered in Chapter 6.

Chapter 4

A Comparison between Class-E DC-DC Design Methodologies for Wireless Power Transfer

4.1 Introduction

Wireless Power Transfer (WPT) is an emerging technique that aims to replace standard wired power supply in an increasing amount of applications, both industrial and biomedical. Focusing on near field transfer only, two basic WPT methodologies can be identified, namely inductive [41, 87] and capacitive coupling [24, 88]. Based on the magnetic field, the first technique results in fewer adverse effects on the human body with respect to the second one, which is based on the electric field. As a result, inductive coupling is the best choice for WPT biomedical applications. Furthermore, even though circuits based on capacitive coupling can often achieve higher power transfer efficiency than those based on inductive coupling, the performance of the former dramatically drops when the working condition slightly deviates from the nominal one.

We, therefore, focus here on WPT circuits based on inductive coupling and on resonant architectures, that allow higher oscillation frequency and consequently a smaller size of reactive circuit elements. Furthermore, since an inductive link is electrically equivalent to a loosely coupled transformer (i.e., a transformer with a low coupling factor k), we can model WPT systems based on inductive coupling as

isolated DC-DC converters (embedding a low-k transformer), where the transmitter and the receiver play the role of the primary and secondary side, respectively. This allows us to exploit all the know-how on the design of isolated converters in the design of inductive coupling WPT systems. The main challenge of this approach is represented by the low coupling factor k, and by its sensitivity on both coils distance and misalignment, which should be carefully checked in any design. The aim of this chapter is to investigate the properties of two WPT systems based on two different isolated power converter topologies, and, in particular, their robustness with respect to k.

The design of a resonant isolated DC-DC converter, class-E particularly [11], is not straightforward due to the components non-linearity and the number of reactive elements, which typically makes it impossible to find a closed-form solution able to describe the system evolution. As such, the so called sinusoidal approximation technique is commonly adopted [13], with negative consequences both in terms of exactness of the solution, and of the needs of additional components in the circuit topology to make such an approximation justifiable.

It is also important to stress that a class-E converter is usually designed for a given operating condition, which could be either the one ensuring the nominal or the maximum output power. To cope with changes in the coupling factor, or even with different output power, a control methodology among the many presented in the Literature may be applied [39, 33]. However, since this work aims to compare the intrinsic properties of the circuit topologies either in the case of a classical design approach or in a novel one, we consider any control strategy to be applied to the designed converters out of the scope of our investigation.

This chapter is organized as follows. In Section 4.2 we briefly introduce the state of the art of WPT systems based on isolated class-E converter design together with its main issues. In Section 4.3 two class-E DC-DC converters, designed to fulfill typical specifications of a WPT system, are presented. The first one is based on a classic design approach, whereas the second one has been designed according to a novel methodology. In Section 4.4 the system performance against coupling factor variations of the two systems is analysed and compared. Finally, we draw the conclusions.

4.2 State of the art

Inductive links are usually designed to operate at high frequency (i.e. in the MHz range) in order to achieve the desired performance with smaller reactive components (particularly with coupled coils of reduced size). Unfortunately, such an increase in the operating frequency results in increasing losses for conventional hard-switching converters, an issue which is addressed relying on circuits typically used in radio-communication systems and based on soft-switching techniques [10].

More specifically, we focus on the class-E topology, characterized by Zero Voltage Switching (ZVS) and Zero Voltage Derivative Switching (ZVDS). Roughly speaking, ZVS consists of reshaping the voltage waveforms across switches (either controlled, like MOS devices, or uncontrolled, such as diodes) to ensure that they naturally reach the zero level immediately before the switch turn-ON time instant. Additionally, if the zero level is reached with a low derivative, the ZVDS is also satisfied. The achievement of both ZVS and ZVDS is usually considered as the optimal class-E operating condition.

The typical design methodology of class-E WPT separately focuses on the transmitter and the received side. The former is usually composed of a typical RF class-E power amplifier, whose only purpose is to drive the primary coil, which is usually designed to achieve the highest possible efficiency. The latter is independently designed as a harvesting block.

Only recently, new approaches focusing on the co-design of the transmitter and receiver side have been proposed, which allow considering WPT systems relying on inductive links as loosely coupled isolated DC-DC converters in which the transmitter and the receiver are located at the primary and secondary side, respectively [7] [27]. This results in a more efficient design method than separately considering power amplifier, coils, and rectifier.

Here, we aim to compare two of such design methodologies, applied, respectively, to the circuit schemes shown in Figure 4.1 and Figure 4.2, which are analyzed in detail in Section 4.3. The first one is a classic class-E topology, composed by a typical class-E inverter on the left-hand side of the transformer, with the necessary choke inductor and a matching network, and a typical class-E rectifier on the right-hand side, in addition to a second-order filter which is needed before the load. The second

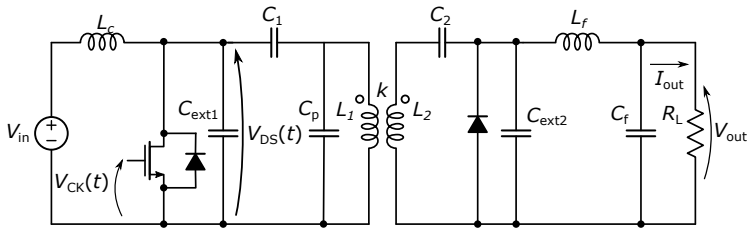


Fig. 4.1 Schematic of the classic isolated class-E converter (that embeds a low-k transformer) taken from [27].

one is a much simpler scheme employing the minimum number of components strictly necessary to build an isolated class-E DC-DC converter.

The first and classic approach relies on the so-called sinusoidal approximation, and it is based on the separate design of the inverter stage (providing DC/AC conversion), and of the rectifier one (in charge of AC/DC conversion), and relies on the assumption that the AC component is made of one single harmonic at the switching frequency f_{SW}. Thanks to this, the rectifier circuit can be linearized and averaged and therefore approximated as an equivalent impedance. With this assumption, one can straightforwardly design the class-E inverter as a single-tone power amplifier loaded by the equivalent impedance of the rectifier at the primary side of the transformer. Since the value of such impedance, which also depends on f_{SW} and k, does not usually lead to the optimal class-E inverter load (i.e. the one ensuring that both ZVS and ZVDS holds for the MOS switch) a matching network, designed to work at that particular working point, is added between the main RF power amplifier and the rectifier.

Note that, for the sinusoidal approximation to be effective, additional filtering circuit elements, such as C_1, L_1 and C_2, L_2 tuned on the first harmonic f_{SW} are required. If these elements are not present, the hypothesis grounding the sinusoidal approximation is no longer supported, and this results in appreciable design errors. In the much simpler topology of Figure 4.2, no circuital elements are introduced to make the sinusoidal approximation reasonable. Therefore, we use the completely different approach proposed in [31] [1] that is based on an exact analysis of the circuit behavior.

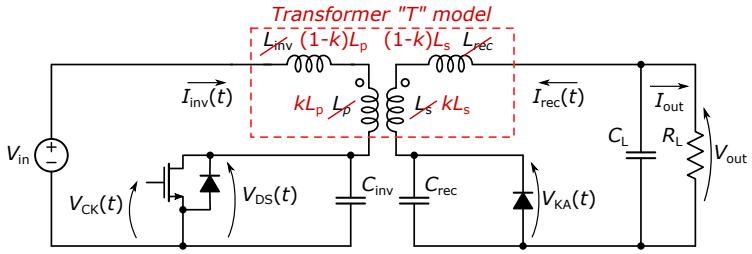


Fig. 4.2 Schematic of the isolated class-E DC-DC converter (black color) and the modification (red color) derived from the novel approach. The low-k transformer leakage inductances are exploited to avoid extra components.

4.3 Class-E Converter designs

4.3.1 Converter specifications

Typical specifications for a loosely coupled class-E DC-DC converter design suitable for a general purpose WPT system are taken from the design example proposed in [27]. The system requires 5 W, with input voltage $V_{in} = 20\,\text{V}$ and $R_{out} = 50\,\Omega$ (so $V_{out} \approx 15.8\,\text{V}$ and $I_{out} \approx 316\,\text{mA}$) operating at the frequency $f_{SW} = 1\,\text{MHz}$. Additionally, the coupled coils result in having a quality factor Q approximately equals to 170 at the nominal frequency and the coupling coefficient is specified to be $k = 0.1$.

4.3.2 Classic Class-E Converter Design

In [27], Nagashima *et al.* present a steady state analysis of the isolated class-E converter outside nominal operation. The key point of the analysis is to transform the classic design of a class-E converter, whose schematics is shown in Figure 4.1, into a typical topology of the class-E inverter: this is somehow equivalent to the classic circuit design methodology previously mentioned.

The class-E inverter is made of a choke inductor L_C, a MOSFET as an active switching device, and three capacitances C_{ext1}, C_1, C_p, which are used to achieve series resonance and impedance transformation. On the other hand, the class-E rectifier consists of a series resonant capacitance C_2, a diode as a non-controlled switching device, an external shunt capacitance C_{ext2}, a second-order low-pass filter $L_f - C_f$ and a load resistance R_L. The two circuits are then connected together by

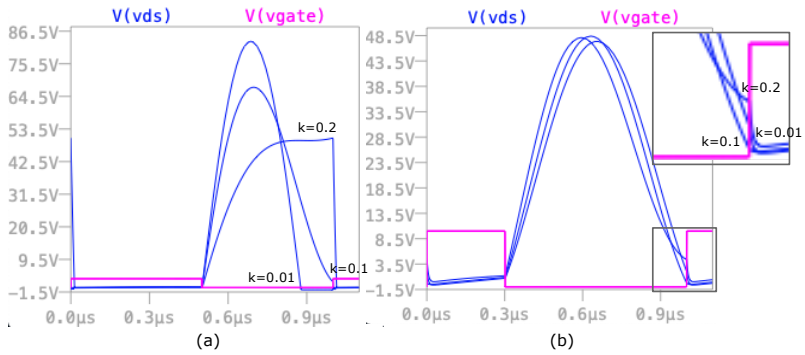


Fig. 4.3 Spice simulations of the proposed designs showing ZVS or quasi-ZVS for three different values of the coupling factor: $k = 0.01$, $k = 0.1$ and $k = 0.2$. (a): voltage across the MOS with respect to the gate control voltage according to the classical approach. (b): voltage across the MOS with respect to the gate control voltage according to the alternative approach. The top right square box represents a zoom at the clock edge to better distinguish the waveforms.

an isolation transformer modeled with two coupled coils L_1 and L_2 with coupling coefficient k.

Regrettably, the major contributions of losses are not taken into account in order not to entangle the analysis. Therefore, the parasitic resistances and the diodes forward voltage drops are assumed to be small enough not to affect the circuit waveforms. As a matter of fact, the dissipated power which occurs in the ESRs, the MOSFET on-resistance and body diode, and diode in the rectifier can only be a-posteriori evaluated. The theoretical analysis, which has also been experimentally validated leads to the following list of components values: $L_1 = 23.1\,\mu\text{H}$, $r_{L_1@1\,\text{MHz}} = 0.891\,\Omega$, $L_2 = 22.7\,\mu\text{H}$, $r_{L_2@1\,\text{MHz}} = 0.829\,\Omega$, $L_C = 284\,\mu\text{H}$, $L_f = 303\,\mu\text{H}$, $C_{\text{ext1}} = 713\,\text{pF}$, $C_1 = 836\,\text{pF}$, $C_p = 434\,\text{pF}$, $C_2 = 1.34\,\text{nF}$, $C_{\text{ext2}} = 2.80\,\text{nF}$, $C_f = 8.35\,\text{nF}$.

The main MOS switch in the design presented in [27] is a SUD06N10-225L from Vishay, switching with a duty cycle $D = 0.5$, and the rectifying diode is a STPS5H100B, a Schottky barrier diode from STMicroelectronics. A screenshot of the drain-source voltage of the MOS switch $V_{DS}(t)$ taken from the Spice simulation is shown in Figure 4.3(a). From the figure, it can be clearly seen that, for $k = 0.1$, the voltage features quasi-ZVS when the MOS turns on. The slight deviation from the ZVS condition, even for the nominal coupling factor value, is due to the simplifying assumptions on which this classic methodology leans on.

4.3.3 Alternative Class-E Converter Design

The simplified circuit of Figure 4.2 features a simpler architecture by reducing the number of passive components required, as only the coupled coils, two resonant inductors (L_{inv} and L_{rec}) and two resonant capacitors (C_{inv} and C_{rec}) are required. Both L-C filters and the large RF choke inductor have been removed. Due to this, the standard sinusoidal approximation cannot be used for its design. We rely its design on an innovative procedure first proposed in [31] and improved in [1] that is based on the exact analysis of the differential equations regulating the converter evolution, and possibly due to the low number of reactive elements in the circuit. Note that, being this analysis exact, it allows a much more accurate design with respect to the previously considered approximated one. Additionally, this procedure is capable of taking into account the main sources of non-idealities like the losses on the reactive elements, on the MOS switch, and on the rectifier diode.

The low-k transformer embedded in the converter is modeled according to the 'T' model, with a coupling factor k and two inductances L_p and L_s at the primary and secondary side, respectively. As in [4], being the coupling coefficient very low, the two large leakage inductances $(1-k)L_p$ and $(1-k)L_s$ (in red in Figure 4.2) can be exploited to take the place of the original resonance ones L_{inv} and L_{rec} (in black in Figure 4.2), while kLp and kLs work as a perfectly coupled transformer. This allows a further reduction in the reactive elements counts, as only the coupled coils and two capacitances C_{inv} and C_{rec} are now required.

Therefore, we configure the transformer to have, for the sake of simplicity, a turn ratio $n_p/n_s = 1$, as well as the transformer of Nagashima *et al.* in [27], and we focus on the solution which allows $L_{inv} = (1-k)L_p$ and $L_{rec} = (1-k)L_s$. While the inductors have been considered to have a quality factor equals to 172, we assume the capacitors to be ceramic with high quality dielectric (e.g., C0G) and therefore with negligible ESR (quality factor $Q > 1000$). For a fair comparison with the classical design approach, which will be carried on in the next section, the main MOS switch is again a SUD06N10-225L (modeled, according to the data-sheet, with an ON resistance $R_{DS}^{ON} = 0.16\,\Omega$ and a forward voltage for the body diode $V_B^{ON} = 0.9\,\mathrm{V}$) and the rectifying diode is a STPS5H100B, (modeled according to the data-sheet with a forward voltage $V_D^{ON} = 0.73\,\mathrm{V}$). The last available degree of freedom for the class-E design is the duty cycle D of the main clock. According to [1] and [37], $D = 30\%$ has been chosen in order to reduce the voltage stress $V_{DS}(t)$ across the main switch.

The lower peak value of the $V_{DS}(t)$ can be clearly appreciated in Figure 4.3. Notice that, if the purpose of the work had not been the two-methodologies comparison, this would have led to a better choice of the values of the active components, particularly a more suitable MOS transistor, guaranteeing better circuit performance.

By putting the latter data into the model developed in [1], the desired design is achieved for $C_{inv} = 32.9\,\text{nF}$, $C_{rec} = 36.3\,\text{nF}$ and $L_p = L_s = 688.7\,\text{nH}$. A screenshot of the voltage $V_{DS}(t)$, taken from the Spice simulation, is shown in Figure 4.3(b) where it can be clearly seen that for $k = 0.1$ the voltage exactly reaches the zero voltage level just before the MOS turn-ON instant (ZVS). As described in [1], if k is too low, it is not possible to satisfy both ZVS and ZVDS unless we add an additional inductance. It is worth noting that the beneficial effects deriving from ZVDS are less relevant than the negative consequences deriving from the addition of an extra passive component in terms of power loss, size, and cost.

4.4 System performance against coupling factor variations

In a WPT system, the coupling factor, which depends on coils distance, misalignment, and transfer medium, strongly affects the system behavior. Since the design cannot rely on k, these resonant systems must be improved either by modifying the circuit topology or by adding a feedback in a way that they become k-resilient at least in a certain range.

In this particular case study, for a fair comparison with [27], no feedback has been considered and the same input/output specifications, as well as the same active devices, have been used. The coupling factor k has been varied from $k = 0.01$ to $k = 0.2$, i.e. from the 10% to the 200% of the nominal value. The consideration of higher k values is not of practical interest in WPT being $k = 0.2$ already difficult to achieve according to [7] and [89].

For $k \neq 0.1$, but in the range $[0.01, 0.2]$, we can say that the system designed according to the alternative methodology, slightly deviates from the sub-optimal condition (ZVS only) and features quasi-ZVS by either reaching an acceptable positive value of $V_{DS}(t)$ at the MOS turn on instant t_{SW}^{ON}, i.e. $V_{DS}(t_{SW}^{ON}) < 4.4\,\text{V}$, or by reaching a negative value greater than the MOSFET body diode forward voltage drop,

i.e. $V_{DS}(t_{SW}^{ON}) > -0.9\,\mathrm{V}$. On the other hand, the classical approach just guarantees quasi-ZVS for $k < 0.1$ (either by turning the MOS body diode on or by reaching an acceptable positive $V_{DS}(t_{SW}^{ON})$ value) and heavily deviates from the sub-optimal condition when $k > 0.1$. To this purpose, in Figure 4.3 the Spice simulations for both design methodologies are depicted in order to show what happens to the voltage across the main switch $V_{DS}(t)$ for the nominal value $k = 0.1$ and for $k = 0.01$ and $k = 0.2$, corresponding to the minimum and maximum coupling factor considered.

The importance of the exact analysis can be appreciated not only because it allows reaching exact ZVS condition, but also because it avoids the use of a matching network, which can provide impedance transformation for just one single specific working point (and so for only one specific k value). Thanks to this, the $V_{DS}(t_{SW}^{ON})$ features k-resilience in a broader coupling factor range by reducing the ZVS condition degradation when the system is designed according to the alternative methodology.

By indicating with the notation $\langle f(t) \rangle$ the average value of $f(t)$ over one period, Figure 4.4(a), derived from Spice simulations of the circuits of Figure 4.1 and Figure 4.2, shows how the efficiency of the two converters η, calculated as $\eta = \langle P_{out} \rangle / \langle P_{in} \rangle$, varies as a function of k. Nagashima *et al.*, as it is shown by the yellow curve of Figure 4.4(a), obtain an efficiency vs coupling factor curve which has the classical tiny bell shape, which confirms a maximum value $\eta \approx 84\%$ at the nominal coupling coefficient $k = 0.1$ and that quickly decreases as k moves away from the nominal point.

On the other hand, the simplified circuit according to the alternative class-E design features an efficiency $\eta \approx 78\%$ at the nominal coupling factor and it stays above the latter value when $k > 0.1$. The efficiency curve of this design is represented by the blue curve in Figure 4.4(a).

The conclusion which derives from the efficiency analysis is consistent with Figure 4.3 that shows the higher sensitivity to the coupling factor for the classical design with respect to the alternative one.

Another important difference between the two circuits regards the way the output power $\langle P_{out} \rangle$ changes with the coupling factor. In the simplified topology, as depicted by the blue curve in Figure 4.4(b) and, contrarily to what happens in the classic design (yellow curve), the power delivered to the load monotonically increases when k increases. Again, since in the classical design methodology the class-E converter is strictly tuned to work just for the designed coupling factor $k = 0.1$, as k changes, the

reflected impedance at the primary side is not the optimal one anymore and the power delivered to the secondary side, as well as the one absorbed by the load, decreases. As a matter of fact, the resonance frequency at the primary side deviates from the desired one f_{SW} so that, the ZVS which guarantees the sub-optimal soft-switching condition is lost. The immediate consequence is that the switching power loss at the primary side increases.

Nevertheless, in both cases when k changes, the desired output power $\langle P_{out} \rangle = 5\,\mathrm{W}$ is not guaranteed anymore but, the circuit designed according to the alternative approach is theoretically able to feed the load even for $k > 0.1$.

It is important to point out that the increase of the output power (when the coupling factor increases) can be an enormous advantage in industrial applications such as battery charging or power delivery but, it can be an issue in biomedical applications such as implantable devices, in which the secondary circuit is often located inside the human body and therefore an excess of power can be dangerous (due to the heat generated in the biological tissue). This is one of the reasons why, in conventional class-E solutions, to cope with coupling factor variation, information from the secondary side is needed, which is usually sent back to the transmitter through telemetry. By exploiting the exact design methodology, a very simple technique, which does not need any feedback from the transmitter side has been proved in [7] by making this converter suitable even for biomedical implants. This reduces the complexity of the circuitry, as well as the size and the power overhead, and theoretically lets the converter work at the maximum efficiency for any k value.

4.5 Conclusion

In this chapter, two WPT systems based on the design of a low-k class-E isolated DC-DC converter have been considered. In particular, two different design methodologies have been compared: a classical one based on strong simplifying assumptions and a novel one based on an analytical approach that recently appeared in the Literature. The performances have been evaluated against coupling factor variations.

The result is a comparable efficiency for the two systems when k is less than the nominal one, whereas the novel approach achieves better performance when k is greater than the nominal one. As a matter of fact, the avoidance of the matching

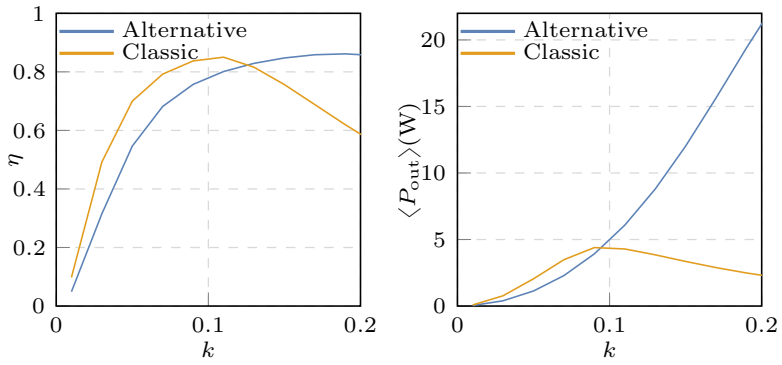


Fig. 4.4 Comparison of the performances between the two class-E DC-DC converter design methodologies against coupling factor variation. (a): efficiency of the converter calculated as $\langle P_{\text{out}} \rangle / \langle P_{\text{in}} \rangle$; (b): power absorbed by a resistive load $R_L = 50\,\Omega$

network, as well as the other extra reactive components, has a twofold advantage. Firstly, it results in ZVS satisfaction in a broader k range, and secondly, it allows a significant reduction in the number of reactive components required, affecting the size and cost of the circuit.

The output power study, which has also been investigated, shows that the two circuits behave in a different way making the choice between the two application-dependent.

Chapter 5

Mutual Inductance Measurement in Wireless Power Transfer Systems Operating in the MHz Range

5.1 Introduction

Wireless Power Transfer (WPT) systems gained increasing attention in recent years and in many areas. For biomedical applications, they represent a viable alternative to overcome issues deriving from the use of implanted batteries, i.e., size, longevity and bio-compatibility. Especially for systems where external and implanted devices are located in close proximity of each other, WPT relies on inductive coupling in which one coil is placed immediately outside the human body and the other inside it, giving rise to a near-field coupled inductance system.

The design of WPT system is always rather challenging. As an example, for biomedical applications[89–92], an immediate issue is related to the operating frequency trade-off. In fact, attenuation of the medium (e.g., the biological tissue between the coils) is roughly increasing with the operating frequency, and it is desirable to maintain it as low as possible. Conversely, the use of a high frequency is important to keep the coils sufficiently small to be easily implanted, especially for invasive applications, such as neurostimulators. One of the most common solutions for this trade-off is to set the nominal operating frequency within the ISM band centered at 6.78 MHz or 13.56 MHz [93, 94].

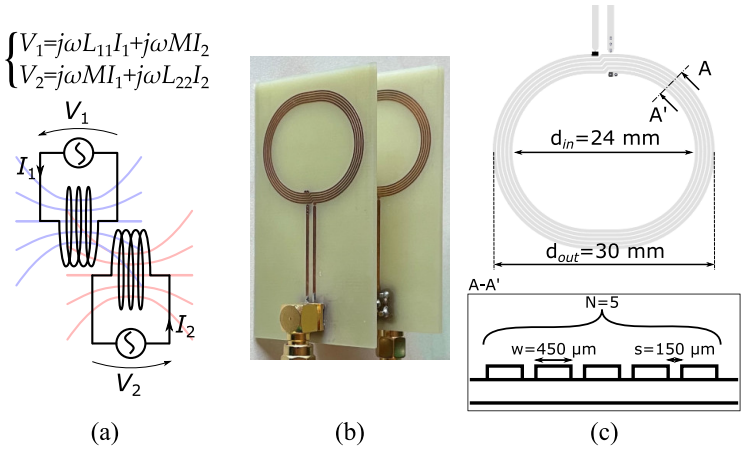


Fig. 5.1 (a) Two inductively coupled coils in a WPT system, mathematically described by the system of equations shown at the top. Assuming the two coils are coreless and not perfectly aligned, the electromagnetic fluxes are not completely concatenated. (b) Picture of the two spiral PCB-printed coils used a reference case. (c) Geometrical characteristics of the coils.

In these settings, the measurement of the self-inductance of the coils is usually simple. Conversely, the measurement of the mutual inductance M (or equivalently, of the coupling factor k) typically represents a tricky task, in particular for a loosely coupled coils system. The main problem, as detailed in the following, is due to the parasitic elements introduced by the measuring system, which are typically negligible with respect to the self-inductance value, but not with respect to the mutual inductance one.

Indeed, many reasons suggest that the mutual inductance M must be carefully evaluated, not only because it affects both the link gain and the load received power, but also because it features a strong sensitivity with respect both to the medium attenuation and to the coils distance and misalignment. If we also consider that many WPT systems are designed with resonant circuits [5] [89, 27, 95, 96] whose behaviour strongly depends on all circuit parameters, the appropriate knowledge of M is even more fundamental. Of course, it is possible to base the circuit design on the expected system parameters (including M) estimated by means of accurate electromagnetic simulation results. However, this may not take into account all parasitics and medium effects existing in a realistic environment. Due to all the above observations, the verification of the system characterization with direct measurement is of paramount importance [97, 98, 89, 99].

The main contribution of this tutorial is to tackle this issue by reviewing established methodologies for conducting such measurements while also shedding light on potential challenges that might emerge. As far as our understanding goes, the existing literature lacks such a comprehensive analysis. To make our analysis more practical, we focus on a case study of a couple of WPT coils for biomedical applications designed to operate at 6.78 MHz and around 100 mW [100].

This chapter is organized as follows. In Section 5.2 the considered model for the coupled coils is proposed, and the state of the art about the available methodologies to measure M is explored. In Section 5.3 we perform the measurement of M on a coupled coils system built to work at 6.78 MHz. In particular, we compare the direct measurement obtained with a Vector Network Analyzer (VNA) to the ones performed with an LCR meter. Finally, we draw the conclusion.

5.2 Coupled coils model and State of the art

Formally, when two (or more) coils are in proximity of each other, the magnetic field generated by one coil interferes with the other one(s), as sketched in Fig. 5.1(a). Modeling the system as a (loosely coupled) transformer may prove helpful in the analysis of the circuit [5, 7][101, 27, 102].

In the phase-vector domain, and neglecting parasictics, one can write

$$\begin{aligned} V_1 &= j\omega L_{11} I_1 + j\omega M I_2 \\ V_2 &= j\omega M I_1 + j\omega L_{22} I_2 \end{aligned} \tag{5.2.1}$$

where M is the mutual inductance, L_{11} and L_{22} are the two self-inductances, and $V_{1(2)}$ and $I_{1(2)}$ are the phase vectors of the input (output) port voltages and currents. While L_{11} and L_{22} are constrained to be positive, M (or equivalently, k) can be either positive or negative[1] according to an in-phase or out-of-phase coupling, respectively. The coupling factor k is defined as the dimensionless quantity $k = M/\sqrt{L_{11}L_{22}}$.

Eq. (5.2.1) is typically used for the sake of simplicity, thus keeping the underlying mathematical model as simple as possible. Indeed, the real behaviour is much more complex and results, if one wants to use (5.2.1), in each term of the model being a

[1] Actually, $M = 0$ is also acceptable, indicating that there is no interaction between the coils.

non-linear function of the frequency. In general, each parameter value is constant at low frequencies and rapidly increases around the so-called self-resonance frequency (SRF). As a consequence, inductances in (5.2.1) are generally described with a low-frequency value and by a SRF value that limits the validity range of the model.

As already said, validation by means of real measurements of both the low-frequency values and of the SRF is fundamental. Yet, among all parameters in (5.2.1), the evaluation of M (i.e., both its low-frequency value and SRF) is more problematic since WPT systems are generally based on loosely coupled coils, with a relatively low value of M (i.e., $M^2 \ll L_{11}L_{22}$). The main problem here is that, when an instrument is set up for the correct measurement of L_{11} and L_{22}, its parasitics are kept negligible with respect to both L_{11} and L_{22}, but may strongly affect the measurement of M if k is small. Additionally, the measurement system may not be optimized for the desired frequency range.

In particular, operating frequencies commonly used in biomedical WPT systems represent a difficult setting as they are at the same time, too low for standard radio-frequency (RF) measurement techniques, and too high for low-frequency or quasi-stationary ones [103]. Yet, little or no attention is given in the literature to these aspects, and many papers can be found suggesting one method or another one [104, 105], without paying attention to their limitations.

Since the first mutual inductance modeling study [106], many results have been achieved both in modeling and measuring the mutual inductance of an inductive link [107–111, 98, 89]. Limiting ourselves to measurement techniques, and neglecting methods employed either in primary metrology (e.g., *three-voltmeter technique* [112]) or that need ad-hoc circuits (e.g., a compensation network in [113] or a whole resonant circuit in [114, 115]), the approaches known in the literature can be grouped into two main classes, according to the required measurement instrument:

a) approaches based on VNA and on the scattering matrix evaluation [105, 104, 116];

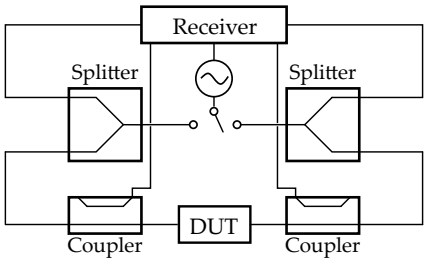
b) approaches based on LCR meter such as the series-antiseries technique [117, 118] (and the dual parallel-antiparallel one [117], not considered here due to space reasons), the direct measurement technique [119] and the one relying on the Z-matrix evaluation [120].

In the following, we detail these methodologies with the help of a reference case. The basic assumption for all these approaches is that the precision of the instrument is high enough to neglect error propagation in all measurement processing steps. Nevertheless, parasitics introduced either by the connection with the instrument ports or by the instrument itself limit the frequency application range of the approach.

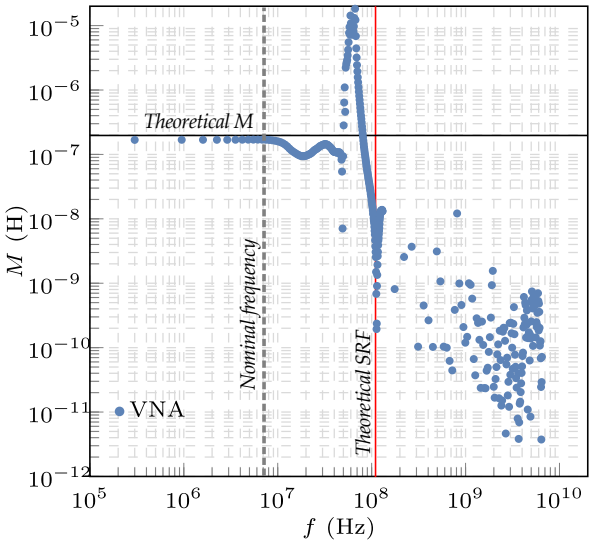
5.3 A case study: Measurements on WPT coils for Biomedical Applications

We consider a system composed of two spiral-shaped printed circuit board (PCB) coils as in Fig. 5.1(b). The coils have been printed over a standard 1.6 mm board with FR4 substrate with a 35 µm copper plating, and are designed for a WPT system operating in the ISM band centered at 6.78 MHz (i.e., the nominal frequency adopted in many WPT systems) and around 100 mW (i.e., the typical power of inductive WPT biomedical implants). Each coil has an inductance of $L_{11} = L_{22} \approx 1.47\,\mu\text{H}$ with a quality factor $Q \approx 50$ at the nominal frequency. The coils have been placed in front of each other at a nominal distance of 13.5 mm, obtaining a 1:1 loosely coupled transformer. Geometrical properties of the coils are detailed in Fig. 5.1(c).

The theoretical electromagnetic model of this structure has been analytically derived in [89]. Nonetheless, the same results can be also achieved with multiphysics software (e.g., ADS by Keysight and Q3D by Ansys) in which the 3D structure can be imported and simulated. Accordingly, M (at the nominal frequency and distance) results to be $\approx 153\,\text{nH}$ ($k \approx 0.1$). Intrinsic parasitic capacitances set the theoretical SRF to be $\approx 110\,\text{MHz}$. If however, for any reason, the electromagnetic simulation does not take into account all intrinsic parasitics, the theoretical SRF can result much higher than the real one. So, to validate the SRF and the M model, measurement is necessary. However, it is important to notice that even the introduction of parasitics in the measurement setup can result in a wrong measurement (and in particular of the SRF). Therefore, careful handling of both theoretical and measured results is required, and reasonable accurate conclusions are drawn when the theoretical and measured results overlap.



(a)



(b)

Fig. 5.2 (a) VNA basic block scheme. (b) VNA measurements obtained with a Keysight P9371A (blue dots). The black and red straight lines show the theoretical values of M and of the self-resonant frequency (SRF), respectively. The dashed gray line indicates the nominal working frequency.

5.3.1 VNA measurements

The VNA is an electronic instrument that estimates the scattering matrix S by measuring the power of the incident and reflected waves. Once S is known, the Z matrix can be easily obtained by performing a simple S-to-Z conversion[2]. The values of L_{11}, L_{22} and M can then be obtained from the imaginary part of the Z matrix according to (5.2.1).

The simplified block diagram of a typical two-port VNA is shown in Fig. 5.2(a). A variable frequency signal waveform is generated within the VNA and it is delivered

[2]The characteristic impedance Z_0 of the line is the only extra parameter needed for the conversion.

to the Device Under Test (DUT), assumed as a two-port circuit represented by the coaxial connectors in Fig. 5.2(a). The power of the incident and reflected waves at both ports of the DUT are alternately measured by toggling an internal switch, as illustrated in the figure. After the switch, the generated wave flows through a splitter, with the twofold purpose of providing a reference signal to the receiver and allowing the generated waveform to flow into the DUT. Additionally, two directional couplers are connected to both DUT ports. The first one collects the fraction of power that is reflected by the DUT. Instead, the power that passes through the DUT is collected by the second directional coupler. Matrix S is provided by the receiver, which compares, for both switch positions, the incident and reflected waveforms collected by the two couplers with the reference one coming from the splitter. To characterize two coupled coils by means of a VNA, one simply needs to connect each coil to a port and the instrument directly provides the corresponding S matrix. The main problem of this approach is that the majority of mid-price range VNAs are generally designed to correctly work at microwave frequencies: in the most common implementation, couplers are made by waveguides that resonate in a suitable RF range, only. Hence, it is quite difficult to get high accuracy measurements in the ISM band centered either at 6.78 MHz or 13.56 MHz. Notwithstanding the above issue, several works in the literature suggest this approach, irrespective of the WPT application and frequency of operation [104, 105].

Measurements of M for the case-study system by means of the Keysight P9371A VNA are shown in Fig. 5.2(b) in the whole frequency range of operation for the instrument as declared by the manufacturer, i.e. $[300\,\text{kHz}, 6.5\,\text{GHz}]$[3]. Experimentally, measurements are in quite good agreement with the theoretically expected results at low frequencies (up to approximately 5 MHz), but matching becomes quite poor before approaching the SRF frequency either because some parasitics are not taken into account in the analytical model or because of the introduction of parasitics by the instrument (or the instrument setup) itself.

5.3.2 LCR meter measurements

The LCR meter, also known as *bridge*, is specifically designed for the low-frequency measurement of impedances with arbitrary phase angles. The impedance definition

[3]Notice that, despite the wide bandwidth, the VNA manufacturer does not provide any accuracy details below 10 MHz.

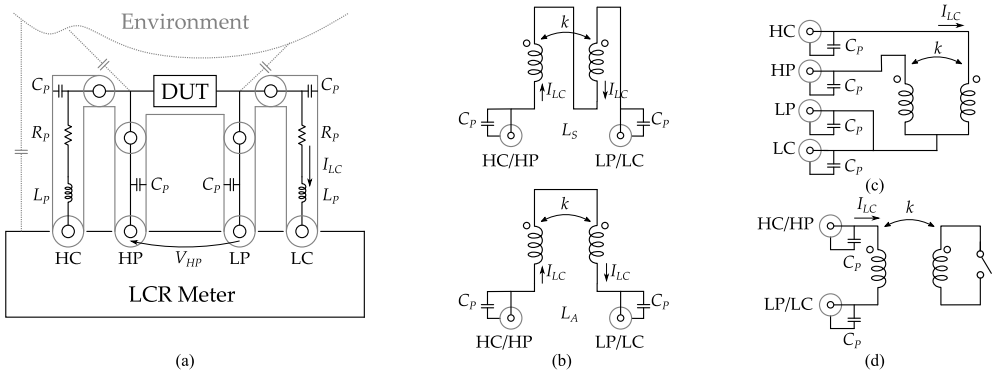


Fig. 5.3 (a) LCR basic block scheme. (b) LCR indirect method: series (L_S) and anti-series (L_A) configuration. (c) Direct method for the measurement of M, consisting in a single self-inductance measurement. (d) Z-matrix method for the measurement of M, consisting in three 1-port measurements of the impedances Z_{1o2}, Z_{2o1} and either Z_{1s2} or Z_{2s1}.

employed by the bridge is dependent on its accuracy class, the best one of which uses a 4-port one [121]. As a matter of fact, the four terminal-pair impedance definition is the most complete one used in electrical metrology. The four ports are generally labeled as High Current (HC), High Potential (HP), Low Potential (LP), and Low Current (LC).

An external *fixture* is typically required for being able to connect the DUT to the four LCR ports. As an example, the typical connection of a 2-terminal DUT to a 4-port LCR meter is shown in Fig. 5.3(a). The four ports are assumed to be coaxial pairs, and the shield is highlighted in grey in the figure. The DUT is excited by injecting a current at port HC, that is measured as I_{LC} at port LC. Conversely, no current is flowing through ports HP and LP, that are used to measure the voltage at the DUT by imposing $V_{\mathrm{LP}} = 0$ and by measuring the voltage V_{HP} at port HP. The impedance of the DUT is then computed as $Z = V_{\mathrm{HP}}/I_{\mathrm{LC}}$.

Thanks to this definition, the LCR meter is able to reject the influence of both the stray resistances and stray inductances labeled as R_P and L_P in Fig. 5.3(a), respectively. Furthermore, also the stray capacitances C_P introduced either by the LCR meter or by the fixture do not theoretically influence the measurement. Capacitances at the HP and HC ports are both driven by the current injected at the HC port and have no influence on I_{LC} and V_{HP}, whereas the ones at the LP and LC ports are virtually shorted by the LCR internal feedback [117]. Additionally parasitics can be compensated by means of OPEN, SHORT, and LOAD corrections,

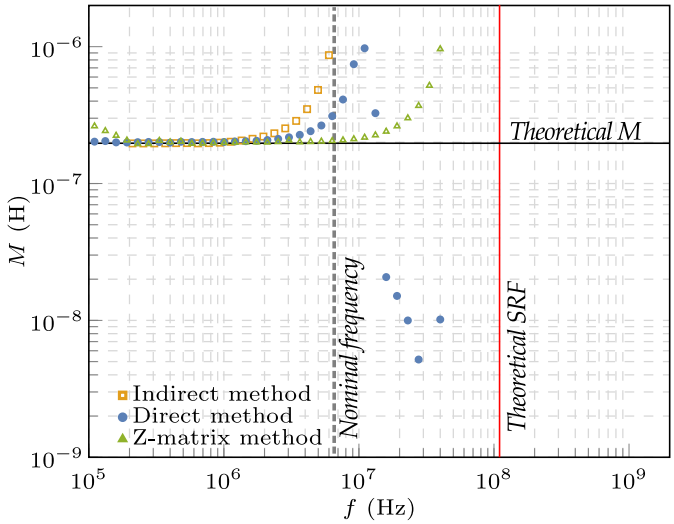


Fig. 5.4 LCR measurements performed according to the three different considered methodologies. The indirect method (in yellow) is performed by means of an HP 4192A. The direct method (in blue) and the Z-method (in green) are performed by means of an Agilent 4294A. The black and red straight lines show the theoretical values of M and of the self-resonant frequency (SRF), respectively. The dashed gray line indicates the nominal working frequency.

available on high-end instruments [119]. Performance is limited at high frequency by the parasitic capacitances between the DUT and the environment.

As already mentioned, this technique can be employed to perform different kinds of mutual inductance measurement which are described in detail in the following.

Indirect method (Series/Antiseries)

the mutual inductance can be indirectly derived from the direct measurement of the self-inductance in the series and antiseries configurations shown in Fig. 5.3(b). Since the series connection leads to $L_S = L_{11} + L_{22} + 2M$, and the antiseries one leads to $L_A = L_{11} + L_{22} - 2M$, the mutual inductance can be calculated as $M = (L_S - L_A)/4$. An equivalent dual measurement approach exploiting a parallel-antiparallel is also possible, but it is not considered here.

Measurements obtained with the 5 Hz-to-13 MHz Keysight/Hewlett-Packard 4192A Impedance Analyzer are shown as the yellow squares in Fig. 5.4 together with the indication of the theoretical M value (dark solid line) and SRF (red solid line). The inductance measurements at low frequency are in good agreement with

the expected value, but the resonance is observed at a frequency much lower than the expected one, as low as the 6.78 MHz operating frequency we are interested in (dashed gray line). As a matter of fact, the upper validity limit of this approach barely goes above one MHz.

The limitation of this methodology is due to the inductances and the stray capacitances of the two (different) custom fixtures required to connect the two coils in the series (to measure L_S) and antiseries (to measure L_A) configuration. The problem is twofold. On the one hand, being the fixtures different (a different connection is required), the parasitics are also different and do not compensate when computing $L_S - L_A$. On the other hand, it is not possible to force the compensation by means of the OPEN, SHORT, and LOAD correction capabilities, as these states are well defined for a single impedance, but not for a connection of more impedances.

Direct method

by connecting the coupled coils as shown in Fig. 5.3(c), the mutual inductance value is directly obtained from the self-inductance measurement of the shown topology. As a matter of fact, when the test current flows from HC through the primary winding, the secondary voltage is measured at HP so that $V_{\mathrm{HP}} = j\omega M \cdot I_{\mathrm{LC}}$.

Measurements in this configuration have been taken with a Keysight/Agilent 4294A Precision Impedance Analyzer, with 110 MHz upper frequency limit, that is much higher than the previously considered one. Results are shown as the blue circles in Fig. 5.4 and are clearly not very different from those observed in the previous case.

The main problem of this method is given by the stray capacitance seen at the HP port, that is virtually connected in parallel to the inductance M. In fact, in this configuration, the instrument forces a current I_{LC} flowing in one coil (i.e., the one connected to HC), but it does not inject any current in the other coil (i.e., the one connected to HP). As a consequence, C_P at the HP port is charged by the current due to the concatenated flux, by therefore altering V_{HP} and the measurement of M.

The expected result is the anticipation of the SRF, which is shown in Fig. 5.4. The upper frequency limit of this approach is slightly higher, but still comparable, to what was observed in the previous case, despite the larger bandwidth of the considered instrument.

Z-matrix method

this method is very similar to that adopted by Suzuki in [122] for calibrating four-terminal pairs admittance standards and the measurement of Z was achieved by adopting one-port VNA measurements, only. The very same procedure can be applied also to LCR meters as in Fig. 5.3(d), and consists in three (or four) one-port measurements Z_{1o2}, Z_{2o1}, Z_{1s2} and/or Z_{2s1}. The notation Z_{1o2} (Z_{2o1}) indicates the impedance at the primary (secondary) port when the secondary (primary) is open-circuited, whereas Z_{1s2} (Z_{2s1}) indicates the impedance at the primary (secondary) port when the secondary (primary) is short-circuited. Note that $Z_{1o2} = j\omega L_{11}$ and $Z_{2o1} = j\omega L_{22}$ in (5.2.1). The value of M is derived in [120] by directly applying the Z-matrix definition to a two-port circuit, and can be easily demonstrated to be $M = \sqrt{(Z_{1s2} - Z_{1o2}) \cdot Z_{2o1}}/\omega$ or $M = \sqrt{(Z_{2s1} - Z_{2o1}) \cdot Z_{1o2}}/\omega$.

Measurements with this approach have been performed by means of the Keysight/Agilent 4294A. Results are shown as the green triangles in Fig. 5.4. With respect to the two previously considered cases the range of validity of the measurements is almost one order of magnitude higher, even though we are still quite far from the expected 110 MHz SRF[4].

The advantage of this methodology lies in its simplicity as it reduces in evaluating the Z matrix of a two-port circuit through one-port measurements only, enabling the capacity of parasitic corrections allowed by high-end instrumentation. Furthermore, no additional fixtures are required (which were conversely necessary in the series/antiseries case), limiting the introduction of parasitic elements. This is the reason why this approach has been shown to be the most reliable one. Measurements are in agreement with the theoretical expected results up to approximately 20 MHz. For the sake of clarity, all the main characteristics of the analyzed methodologies are summarized in Table 5.3.1.

5.4 Conclusion

In this chapter, we have reviewed the available methodologies that can be in principle used to measure the mutual inductance of coupled coils in WPT applications that

[4]Measuring such value would indeed not be possible with the Keysight/Agilent 4294A as it coincides with the upper limit of the instrument bandwidth.

Table 5.3.1 Comparison of the examined methodologies

Instrument	VNA	LCR		
Methodology		Indirect	Direct	Z-matrix
Model	Keysight P9371	HP 4192A	Agilent 4294A	Agilent 4294A
N° of Measures	one	two	one	two
Validity up to	≈ 5 MHz	≈ 1 MHz	≈ 10 MHz	≈ 20 MHz
Ad hoc fixture	no	yes	yes	no

adopt either the VNA or the LCR meter. It is important to note that our intention was not to assert which techniques can be universally employed and deemed superior to others, but rather to comprehensively understand the potential issues that can arise during these measurements. This knowledge can be used to carefully interpret the results and helps to understand the most appropriate methodology for a given case study. We have shown that mid-price range VNAs do not always provide accuracy details below a certain frequency, although they can outperform some techniques employing the LCR meter. Despite limitations in LCR-meter methodologies, the Z-matrix method stands out as the most suitable technique both for its simplicity and validity in a wider frequency range.

Chapter 6

A Primary-side Control Solution in Wireless Power Transfer Systems: Theory and Validation

6.1 Introduction and State of the art

Wireless Power Transfer (WPT) refers to a wealth of energy transfer techniques that have found employment in a large variety of applications, from low-power portable electronic devices [123–125], to medical devices [89, 93] [7] and high-power electronic ones [126–128].

Design methodologies for WPT systems are well-known in the literature. They may either be based on a separate design of transmitter and receiver [76, 74, 129] or on the design of the whole system as an isolated dc-dc converter [27, 24][1]. Following the latter approach is quite common referring to the transmitter as the primary side, and the receiver as the secondary side.

Additionally, the link could be inductive [7][89] or capacitive [24, 125]. In all cases, one of the most important parameters is the coupling factor k, which is typically low and characterized by the distance of the coils or of the plates, their alignment, and the interposed medium.

This chapter is focused on a particular case where the secondary side is low-power and low-complexity so that all the circuitry and intelligence for the regulation

of the delivered power should be placed at the primary side. This approach is usually referred to as *primary-side control* [130–132].

Motivations for studying primary-side control techniques rely on the fact that the output power regulation in a WPT system is both critical and challenging. On the one hand, one has always to cope with variability in k (due, for example, to misalignment of the coils or of the plates) and in the load (that has to be considered as a time-varying electronic system, with its own internal state that could change according, for example, to the battery charge level when charging a portable device, or the condition of the tissues in a biomedical implant such as a neurostimulator). On the other hand, while it is easy to introduce a dc-dc converter at the primary side to regulate the transmitted energy, estimating the working condition of the secondary side by only sensing the quantities available at the primary side is challenging, and the most common approach is to send information about the received power back to the transmitter (back-telemetry) either via the same link [133, 134] or via an extra link [135, 136]. This clearly increases the complexity of the overall system and in particular the secondary side. If this is not allowed, a primary-side control is required.

The primary-side estimation of k and of the load based on a known model of the WPT system is a common way to enable primary-side control. Indeed, this approach often suffers [130] from the problem of dealing with both k and load as parameters that are both unknown at the same time, which is usually a not possible assumption for standard approaches.

Recent studies have proposed closed-loop control schemes capable of simultaneously maintaining output power regulation and maximum efficiency, irrespective of the load and the coupling coefficient. They generally take advantage of techniques that pass under the name of MEPT (Maximum Efficiency Point Tracking) [137] or MET (Maximum Efficiency Transfer) [127] algorithms that aim at regulating the output power to the desired level without introducing additional energy losses.

Preserving high efficiency, in response to load or coupling coefficient variation, requires MET techniques aimed at adjusting the equivalent load resistance of the system to the optimal one (i.e., the one ensuring maximum efficiency) through impedance conversion, by using either passive impedance matching networks [74, 76, 138] or by employing load modulation techniques [139–141].

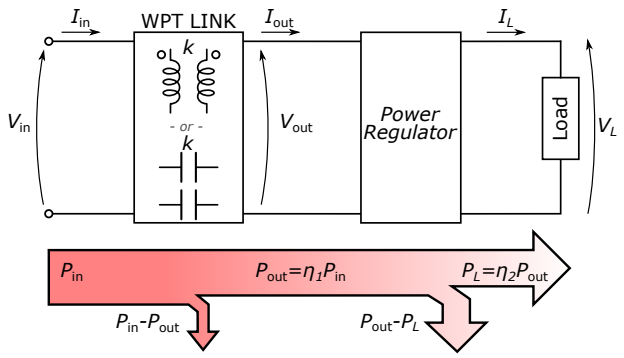


Fig. 6.1 Schematic diagram of a WPT system (inductively or capacitively coupled) including a power regulator between the WPT link and the load.

However, the former requires the use of extra reactive elements (especially inductors) often organized in cumbersome matrices (along with their selection switches), making the approach effective only at very high frequencies. The latter instead is more common and suitable in case of dynamic variation of the coupling factor and of the load impedance. A third group of techniques exists, based on the regulation of the output power at the receiver side while controlling the efficiency at the transmitter by dynamically looking for the minimum input power at any given output power [132, 142, 127].

Inspired by these techniques, we consider the setup illustrated by Figure 6.1. Assuming that the energy transferred by the WPT link (and characterized by the efficiency η_1) exceeds the power required by the load, one could add a simple linear power regulator (characterized by the efficiency η_2) at the secondary side and dissipate the excess of power. An approach like this certainly guarantees output power regulation, but at the cost of low whole system efficiency (that can be estimated as $\eta = \eta_1\eta_2$), which furthermore decreases as the excess of power increases (i.e., η_2 decreases).

The aim of this chapter is to show that the additional linear power regulator at the secondary side allows a primary-side control for the WPT system at virtually no cost (or, with a very limited cost) in terms of efficiency, under the assumption that the variations observed in η_1 are limited, and negligible with respect to the variation range of η_2. The key idea is that the primary side is capable of detecting the exact point when the additional regulation turns on and starts dissipating power. In this point, the power transferred by the WPT system is almost the same as the power required by the load, and setting this as an operating point would ensure that

i) the power delivered to the load is the desired one; and *ii*) the efficiency of the overall WPT system is not affected, as the amount of power wasted by the additional regulator is negligible. We define this condition as the Desired Operating Point (DOP).

With respect to all the aforementioned works, the advantage of the proposed approach is twofold. On the one hand, it is possible to abstract the analysis from the concept of optimal impedance (employed to calculate the WPT efficiency as in [137]) that is not well-suited (i.e., not well-defined) to represent the nonlinear time-varying electronics present in every WPT circuit.

On the other hand, it is possible to fill the literature gap underlined in [130] about the simultaneous estimation of the coupling coefficient and the load.

In the proposed system, provided that the WPT circuit parameters comply with very general conditions, an easy-to-identify corner point corresponding to the DOP appears in the primary-side voltage-current characteristic of the WPT link. In other words, the computation of the voltage-current characteristic of the WPT link at the primary side is sufficient to allow the WPT system to work at the DOP, without the need for the exact knowledge of the circuit model and its parameters such as load power and coupling factor. Of course, the location of the DOP depends on both the coupling coefficient and the load, so that an identification (and possibly also a tracking) algorithm is needed, but the proposed approach is completely model- and parameters-agnostic.

This chapter is organized as follows. Section 6.2 derives the mathematical properties of the DOP, analyzing the two dual cases of constant current- and constant voltage-driven loads, under the limit conditions of purely resistive and ideal source load models. In Section 6.3 the corner point corresponding to the DOP point is observed on a physical prototype, whose design process is also detailed, and an elementary DOP identification algorithm is described. Finally, conclusions are drawn.

6.2 Theoretical Analysis: Desired Operating Point characterization

Let us focus on the WPT link depicted on the left side of Figure 6.1, considering it as a voltage-controlled black box whose output power P_{out} depends on the input voltage V_{in} and on the coupling factor k. The WPT link is then connected to a power regulator that dissipates the excess power, delivering P_L to the load.

We remark that, for the sake of generality, we assume the load is non-linear and time-varying. Its *nominal* power P_N, either defined as $P_N = V_N f(V_N, t)$ or $P_N = f(I_N, t) I_N$, in case of a voltage-controlled load (being V_N the nominal voltage) or a current-controlled one (being I_N the nominal current), respectively, can change over time. The value of k may change over time, as well.

In order to account for these phenomena while keeping our model as simple as possible, we assume in the following that the system is quasi-stationary: changes either in k or P_N are sufficiently slow to be considered unknown but constant in a given time interval.

Hence, in the system depicted in Figure 6.1, setting the load power P_L to the desired value P_N requires that *i*) the regulator is aware of P_N; and *ii*) $P_{\text{out}} > P_N$. The regulator dissipates $P_{\text{out}} - P_N$, so that $P_L = P_N$. Of course, this situation is quite far from being optimal, since the efficiency of the system may be very low due to the power dissipated on the regulator. The only acceptable situation is when the regulator is only marginally ON, dissipating a negligible amount of power. This case, where we have $P_{\text{out}} \approx P_N$, is exactly the DOP we are looking for.

Practically, as we have assumed that the WPT block is a voltage-controlled circuit, achieving the DOP is equivalent to finding the optimal input voltage level $V_{\text{in}}^{(opt.)}$ that ensures $P_{\text{out}} \approx P_N$. This would pave the way for primary-side control, as no actions are required at the secondary side to achieve the desired power level.

The main issue in the proposed approach is that $V_{\text{in}}^{(opt.)}$ depends on both P_N and k, thus an estimation of these quantities, as well as an advanced system model would generally be required. In the following, we will observe that, under certain hypotheses, the value of $V_{\text{in}}^{(opt.)}$ can be easily identified by looking at the current-to-voltage characteristic of the WPT-link primary side. The curve in the I_{in}–V_{in} plane shows a *corner point*, i.e., a *discontinuity* in its derivative, that can be used to

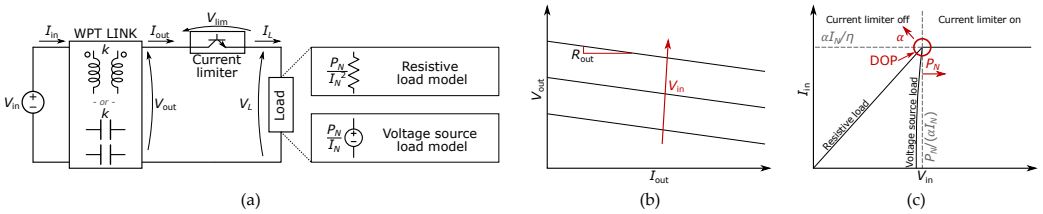


Fig. 6.2 WPT system employing a current limiter power regulator: (a) schematic diagram; (b) V_{out}–I_{out} characteristic of a WPT link behaving as a controlled real voltage source. The output voltage is an increasing function of V_{in}; (c) I_{in}–V_{in} characteristic of a WPT link with two different load models, both having nominal power P_N.

identify the DOP even without the knowledge of k and P_N or of the system model. Once the desired point has been identified, it can be tracked to compensate for possible variations in k and P_N and therefore ensure appropriate power to the load with minimum power dissipated by the regulator.

We theoretically derive the mathematical properties of a dc-based system (minor variations are required if assuming sinusoidal voltages and currents) under two assumptions:

- the WPT link efficiency η_1 features a constant (or almost constant) value[1]. The power balance of the WPT link reads

$$V_{\text{out}} I_{\text{out}} = P_{\text{out}} = \eta_1 P_{\text{in}} = \eta_1 V_{\text{in}} I_{\text{in}} \tag{6.2.1}$$

  where the quantities I_{in}, I_{out} are the average input and output currents and V_{out} is the output voltage of the WPT link;

- the power regulator is built either as a current limiter (with a series connection to the load), or as a voltage limiter (with a parallel connection to the load).

6.2.1 Current-limiter Power Regulator

Let us assume that the power regulator is a current limiter that sets an upper bound I_N to the load current. The simplest implementation of this regulator, as in the schematic

[1] more precisely, we require that the variations of η_1 are small when compared to that observed in η_2 so that the efficiency variations in the overall system are dominated by the variations in η_2.

of Figure 6.2(a), is a BJT working in the active region and biased with constant base current, i.e., constant emitter current.

This scenario fits the case of a load designed to work with a *constant and well-known* nominal current I_N. With the load reasonably assumed to be a current-controlled circuit, let us indicate as $V_L = f(I_L)$ its current-to-voltage relation, with $f(\cdot)$ being not depending on time but unknown due to the quasi-stationary hypothesis. Therefore, when the load current is set to the nominal value I_N, its power $P_N = I_N f(I_N)$ is unknown even if I_N is known and fixed.

In order to compute an expression for the I_{in}–V_{in} curve, let us linearize the WPT link and model it as a real, controlled voltage source (an ideal voltage source with an output series resistance R_{out}):

$$V_{\text{out}} = \alpha V_{\text{in}} - R_{\text{out}} I_{\text{out}}\,, \tag{6.2.2}$$

with the conversion ratio α being unknown as it depends on k, and where we will further assume that R_{out} is small. An example has been plotted in Figure 6.2(b). The series current regulator decreases its voltage V_{lim} to increase the load current up to the I_N value; if not possible, the regulator turns into a short circuit ($V_{\text{lim}} = 0$), with $I_{\text{out}} = I_L < I_N$.

The I_{in}–V_{in} characteristic clearly depends on the specific $f(\cdot)$. For the sake of simplicity, two linear cases will be considered, a purely resistive load and an ideal voltage source, as shown within the insets of Figure 6.2(a). Both load types have been designed to have a nominal power consumption P_N. It can be proven that a generic load, being modeled as a real voltage source, shows an intermediate behavior within the boundaries discussed here. In all these cases, as computed in the following, the I_{in}–V_{in} characteristic is a non-decreasing curve that, under the assumption of a small R_{out}, features an easy-to-identify corner point.

Resistance load model

the desired power constraint for a resistance load sets $R_L = P_N/I_N^2$. The regulator is OFF for $I_{\text{out}} = I_L < I_N$; here $V_{\text{out}} = V_L = R_L I_L = \left(P_N/I_N^2\right) I_L$. By replacing this value in (6.2.2), we get $I_{\text{out}} = \alpha V_{\text{in}} / \left(R_{\text{out}} + I_N^2/P_N\right)$. Under the assumption that R_{out}

is small enough, we have $I_{\text{out}} \approx \alpha V_{\text{in}} I_N^2 / P_N$, and $V_{\text{out}} \approx \alpha V_{\text{in}}$, leading to

$$I_{\text{in}} = \frac{V_{\text{out}} I_{\text{out}}}{\eta_1 V_{\text{in}}} \approx \frac{\alpha^2 I_N^2}{\eta_1 P_N} V_{\text{in}}\,, \tag{6.2.3}$$

i.e., I_{in} is proportional to V_{in}. This holds if $I_{\text{out}} < I_N$, i.e., from (6.2.2)

$$V_{\text{in}} < \frac{P_N}{\alpha I_N} + \frac{R_{\text{out}} I_N}{\alpha} = V_{\text{in}}^{(opt.)}\,, \tag{6.2.4}$$

with $V_{\text{in}}^{(opt.)} \approx P_N/(\alpha I_N)$ if we assume that R_{out} is small enough. Note that, assuming $V_{\text{in}} \approx V_{\text{in}}^{(opt.)}$ in (6.2.3), we have $I_{\text{in}} \approx \alpha I_N / \eta_1$.

For $V_{\text{in}} > V_{\text{in}}^{(opt.)}$, the current limiter turns on, so that $I_{\text{out}} = I_L = I_N$. Using this value in (6.2.2), and exploiting (6.2.1), we get

$$I_{\text{in}} = \frac{V_{\text{out}} I_{\text{out}}}{\eta_1 V_{\text{in}}} = \frac{(\alpha V_{\text{in}} - R_{\text{out}} I_N) I_N}{\eta_1 V_{\text{in}}} \approx \frac{\alpha I_N}{\eta_1}\,, \tag{6.2.5}$$

that, under the assumption of a sufficiently small R_{out}, is independent of V_{in}. The complete I_{in}–V_{in} characteristic has been plotted in Figure 6.2(c).

Voltage-source load model

The load is assumed as an ideal voltage source with $V_L = P_N/I_N$ according to the P_N constraint. The current limiter is OFF for $I_{\text{out}} = I_L < I_N$, with $V_{\text{out}} = V_L = P_N/I_N$. From (6.2.2) we have $I_{\text{out}} = (\alpha V_{\text{in}} - P_N/I_N)/R_{\text{out}}$. The presence of the term $1/R_{\text{out}}$ does not allow us any simplification, and we formally have:

$$I_{\text{in}} = \frac{V_{\text{out}} I_{\text{out}}}{\eta_1 V_{\text{in}}} = \frac{\alpha P_N}{\eta_1 R_{\text{out}} I_N} - \frac{P_N^2}{\eta_1 R_{\text{out}} I_N^2} \frac{1}{V_{\text{in}}}, \tag{6.2.6}$$

that holds for $I_{\text{out}} < I_N$, i.e., $V_{\text{in}} < V_{\text{in}}^{(opt.)}$, where the value of $V_{\text{in}}^{(opt.)}$ is the same defined in (6.2.4). Note that the assumption of a small value of R_{out} implies that also the value of $\alpha V_{\text{in}} - P_N/I_N$ has to be small. As in the resistance load model case, for $V_{\text{in}} = V_{\text{in}}^{(opt.)}$, it is $I_{\text{in}} = \alpha I_N$.

For $V_{\text{in}} > V_{\text{in}}^{(opt.)}$, the current limiter turns on. Computations are the same as in the resistance load model case and lead again to (6.2.5).

The I_{in}–V_{in} characteristic for the voltage-source load case has been plotted in Figure 6.2(c) along with the characteristic found for the resistance case. Both curves are continuous, and exhibit an easily detectable corner point for $V_{\text{in}} = V_{\text{in}}^{(opt.)}$. It is clear that, regardless of the load model and even without the knowledge of the system parameters (i.e., P_N and k), the DOP is detectable from the primary side under the assumption of being able to estimate the I_{in}–V_{in} characteristic.

6.2.2 Voltage-limiter Power Regulator

The case dual to the previously considered one is a parallel shunt regulator that limits the load voltage to the fixed and known value V_N. Its simplest implementation is a common zener diode, as depicted in Figure 6.3(a). This case fits a load circuit designed to work at a constant nominal voltage V_N. Assuming a voltage-to-current characteristic $I_L = f(V_L)$, the load nominal power is $P_N = V_N f(V_N)$.

Here we linearize the WPT link as a real controlled current source

$$I_{\text{out}} = gV_{\text{in}} - G_{\text{out}}V_{\text{out}}\,, \tag{6.2.7}$$

with the transconductance g depending on k, and where we assume that G_{out} is small. An example has been depicted in Figure 6.3(b).

The I_{in}–V_{in} characteristic can be computed in the very same way as in the previous subsection, and leads to similar results, under the assumption of a sufficiently small G_{out}.

Conductance load model

the load is a conductance $G_L = P_N/V_N^2$. For $V_{\text{out}} = V_L < V_N$ the shunt is OFF. From (6.2.1) and (6.2.7), and assuming G_{out} small enough, we get

$$I_{\text{in}} = \frac{V_{\text{out}}I_{\text{out}}}{\eta_1 V_{\text{in}}} \approx \frac{g^2V_N^2}{\eta_1 P_N}V_{\text{in}}\,, \tag{6.2.8}$$

i.e., I_{in} proportional to V_{in}. This holds for $V_L < V_N$, i.e., from (6.2.7)

$$V_{\text{in}} < \frac{P_N}{gV_N} + \frac{G_{\text{out}}V_N}{g} = V_{\text{in}}^{(opt.)}\,, \tag{6.2.9}$$

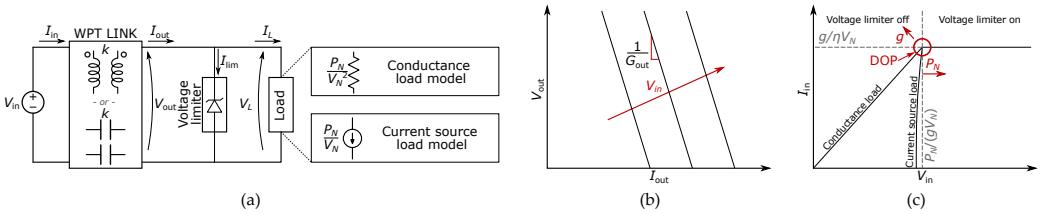


Fig. 6.3 WPT system employing a voltage limiter power regulator: (a) schematic diagram; (b) V_{out}–I_{out} characteristic of a WPT link behaving as a controlled real current source. The output current is an increasing function of V_{in}; (c) I_{in}–V_{in} characteristic of a WPT link with two different load models, both having nominal power P_N.

that can be approximated to $V_{\text{in}}^{(opt.)} \approx P_N/(gV_N)$ if G_{out} is small enough.

For larger values of V_{in}, the shunt turns on, and $V_{\text{out}} = V_N$. From (6.2.7) we get

$$I_{\text{in}} = \frac{V_N\,(gV_{\text{in}} - G_{\text{out}}V_N)}{\eta_1 V_{\text{in}}} \approx \frac{gV_N}{\eta_1}\,. \tag{6.2.10}$$

The I_{in}–V_{in} characteristic has been plotted in Figure 6.3(c).

Current-source load model

The load is assumed as an ideal current source, with $I_L = P_N/V_N$. When the shunt is OFF, $I_{\text{out}} = I_L$, and from (6.2.7) we get

$$I_{\text{in}} = \frac{gP_N}{\eta_1 G_{\text{out}} V_N} - \frac{P_N^2}{\eta_1 G_{\text{out}} V_N^2}\frac{1}{V_{\text{in}}}\,, \tag{6.2.11}$$

that holds for $V_L < V_N$, i.e., for $V_{\text{in}} < V_{\text{in}}^{(opt.)}$ as defined in (6.2.9).

For larger values of V_{in} the shunt is ON, and (6.2.10) still holds.

The I_{in}–V_{in} characteristic for this case has been plotted in Figure 6.3(c) and compared to the characteristic of the conductance load. The features already observed in Figure 6.2(c) are still present: regardless of the load model and of the coupling factor value (that mainly affects g), the I_{in} plot is continuous with respect to V_{in}, with a discontinuity in its derivative that clearly identifies the DOP. This allows us to simply identify the DOP from the primary side without the need to know either k or P_N.

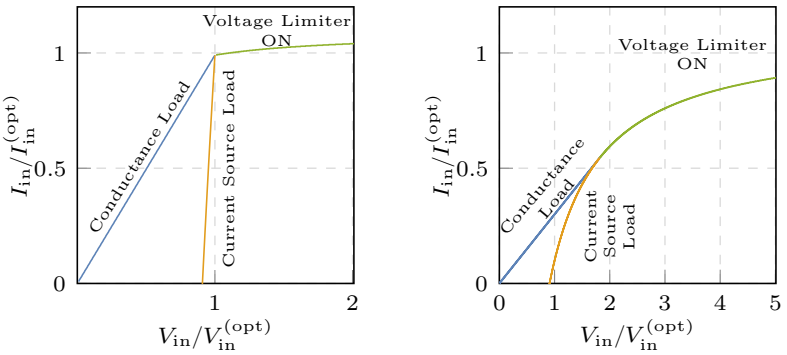


Fig. 6.4 I_{in}–V_{in} characteristic in the case of a voltage-limiter power regulator, normalized with respect to $I_{in}^{(opt)} = \frac{gV_N}{\eta_1}$ and $V_{in}^{(opt)} = \frac{P_N}{gV_N}$, respectively. The normalized characteristics depend on the ratio $G_{out}/\frac{P_N}{V_N^2}$, only:
(a) $G_{out}/\frac{P_N}{V_N^2} = 0.1$; (b) $G_{out}/\frac{P_N}{V_N^2} = 1$.

6.2.3 Circuit Design Considerations

This section provides a brief discussion of the assumptions introduced in the above theoretical analysis.

The efficiency of the WPT link, being used in (6.2.1), has been considered (almost) constant and independent of the operating point. If not, the $V_{in} - I_{in}$ characteristic of Figure 6.2(c) and 6.3(c) would be affected, consequently. Indeed, since the only purpose of the characteristic is to identify the DOP, it is reasonable to assume that a mildly variable efficiency around that point is sufficient for allowing the correct DOP identification.

Similarly, a non-linearity either in the WPT link or in the load will affect the I_{in}–V_{in} characteristic. Mild non-linearities should not prevent the detection of the DOP.

The most critical condition to be met is the small output resistance of the WPT link in the case of the current-limiter power regulator, or the small output conductance in the voltage-limiter one. This is discussed in the following.

Let us consider again the current-limiter case of Section 6.2.1, but without introducing any simplification do to the value of R_{out}. Let us focus on the resistive load model representing the worst case for the detection of the corner point, as can be seen in Figure 6.2(c). A condition to ask for the easy detection of the DOP is

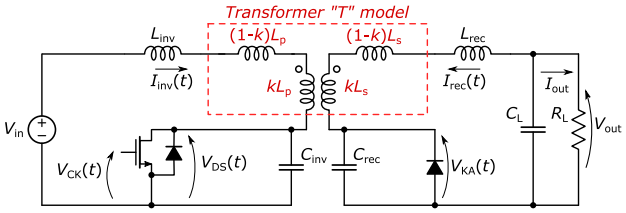


Fig. 6.5 Schematic diagram of the isolated class-E converter implementing the WPT link in the designed prototype.

that, for values of V_{in} close to $V_{\text{in}}^{(opt.)}$, the slope of the I_{in}–V_{in} characteristic when the power regulator is OFF is much higher than the slope when the regulator is ON.

In the regulator-OFF region, the slope can be reasonably assumed independent of V_{in} and equal to $\alpha^2 I_N^2/P_N$. In the ON region, we can consider derivative of (6.2.5) computed for $V_{\text{in}} = V_{\text{in}}^{(opt.)}$ that is $R_{\text{out}}\alpha^2 I_N^4/P_N^2$. By comparing the two values, we get

$$R_{\text{out}} \ll \frac{P_N}{I_N^2}\,. \tag{6.2.12}$$

A similar computation for the voltage-limiter case leads to

$$G_{\text{out}} \ll \frac{P_N}{V_N^2}\,. \tag{6.2.13}$$

Equations (6.2.12) and (6.2.13) represent the mathematical conditions of what we mean by small R_{out} and small G_{out}, respectively.

To highlight this issue, the effects of different $G_{\text{out}}/(P_N/V_N^2)$ ratios in the I_{in}–V_{in} characteristic are compared in Figure 6.4, for a WPT system with a voltage limiter power regulator. Results are obtained from the linear model proposed in Section 6.2.2 but without making any approximation regarding G_{out}. The corner can be easily seen for a ratio of 0.1, but the transition becomes smoother when the ratio grows to 1, in agreement with (6.2.13).

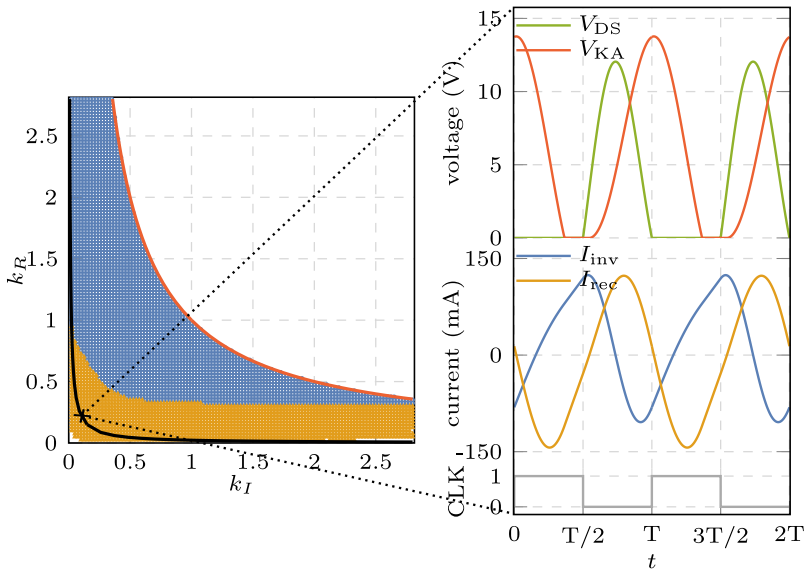


Fig. 6.6 Space of solutions of the lossless and normalized class-E design problem for a clock duty cycle $D = 50\%$. The blue points refer to optimal (ZVS + ZVDS) class-E operation, and the orange ones to sub-optimal solutions (ZVS only). The black line highlights solutions featuring $L_{\text{inv}} = L_{\text{rec}} = 0$ with $k = 0.15$. The waveforms for the chosen design solution are shown on the right.

6.3 Validation on a Class-E based WPT System

The prototype considered in this chapter has been built to drive a constant voltage load by means of a shunt regulator and a WPT link based on an isolated resonant class-E dc-dc converter.

6.3.1 Prototype design

Class-E converters [13, 16, 19, 77, 34, 78][1] are based on the soft-switching technique [10, 13, 63][1]. In particular, the *optimum* class-E switching condition is ensured if both Zero-Voltage Switching (ZVS) and Zero-Voltage-Derivative Switching (ZVDS) are ensured at the main MOS switch, i.e., the drain-source voltage goes to zero with zero time-derivative immediately before the switch turn-on instant. In some designs, ZVDS cannot be satisfied, and only ZVS is achieved. In this case, the class-E converter is said to operate under *sub-optimum* condition. Even if performance in the two cases is generally aligned, optimal condition is preferred

as some secondary-order aspects (such as, for example, the sensitivity to the clock jitter) show better behavior.

The adopted topology has been taken from [1], and it is shown in Figure 6.5. It ensures galvanic isolation between the primary and secondary side by means of coupled coils L_p and L_s, and includes four additional resonant elements, i.e., the inductances L_inv, L_rec, and the capacitances C_inv and C_rec. The C_L capacitance, instead, is simply used as an output filter capacitance.

For the design of the class-E converter we have followed the semi-analytical methodology first proposed in [31] and refined in [1] that overcomes the inherent limitations associated to the common sinusoidal approximation. A comprehensive description of the design procedure is out of the scope of this work and the interested reader is referred to [1] for a detailed discussion. Suffice it to say that it relies on the design of a 1 W, 1 V-to-1 V normalized converter operating at 1 rad/s by means of five dimensionless parameters, two of which (k_I, k_R) are degrees of freedom, and three (q_M, q_I, and q_R) are numerically computed to ensure optimum class-E operations of the normalized converter. Then, given the desired values of input voltage V_in, output voltage V_out, output current I_out and operating frequency f_s, the following denormalization relations hold:

$$\begin{aligned} C_\mathrm{inv} &= \frac{V_\mathrm{out} I_\mathrm{out}}{V_\mathrm{in}^2} \frac{1}{2\pi f_s q_I},\ C_\mathrm{rec} = \frac{I_\mathrm{out}}{V_\mathrm{out}} \frac{1}{2\pi f_s q_R}, \\ M &= \frac{q_M V_\mathrm{in}}{2\pi f_s I_\mathrm{out}},\ L_\mathrm{inv} + L_p = M \frac{V_\mathrm{in}}{V_\mathrm{out}} \frac{1}{k_I}, \\ & L_\mathrm{rec} + L_s = M \frac{V_\mathrm{out}}{V_\mathrm{in}} \frac{1}{k_R}. \end{aligned} \tag{6.3.14}$$

where $M = k\sqrt{L_p L_s}$ is the mutual inductance of the coupled coils. The procedure can also account for the main sources of losses from all active and passive devices.

With respect to a typical isolated dc-dc converter, a low value of k results in non-negligible leakage inductances $(1-k)L_p$ and $(1-k)L_s$. We can take advantage of this by exploiting them as the main resonant inductances, i.e., by constraining $L_\mathrm{inv} = L_\mathrm{rec} = 0$. According to (6.3.14), this yields $k_I k_R = k^2$, reducing the number of degrees of freedom in the design to one.

Figure 6.6 is adopted from [1], and represents the state space of solutions for class-E dc-dc converters as a function of the two degrees of freedom k_I and k_R.

Blue data points refer to converters featuring the optimum class-E condition, whilst for orange ones only suboptimal operation can be ensured. The solid black line represents points featuring $k_I k_R = k^2$ (i.e., $L_{\text{inv}} = L_{\text{rec}} = 0$) when $k = 0.15$, similar to the one selected for the current design, and highlights how a single degree of freedom is present. Following the suggestions of [1] in the choice of the operating point, only a suboptimal converter can be designed given this constraint.

As a proof of concept, we design a 60 mW-class-E converter prototype, featuring $V_{\text{out}} = 6\,\text{V}$. Available degrees of freedom are exploited to guarantee a high enough efficiency while satisfying (6.2.13). The coils being used, which have been realized as planar PCB coils printed over a standard 1.6 mm board with FR4 substrate, feature an inductance of 1.47 µH with a quality factor $Q \approx 50$ at the nominal frequency of 6.78 MHz. According to the electromagnetic model [89], the nominal coupling factor in air is $k = 0.163$ ($M = 240\,\text{nH}$) at a distance $d \approx 10\,\text{mm}$. Accordingly, the converter is designed to operate at 6.78 MHz with a 50% clock the duty cycle, and with $V_{\text{out}} = 6\,\text{V}$ and $I_{\text{out}} = 10\,\text{mA}$. In the design, capacitors are assumed ideal ($Q_{C_{\text{inv}}} = Q_{C_{\text{rec}}} = 1000$) as it is known that ceramic capacitors with high-quality dielectric (such as C0G) have high-quality factors with negligible series resistance. The rectifying diode has been considered with a 0.6 V voltage drop with a 10 mΩ series resistance and the MOS transistors with a 33 mΩ series resistance when turned on and a body diode with a voltage drop of 1 V and a series resistance of 10 mΩ. The converter model is then completed with two additional 100 mΩ current sensing resistors in series to the input power supply and the load, respectively.

By feeding all these parameters in the model proposed in [1], we have a normalized solution described by $k_I = 0.0969$, $k_R = 0.2750$, $q_I = 0.4255$, $q_R = 0.1002$, $q_M = 0.0266$. The corresponding component values from (6.3.14) are $L_{\text{inv}} = L_{\text{rec}} = 0$, $L_p = L_s = 1.47\,\mu\text{H}$ and $M = 240\,\text{nH}$ as according to constraints, and $C_{\text{inv}} = 239.65\,\text{pF}$, $C_{\text{rec}} = 389.53\,\text{pF}$, when the input voltage is $V_{\text{in}} = 3.67\,\text{V}$ and the output voltage is V_{out}=6 V. The waveforms associated with this operating point are shown in Figure 6.6. The value of the time derivative of the MOS drain-source voltage at the switching time (that for sub-optimum conditions is an additional degree of freedom, as it cannot be constrained to zero) is equal to $0.333\,\text{V}/\mu\text{s}$.

In the actual prototype, shown in Figure 6.7, capacitor values have been slightly decreased to account for the parasitic capacitances of the Infineon IRLM0030TRPBF MOS switch and the Diode Incorporated SD103AW diode, evaluated (in simulation)

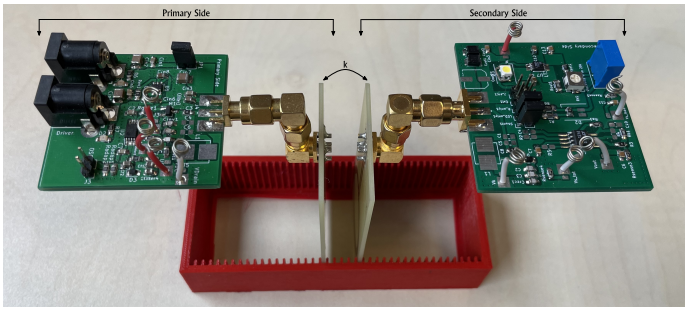


Fig. 6.7 A picture of the designed prototype. The transmitter is located on the left, while the receiver is on the right.

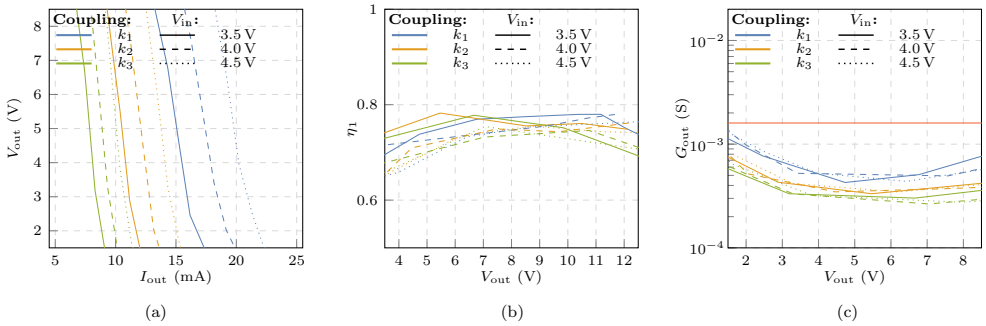
to be approximately 100 pF and 40 pF, respectively. Finally, the MOS transistor is driven by means of an ISL5510IVZ high-speed MOS gate driver by Renesas.

According to the theory of Section 6.2.2, a shunt regulator has been interposed between the converter and the load. The selected limiter is the LT1431 by Analog Device suitably configured to provide 6 V. In order to highlight how different ratios of the converter output conductance over the load conductance can affect the DOP detectability, the prototype features both a resistive trimmer and a variable current source load. The latter has been implemented using an LT3085 LDO by Analog Devices.

6.3.2 Hypotheses Verification

According to the theoretical analysis of Section 6.2, the mathematical hypotheses necessary to guarantee the DOP to a constant voltage-driven load are: *i*) a mild non-linearity of the WPT link and of the load; *ii*) a mildly variable efficiency; and *iii*) $G_{\text{out}} \ll P_N/V_N^2$. Hence, it is worth validating these hypotheses for the designed prototype.

Figure 6.8(a) depicts the V_{out}–I_{out} characteristic of the converter and proves that the WPT system exhibits a good linearity. It fits well a real, controlled current source described by (6.2.7) even as k and V_{in} are varied. The curves have been obtained for different coupling factors and input voltage values. To control the values of k being tested, a PCB holder (the red structure in Figure 6.7) has been purposely 3D-printed to align the coils at repeatable distances. Three different distances $d_1 = 6$ mm,



(a) (b) (c)

Fig. 6.8 Measurements performed to validate the assumptions underlying the theoretical analysis of Sec 6.2. (a) V_{out}–I_{out} curves demonstrating the controlled current source behavior of the WPT link; (b) WPT link efficiency. (c) Output conductance G_{out} of the WPT link compared to P_N/V_N^2 (red solid line);

$d_2 = 8.5\,\text{mm}$ and $d_3 = 11\,\text{mm}$, related to the coupling factor values $k_1 > k_2 > k_3$ have been considered.

In Figure 6.8(b) we can confirm that the efficiency mildly varies with the input voltage and the coupling factor. Note that efficiency is maximized at the nominal operating point thanks to the achievement of ZVS. However, when changing either k or the value of the input or output voltage, ZVS is not achieved anymore. Indeed, thanks to the low k, only a limited variation in the operating point is expected, as observed in [5], with also a limited variation in the efficiency.

Finally, the output conductance of the converter has been computed and plotted in Figure 6.8(c). Compared to the P_N/V_N^2 for the target application (shown as a horizontal red line in the figure), (6.2.13) is always ensured around the nominal output voltage $V_N = 6\,\text{V}$, regardless of the input voltage and the coupling factor. Notice that the higher the coupling factor, the higher the output conductance and consequently the more difficult the corner point in the I_{in}–V_{in} curve to detect.

6.3.3 I_{in}–V_{in} Characteristic

To verify the existence of the DOP under different operating conditions, we have tested operations with the two load types (a conductance and a current source), with the three different k considered above, and at the nominal power level $P_N = 60\,\text{mW}$ and a $\pm 20\%$ variation around it.

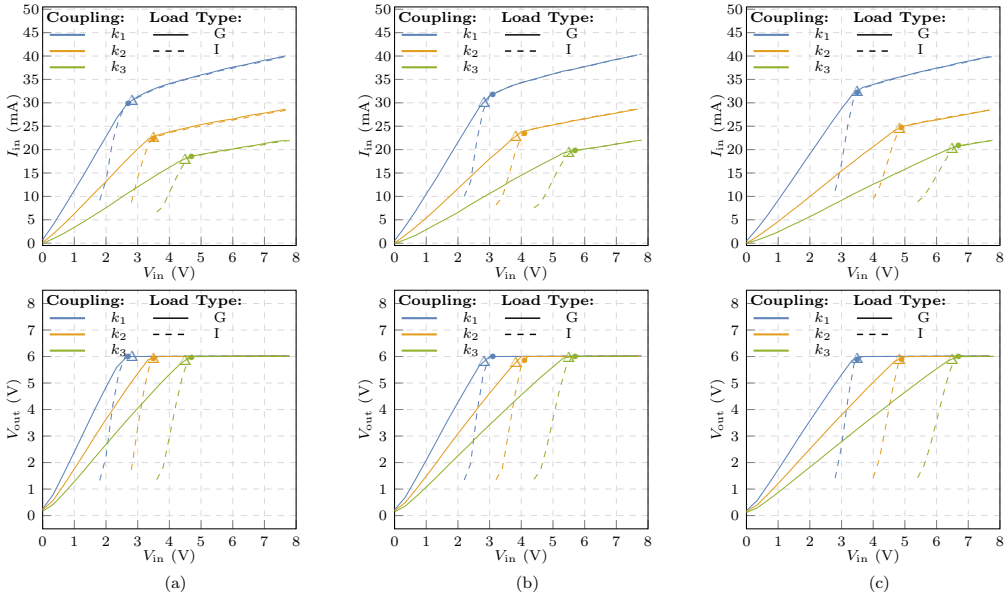


Fig. 6.9 Measurements performed on the WPT system to observe the predicted DOP for three coupling factor values, two output load models (i.e., conductance load 'G' and current generator load 'I'), and three different power levels. (a): $P_N = 48\,\text{mW}$; (b) $P_N = 60\,\text{mW}$; (c) $P_N = 72\,\text{mW}$. The markers highlight the DOP estimated by Algorithm 1 ($\triangle$ for the conductance load and $\bullet$ for the current generator one).

The measurement results are shown in Figure 6.9. Irrespective of the load model, of the output power, and of the coupling coefficient, two regions with different slopes can always be identified, with a higher slope always associated with the shunt regulator being OFF, especially when driving the current-source load. Therefore, even without the knowledge of k, of P_N, and of the load model, the DOP point can be easily identified by detecting the point in which the shunt turns on and $V_{\text{out}} = V_N = 6\,\text{V}$. In agreement with the developed theory, the blue curve that is associated with the highest coupling coefficient is also the one with the smoothest slope variation at the DOP.

6.3.4 DOP identification

The proposal and the comprehensive analysis (including the stability analysis and bandwidth) of a DOP tracking algorithm are out of the scope of this work. Anyway,

we here briefly outline a possible k- and P_N-agnostic procedure capable of identifying the corner point around $V_{\text{in}}^{(opt.)}$.

Starting with an input voltage sufficiently high so that the power regulator is surely ON, V_{in} is continuously reduced using a sufficiently small step while monitoring I_{in} to detect the abrupt slope change of the I_{in}–V_{in} curve identifying the DOP. Let us consider, at each step, the tangent line of the identified characteristic, and express it as $f(V_{\text{in}}) = I_{\text{in}}^0 + mV_{\text{in}}$, in which I_{in}^0 is the intercept at the $V_{\text{in}} = 0$ axis, and m the slope. At the DOP, observed around $V_{\text{in}}^{(opt.)}$, we detect both an abrupt change in the value of m but also in the value of I_{in}^0, which is easier to identify.

In the aim of developing a condition identified only by dimensionless parameters, let us denote as $I_{\text{in}}^0|_{\text{ON}}$ the intercept when the regulator is surely ON. The DOP can be identified when the I_{in}^0 intercept, estimated at the currently applied voltage, is sufficiently smaller than $I_{\text{in}}^0|_{\text{ON}}$. Mathematically, let us say $I_{\text{in}}^0 < \gamma I_{\text{in}}^0|_{\text{ON}}$, with $\gamma < 1$. Notice that any estimation technique being employed should be robust towards noisy measurements.

Looking at the plots of Fig. 6.9, when the series regulator is ON, the tangent line of the I_{in}–V_{in} curve crosses the I_{in} axes with a positive I_{in}^0. Conversely, I_{in}^0 is almost null if computed in the resistive load region, and negative in the current source one.

Applying Algorithm 1 to the data in Figure 6.9, with the corner identified using $\gamma = .5$, the DOPs highlighted with the triangular (conductance load) or the circular (current generator load) markers are found. They correctly identify the condition in which V_{out} reaches the $\approx 6\,\text{V}$ target value.

Algorithm 1: DOP identification

Result: $V_{\text{in}} \approx V_{\text{in}}^{(opt.)}$, $P_{\text{out}} \approx P_L \approx P_N$
Apply V_{in} ensuring the power regulator is ON
Estimate $I_{\text{in}}^0|_{\text{ON}}$
repeat
  Reduce V_{in}
  Estimate I_{in}^0
until $I_{\text{in}}^0 > 0.5 I_{\text{in}}^0|_{\text{ON}}$

6.4 Conclusion

In this work, a parameters-agnostic power regulation method is proposed and experimentally validated. It requires the addition of a power regulator cascaded to the wireless power transfer link, so that a corner appears in the I_{in}–V_{in} characteristic of the overall system, irrespective of the load type, nominal power level, and coupling coefficient. A prototype based on a 60 mW-class-E WPT link working at 6.78 MHz has been built and an elementary procedure capable of detecting the corner, by requiring no knowledge of the system parameters and by relying only on observations performed at the primary side, is proposed.

Chapter 7

Evaluation of a Primary-side Parameters-agnostic Power Regulation Method on Different WPT Topologies

7.1 Introduction

Wireless Power Transfer (WPT) is an emerging technique that aims to replace standard wired power supplies in an increasing amount of applications. Limiting the scope to near field transfer only, two basic WPT methodologies can be identified, namely inductive [41, 87] and capacitive coupling [24, 88].

Design methodologies for WPT systems can either focus separately on the power transmitter and power receiver side [89, 143–145] or consider these two blocks simply as part of an isolated DC-DC converter characterized by a low coupling factor k [54, 146, 24, 27, 147].

Whatever the adopted design methodology, a robust WPT system should deal with load variations, the load being the time-varying electronics that must be fed by the source at the primary side, as well as misalignment, variable distance, and medium between transmitter and receiver that turn the parameter k into an unknown variable. In order to improve the system robustness and guarantee the Desired

Operating Point (DOP) [8][138] to the load, information about the received power is conventionally sent back to the transmitter via the same link (back telemetry) [133, 134, 144]. However, the complexity and power consumption of the receiver unit increase, resulting in limited efficiency and data rates. Therefore, links that adjust their operation by sensing the performance exclusively at the transmitter side (without the need for feedback) are desirable.

The foundation of this work was laid in [7] and later expanded in [8], where both theoretical and experimental investigations were conducted on the existence and identification of a DOP point when a regulator is added at the secondary side. Indeed this leads to a corner in the input–voltage characteristic of the converter and allows the primary-side-only control without the need for additional data links or complex circuitry at the secondary side. Moreover, the technique is robust even against the variation of both the coupling coefficient and load.

Here, we expand the observations in [8], where the solution was proven to work on a specific circuit only, by identifying the presence of the DOP point in recently proposed, state-of-the-art WPT systems.

This chapter is organized as follows. In Section 7.2 we briefly overview the DOP methodology shown in [8]. In Section 7.3 we apply the methodology to recent WPT systems available in the literature. Finally, we draw the conclusion.

7.2 Review of the methodology

In this section, we briefly review the methodology for the DOP point identification, fully detailed in [8]. Accordingly, it is required the addition of a power regulator between the WPT link and the load, as depicted in Figure 7.1(a).

For the sake of simplicity, the WPT system is considered as a voltage-controlled black box whose output power P_{out} depends on the input voltage V_{in} and on the coupling factor k. Then, the WPT link is connected to the power regulator that dissipates the excess power and delivers the right power P_L to the load. P_L can also be time-varying (i.e., the absorbed *nominal* power, P_N, can change over time).

As shown in Figure 7.1(a), in order to set the load power P_L to the desired value P_N it is required that the regulator is aware of P_N and that $P_{\text{out}} > P_N$. The regulator dissipates $P_{\text{out}} - P_N$, so that $P_L = P_N$. However, the DOP condition is not encountered

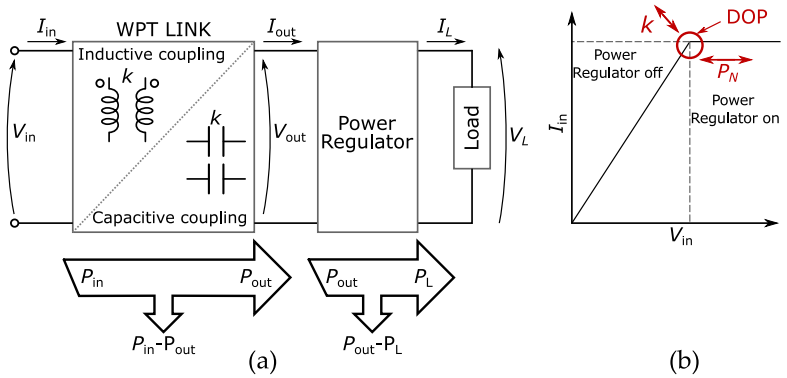


Fig. 7.1 (a) Schematic diagram of a WPT system including a power regulator between the DC-DC and the load. (b) $I_{\text{in}} - V_{\text{in}}$ curve that clearly shows a corner point when the DOP condition is encountered.

unless the the power regulator is only marginally on, dissipating a negligible amount of power. In this case, $P_{\text{out}} \approx P_N$, and the DOP condition is ensured. In practice, the DOP condition can be achieved by setting V_{in} to the value resulting in $P_{\text{out}} \approx P_N$. We denote this level as $V_{\text{in}}^{(opt.)}$.

In [8], it has been demonstrated that the value of $V_{\text{in}}^{(opt.)}$ can be easily identified by looking at the current-to-voltage characteristic from the WPT-link primary side, only. The I_{in}–V_{in} curve shows a *corner point*, i.e., a *discontinuity* in its derivative as simplified in Figure 7.1(b), that corresponds exactly to the DOP point, leading to its correct identification with no knowledge of k, P_N or even the system model. Once the DOP point has been found, it can also be tracked to compensate for possible variations in k and P_N and therefore ensure the right power to the load while achieving minimum power dissipation by the regulator.

According to [8], in which two types of power regulators (i.e., a series power regulator and a shunt one) are considered, the only requirement to be satisfied for an accurate DOP identification concerns the output resistance (or conductance) of the WPT link with respect to the load resistance (or conductance) computed at the nominal operating point. This is paramount since the DOP point can be identified if the corner point in the I_{in}–V_{in} curve can be easily observed, i.e.

$$R_{\text{out}} \ll \frac{P_N}{I_N^2}, \tag{7.2.1}$$

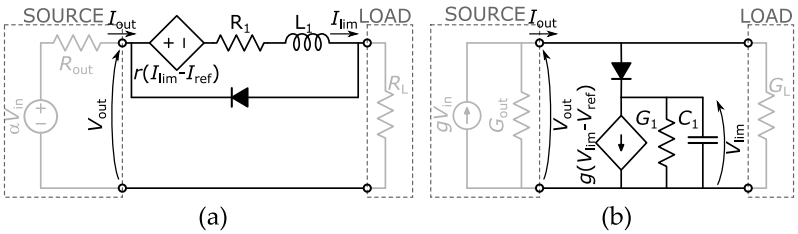


Fig. 7.2 (a) Schematic of the circuit used as series power regulator (current limiter). (b) Schematic of the circuit used as shunt power regulator (voltage limiter).

for a series power regulator. While:

$$G_{\text{out}} \ll \frac{P_N}{V_N^2}. \tag{7.2.2}$$

for a parallel power regulator. The derivation of the above expressions is based on the comparison of the derivatives of the I_{in}–V_{in} curve on both sides of the DOP point and is included in full in [8].

7.3 Application to state-of-the-art WPT systems

In this section, three recently proposed WPT systems [27, 24, 147] are analyzed by means of SPICE simulations. The analysed topologies are significantly different from one another, and also from the topology of the reference methodology [7, 8] so as to highlight the versatility of the proposed DOP identification method for the robust regulation of the load operating conditions against coupling factor and load variations. We consider each design exactly as proposed in the corresponding reference publication, with the addition of either a current limiter or a voltage limiter as power regulator, depending on the circuit characteristics according to (7.2.1) and (7.2.2).

The schematic used for the current limiter is shown in Figure 7.2(a), assuming the simple case of a resistive load R_L and a Thevenin circuit equivalent source. The circuit is based on a transresistance difference amplifier with gain r, operating in negative feedback. Assuming $R_{\text{out}} \ll R_L \ll R_1$, the open-loop gain is $A = I_{\text{lim}}/(I_{\text{lim}} - I_{\text{ref}}) = r/R_1$ (I_{ref} being the reference current for the power regulator), and the feedback loop sets $I_{\text{lim}} \approx AI_{\text{ref}}/(1+A)$, which approximates I_{ref} for sufficiently large values of A. When the (ideal) diode is off, we get $I_L = I_{\text{lim}}$, whereas for $I_L < I_{\text{ref}}$ the diode

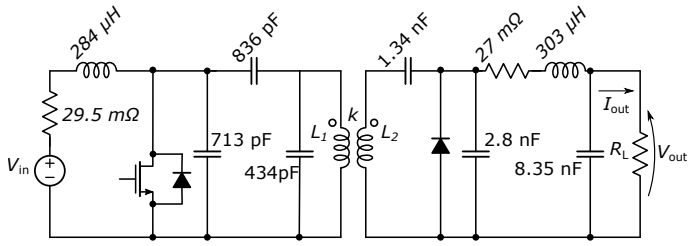


Fig. 7.3 Schematic of the Class-E^2 DC-DC converter based on inductive coupling taken from [27].

turns on, thus disabling the current limiter. The inductance L_1 is added to limit the bandwidth of the current limiter, as it adds a pole at a frequency of approximately $r/(2\pi L_1)$.

The schematic used for the voltage limiter in the simple case of a conductance load G_L and a Norton equivalent circuit source is depicted in Figure 7.2(b) and it is based on a transconductance difference amplifier with gain g. Assuming $G_{\text{out}} \ll G_L \ll G_1$, the open-loop gain is $A = V_{\text{lim}}/(V_{\text{lim}} - V_{\text{ref}}) = g/G_1$ (V_{ref} being the reference voltage for the power regulator) and $V_{\text{lim}} \approx AV_{\text{ref}}/(1+A)$ that approximates V_{ref} for sufficiently large values of A. When the ideal diode is on we have $V_L \approx V_{\text{lim}}$, whereas for $V_L < V_{\text{ref}}$ the diode turns off thus disabling the limiter. The role of C_1 is to limit the bandwidth by adding a pole at approximately $g/(2\pi C_1)$.

In the following, we will set $A = 100$ and limit the bandwidth of the limiter to $1/10$ of the WPT switching frequency.

7.3.1 Classic Inductive Class-E ^{2} converter topology

The class-E^2 converter in Figure 7.3 is taken from [27], and its design relies on the classic approach known as *sinusoidal approximation*. This method considers the AC component of all waveforms as a single tone at the switching frequency f_s. The rectifier circuit (at the secondary side of the transformer) can then be approximated as an equivalent impedance and, therefore the class-E inverter (at the primary side of the transformer) can be designed as a single-tone power amplifier loaded by the reflected impedance of the rectifier. Of course, for the sinusoidal approximation to be effective, additional filtering elements tuned at the first harmonic are required, so that the actual waveforms resemble sinusoids.

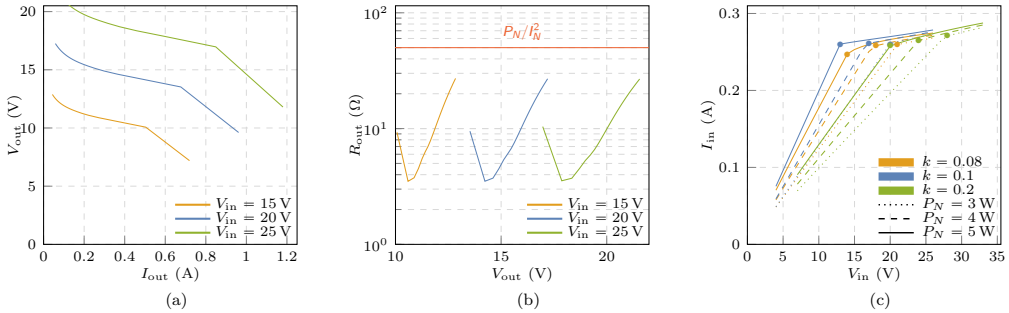


Fig. 7.4 Characteristics of the classical class-E^2 DC-DC converter based on inductive coupling: (a) output curves of the converter for three different input voltages from which the voltage source behaviour becomes clear. (b) output resistance of the converter compared to that of the nominal load in order to justify the use of a current limiter. (c) I–V characteristics observed at the primary side of the DC-DC isolated converter for three different coupling factor values $k = 0.08$, $k = 0.1$, $k = 0.2$ and three different nominal power levels $P_N = 3\,\mathrm{W}$, $P_N = 4\,\mathrm{W}$, $P_N = 5\,\mathrm{W}$. The bullet points indicate the DOP point identified according to the algorithm proposed in [8].

Specs and Nominal Design–The system in [27] is designed for $P_{\mathrm{out}} = 5\,\mathrm{W}$, input voltage $V_{\mathrm{in}} = 20\,\mathrm{V}$ and a resistive load $R_L = 50\,\Omega$ (so $I_{\mathrm{out}} = 316\,\mathrm{mA}$), and operates at the frequency $f_s = 1\,\mathrm{MHz}$. Additionally, the coupled coils have a quality factor $Q \approx 170$ at the nominal frequency and the coupling coefficient is specified as $k = 0.1$.

The active devices were simulated using the available SPICE models of the actual components used in [27], i.e. a SUD06N10-225L by Vishay as the main MOS, switching with a duty cycle $D = 0.5$, and a STPS5H100B Schottky barrier diode by STMicroelectronics as the rectifying diode. All other components have been either assumed ideal, or their parasitics have been explicitly shown in Figure 7.3. Component values are directly shown in the figure.

Output Characteristic–The V_{out}–I_{out} characteristic of this DC-DC converter can be seen in Figure 7.4(a), and has been obtained by sweeping the resistive load at the nominal input voltage $V_{\mathrm{in}} = 20\,\mathrm{V}$ and variations of $\pm 25\%$ around it.

The plot shows a real voltage source behaviour, hence regulation can be obtained by adding a series limiter to the secondary side. To be consistent with [27], we set $I_N = 316\,\mathrm{mA}$. Furthermore, (7.2.1) is satisfied, as can be seen from Figure 7.4(b) that compares the observed value of R_{out} from Figure 7.4(a) with the $50\,\Omega$ resistive load.

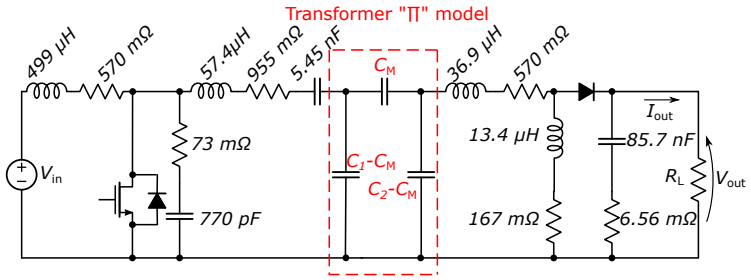


Fig. 7.5 Schematic of the class-E^2 DC-DC converter based on capacitive coupling taken from [24].

Input Characteristic and DOP point–For this system we have considered three different nominal power levels $P_N = 3\,\mathrm{W}$, $P_N = 4\,\mathrm{W}$ and $P_N = 5\,\mathrm{W}$, and three coupling coefficient values $k = 0.08$, $k = 0.1$, $k = 0.2$.[1] Only the case of a resistive load $R_L = P_N/I_N^2$ has been considered.

The I_{in}–V_{in} characteristic has been plotted in Figure 7.4(c), and shows the expected behaviour. Irrespective of the nominal power and of the coupling coefficient, the system shows a discontinuity in the derivative of the I_{in}–V_{in} curve. Therefore, this point, which represents the DOP point, can be easily identified even without knowledge of k and P_N.

7.3.2 Capacitive Class-E^2 Converter Topology

In [24], a WPT system based on capacitive coupling and designed according to the aforementioned sinusoidal approximation, is proposed. Its schematic is depicted in Figure 7.5, highlighting the π capacitive transformer model. Capacitances C_1 and C_2 represent the total primary and secondary capacitance, respectively. The mutual capacitance is $C_M = k\sqrt{C_1 C_2}$, with k the coupling coefficient, as in the inductive case. Their value is $C_1 = C_2 = 559\,\mathrm{pF}$ and $C_M = 55.9\,\mathrm{pF}$.

Specs and Nominal Design–The specifications are: $f_s = 1\,\mathrm{MHz}$, $V_{\mathrm{out}} = 15\,\mathrm{V}$, $P_{\mathrm{out}} = 2\,\mathrm{W}$ at $D = 0.5$[2] and $k = 0.1$. Furthermore, $R_L = 111\,\Omega$ and the nominal behaviour is achieved for $V_{\mathrm{in}} = 11\,\mathrm{V}$.

[1] Note that, the perturbations of both the coupling factor and of the nominal power are limited since a larger variation would lead to unacceptable stress on the MOS.

[2] In [24], the duty cycle is declared to be $D = 0.6$. However, according to the measurements shown by the authors, it is clear that $D = 0.5$.

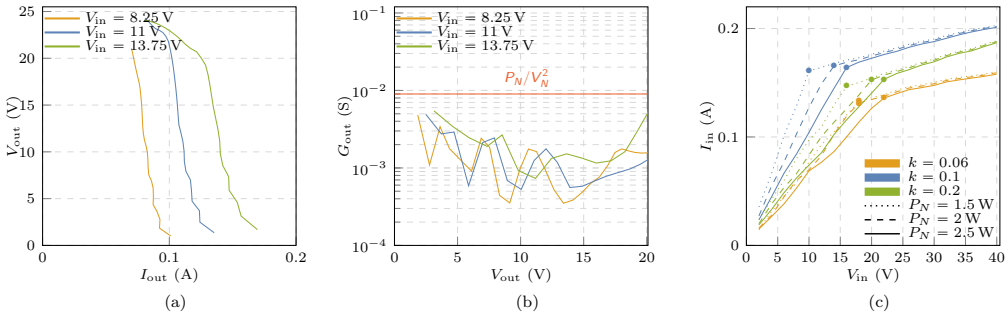


Fig. 7.6 Characteristics of the classical class-E^2 DC-DC converter based on capacitive coupling: (a) output curves of the converter for three different input voltages from which the current source behaviour becomes clear; (b) output conductance of the converter compared to that of the nominal load in order to justify the use of a shunt regulator; (c) characteristics observed at the primary side of the DC-DC isolated converter for three different coupling factor values $k = 0.06$, $k = 0.1$, $k = 0.2$ and three different nominal power levels $P_N = 1.5\,\mathrm{W}$, $P_N = 2\,\mathrm{W}$, $P_N = 2.5\,\mathrm{W}$. The bullet points indicate the DOP point identified according to the algorithm proposed in [8].

For the MOS transistor and the diode we have used the available SPICE model of the IRF510 and RB160VAM-60, respectively. For all reactive components, a simple model with parasitic series resistance has been considered, as explicitly shown in Figure 7.3.

Output Characteristic–The circuit, according to the I_{out}–V_{out} characteristic of Figure 7.6(a), computed for the nominal input voltage $V_{\mathrm{in}} = 11\,\mathrm{V}$ and its $\pm 25\%$ variations $V_{\mathrm{in}} = 8.25\,\mathrm{V}$ and $V_{\mathrm{in}} = 13.75\,\mathrm{V}$, has the same behavior as a real current source. Therefore, the DOP identification can be performed by adding a shunt regulator (we set $V_N = 15\,\mathrm{V}$) and by satisfying (7.2.2). To this purpose, we have compared in Figure 7.6(b) the observed output conductance of the DC-DC converter with the load conductance value $P_N/V_N^2 = 9\,\mathrm{mS}$ at $P_N = 2\,\mathrm{W}$. It is clear from the figure that (7.2.2) is satisfied.

Input Characteristic and DOP point–The I_{in}–V_{in} characteristic for this system has been plotted in Figure 7.6(c). We have considered three nominal power levels $P_N = 1.5\,\mathrm{W}$, $P_N = 2\,\mathrm{W}$ and $P_N = 2.5\,\mathrm{W}$, and three nominal coupling coefficient $k = 0.06$, $k = 0.1$ and $k = 0.2$. Only the conductive load case has been taken into account.

Again, irrespective of the nominal power, the system behaves in a similar way in all cases by showing a discontinuity in the derivative of the I_{in}–V_{in} curve. Therefore

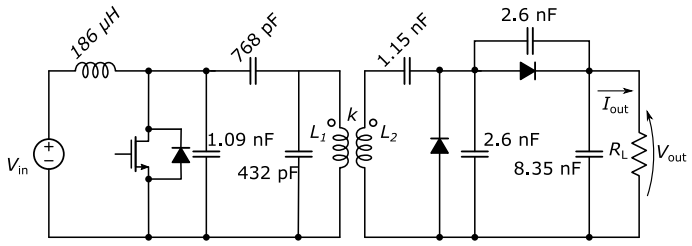


Fig. 7.7 Schematic of the class-E-DE converter based on inductive coupling taken from [147]

this point, which represents the DOP point, can be easily identified independently of k and P_N.

7.3.3 Inductive Class-E-DE Circuit Topology

In [147], one more WPT system based on inductive coupling is proposed. The converter schematic is depicted in Figure 7.7 and it is made of a class-E inverter and a class-DE rectifier.

Specs and Nominal Design–The system in [147] is designed for $P_{\text{out}} = 10\,\text{W}$, input voltage $V_{\text{in}} = 24\,\text{V}$ and a resistive load $R_L = 50\,\Omega$ (so $I_{\text{out}} = 447\,\text{mA}$)[3], and operates at the frequency $f_s = 1\,\text{MHz}$. Additionally, the coupled coils L_1 and L_2 have a quality factor Q at the nominal frequency equals to 165 and 170, respectively, and the coupling coefficient is specified to be $k = 0.056$.

The active devices were simulated using the available SPICE models of the actual components used in [147], i.e. a IRFS4410 by International Rectifier as the main MOS, switching with a duty cycle $D = 0.5$, and a STPS5H100B Schottky barrier diode by STMicroelectronics as diodes at the rectifier side. All other components have been either assumed ideal, or their parasitics have been explicitly shown in Figure 7.3. Component values are directly shown in the figure.

Output Characteristic–The circuit, according to the V_{out}–I_{out} characteristic of Figure 7.8(a), computed for the three input voltages $V_{\text{in}} = 18\,\text{V}$ and $V_{\text{in}} = 22\,\text{V}$ and $V_{\text{in}} = 24\,\text{V}$, shows the behavior of a real voltage source. Therefore, the DOP identification can be performed by adding a current limiter and by setting $I_N = 360\,\text{mA}$ according to the nominal SPICE simulations. Furthermore, (7.2.1) is satisfied as can

[3] Spice simulations by using available SPICE models of the adopted components show $I_{\text{out}} = 360\,\text{mA}$ and therefore $P_{\text{out}} = 6.5\,\text{W}$.

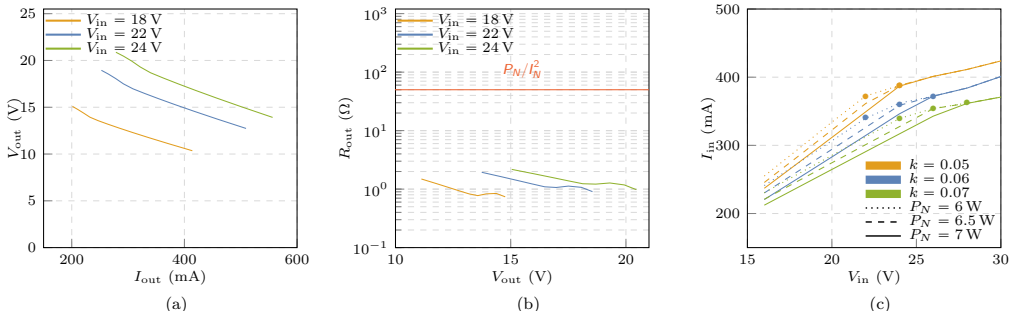


Fig. 7.8 Characteristic of the class-E-DE DC-DC converter based on inductive coupling: (a) output curves of the converter for three different input voltages from which the voltage source behaviour becomes clear; (b) output resistance of the converter compared to that of the nominal load in order to justify the use of a current limiter; (c) characteristics observed at the primary side of the DC-DC isolated converter for three different coupling factor values $k = 0.05$, $k = 0.06$, $k = 0.07$ and three different nominal power levels $P_N = 6\,\mathrm{W}$, $P_N = 6.5\,\mathrm{W}$, $P_N = 7\,\mathrm{W}$. The bullet points indicate the DOP point identified according to the algorithm proposed in [8].

be seen from Figure 7.8(b) that compares the observed value of R_{out} with the $50\,\Omega$ resistive load.

Input Characteristic and DOP point–For this system we have considered three different nominal power levels $P_N = 6\,\mathrm{W}$, $P_N = 6.5\,\mathrm{W}$ and $P_N = 7\,\mathrm{W}$, and three coupling coefficient values $k = 0.05$, $k = 0.06$, $k = 0.07$. Only the case of a resistive load $R_L = P_N/I_N^2$ has been considered.

The I_{in}–V_{in} characteristic has been plotted in Figure 7.8(c), and shows the expected behaviour. Irrespective of the nominal power and of the coupling coefficient, the system shows a discontinuity in the derivative of the I_{in}–V_{in} curve. Therefore, this point, which represents the DOP point, can be easily identified even without any knowledge of k and P_N.

7.4 Conclusion

This chapter validated a Maximum Efficiency Transfer identification methodology to regulate load power without any information from the receiver part (such as, for example, in the case of active telemetry) or a precise system model. In all the setups being evaluated, a corner point (i.e., a discontinuity in the derivative) in the current–voltage characteristic at the transmitter side, could be observed, notwithstanding

both coupling factor and load variations. The addition of either a current limiter, or a shunt regulator, at the receiver side was based on the ratio of the converter output resistance versus the load one. The robustness of the technique in SPICE simulations of recently proposed state-of-the-art WPT systems (i.e, a classic inductive class-E^2, a classic capacitive class-E^2, and an inductive class-E-DE topology) proved the validity of the methodology.

Part III

Spread Spectrum for EMI Reduction

Introduction

This part focuses on the Spread Spectrum technique as a well-known methodology to mitigate ElectroMagnetic Interference (EMI) issues in a large variety of circuits. As a matter of fact, the spread spectrum refers to the possibility of spreading the signal spectrum around the ideal frequency of the signal thanks to the addition of an intentional "jitter" to the synchronization signals.

While the literature is full of examples and applications regarding single-phase circuits, there is only limited coverage regarding 3-phase ones (e.g.,[148–150]) and the few available works present:

- No detailed analysis including optimization and tradeoffs
- No practical analysis. It means that the EMI is considered just from a theoretical point of view (e.g., they do not take into account the international regulations guidelines)
- No analytical criteria are used for the spread spectrum parameters to be chosen.

Furthermore, secondary-order effects that become important at high frequency are often neglected. For this reason, these methodology fundamentals are properly explained in Chapter 8 and the state of the art is improved on the duplex side. On the one hand, the SS theory is revised so to keep into account the harmonics-overlap phenomenon (i.e., a phenomenon that often happens at a higher frequency that is typically neglected). On the other hand, the theory is demonstrated and validated on a closed-loop 3-phase SiC inverter.

By remaining in the field of SS power electronics, this technique has also been correctly employed and proven to work in Talkative Power Converters, where the EMI issues are usually neglected. Preliminary analyses are part of Chapter 9.

Chapter 8

Spread Spectrum in 3-phase inverters

8.1 Introduction

The SS methodology can be located in the field of software techniques for EMI reduction in electronic circuits such as DC-DC converters. The scope of this part is to introduce the reader to the EMI field before entering the details of the SS as well as the aimed performance to comply with international regulations.

In the ElectroMagnetic Compatibility (EMC) field, EMI usually refers to any unwanted power transfer between a source system/circuit and a victim one. The transferred power can be either radiated by electromagnetic wave propagation or conducted if the electromagnetic energy occurs by direct conduction on metallic conductors. With the increasing use of switching electronics, each system must comply nowadays with international standards. Accordingly, they impose regulations that guarantee three basic criteria i.e.: i) a system must not cause interference with other systems; ii) it must not be susceptible to emissions from other systems and eventually iii) must also not cause interference with itself. It follows that in order for the interference to be prevented, it is necessary to i) suppress the emissions at the source side, ii) make the coupling paths as inefficient as possible and iii) make the receiver systems as insensitive to emissions as possible. In principle, without entering into the details of the regulations yet, they require the power spectrum of any interfering signal (i.e., either radiated or conducted) both to comply with a prescribed mask and withstand a certain level of incoming EMI. EMI reduction can be achieved both at the Hardware (HW) and Software (SW) level. General-purpose HW methodologies for

EMI reduction aim at reducing the coupling path between the source and the victim with shielding (for radiated emissions) or filtering (for conducted emissions). Nevertheless, in many situations, these approaches cannot be taken into account (e.g., the source and the victim share the same board) and ad-hoc solutions must be employed. Furthermore, HW approaches are usually characterized by very low flexibility: if the interference exceeds the prescribed limits, the hardware is not able to comply with the regulations anymore and must be redesigned. Therefore, in order to address this issue, EMI methods based on SW algorithms, capable of reducing the EMI by avoiding extra HW elements, have been developed. Among these, two of them are quite popular, the voltage waveforms-shaping techniques (e.g., S shape control, slew rate control) and the dithering ones. The former techniques act on redefining the derivative of the voltage/current waveforms (i.e., dv/dt and di/dt) to reduce the spectral components. The latter, also known as spread spectrum clocking techniques, aim at altering the shape of the conducted/radiated interfering power spectrum by acting on the clock to achieve the peak-frequency-component level reduction. While the voltage-waveforms-shaping techniques require a complex and expensive control system and they are quite efficient at high frequency, only (i.e., the effect at lower frequency may be limited), the SS ones do not feature these limitations. The main idea grounding this technique is the introduction of a jitter in the synchronization signal (e.g., the clock) to avoid the perfect periodic behavior of all waveforms in the circuit, thus spreading the power of their spectral component over a bandwidth that depends on the circuit characteristics. Interestingly, this EMI technique can be considered as an additional and complementary methodology with respect to the aforementioned ones. In the literature, SS is recognized to be an effective modulation strategy to reduce EMI in a large variety of high and low-power applications, ranging from class-D power amplifiers to microprocessor clock generators and switching power converters. It is precisely to this last application that the closest attention will be devoted.

8.2 International Regulations

EMC results from the imposition of additional design objectives for electronic systems over those required for the only functional performance of the system. These additional design objectives stem from the overall requirement of the system

being electromagnetically compatible with its environment. Therefore, there are two classes of EMI requirements that are imposed on electronic systems: the ones coming from governmental agencies and those imposed by the product manufacturer. While the former are legal requirements and cannot be waived if a product is intended to be marketed (the aim is to have electromagnetic pollution under control), the latter is only intended to result in customer satisfaction (the aim is to obtain a reliable and quality product).

By focusing on governmental requirements, it is important to understand that the regulations may change according to the different countries. Besides this, the regulations of each country are further subdivided into those for commercial (still divided into class-A and class-B based on the intended purpose of the device) and military use. For example, in the US, the Federal Communications Commission (FCC) is the government agency that imposes requirements on the placement of electrical products on the market, whereas European standards are regulated by the Comité International Spécial des Perturbations Radioélectriques (CISPR), which is part of the International Electrotechnical Commission (IEC). The limits concern both the conducted and radiated emissions. As previously said, conducted emissions are related to those currents that are passed out through the ac power cord unit and placed on the common power net, where they may radiate and interfere with other devices. The frequency range for conducted emissions extends from 150 kHz to 30 MHz and, in brief, compliance is verified by inserting a line impedance stabilization network (LISN) into the AC power cord unit. Although the emissions to be controlled are due to the current passing out the AC line cord, the limits are given in volts because the LISN measures a voltage that is directly related to the interference current. On the other hand, radiated emissions concern the electric and magnetic fields radiated by the device that may be received by other electronic devices, causing interference. The regulatory agencies require measurements of the radiated and electric field and their limits are given in terms of dBmV/m in the range 30 MHz-40GHz. It is important to notice that the regulations set a limit on the acceptable density of the spectrum (and not on the total amount of energy) and it is indeed this characteristic that allows to exploit the spread spectrum technique since it is not the total amount of energy that matters but the amplitude of the peaks. As a matter of fact, SS techniques are able to lower the power spectrum peak value of an interfering signal at the cost of adding additional spectrum components to it. The key instrument in determining this level is the Spectrum Analyzer which is able to evaluate the energy associated to a

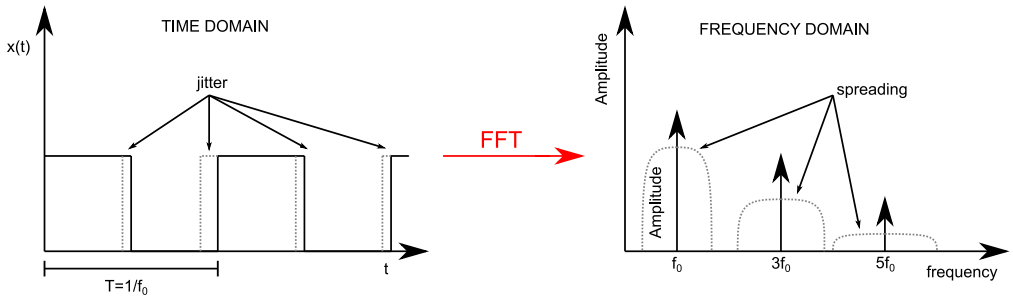


Fig. 8.1 Spreading effect in the frequency domain due to an applied in the time domain signal.

certain resolution bandwidth (RBW) chosen by the operator. Being the measured value dependent on the RBW of the instrument, the regulations agencies specify the RBW to be used, too.

As detailed in [17], the maximum theoretical gain by means of the SS technique is achieved when the energy of a narrow-band signal (i.e., any harmonic of the clock signal) is spread uniformly into the available bandwidth, assumed to be $f0-\Delta f, f_0+\Delta f$, i.e., a frequency band whose width is $2\Delta f$. The achieved reduction (in dB) is given by $10\log((\text{RBW})/2\Delta\text{f})$.

8.3 Spread Spectrum Theoretical Fundamentals

Spread spectrum clocking is a technique used in electronic designs to intentionally modulate the ideal position of the edge of the synchronization signal (i.e., a "jitter") such that the resulting signal spectrum is “spread” around the ideal frequency of the synchronization signal. The result is the reduction of the energy around the fundamental tone (and also its harmonics) of the clock signal, with the spreading of the original energy in a bandwidth usually located around the fundamental tone (and around its harmonics). To this scope, Figure 8.1 illustrates in a simple way the spread spectrum fundamentals by comparing the spectrum of a 50% duty-cyle square wave (black solid line) with its “jittered” version (grey dotted line). The energy associated with each single odd harmonic of the square wave is “spread” around a larger bandwidth leading to a reduction in the peak amplitude.

EMC regulations require that the interfering signal power spectrum fits below a predetermined mask, i.e., that its peak level does not exceed a given value. According

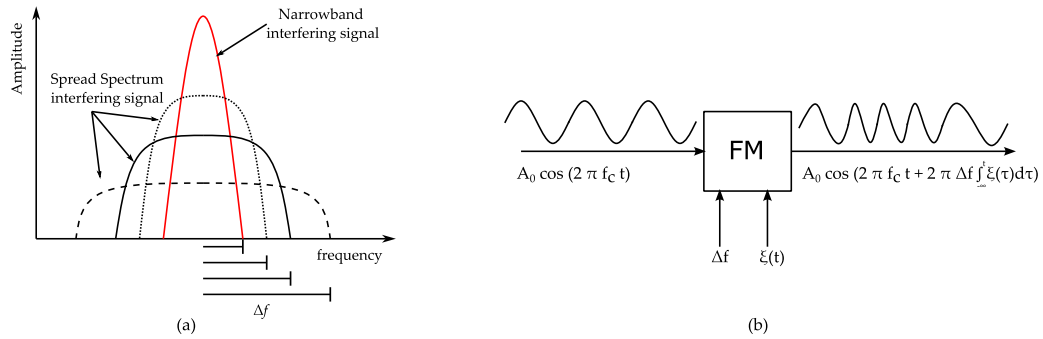


Fig. 8.2 Fundamentals of SS and FM:(a)Narrow band signal compared with the center-spread one for different spread bandwidth to highlight that the higher Δf the lower the peak. (b) Basic principle of a frequency modulation applied to a sinusoidal tone.

to this point of view, any digital circuit or switching power converter is a potential EMI source, due to the narrow-band characteristic of the spectrum of their typical signals, for which energy is mainly located around a fundamental tone and its harmonics. Spreading techniques aim to increase the EMC of these circuits by lowering the power spectrum peak value of an interfering signal at the cost of adding additional spectrum components to it. As previously said, this is achieved by introducing a controlled jitter in the reference timing signal and therefore by changing the instantaneous working frequency. The result is a modification of all signals synchronous with the reference clock, altering their conducted/radiated power spectrum. In other words, these techniques aim to turn narrow-band interference into a (usually more tolerated) background EMI noise.

Even if plenty of approaches can be found in the literature, the spreading is typically obtained by means of modulation of the syncronization signal. The most common techniques applied are:

- Center-spreading. Given a nominal oscillation frequency f_c, the intentional jitter is introduced to modify the actual oscillation frequency by both increasing it and decreasing it, so that f_c is the new mean frequency in time. This has been considered in the example of Figure 8.2(a), when respect to the narrowband interfering signal (red spectrum) at frequency f_c, the energy of the spread-spectrum signal is spread into the band $[f_c - \Delta f, f_c + \Delta f]$.
- Frequency Modulation. Plenty of approaches can be found in the literature for introducing spreading to a reference timing signal. Frequency modulation

(schematized in Figure 8.2(b)) is identified as the optimal choice [151, 152], with small advantages with respect to the period modulation [153, 154] and large advantages with respect to the phase modulation [155, 156].

For the sake of simplicity, the modulation of a sinusoidal tone is considered here. Then, by defining f_c as the carrier frequency, Δf as the frequency deviation (i.e., the "spread"), and $\xi(t)$, in the range $[-1,1]$, as the (normalized) driving signal, the center spread modulation of the single-tone signal reads

$$s(t) = A_0 \cos(2\pi f_c t + 2\pi\Delta f \int_{-\infty}^{t} \xi(\tau)\, d\tau) = A_0 \cos(\phi(t)) \tag{8.3.1}$$

where $\phi(t)$ is known as the instantaneous phase, and $d\phi(t)/dt$ the instantaneous angular frequency, approximately equal to $2\pi f_c + 2\pi\Delta f \xi(t)$. Note that the power of $s(t)$ is unchanged with respect to the unmodulated signal and equals to $A_0^2/2$. Basically, in the frequency modulation of a sinusoidal tone, the instantaneous frequency of the signal changes from $f_c - \Delta f$ (when $\xi(t) = -1$) to $f_c + \Delta f$ f (when $\xi(t) = +1$), so that the energy of the signal is spread in a band whose width is $2\Delta f$. Regarding the actual shape of the spectrum of $s(t)$, it depends on the modulation parameters Δf and $\xi(t)$. When $\xi(t)$ is a periodic function with period $T = 1/f_m$, the spectrum of $s(t)$ is discrete with components located at

$$f = f_c \pm k/T = f_c \pm k f_m, k \in Z \tag{8.3.2}$$

so that

$$s(t) = \sum_{k=-\infty}^{\infty} A_k \cos(2\pi(f_0 + k f_m)t) \tag{8.3.3}$$

where the coefficients A_k need to be properly computed according to $\xi(t)$. Even assuming a periodic modulation, it is important to recall that the resolution of the measurement is limited and indicated above with RBW. If the modulation can be addressed as a slow one, i.e., when $f_m = 1/T$ is smaller with respect to RBW, the components in the spectrum are so close to each other that it is impossible to distinguish them within a measurement, and the spectrum therefore appears as a continuous one. In this case, the shape of the spectrum is almost independent of the resolution of the measurement instrument.

- Triangular modulation. The choice of the shape of $\xi(t)$ is of great importance. The optimal trade-off between implementation complexity and performance is given by a triangular waveform. This case is discussed in detail in [157], and the A_k coefficients can be computed as

$$A_k = \frac{A_0}{\sqrt{2m}} \cos\left(\frac{\pi(m-k)^2}{4m}\right)\left(C\left(\frac{m-k}{\sqrt{2m}}\right)+C\left(\frac{m+k}{\sqrt{2m}}\right)\right)+\frac{A_0}{\sqrt{2m}} \sin\left(\frac{\pi(m-k)^2}{4m}\right)\left(S\left(\frac{m-k}{\sqrt{2m}}\right)+S\left(\frac{m+k}{\sqrt{2m}}\right)\right) \tag{8.3.4}$$

  with C and S are the FresnelC and FresnelS coefficients, respectively. Also in this case, if $f_m < RBW$, the spectrum appears as continuous, with the power measured in a bandwidth RBW is given by the sum of the power of all discrete components enclosed in RBW.

For the spread spectrum to be effective, some thread-offs must be considered: i) Δf must be sufficiently small to limit the output ripple and sufficiently large to reduce the EMI interference. ii) T must be sufficiently high to have a continuous spectrum by keeping in mind that, the higher is T, the more the signal remains unmodulated preventing the spread spectrum beneficial effects. Therefore, to be consistent with [17], the modulation index $m = \Delta f \cdot T$ is the second degree of freedom. iii) If a random-like PAM driving signal is chosen there is an extra degree of freedom due to the statistical properties of the driving signal. Accordingly, once either Δf or T has been chosen, the EMI measurements show a minimum for an intermediate value of m. A frequency-domain-based analysis will take into account only the average power transferred to the victim, while the actual condition to be avoided is that the noise generated by EMI in the victim circuit is, at any time instant, below a critical level. According to these observations, a twofold approach in evaluating the optimal spreading parameters tuning, both from a frequency domain point of view and from a time domain point of view, is proposed. From the frequency domain point of view, since it is not possible to a-priori know the sensitivity bands of the EMI victim circuit, the best approach is to adopt a spreading such that the resulting signal spectrum is as flat as possible. As a matter of fact, international regulations requirements, by limiting the peak value of the interfering spectrum, are coherent with this point of view. From the time domain point of view, we can recall that the modulation of a timing signal means changing its instantaneous frequency. Then, there is a transfer of power between the EMI source and the EMI victim when the instantaneous frequency

of the interfering signal is exactly located in one of the victim sensitivity frequency ranges, only. In this case, the victim circuit behaves like a receiver filter tuned at the interfering signal frequency. However, like any linear or even non-linear filter, an (interfering) signal is generated in the victim only after a transient time: every filter has a settling time in which the output signal is initially very low, and only after a settling time reaches the steady-state value. This has been illustrated in detail in [17]. Therefore, it is not relevant whether the instantaneous interfering signal frequency enters or not the victim sensitivity band, but it is mandatory that the time interval in which the instantaneous interfering signal frequency is within a victim sensitivity band is much shorter with respect to the settling time of the victim circuit. This is exactly the short-time effect discussed in [158].

The receiver circuit is perfectly in line with the working principle of the EMI receiver, in which independently of the digital or analog implementation, the working principle is that of a filter whose bandwidth is constant and given by RBW, and whose center frequency is swept across all the band to be analyzed. Therefore, The RBW filter plays the role of the victim circuit filter.

This effect leads to some differences between the theoretically computed spectrum as in the previous chapter, and the measured spectrum according to an EMI receiver. This aspect has been first considered in [157], where it has been observed that for a fast modulation, the theoretically computed spectrum is equivalent to the measured spectrum, whereas, in a slow modulation, the power measured by the EMI receiver is larger than the expected theoretical power. If one considers the theoretical spectrum, the optimum is achieved for a high value of the modulation index m, i.e., for an indefinitely slow modulation. The maximum reduction also depends, as observed in the previous section, on the resolution RBW used for measuring the spectrum: the larger the RBW, the higher the amount of power capable of passing through the RBW filter, and the lower the reduction. It can be seen that the maximum achievable reduction is a decreasing function of the dimensionless parameter $\rho = \mathrm{RBW}/\Delta f$. Indeed, according to the short-term observation, any victim circuit will not be able to distinguish between an indefinitely slow modulated signal and an unmodulated signal, so this setting should be avoided. When considering the actual EMI receiver model, the optimal performance is achieved for a finite and precise value of m, which depends on the RBW, or more precisely, on the dimensionless parameter ρ defined above, whereas for values of m indefinitely high, the spread

spectrum is ineffective. Consequently, the maximum EMI reduction achievable for SS, is mentioned to be

$$10\log\frac{RBW}{2\Delta f} = 10log\frac{\rho}{2} \tag{8.3.5}$$

cannot be achieved in some specific cases, only.

When this theory, is applied to closed-loop high-power high-frequency three-phase inverters, two questions generally arise:

- Will the converter work with the same performance (i.e. the one when no SS is applied) in terms of stability, efficiency, and capability to drive the motor (e.g., the torque)?
- Are these SS optimization techniques, usually applied to DC-DC converters, valid even in the case of closed-loop 3-phase inverters?

The following sections aim to answer these questions.

8.4 Behaviour of a 3-phase inverter under spread spectrum control model

The converter considered in this analysis is a DC/AC converter with the following specifications. It is supplied by a continuous DC voltage equal to 400 V and it is meant to work at a switching frequency $f_{\text{sw}} = 50kHz$. The line voltage at the load is instead intended to work at $f_c = 50Hz$. The converter is a 3-phase 2-level converter made of 3 legs with an RLE load (i.e., a simplification of the motor load) and it is driven with a PWM with zero sequence injection in order to extend the inverter linearity region. The basic idea is in fact to inject a third harmonic in the mobile mean of the common voltage. Whether the zero sequence is present or not, the modulation can be added to the reference carrier in a way to achieve spread spectrum. This can be easily implemented in PLECS by using a variable-frequency PWM block [1] The basic idea of the inverter is shown in Figure 8.3(a), in which the sketch of the

[1](not available for PLECS versions older than 4.7.4), by writing a proper C-code, or by importing a MATLAB file.

inverter along with the PWM controller, is shown. The easiest way to add spreading capabilities to the converter is by directly altering the reference timing signal, which is represented in this schematic by the triangular signal regulating the PWM block. In this way, all the signals present in the circuit, including the one of interest (i.e., the IDC current as the one that is responsible for the conducted EMI) will be modulated according to the same parameters as the reference timing signal. It is important to point out that all the circuit signals, such as the triangular signal regulating the PWM (and the IDC), are not sinusoidal tones. It means that all the mathematical theories previously developed need to be slightly modified. We refer to the following subsection for the modulation of an arbitrary signal.

The block in charge of applying the spread spectrum, which modifies the triangular carrier entering the PWM block, is highlighted in the red color in Figure 8.3(a). Basically, the triangular carrier $V_{\text{tr}}(t)$ is modulated according to the FM parameters (i.e., the frequency deviation Δf and the modulating signal $\xi(t)$) so to generate $V_{\text{trmod}}(t)$. For the sake of clarity, in Figure 8.3(b) the triangular waveform $V_{\text{tr}}(t)$, along with its modulated version $V_{\text{trmod}}(t)$, is shown. It is important to notice that while the unmodulated waveforms (i.e., the first one from top to bottom in Figure 8.3(b)) feature a constant frequency, the modulated ones do not. Furthermore, the frequency modulation (i.e., the second waveform from top to bottom in Figure 8.3(b)) creates distortion due to the continuous phase change, and it is not composed anymore of linear segments. This may be tricky when looking at a hardware implementation. Either in the case the PWM signal is generated by means of digital hardware or by analog hardware, switching instants are always computed by comparing a ramp (representing the triangular signal) with a constant value. While it is straightforward to change the slope of the ramp, changing the ramp to a generic curve (as required for exactly implementing a frequency modulation) is generally trickier.

For this reason, it is suggested to replace the Frequency Modulation (i.e., the third one from top to bottom in Figure 8.3(b)) with a Period Modulation and:

- Given the SS parameters, in particular since the main oscillation frequency f_c is much larger than the modulation one $f_m$of the driving signal $\xi(t)$, there is a small difference between the spectra of the two modulations. It means that the difference between the frequency modulation and the period modulation can be considered negligible.

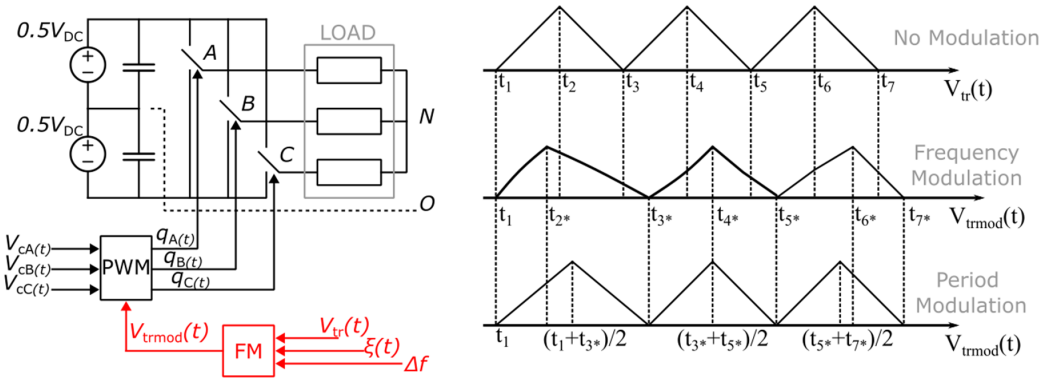


Fig. 8.3 (a)Sketch of the inverter schematic along with the PWM controller and the FM block in charge of the SS. (b)The triangular carrier is shown to highlight the difference among the unmodulated version and the FM and the Period modulated ones.

- The Period Modulation can be easily implemented at the hardware level by computing the slope of the triangular signal $V_{\text{trmod}}(t)$ at the beginning of each period, whereas it is still possible to adopt the mathematical theory developed for the Frequency Modulation.

Intensive PLECS simulations have been conducted to test the behavior of the three-phase inverter when spread-spectrum is introduced and the PLECS schematics are shown in Figure 8.4.

Thanks to the PLECS simulations, it is possible to notice that when the spread spectrum is properly applied (i.e., the frequency deviation Δf and the frequency of the modulating signal $\xi(t)$, are properly chosen) the power converter performance is almost unaltered with respect to the unmodulated case. It means that the converter efficiency, as well as the motor torque and the stability parameters, do not feature appreciable changes. It is therefore possible to conclude that, according to the simulation and measurement results, SS can be applied to the inverter without impairing its performance

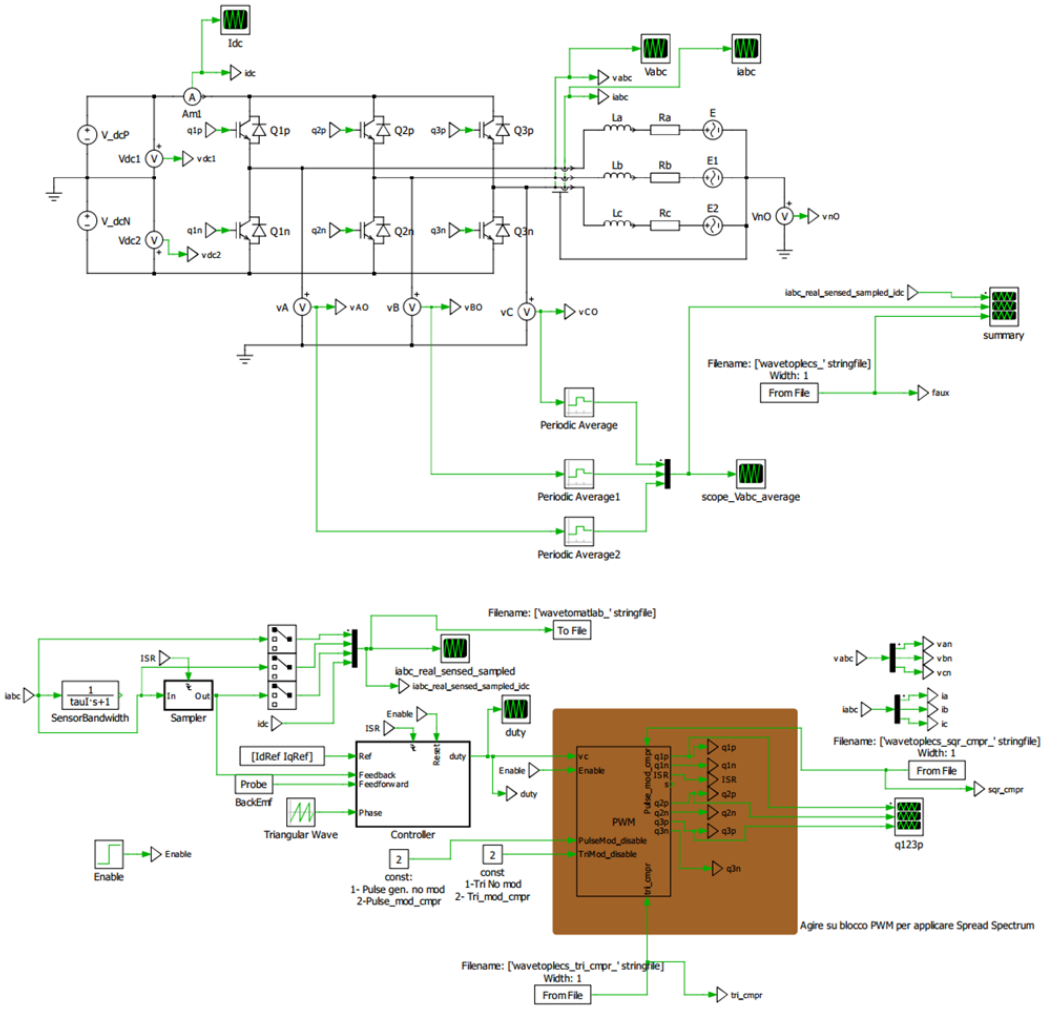


Fig. 8.4 Overview of the PLECS schematics

8.5 EMI spectrum of a 3-phase inverter under spread spectrum control model

According to international regulations, as in all relatively low-frequency devices, EMC has to be verified by measuring the level of interference propagated through the power supply line. This is the most effective way to consider EMI for frequencies lower than 30 MHz. Therefore, the focus is on the spectrum of the power supply current IDC, only, which is given by the sum of the three legs current I_A, I_B and I_C.

Under the assumption that the timing signal (i.e., as in Section 8.4, the triangular waveform at frequency f_c used for generating – either digitally or by means of an analog circuit- the PWM) has been frequency modulated using a frequency deviation Δf and a periodic driving signal $\xi(t)$ with frequency f_m, this signal will result in frequency modulated with the very same parameters, too. The main issue is that such a signal contains more spectral components with respect to the single tone of the sinusoidal case, considered in Section 8.3. In particular, this signal will present harmonics at the fundamental tone f_c and at all its harmonics nf_c.

In order to understand the shape of the spectrum of a generic signal $s(t)$, it is useful to consider the Fourier series expansion of a generic unmodulated signal $\Psi(t)$ with amplitude A_0, that reads as

$$s(t) = A_0\Psi(2\pi f_c t) = A_0\Psi_1\cos(2\pi f_c t + \phi_1) + A_0\Psi_2\cos(4\pi f_c t + \phi_2) + \cdots + A_0\Psi_n(2n\pi f_c t + \phi_n) + \cdots \tag{8.5.6}$$

For the sake of simplicity, the generic $s(t)$ signal can be considered as having a zero average value since the DC component is not meaningful in the Fourier Spectrum for EMI purposes. Each harmonic has a different power; the n-th harmonic has an associated power equal to $A_0^2\Psi_n^2/2$, i.e., proportional to the amplitude (squared) of the overall signal, and to a coefficient associated with the order of harmonic. Usually, the harmonic with the highest power is the first one ($n = 1$), whereas the associated power becomes negligible as n increases. Modulating such a signal is equivalent to perturbing the instantaneous phase $\phi(t)$ as considered in Section 3.2. The modulated signal reads as

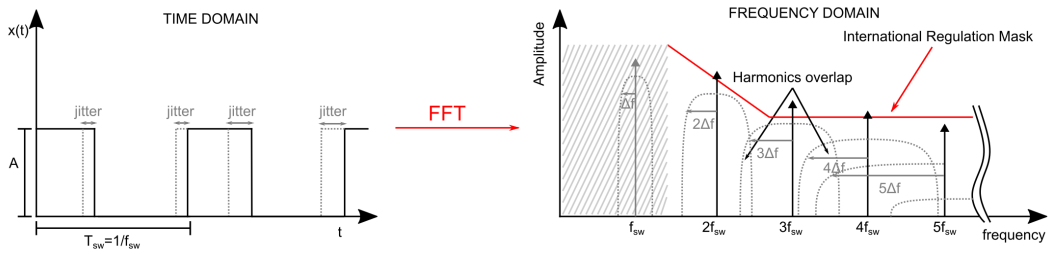


Fig. 8.5 Spreading of a generic signal. Lower order harmonics may be outside of the band of interest for the CISPR 25, whereas higher order harmonics may present overlapping between each other

$$s(t) = A_0\Psi(\phi(t)) = A_0\Psi_1\cos(\phi(t)+\phi_1) + A_0\Psi_2\cos(2\phi(t)+\phi_2) + \cdots + A_0\Psi_n(n\phi(t)+\phi_n) + \cdots \tag{8.5.7}$$

i.e., one can consider such a signal still composed of many components, each of them related to each harmonic of the unmodulated signal. The component generated from the n-th harmonics reads as follows

$$A_0\Psi_n\cos(n\phi(t)+\phi_n) = A_0\Psi_n\cos\left(2n\pi f_c t + 2n\Delta f\int_{-\infty}^{t}\xi(\tau)\phi(n)\right) \tag{8.5.8}$$

and can be considered as the frequency modulation of the n-th harmonic, using a frequency deviation equal to $n\Delta f$, but the same driving signal. So, the n-th harmonic is centered at nf_c and spread over a bandwidth $2n\Delta f$.

This situation has been highlighted in Figure 8.4 and from it, three main observations arise:

- The first harmonic (i.e., the fundamental tone with $n = 1$) is usually the one with the highest power (i.e., the one for which the SS is optimized) and most probably is not important if dealing with the CISPR 25 regulation since an oscillation frequency greater than 150 kHz is not common in high-power inverters. Therefore, in a scenario like this, it is important to identify which is the most problematic harmonic in terms of EMI and optimize the SS on it.

- All the harmonics have different modulation parameters. In particular, the n-th harmonic is modulated with a frequency deviation $n\Delta f$, so that the optimization, in accordance with the EMI receiver model analyzed in Section 8.3, may be different.
- At higher harmonics, since the width of the spreading bandwidth is increasing with the order of the harmonic n, overlapping (i.e., superpositioning) of the spread bandwidth related to different harmonics cannot be avoided. While this phenomenon is usually ignored in the most common SS applications, where the first harmonic only is considered, it may become relevant here in the neighborhood of the 150 kHz CISPR frequency limit.

In other words, the identification of the worst case (i.e., the location of the highest peak in the EMI spectrum) is not always straightforward, as well as the choice of the SS optimization parameters, at higher frequencies when the harmonics overlap. An approximated procedure for the peak amplitude identification in the signal power spectrum is proposed in order to make the worst-case identification easier.

8.5.1 Amplitude of harmonics in a variable duty-cycle square wave

The PWM driving signal of each leg is a square wave with duty-cycle D and its value changes in time to generate the three iso-frequential sinusoidal waveforms of the three inverter legs, phase-shifted of $2\pi/3$. The variation range of D depends on the load, which is usually an unknown variable. Furthermore, the signal of interest for the conducted EMI emission (i.e., the *IDC* current) is given by the superposition of the three legs current signals, each of them approximately equal with the same shape of the square wave controlling the leg. Therefore, the analytical prediction of the *IDC* current spectrum is not straightforward.

Nevertheless, it is possible to shift the focus on a generic square wave with unknown duty-cycle D and consider its spectrum from a statistical point of view, assuming D is a random variable with a given distribution. By considering the generic square-wave signal $\Psi(t)$ with amplitude A_0, it yields

$$s(t) = A_0\Psi(2\pi f_c t) \tag{8.5.9}$$

that is the same definition mentioned at the beginning of Section 8.4 for a generic signal. For the sake of simplicity, $\Psi(t)$ can also be considered as having a zero average value since the zero-frequency component is not meaningful for the EMI Fourier Spectrum. According to the Fourier theory, the amplitude of the n-th harmonic of $\Psi(t)$ is

$$\Psi_n = \frac{2}{n\pi} sin(n\pi D), n \in N \tag{8.5.10}$$

and its related power

$$\frac{\Psi_n^2}{2} = \frac{2}{n^2\pi^2} sin^2(n\pi D), n \in N \tag{8.5.11}$$

suggesting that the amplitude and power of the harmonics in a square waveform will decay as $1/n$ and $1/n^2$, respectively, being n the harmonic number, again. Considering that the value of D is unknown, the power of the n-th harmonic can be estimated by considering its expected value over different values of D. By assuming D as a statistical variable uniformly distributed in the interval $[0,1]$, the expected value of the power associated with the n-th harmonic of $s(t)$ is defined as

$$E_n\left[A_0^2 \frac{\Psi_n^2}{2}\right] = \int_0^1 A_0^2 \frac{2}{n^2\pi^2} sin^2(n\pi D) dD = \frac{A_0^2}{n^2\pi^2} \tag{8.5.12}$$

Assuming that it is reasonable to approximate the power of each harmonic of a square wave with a function that decreases as $1/n^2$, and since the *IDC* can be approximated as the sum of three square-wave functions, it is also reasonable to approximate the power of all the *IDC* harmonics as function that decreases as $1/n^2$. Therefore, the power of the generic harmonic reads as

$$k^H \frac{A_0^2}{n^2} \tag{8.5.13}$$

where k^H is a proper constant, and A_0^2 relates the power of the harmonics to the amplitude of the signal. This is the relation that links the amplitude of the current set by the load to the *IDC*.

In order to experimentally verify these assumptions, the *IDC* current coming from the PLECS simulation has been loaded into an arbitrary waveform generator, and

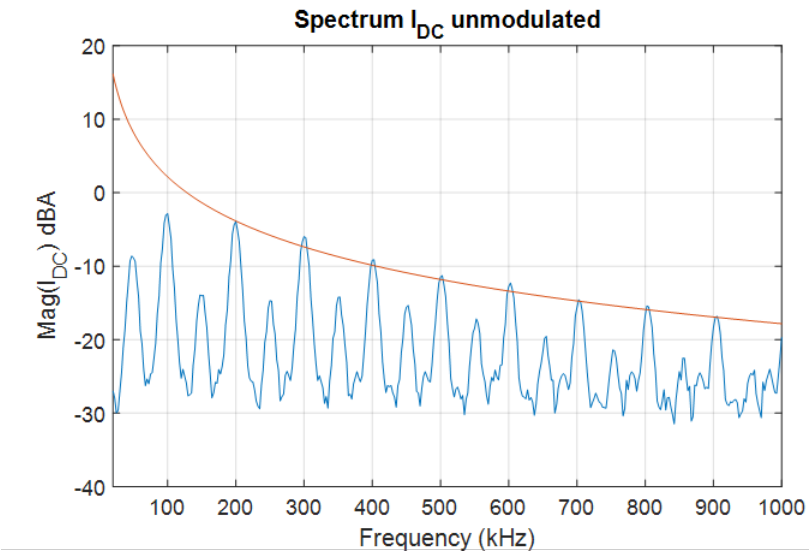


Fig. 8.6 IDC simulated and exported to the spectrum analyzer, compared with the $1/n^2$ decay (in power).

Table 8.5.1 Spread Spectrum modulation parameters

Harmonic order	1st	2nd	3d	4th	5th	6th
Modulation Index	m	$2m$	$3m$	$4m$	$5m$	$6m$
Normalized Resolution	ρ	$\rho/2$	$\rho/3$	$\rho/4$	$\rho/5$	$\rho/6$

its spectrum has been measured with a spectrum analyzer and shown in Figure 8.6. The $1/n^2$ trend well approximates the envelope of the power of harmonics at high frequencies and this results very important in the following.

8.5.2 Short-term effects on different harmonics

Being all harmonics in a spread spectrum generic signal modulated with different parameters, it is worth investigating how optimization according to the measurement conditions is achieved for the different harmonics. In particular, two parameters are fundamentals in the short-term effect optimization, i.e., the modulation index $m = \Delta f / f_m$ and the normalized resolution $\rho = \mathrm{RBW}/\Delta f$. Indicating with m and ρ the value of these quantities for the first harmonic, and recalling that the frequency deviation for the n-th harmonic is $n\Delta f$ whereas other parameters are unchanged, each harmonic is modulated according to the following parameters.

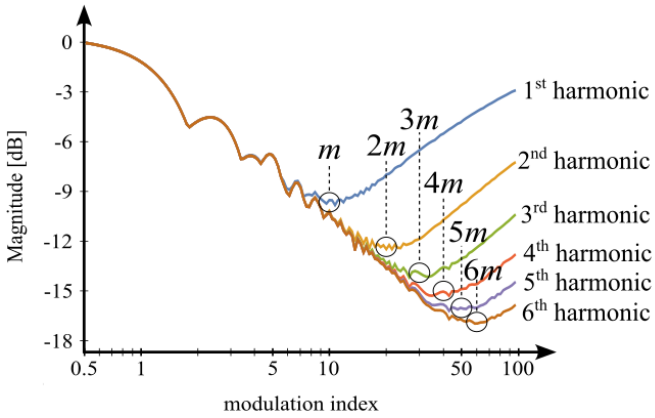


Fig. 8.7 Optimization curves for the short-time effect for different harmonics

Interestingly, in Figure 8.7 the optimization curves for an example case that considers the first six harmonics, along with their different optimization curves with a normalized resolution from $\rho = 0.06$ to $\rho/6 = 0.01$, is shown. Each curve represents the expected reduction in the peak amplitude of the spectrum associated with the n-th harmonic when the spread spectrum is applied, with respect to the amplitude of the harmonic when no spreading is added (i.e., narrow-band spectrum). The optimum point is reached for different values of the modulation index m, as expected. However, the optimum point is obtained for a value of the modulation index that is linearly increasing with the number of the harmonic. The result is that all harmonics are optimized for the same set of parameters, i.e., when the first harmonic is optimized, all others are optimized, as well.

Furthermore, it is also possible to notice that, the higher the order of the harmonic n, the higher the expected reduction in the peak of the power spectrum (mainly due to the increase of the spreading bandwidth, given by $2n\Delta f$). However, the mathematical theory that explains the EMI reduction for each harmonic does not allow one to read a straightforward mathematical expression regulating the expected reduction in power.

Nevertheless, in Figure 8.8 it has been plotted the expected power reduction in the optimal point (i.e., the one that features the minimum peak reduction) for a sufficiently large number of harmonics and by keeping the same set of parameters considered in Figure 8.7. Each blue point represents the expected EMI reduction $R_n^{S.T.}$ for the n-th harmonic considering the short-term effects. The trend is somehow regular, and the value of the EMI reduction can be approximated by

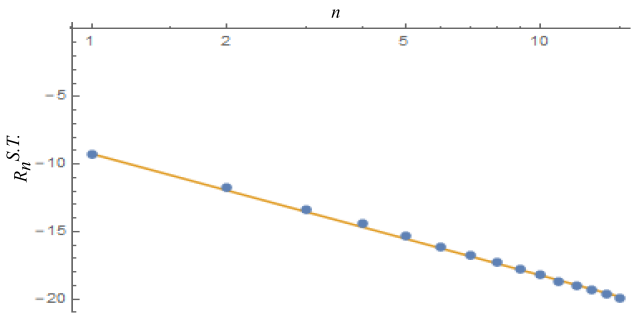


Fig. 8.8 Trend for the reduction of the generic n-th harmonic

$$R_n^{S.T.} \approx R_1^{S.T.} \frac{k^{S.T.}}{n^{\alpha}}, \alpha \in [0.8, 1] \tag{8.5.14}$$

in which $R_n^{S.T.}$ is the reduction of the first harmonic, and $k^{S.T.}$ is a constant to be set for a better matching (usually ≈ 1). The value of α is experimentally proven to be between 0.8 and 1, but in the majority of the cases, the observed value is $\alpha \approx 0.9$, which will be considered as a reference value.

8.5.3 Harmonics Overlap Estimation

When the spread spectrum is applied, overlapping between the n-th harmonic and the (n+1)-th harmonic is possible if n is sufficiently high. It is important to remind that that:

- The spectrum of the n-th harmonic is a discrete spectrum with components at frequencies $nf_c + kf_m$ with $k = 0, \pm 1, \pm 2, \ldots$ and have a band approximately ranging from $nf_c - n\Delta f$ to $nf_c + n\Delta f$.
- The spectrum of the (n+1)-th harmonic is a discrete spectrum with components at frequencies $(n+1)f_c + lf_m$ with $l = 0, \pm 1, \pm 2, \ldots$ and have a band approximately ranging from $(n+1)f_c - (n+1)\Delta f$ to $(n+1)f_c + (n+1)\Delta f$.

Superposition between these two harmonics occurs if $nf_c + n\Delta f > (n+1)f_c - (n+1)\Delta f$, i.e., $n > (f_c - \Delta f)/(2\Delta f)$. Therefore, for the computation of the resulting signal, two different cases must be considered:

- The two spectral components have different frequencies, but their difference is sufficiently small that the two components cannot be distinguished due to the limited resolution of the measurement. In this case, assuming the power of the first component to be $A^2/2$ and the power of the second one is $B^2/2$, it yields

$$Acos(2\pi f_A t + \phi_A) + Bcos(2\pi f_B t + \phi_B) \tag{8.5.15}$$

  Therefore the measured power will be $A^2/2 + B^2/2$.

- The two spectral components have the same frequency. In this case, the sum of two iso-frequential sinusoidal signals must be considered. It follows that

$$Acos(2\pi ft + \phi_A) + Bcos(2\pi ft + \phi_B) = Ccos(2\pi ft + \phi_C) \tag{8.5.16}$$

  in which the power of the two tones is $A^2/2$ and $B^2/2$, and the phase is ϕ_A and ϕ_B, respectively. This case gives rise to a sinusoidal tone, the amplitude of which is $C = \sqrt{A^2 + B^2 + 2AB\cos(\phi_B - \phi_A)}$.

  Since the phase $\phi_B - \phi_A = \phi$ is unknown, a random variable ϕ can be considered, and the expected value can be computed. Assuming a uniform distribution in $[0, 2\pi]$ for the random variable ϕ, the power of the resulting sinusoidal will be be

$$\frac{C^2}{2} = \frac{1}{2}E_\phi[A^2 + B^2 + 2ABcos\phi] = \frac{1}{2}\int_0^{2\pi}(A^2 + B^2 + 2ABcos\phi)\frac{d\phi}{2\pi} = \frac{A^2}{2} + \frac{B^2}{2} \tag{8.5.17}$$

In results in both cases it is reasonable to assume that when two (or more) components are superimposed, the total power can be calculated as the the sum of the power of the original components.

8.5.4 Theory Validation

This simplified analysis above becomes extremely helpful in estimating the spectrum when the SS is used and the higher harmonics overlap must be considered. Under

the assumption that the power of the harmonics of the *IDC* decreases as $1/n^2$ (i.e., the theory cannot be applied otherwise), it is possible to assume that

- The n-th harmonic is spread over a bandwidth $[n(f_c-\Delta f), n(f_c+\Delta f)]$. For the sake of simplicity, the power spectrum is considered constant and with a level that is equal to the power of the n-th harmonic. Furthermore, the reduction at the n-th harmonic when the SS is applied takes into account the short-term effect. It yields that

$$A_0^2\frac{\Psi_n^2}{2}R_n^{S.T.} \approx k^H\frac{A_0^2}{n^2}R_1^{S.T.}\frac{k^{S.T.}}{n^\alpha} = k^H k^{S.T.}A_0^2R_1^{S.T.}\frac{1}{n^{2+\alpha}} \tag{8.5.18}$$

- When two (or more) harmonics are overlapping, it is sufficient to consider, in the intersection interval, a power equal to the sum of the power of the harmonics, assumed constant all over the spread bandwidth.

- As the number of harmonic n increases, the number of intervals that overlap is also increasing. This may be a problem due to the increasing power. Indeed, with the developed model, it is possible to prove that even considering the worst-case scenario, in which an infinite number of harmonics overlap, the total power is still limited. If all the harmonics from the k-th onwards overlap at the same time, the power can be calculated by considering the Hurwitz Zeta function ζ, implicitly defined as

$$\sum_{n=k}^{\infty} k^H k^{S.T.}A_0^2R_1^{S.T.}\frac{1}{n^{2+\alpha}} = k^H k^{S.T.}A_0^2R_1^{S.T.}\sum_{n=k}^{\infty}\frac{1}{n^{2+\alpha}} = k^H k^{S.T.}A_0^2R_1^{S.T.}\zeta(2+\alpha,k) \tag{8.5.19}$$

  and the $\zeta(2+\alpha,k)$ is a decreasing function in k for any value of α, with a trend very similar to $1/k^2$.

This mathematical background has been validated by performing measurements on a simple setup. A standard sawtooth at $f = 150$ kHz and its spread counterpart (using frequency-modulation with triangular deriving signal) with $f_m = 9$ kHz and $\Delta f = 25$ kHz has been measured with a Spectrum Analyzer. The sawtooth waveform has been selected as its Fourier series expansion is such that the power of the harmonics decreases as $1/n^2$. The measurements have been exported and plotted in

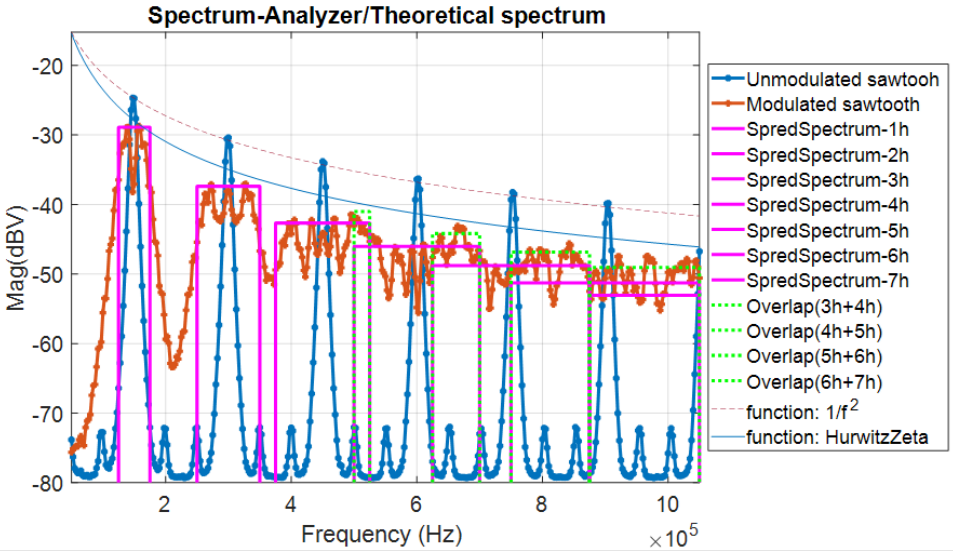


Fig. 8.9 FFT of a sawtooth, along with its modulated version. The rectangles represent the estimated peaks after modulation

Figure 8.9 with the blue and orange colors, respectively. By applying the previously explained theory, the peak reduction of the harmonic amplitude can be foreseen both when the harmonic overlap is present and when it is not. As a matter of fact, the rectangles colored in magenta simplify the spread area when the single tone is spread with $\Delta f_n = n25$ kHz across the n-th tone. On the other hand, the green one well predicts what happens in the overlap area

In Figure 8.9, it is also possible to detect the $1/n^2$ decay of the power of the harmonics as well as the decreasing trend of the cumulative sum depending on the Hurwitz Zeta function ζ, previously described. If for instance, the focus is on the overlap between the third and the fourth harmonics, the cumulative sum considers the pessimistic case in which all the harmonics from the third one onwards are summing up (i.e., overlapping), highlighting that the considered overlap will be the higher one.

8.5.5 Application of the theory

In order to apply the theoretical analysis explained in the previous subsections, the application of the inverter must be properly defined. Only after the definition of the application, the international regulations to be compliant with can be chosen.

Accordingly, the range of harmonics that must be carefully analyzed is fixed, as well as the spectrum analyzer parameters that must be adopted for the measurement.

At this point, the harmonics of the voltage waveform under test can be analyzed and the SS can be applied to reduce the higher peak. As earlier explained, the application of SS can lead to the harmonics overlap phenomenon so that the higher peak may be the combination of more spectra, whose contribution can still be reduced by applying the right optimization parameters.

The analysis proposed in the previous sections can be used to quickly identify which part of the spectrum is the most problematic. A guideline with the suggested step is described in the following:

- The harmonics power is assumed to decrease as $1/n^2$. This assumption is useful to proceed with a statistical analysis for the EMI reduction with SS is applied. The real mathematical law that describes how the power of the harmonics decreases depends on the inverter operating point. Therefore, this results in the only way to provide a general approach.
- The harmonics that fall in the bandwidth of interest (i.e., according to international regulations) must be considered. As an example, the harmonics from 3rd one onward may be considered. For a rough calculation, a finite number of harmonics, such as the ones from the 3rd to the 6th, is considered.
- For all these harmonics (i.e., from the 3rd to the 6th), the expected EMI power level can be computed according to the given formulas.
- If overlap arises in the spectrum among the considered harmonics, the expected power can also be calculated according to the formulas (e.g., the power of the overlap between 3rd and 4th harmonics, the one between 4th and 5th, and so on so forth).
- By comparing the computed values, it is possible to identify which part of the spectrum is, is with the highest probability, the one with the highest peak. In order to understand what happens to the higher part of the spectrum (i.e., the harmonics that are not considered in the previous steps) one can exploit the Hurwitz Zeta function that evaluates the worst-case scenario in which all the harmonics, from a certain one onwards overlap. For example, $\zeta(2+\alpha,6)$ indicates the value of the peak resulting from the superposition of all the

harmonics from the 7th onwards). When the $\zeta(2+\alpha,n)$ will be lower than the peak, all the harmonics from harmonic n+1 onward will be negligible in terms of EMI, confirming that there will be no peaks higher than the identified one in the upper part of the spectrum.

In the example of Figure 8.9, assuming that the first two harmonics are not of interest, and so limiting the analysis to the harmonics from the 3rd to the 6th, the expected peak is given by the superpositioning of the 3rd and 4th harmonics. The level of the Hurwitz Zeta function at n=6 (i.e., the value at the center frequency of the 6th harmonic in the plot) is lower with respect to this value (i.e., the one given by the overlap between 3rd and 4th harmonics), so no peaks are expected in the upper part of the spectrum.

8.6 Conclusion

In this chapter, an overview of the spread spectrum technique for EMI reduction is provided, taking into account the limited state-of-the-art coverage for three-phase circuits. The developed mathematical theory demonstrates SS effectiveness in three-phase inverters and tackles high-frequency optimization challenges, specifically, the harmonics overlap phenomenon.

Chapter 9

Spread Spectrum in Talkative Power Converters

9.1 Introduction

Power electronic converters have become a universal tool for interconnecting different loads and sources owing to their control and signal processing peculiarities in power conversion. Thereby power converters have been used to transmit and receive digital data acting as a transceiver [159]. A basic sketch is represented in Figure 9.1(a). The PWM carrier signal was used in [160] for the first time to create communication among different DC power supplies. A complete analysis and analogy of the time and frequency domain for such a converter was given in [161]. However, the implementation of new functions into power converters is severely restricted by EMI regulations and there is limited study on the EMI compatibility of the modulations applied to Talkative Power Converters (TPC) and the EMI performance (related to TPC) remains a challenge.

EMI reduction can be achieved both at the Hardware (HW) and Software (SW) levels. HW methodologies for EMI reduction aim at reducing the coupling path between the source and the victim with shielding (for radiated emissions) or filtering (for conducted emissions). Nevertheless, in many situations, these approaches cannot be taken into account (e.g., the source and the victim share the same board) and ad-hoc solutions must be employed. Furthermore, HW approaches are usually characterized by very low flexibility: if the interference exceeds the prescribed

limits, the hardware is not able to comply with the regulations anymore and must be redesigned.

Therefore, in order to address this issue, EMI methods based on SW algorithms, capable of reducing the EMI by avoiding extra HW elements, have been developed. Among these, the dithering ones that also go under the name of Spread Spectrum (SS) techniques [157], come into play. The main idea grounding this technique is the introduction of jitter in the synchronization signal to avoid the perfect periodic behavior of all waveforms in the circuit, thus spreading the power of their spectral component over a bandwidth that depends on the circuit characteristics. Interestingly, this technique can be considered as an additional methodology with respect to the HW ones.

To the best of my knowledge, SS was applied in TPC, recently, to reduce the amplitude level of the harmonics in [162], where a bit expansion method has been proposed to realize a direct sequence SS technique. Nevertheless, the focus is on the harmonics from a theoretical perspective by neglecting some important parameters that must be considered for a real EMI optimization analysis.

The parameters that are defined by the regulations (i.e., the resolution bandwidth RBW) and the ones that take into account the real victim circuit (i.e., short-time effect) directly impact the SS modulation parameters such as modulation frequency (and consequently the TPC bit rate) and EMI attenuation.

The motivation of this research is to tackle the shortcomings of the literature in regard to the EMI compatibility of TPC and allow a straightforward EMI-aware TPC design by giving guidelines that take into consideration the EMI international regulation specification. An SS modulation technique by means of a B-FSK (i.e., SS-B-FSK) is presented (and sketched in Figure 9.1b) and optimized concerning the EMI when the converter is transmitting only bits "0" or "1". Therefore, the EMI can be effectively attenuated, disregarding the converter data sequence as in [163] and by considering the RBW (fixed by international regulation) and the short-time effect. Theoretical analysis and preliminary experimental results are provided to validate the proposed method.

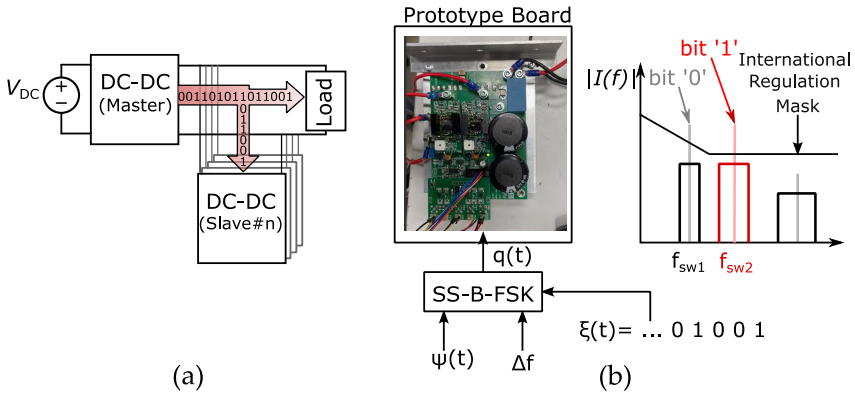


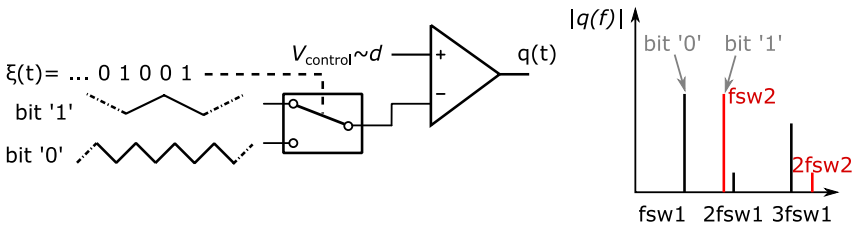
Fig. 9.1 (a) TPC basic block scheme. (b) Sketch of the proposed SS-B-FSK to allow EMI reduction in order to spread the power of the single tone, associated with the stream of bit $\xi(t)$. $\Psi(t)$ and Δf are the FSK parameters that allow the $2\Delta f$ spread across the single tone at f_{sw1} and f_{sw2}. An example of an International Regulation Mask is also drawn to highlight how the SS can allow EMI compliance.

9.2 Talkative Power Converter Communication

The basic principle employed in Talkative Power Converter systems is based on the modulation of the converter switching frequency. In particular, a continuous-phase frequency-shift keying (FSK) modulation is considered. According to this approach, the output instantaneous frequency is changed according to the symbol to be transmitted. For the sake of simplicity, this work has been limited to the Binary FSK (B-FSK) case, where all the transmitted symbols may be either 0 or 1. In this section, the basic B-FSK theory is introduced and then extended to improve the EMC performance by applying the SS. The B-FSK with the addition of the SS will be called SS-B-FSK.

9.2.1 B-FSK

The B-FSK is a well-known modulation, usually employed for its limited complexity and good system robustness, where all transmitted symbols may be either 0 or 1, and the output instantaneous frequency assumes, respectively, the two values f_0 or f_1. Furthermore, this modulation is equivalent to an analog frequency modulation, i.e., in the case of a sinusoidal tone



(a) (b)

Fig. 9.2 (a) Sketch of the PWM generation according to the classical B-FSK. The stream of bits is used to drive a switch which selects the appropriate carrier. The FFT associated with the driving PWM signal $q(t)$ is shown in (b).

$$s(t) = A_0 \cos(2\pi f_c t + 2\pi\Delta f \int_{-\infty}^{t} \xi(\tau)\, d\tau) \tag{9.2.1}$$

where $\xi(\tau) \in \{0, +1\}$ is the binary driving signal embedding the succession of symbols to be transmitted, f_c is the carrier frequency, and Δf is the frequency deviation. The output signal instantaneous frequencies are given by $f_0 = f_c - \Delta f$ and $f_1 = f_c - \Delta f$.

This approach results in a straightforward implementation since the connection of a B-FSK modulator to a DC-DC converter consists of applying the modulation on the triangular waveform used for the PWM generation [157] as in Fig. 9.2(a). To generate the PWM signal in a DC-DC converter, the reference control voltage is compared to the triangular waveform. The communication is embedded in the fundamental tone of the triangular waveform and therefore of the PWM signal. It means that the triangular waveform switches from f_0 to f_1 when transmitting bit 0 or bit 1, respectively.

In [157], in which this methodology has already been applied, it is shown that an analog frequency modulation of the switching frequency, under the assumption that $\Delta f \ll f_c$, does not affect the DC-DC converter behavior, including efficiency and ripple amplitude (i.e., only the frequency of the ripple is changing). We can therefore conclude that the two switching frequencies, laying apart of a Δf must be sufficiently far to be easily identified as two different ones, and must be sufficiently close not to cause a meaningful drop in the converter efficiency.

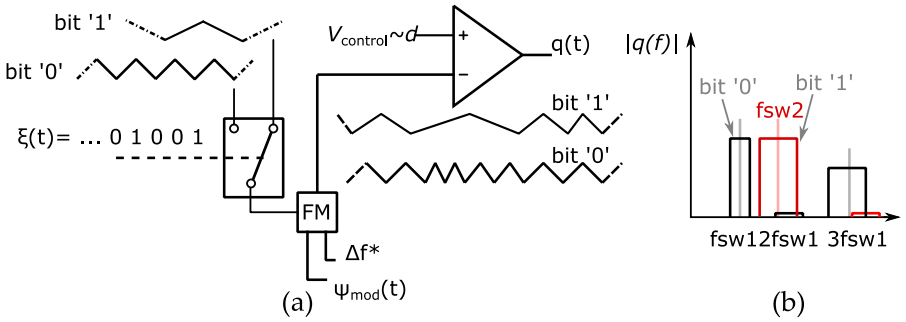


Fig. 9.3 (a) Sketch of the PWM generation according to the SS-B-FSK. To the B-FSK scheme represented in Figure 9.2(a) is added a further FM block in charge of spreading the signal. The FFT associated with the driving PWM signal $q(t)$ is shown in (b).

A modulation block like this can be simply represented as a bit-driven switch that lets the triangular carrier at frequency f_0, when the bit is 0, and the frequency f_1 when the bit is 1, pass. The basic block scheme describing this system is shown in Figure 9.2(a) along with the deriving effects in the frequency domain, in Figure 9.2(b).

9.2.2 SS-B-FSK

The implementation employed here grounds its roots in the B-FSK explained in the previous subsection. As a matter of fact, the basic idea is to spread the energy of the single tone either at f_0 or f_1, according to the SS theory, in a way that the single bit is represented by a frequency band (and not by a single tone) around f_0 or f_1. If the SS is correctly employed, the amplitude of the harmonics will be lower so that the system features improved EMI capabilities.

Likewise the previous case, the modulation is applied to the triangular waveform used to create the PWM signal. In particular, a second FM block is cascaded to the previous one. According to the SS theory explained in Section 8.3 of the previous chapter, this modulation must be sufficiently slow to get the desired EMI reduction and sufficiently fast to avoid the short-time effect mentioned in [157, 158]. For a comprehensive analysis of the SS optimal parameters choice, [17] continues to be considered as a reference.

Accordingly, by adding a second modulation step, (9.2.1) becomes

$$s(t) = A_0 \cos(2\pi f_c t + 2\pi\Delta f \int_{-\infty}^{t} \xi(\tau)\, d\tau + 2\pi\Delta f^* \int_{-\infty}^{t} \psi(\tau)\, d\tau) \tag{9.2.2}$$

where $\Psi(t) \in [-1,1]$ is the modulating signal for the Spread Spectrum that allows the spreading of the tone at f_0 in the bandwidth $[f_0 - \Delta f^*, f_0 + \Delta f^*]$, for bit 0, and the spreading of the tone at f_1 in the bandwidth $[f_1 - \Delta f^*, f_1 + \Delta f^*]$, for bit 1. It is important to notice that, on the one hand, $\xi(t)$ is a square waveform that assumes either the value 0 or the value 1 according to the bit-stream. On the other hand $\Psi(t)$ is in charge of properly spreading the signal and for this reason, according to [17] is a triangular waveform.

According to [17], when the aim is to comply with a certain regulation, the optimization parameters can be chosen only after the RBW is defined. It means that the RBW cannot be considered as a degree of freedom, and therefore chosen as the smallest possible bandwidth to increase the EMC performance. Furthermore, the modulation frequency cannot be considered as the smallest possible frequency to arbitrarily reduce the harmonics content since at a certain point their reduction effect is null due to the short-time effect. The first thing to do is to fix the frequency deviation Δf keeping into account that, on the one hand, the larger the Δf, the more the EMI reduction. On the other hand, if Δf is exceptionally large, the overlap between the bands representing the two bits is likely to happen (as described in Chapter 8) as well as an efficiency drop in the converter behavior.

If Δf is considered to be the 10% of the carrier frequency (i.e., the triangular at f_0 or f_1), the optimal modulation index m_{opt} is approximately $\Delta f/\text{RBW}$ according to [17] and therefore the optimal modulation frequency f_m of $\Psi(t)$ can be calculated as $\Delta f/m_{\text{opt}}$. It can be straightforwardly seen that f_m is limited by the RBW.

The basic block scheme describing this system is shown in Figure 9.3(a) along with the effects in the frequency domain, in Figure 9.3(b).

Measurements have been performed on a buck converter going from 48 V to 24 V (4 A) switching from $f_{\text{sw}} = 20\,\text{kHz}$ to $f_{\text{sw}} = 30\,\text{kHz}$ when transmitting bit 0 and bit 1, respectively.

Eventually, SS with a sideband deviation Δf equal to 10% of f_{sw} has been applied to achieve a reduction in the EMI spectrum of the buck inductor and at the same time

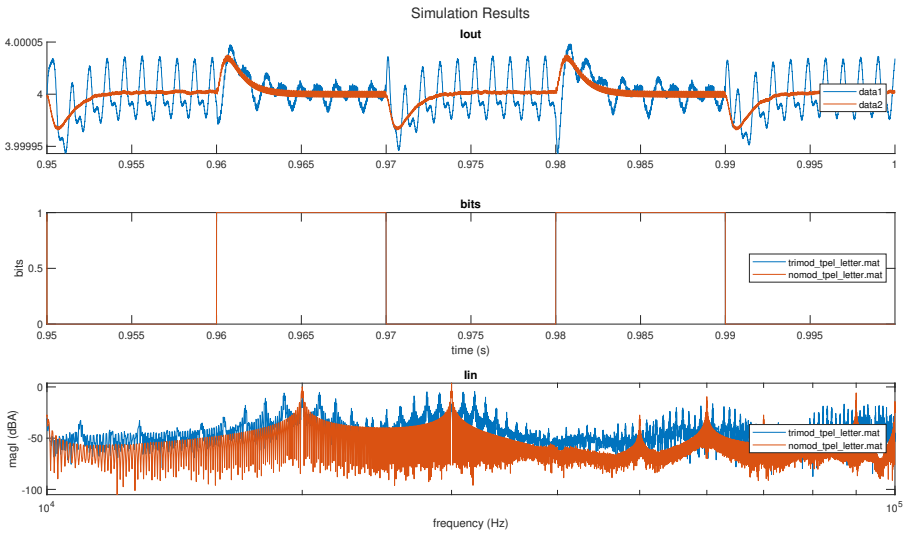


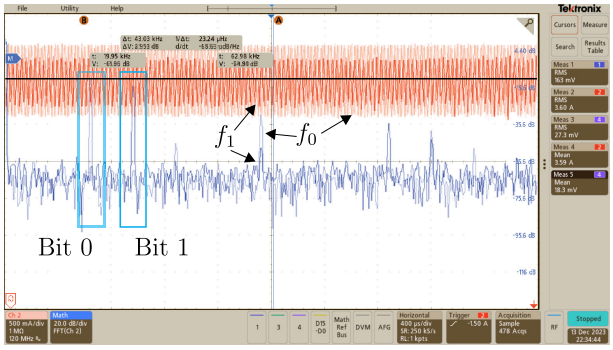
Fig. 9.4 Simulation results showing from top to bottom: the output current (time domain), the train of pulses (i.e., the bits) and the FFT of the input current. The blue color is associated with the SS while the orange color to the non-spread waveforms.

not to alter the working principle of the whole converter. This choice is also in line with the fact the harmonics spectra referring to the two bits should not overlap.

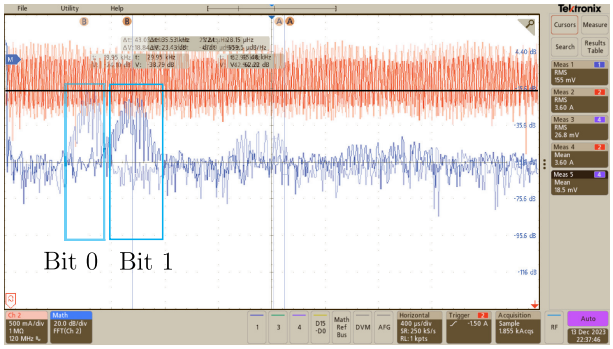
The system used has been optimized over an RBW of 1 kHz, just used for the proof of concept. The modulation frequency has been chosen accordingly to be $f_m = 1\,\text{kHz}$ (i.e., $\approx RBW$).

The system has been simulated in PLECS and the results are shown in Figure 9.4. In the first plot of Figure 9.4, the time domain waveforms of the output current both when SS is applied (i.e., blue curves) and when it is not (i.e., orange curves), are shown. The second plot shows the train of pulses (i.e., the bits), and the last one is the FFT of the input current (that usually must be under control in the EMI field).

Then, preliminary measurements are performed on the prototype by means of an oscilloscope Tektronix MDO34 which features a dedicated spectrum analyzer channel. The oscilloscope screenshots of the inductor current, along with the FFT, both when transmitting bits '0' and '1' are shown in Figure 9.5. The two measurements are performed with the classical B-FSK (i.e., Figure 9.5(a)) and with the proposed SS-FSK (i.e., Figure 9.5(b)).



(a)



(b)

Fig. 9.5 Experimental results for B-FSK TPC: (a) without SS (i.e., B-FSK) and (b) with SS (i.e., SS-B-FSK). In both cases, it is possible to identify the two bits highlighted in the blue rectangle. The time domain waveforms of the output current are represented in red, as well as the 4 A mean value (in black).

9.3 Conclusion

Spread-Spectrum Binary Frequency-Shift Keying (SS-B-FSK) was proposed to attenuate effectively the EMI in Talkative Power Converters (TPC). The signal power distribution can be separately carried out when the converter is encoding bit "0" or "1". The proposed technique was applied to a synchronous converter. The theoretical foundations were developed and the effectiveness of the proposed techniques was validated over a 48 V to 24 V (4 A) power converter switching from $f_{sw} = 20\,\text{kHz}$ to $f_{sw} = 30\,\text{kHz}$ when transmitting bit 0 and bit 1, respectively.

Publications

[1] Andrea Celentano, Fabio Pareschi, Victor R. Gonzalez-Diaz, Riccardo Rovatti, and Gianluca Setti. A Methodology for Practical Design and Optimization of Class-E DC-DC Resonant Converters. *IEEE Access*, pages 205568–205589, 2020.

[2] Andrea Celentano, Fabio Pareschi, Victor R. Gonzalez-Diaz, Riccardo Rovatti, and Gianluca Setti. Analytical approach for the design of class-E dc-dc resonant converters: Matlab software and datasets, 2020. doi: 10.5281/zenodo.3898565.

[3] Andrea Celentano, Fabio Pareschi, Riccardo Rovatti, and Gianluca Setti. A zero-transient dual-frequency control for class-E resonant DC-DC converters. *IEEE Transactions on Power Electronics*, pages 1–11, 2022.

[4] Fabio Pareschi, Andrea Celentano, Mauro Mangia, Riccardo Rovatti, and Gianluca Setti. Through-The-Barrier Communications in Isolated Class-E Converters Embedding a Low-K Transformer. In *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5, October 2020.

[5] Andrea Celentano, Fabio Pareschi, Virgilio Valente, Riccardo Rovatti, Wouter A. Serdijn, and Gianluca Setti. A Comparison between Class-E DC-DC Design Methodologies for Wireless Power Transfer. In *Inter. Midwest Symp. on Circ. and Systems*, pages 71–74, August 2021.

[6] Andrea Celentano, Carmine Paolino, Fabio Pareschi, Luca Callegaro, Riccardo Rovatti, and Gianluca Setti. Mutual Inductance Measurement in Wireless Power Transfer Systems Operating in the MHz Range. *IEEE Transactions on Circuits and Systems II: Express Briefs*, pages 1–1, 2023.

[7] Andrea Celentano, Fabio Pareschi, Virgilio Valente, Riccardo Rovatti, Wouter A. Serdijn, and Gianluca Setti. A Wireless Power Transfer System for Biomedical Implants based on an isolated Class-E DC-DC Converter with Power Regulation Capability. In *63rd Intern. Midwest Symp. on Circ. and Systems*, pages 190–193, August 2020.

[8] Andrea Celentano, Carmine Paolino, Fabio Pareschi, Virgilio Valente, Riccardo Rovatti, Wouter A. Serdijn, and Gianluca Setti. A Primary-side Maximum Efficiency Transfer Solution in Wireless Power Transfer Systems: Theory and Validation. *TechRxiv Preprint*, 2023.

References

[9] N.O. Sokal and A.D. Sokal. Class E-A new class of high-efficiency tuned single-ended switching power amplifiers. *IEEE J. Solid-State Circuits*, 10(3):168–176, June 1975.

[10] R.J. Gutmann. Application of RF Circuit Design Principles to Distributed Power Converters. *IEEE Trans. Ind. Electron. and Control Instr.*, IECI-27(3):156–164, August 1980.

[11] R. Redl, Bela Molnar, and N.O. Sokal. Class E Resonant Regulated DC/DC Power Converters: Analysis of Operations, and Experimental Results at 1.5 MHz. *IEEE Trans. Power Electron.*, PE-1(2):111–120, April 1986.

[12] K. H. Liu, R. Oruganti, and F. C. Y. Lee. Quasi-resonant converters-topologies and characteristics. *IEEE Trans. Power Electron.*, PE-2(1):62–71, January 1987.

[13] M.K. Kazimierczuk and J. Jozwik. Resonant DC/DC converter with class-E inverter and class-E rectifier. *IEEE Trans. Ind. Electron*, 36(4):468–478, November 1989.

[14] J.M. Rivas, R.S. Wahby, J.S. Shafran, and D.J. Perreault. New Architectures for Radio-Frequency DC-DC Power Conversion. *IEEE Trans. on Power Electron.*, 21(2):380–393, March 2006.

[15] D.J. Perreault, Jingying Hu, J.M. Rivas, Yehui Han, O. Leitermann, R.C.N. Pilawa-Podgurski, A. Sagneri, and C.R. Sullivan. Opportunities and Challenges in Very High Frequency Power Conversion. In *24th annu. IEEE applied power electronics conf. and expo. (APEC2009)*, pages 1–14, February 2009.

[16] Marian K. Kazimierczuk and Dariusz Czarkowski. *Resonant Power Converters*. Wiley, 2nd edition, March 2011.

[17] Fabio Pareschi, Riccardo Rovatti, and Gianluca Setti. EMI Reduction via Spread Spectrum in DC/DC Converters: State of the Art, Optimization, and Tradeoffs. *IEEE Access*, 3:2857–2874, 2015.

[18] Marian K. Kazimierczuk. *RF Power Amplifiers*. Wiley, 2nd edition, November 2014.

[19] M. K. Kazimierczuk and J. J. Jozwik. Optimal topologies of resonant DC/DC converters. *IEEE Trans. Aerosp. Electron. Syst.*, 25(3):363–372, May 1989.

[20] Yuki Hirama and Hirotaka Koizumi. Class E Resonant Low dv/dt Rectifier Using Common Grounded Switch Controlled Capacitor. In *IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 1389–1393. IEEE, September 2019.

[21] T. Suetsugu and M. K. Kazimierczuk. Analysis of sub-optimum operation of class E amplifier. In *46th Midwest Symposium on Circuits and Systems (MWCAS)*, volume 3, pages 1071–1074, Vol. 3, December 2003.

[22] T. Suetsugu and M. K. Kazimierczuk. Design procedure of class-E amplifier for off-nominal operation at 50% duty ratio. *IEEE Trans. Circuits Syst. I, Reg. Papers*, 53(7):1468–1476, July 2006.

[23] X. Du, J. Nan, W. Chen, and Z. Shao. 'New' solutions of Class-E power amplifier with finite dc feed inductor at any duty ratio. *IET Circuits Devices Syst.*, 8(4):311–321, July 2014.

[24] H. Ueda and H. Koizumi. Class-e2 DC-DC converter with basic class-e inverter and class-e ZCS rectifier for capacitive power transfer. *IEEE Trans. Circuits Syst. II Express Briefs*, 67(5):941–945, May 2020.

[25] J.J. Jozwik and M.K. Kazimierczuk. Analysis and design of class-E^2 DC/DC converter. *IEEE Trans. Ind. Electron*, 37(2):173–183, April 1990.

[26] H. Sekiya and and T. Yahagi. Design of generalized class E^2 DC/DC converter. In *2002 IEEE International Symposium on Circuits and Systems (ISCAS)*, volume 3, pages III–III, May 2002.

[27] T. Nagashima, X. Wei, E. Bou, E. Alarcon, M. K. Kazimierczuk, and H. Sekiya. Steady-state analysis of isolated class-e^2 converter outside nominal operation. *IEEE Trans. Ind. Electron*, 64(4):3227–3238, April 2017.

[28] K. J. Herman and R. E. Zulinski. The infeasibility of a zero-current switching class-E amplifier. *IEEE Trans. Circuits Syst.*, 37(1):152–154, January 1990.

[29] H. Sekiya, T. Ezawa, and Y. Tanji. Design procedure for class E switching circuits allowing implicit circuit equations. *IEEE Trans. Circuits Syst. I, Reg. Papers*, 55(11):3688–3696, December 2008.

[30] G. Chen, Y. Deng, Y. Tao, X. He, Y. Wang, and Y. Hu. Topology derivation and generalized analysis of zero-voltage-switching synchronous DC-DC converters with coupled inductors. *IEEE Trans. Ind. Electron*, 63(8):4805–4815, August 2016.

[31] Nicola Bertoni, Giovanni Frattini, Roberto Massolini, Fabio Pareschi, Riccardo Rovatti, and Gianluca Setti. An Analytical Approach for the Design of Class-E Resonant DC-DC Converters. *IEEE Trans. Power Electron.*, 31(11):7701–7713, November 2016.

[32] J. W. Yang and H. L. Do. Soft-switching dual-flyback DC-DC converter with improved efficiency and reduced output ripple current. *IEEE Trans. Ind. Electron*, 64(5):3587–3594, May 2017.

[33] S. Park and J. Rivas-Davila. Duty cycle and frequency modulations in class-e DC–DC converters for a wide range of input and output voltages. *IEEE Trans. Power Electron.*, 33(12):10524–10538, December 2018.

[34] Fabio Pareschi, Nicola Bertoni, Mauro Mangia, Riccardo Rovatti, and Gianluca Setti. A Unified Design Theory for Class-E Resonant DC-DC Converter Topologies. *IEEE Access*, 7:83825–83838, 2019.

[35] Y. Li, X. Ruan, L. Zhang, J. Dai, and Q. Jin. Variable switching frequency ON–OFF control for class e DC–DC converter. *IEEE Trans. Power Electron.*, 34(9):8859–8870, September 2019.

[36] Y. Li, X. Ruan, L. Zhang, and Y. Lo. Multipower-level hysteresis control for the class e DC–DC converters. *IEEE Trans. Power Electron.*, 35(5):5279–5289, May 2020.

[37] J.M. Rivas, O. Leitermann, Yehui Han, and D.J. Perreault. A very high frequency DC-DC converter based on a class ϕ_2 resonant inverter. *IEEE Trans. Power Electron.*, 26(10):2980–2992, October 2011.

[38] A. Mediano and N.O. Sokal. A class-E RF power amplifier with a flat-top transistor-voltage waveform. *IEEE Trans. Power Electron.*, 28(11):5215–5221, November 2013.

[39] J. M. Burkhart, R. Korsunsky, and D. J. Perreault. Design Methodology for a Very High Frequency Resonant Boost Converter. *IEEE Trans. Power Electron.*, 28(4):1929–1937, April 2013.

[40] M. Hayati, A. Lotfi, M. K. Kazimierczuk, and H. Sekiya. Generalized design considerations and analysis of class-e amplifier for sinusoidal and square input voltage waveforms. *IEEE Trans. Ind. Electron*, 62(1):211–220, January 2015.

[41] Koenraad van Schuylenbergh and Robert Puers. *Inductive powering: Basic theory and application to biomedical systems*. Analog circuits and signal processing. Springer, Dordrecht, 2009.

[42] T. Nagashima, K. Inoue, X. Wei, E. Bou, E. Alarcón, M. K. Kazimierczuk, and H. Sekiya. Analytical design procedure for resonant inductively coupled wireless power transfer system with class-E^2 DC-DC converter. In *2014 IEEE international symposium on circuits and systems (ISCAS)*, pages 113–116, 2014.

[43] Ui-Gyu Choi and Jong-Ryul Yang. A 120 w class-E power module with an adaptive power combiner for a 6.78 MHz wireless power transfer system. *Energies*, 11(8):2083, 2018.

[44] Alexander Sutor, Martin Heining, and Rainer Buchholz. A class-E amplifier for a loosely coupled inductive power transfer system with multiple receivers. *Energies*, 12(6):1165, 2019.

[45] H. Oh, W. Lee, H. Koo, J. Bae, K. C. Hwang, K. Lee, and Y. Yang. 6.78 MHz wireless power transmitter based on a reconfigurable Class–E power amplifier for multiple device charging. *IEEE Trans. Power Electron.*, 35(6):5907–5917, June 2020.

[46] Fabio Pareschi, Nicola Bertoni, Mauro Mangia, Roberto G. Massolini, Giovanni Frattini, Riccardo Rovatti, and Gianluca Setti. Class-E isolated DC-DC converter with high-rate and cost-effective bidirectional data channel. *IEEE Trans. Power Electron.*, 35(5):5304–5318, 2020.

[47] Ying Li, Xinbo Ruan, Li Zhang, Jiandong Dai, and Qian Jin. Optimized Parameters Design and Adaptive Duty-Cycle Adjustment for Class E DC–DC Converter With on-off Control. *IEEE Trans. Power Electron.*, 34(8):7728–7744, August 2019.

[48] W. A. Tabisz, P. M. Gradzki, and F. C. Y. Lee. Zero-voltage-switched quasi-resonant buck and flyback converters-experimental results at 10 MHz. *IEEE Trans. Power Electron.*, 4(2):194–204, April 1989.

[49] Ignacio Ramos, María N. Ruiz Lavín, José A. García, Dragan Maksimović, and Zoya Popović. GaN Microwave DC–DC Converters. *IEEE Trans. Microw. Theory Techn.*, 63(12):4473–4482, December 2015.

[50] Yaoxia Shao, Chengbin Ma, and Ming Liu. A 6.78-MHz Class E^2 Converter with the Flexible DC-DC Voltage Ratio. In *13th IEEE Int. Conf. on Compatibility, Power Electr. and Power Eng. (CPE-POWERENG)*, pages 1–5, April 2019.

[51] Taufik, P. Luther, and M. Anwari. Digitally controlled ZVS quasi-resonant boost converter with M-type switch. In *2007 International conference on intelligent and advanced systems (ICIAS)*, pages 823–828, November 2007.

[52] R.C.N. Pilawa-Podgurski, A.D. Sagneri, J.M. Rivas, D.I. Anderson, and D.J. Perreault. Very-high-frequency resonant boost converters. *IEEE Trans. Power Electron.*, 24(6):1654–1665, June 2009.

[53] E. Firmansyah, S. Tomioka, S. Abe, M. Shoyama, and T. Ninomiya. A zero-current-switch quasi-resonant boost converter with transformer compensated clamp circuit. In *13th European conference on Power Electronics and applications (EPE)*, pages 1–8, September 2009.

[54] Ming-Jei Liu and Shawn S. H. Hsu. A Miniature 300-MHz Resonant DC–DC Converter With GaN and CMOS Integrated in IPD Technology. *IEEE Trans. Power Electron.*, 33(11):9656–9668, November 2018.

[55] J. M. Rivas, Y. Han, O. Leitermann, A. D. Sagneri, and D. J. Perreault. A high-frequency resonant inverter topology with low-voltage stress. *IEEE Trans. Power Electron.*, 23(4):1759–1771, July 2008.

[56] F. Pareschi, R. Blecic, M. Mangia, A. Baric, R. Rovatti, and G. Setti. Tuning a resonant DC/DC converter on the second harmonic for improving performance: A case study. In *2019 IEEE international symposium on circuits and systems (ISCAS)*, pages 1–5, May 2019.

[57] Shuangke Liu and Chengbin Ma. Low-harmonic-distortion and high-efficiency class E ^{2} DC-DC converter for 6.78 MHz WPT. In *2018 IEEE International Conference on Industrial Electronics for Sustainable Energy Systems (IESES)*, pages 421–425, Hamilton, January 2018. IEEE.

[58] Carlos Bernal, Estanis Oyarbide, Pilar Molina Gaudo, and Arturo Mediano. Dynamic Model of Class-E Inverter With Multifrequency Averaged Analysis. *IEEE Transactions on Industrial Electronics*, 59(10):3737–3744, October 2012.

[59] José A. Garcia, Reinel Marante, and María de las Nieves Ruiz Lavin. GaN HEMT Class E^2 Resonant Topologies for UHF DC/DC Power Conversion. *IEEE Trans. Microwave Theory Techn.*, 60(12):4220–4229, December 2012.

[60] Jose A. Garcia and Zoya Popovic. Class-E Rectifiers and Power Converters: The Operation of the Class-E Topology as a Power Amplifier and a Rectifier with Very High Conversion Efficiencies. *IEEE Microwave Magazine*, 19(5):67–78, July 2018.

[61] J.M. Rivas, D. Jackson, O. Leitermann, A.D. Sagneri, Yehui Han, and D.J. Perreault. Design Considerations for Very High Frequency dc-dc Converters. In *2006 IEEE Power Electronics Specialists Conf. (PESC)*, pages 1–11, June 2006. ISSN: 0275-9306.

[62] A. Reatti and M.K. Kazimierczuk. Comparison of the efficiencies of class D and class E rectifiers. In *Proceedings of 36th Midwest Symposium on Circuits and Systems*, pages 871–874, Detroit, MI, USA, 1993. IEEE.

[63] Shohei Saito, Shohei Mita, Wenqi Zhu, Hiroyuki Onishi, Shingo Nagaoka, Takeshi Uematsu, Kien Nguyen, and Hiroo Sekiya. Novel Design Approach of Soft-Switching Resonant Converter With Performance Visualization Algorithm. *IEEE Access*, 8:59922–59933, 2020.

[64] Santanu Kapat and Philip T. Krein. A Tutorial and Review Discussion of Modulation, Control and Tuning of High-Performance DC-DC Converters Based on Small-Signal and Large-Signal Approaches. *IEEE Open Journal of Power Electronics*, 1:339–371, 2020.

[65] Luca Corradini, Dragan Maksimović, Paolo Mattavelli, and Regan Zane. *Digital control of high-frequency switched-mode power converters*. Wiley-IEEE Press, 2015. OCLC: 890793109.

[66] Guangfu Ning and Wu Chen. Asymmetric Pulse Frequency Modulation With Constant On-Time for Series Resonant Converter in High-Voltage High-Power Applications. *IEEE Access*, 7:176971–176981, 2019.

[67] Steve Hung-Lung Tu and Hsin-Wei Yeh. A PWM controller with table look-up for DC-DC class E buck/boost conversion. In *2013 IEEE International Conference of Electron Devices and Solid-state Circuits*, pages 1–2, Hong Kong, Hong Kong, June 2013. IEEE.

[68] Sanghyeon Park and Juan Rivas-Davila. FPGA-based Dynamic Duty Cycle and Frequency Controller for a Class-E ^{2} DC-DC Converter. In *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, pages 282–288, Niigata, May 2018. IEEE.

[69] Hossein Mousavian, Alireza Bakhshai, and Praveen Jain. A ZVT cell for high-frequency quasi-resonant converters in ON-OFF mode for solar applications. In *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 15–22, Cincinnati, OH, October 2017. IEEE.

[70] Ying Li, Xinbo Ruan, Li Zhang, Jiandong Dai, and Qian Jin. Variable Switching Frequency ON–OFF Control for Class E DC–DC Converter. *IEEE Transactions on Power Electronics*, 34(9):8859–8870, September 2019.

[71] Hossein Mousavian, Alireza Bakhshai, and Praveen Jain. An improved PDM control method for a high frequency quasi-resonat converter. In *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, pages 1–8, Milwaukee, WI, USA, September 2016. IEEE.

[72] Ying Li, Xinbo Ruan, Li Zhang, and Yu-Kang Lo. Multipower-Level Hysteresis Control for the Class E DC–DC Converters. *IEEE Transactions on Power Electronics*, 35(5):5279–5289, May 2020.

[73] Euihoon Chung, Kyung-Hwan Lee, Yongsu Han, and Jung-Ik Ha. Single-Switch High-Frequency DC–DC Converter Using Parasitic Components. *IEEE Transactions on Power Electronics*, 32(5):3651–3661, May 2017.

[74] Yongseok Lim, Hoyoung Tang, Seungok Lim, and Jongsun Park. An Adaptive Impedance-Matching Network Based on a Novel Capacitor Matrix for Wireless Power Transfer. *IEEE Trans. Power Electron.*, 29(8):4403–4413, August 2014.

[75] Henry Kennedy, Rares Bodnar, Teerasak Lee, and William Redman-White. A Self-Tuning Resonant-Inductive-Link Transmit Driver Using Quadrature Symmetric Delay Trimmable Phase-Switched Fractional Capacitance. *IEEE Journal of Solid-State Circuits*, 53(6):1694–1706, June 2018.

[76] Fanpeng Kong, Maysam Ghovanloo, and Gregory D. Durgin. An Adaptive Impedance Matching Transmitter for a Wireless Intraoral Tongue-Controlled Assistive Technology. *IEEE Trans. Circuits Syst. II Express Briefs*, 67(2):240–244, February 2020.

[77] Marian K. Kazimierczuk. *Pulse-Width Modulated DC-DC Power Converters: Kazimierczuk/Pulse-width Modulated DC-DC Power Converters*. John Wiley & Sons, Ltd., Chichester, West Sussex, September 2008.

[78] Ling Gu and Wei Zhu. A Family of Zero-Voltage-Switched Resonant Converters: Derivation, Operation, and Design. *IEEE J. Emerg. Sel. Topics Power Electron.*, 9(2):2098–2108, April 2021.

[79] W. Liu, K. Vichienchom, M. Clements, S. C. DeMarco, C. Hughes, E. McGucken, M. S. Humayun, E. De Juan, J. D. Weiland, and R. Greenberg. A neuro-stimulus chip with telemetry unit for retinal prosthetic device. *IEEE J. Solid-State Circuits*, 35(10):1487–1497, October 2000.

[80] M. Ghovanloo and S. Atluri. A wide-band power-efficient inductive wireless link for implantable microelectronic devices using multiple carriers. *IEEE Trans. Circuits Syst. I, Reg. Papers*, 54(10):2211–2221, October 2007.

[81] G. Wang, P. Wang, Y. Tang, and W. Liu. Analysis of dual band power and data telemetry for biomedical implants. *IEEE Trans. Biomed. Circuits Syst.*, 6(3):208–215, June 2012.

[82] M. Jain, M. Daniele, and P. K. Jain. A bidirectional DC-DC converter topology for low power application. *IEEE Trans. Power Electron.*, 15(4):595–606, July 2000.

[83] I. Barbi and R. Gules. Isolated DC-DC converters with high-output voltage for TWTA telecommunication satellite applications. *IEEE Trans. Power Electron.*, 18(4):975–984, July 2003.

[84] R. S. Yang, L. K. Chang, and H. C. Chen. An isolated full-bridge DC-DC converter with 1-MHz bidirectional communication channel. *IEEE Trans. Ind. Electron*, 58(9):4407–4413, September 2011.

[85] A. Seidel, M. Costa, J. Joos, and B. Wicht. Isolated 100% PWM gate driver with auxiliary energy and bidirectional FM/AM signal transmission via single transformer. In *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 2581–2584, March 2015.

[86] P. Lombardo, V. Fiore, E. Ragonese, and G. Palmisano. A fully-integrated half-duplex data/power transfer system with up to 40Mb/s data rate, 23mW output power and on-chip 5kV galvanic isolation. In *IEEE international solid-state circuits conference (ISSCC)*, pages 300–301, February 2016.

[87] Tianjia Sun, Xiang Xie, and Zhihua Wang. *Wireless power transfer for medical microsystems*. Springer, New York, 2013.

[88] Eli Abramov, Ilya Zeltser, Mor Mordechai Peretz, and Mor Mordechai Peretz. A Network-Based Approach for Modeling Resonant Capacitive Wireless Power Transfer Systems. *CPSS Transactions on Power Electronics and Applications*, 4(1):19–29, March 2019.

[89] Matthew Schormans, Virgilio Valente, and Andreas Demosthenous. Practical Inductive Link Design for Biomedical Wireless Power Transfer: A Tutorial. *IEEE Trans. Biomed. Circuits Syst.*, 12(5):1112–1130, October 2018.

[90] Jaechun Lee, Hankyu Lee, Yeunhee Huh, Seungchul Jung, Young-Jun Hong, and Sang Joon Kim. Wireless Power Transfer for Small Implantable Devices by using Smartphones with Relay Coils. In *Intern. Symp. on Antennas and Prop. and North American Radio Sc. Meeting*, pages 1395–1396, July 2020.

[91] Sushree S Biswal, Durga P. Kar, Satish Kumar Samal, and Satyanarayan Bhuyan. Investigation of correlation of design parameters in wireless power transfer system. *IET sci. meas. technol.*, 15(5):427–433, July 2021.

[92] Sebastian Stoecklin, Adnan Yousaf, Tobias Volk, and Leonhard Reindl. Efficient Wireless Powering of Biomedical Sensor Systems for Multichannel Brain Implants. *IEEE Trans. Instrum. Meas.*, 65(4):754–764, April 2016.

[93] Yaoyao Jia, S. Abdollah Mirbozorgi, Byunghun Lee, Wasif Khan, Fatma Madi, Omer T. Inan, Arthur Weber, Wen Li, and Maysam Ghovanloo. A mm-Sized Free-Floating Wirelessly Powered Implantable Optical Stimulation Device. *IEEE Trans. Biomed. Circuits Syst.*, 13(4):608–618, August 2019.

[94] Byunghun Lee, Yaoyao Jia, S. Abdollah Mirbozorgi, Mark Connolly, Xingyuan Tong, Zhaoping Zeng, Babak Mahmoudi, and Maysam Ghovanloo. An Inductively-Powered Wireless Neural Recording and Stimulation System for Freely-Behaving Animals. *IEEE Trans. Biomed. Circuits Syst.*, 13(2):413–424, April 2019.

[95] Junwei Liu, Guibin Wang, Gang Xu, Jianchun Peng, and Hui Jiang. A Parameter Identification Approach With Primary-Side Measurement for DC–DC Wireless-Power-Transfer Converters With Different Resonant Tank Topologies. *IEEE Trans. Transp. Electrific.*, 7(3):1219–1235, September 2021.

[96] Mehdi Kiani. Wireless Power Transfer and Management for Medical Applications: Wireless power. *IEEE Solid-State Circuits Mag.*, 14(3):41–52, 2022.

[97] Deyan Lin, Jian Yin, and S. Y. Ron Hui. Parameter identification of wireless power transfer systems using input voltage and current. In *Energy Conv. Cong. and Exposition*, pages 832–836, September 2014.

[98] William Gerard Hurley, Maeve Catherine Duffy, Jun Zhang, Ignacio Lope, Bettina Kunz, and Werner Hugo Wolfle. A Unified Approach to the Calculation of Self- and Mutual-Inductance for Coaxial Coils in Air. *IEEE Trans. Power Electron.*, 30(11):6155–6162, November 2015.

[99] Sheng Liu, Yue Feng, Wanying Weng, Jinghui Chen, Jiande Wu, and Xiangning He. Contactless Measurement of Current and Mutual Inductance in Wireless Power Transfer System Based on Sandwich Structure. *IEEE J. Emerg. Sel. Topics Power Electron.*, 10(5):6345–6357, October 2022.

[100] Aref Trigui, Sami Hached, Ahmed Chiheb Ammari, Yvon Savaria, and Mohamad Sawan. Maximizing Data Transmission Rate for Implantable Devices Over a Single Inductive Link: Methodological Review. *IEEE Rev. Biomed. Eng.*, 12:72–87, 2019.

[101] Wei Zhang, Jeff C. White, Arpith Mathew Abraham, and Chunting Chris Mi. Loosely Coupled Transformer Structure and Interoperability Study for EV Wireless Charging Systems. *IEEE Transactions on Power Electronics*, 30(11):6356–6367, November 2015.

[102] Ananth Bharadwaj, Ashwani Sharma, and Chakradhar C. Reddy. An Unconventional Measurement Technique to Estimate Power Transfer Efficiency in Series–Series Resonant WPT System Using S-Parameters. *IEEE Trans. Instrum. Meas.*, 71:1–9, 2022.

[103] Luca Callegaro. The metrology of electrical impedance at high frequency: a review. *Meas. Sci. Technol.*, 20(2):022002, February 2009.

[104] Assyfa Ariffin, Atsushi Mori, and Mamiko Inamori. Analyzation of antenna measurement method for wireless power transmission. In *IEEE Region 10 Conference*, pages 219–222, November 2017.

[105] Seon-Jae Jeon and Dong-Wook Seo. Coupling Coefficient Measurement Method with Simple Procedures Using a Two-Port Network Analyzer for a Multi-Coil WPT System. *Energies*, 12(20):3950, October 2019.

[106] F.W. Grover. The Calculation of the Mutual Inductance of Circular Filaments in Any Desired Positions. *Proceedings of the IRE*, 32(10):620–629, October 1944.

[107] Mohammed Al-Saadi, Stanimir Valtchev, José Gonçalves, and Aurelian Crăciunescu. New Analytical Formulas for Coupling Coefficient of Two Inductively Coupled Ring Coils in Inductive Wireless Power Transfer System. In Xiaolin Jiang and Peng Li, editors, *Green Energy and Networking*, volume 333, pages 117–127. Springer International Publishing, 2020.

[108] Zhongqi Li and Min Zhang. Mutual inductance calculation of circular coils arbitrary positioned with magnetic tiles for wireless power transfer system. *IET Power Electron.*, 13(16):3522–3527, December 2020.

[109] Tao Liu, Zhiqiang Wei, Haokun Chi, and Bo Yin. Inductance Calculation of Multilayer Circular Printed Spiral Coils. *J. Phis.:Conf. Ser.*, 1176:062045, March 2019.

[110] Anele O. Amos, Hamam Ykandar, Alayli Yasser, and Djouani Karim. Computation of the mutual inductance between circular filaments with coil misalignment. In *Africon*, pages 1–5, September 2013.

[111] J. Acero, C. Carretero, I. Lope, R. Alonso, O. Lucia, and J. M. Burdio. Analysis of the Mutual Inductance of Planar-Lumped Inductive Power Transfer Systems. *IEEE Trans. Ind. Electron.*, 60(1):410–420, January 2013.

[112] J. Bohacek, T. Jursa, and R. Sedlacek. Calibrating Standards of Mutual Inductance. In *Instrumen. Meas. Tech. Conf. Proceedings*, volume 2, pages 1002–1004, 2005.

[113] Zhengkun Li, Zhonghua Zhang, Qing He, Yaqiong Fu, Jianting Zhao, Bing Han, Shisong Li, Jiang Lan, and Chen Li. A Compensation Method to Measure the Mutual Inductance at Low Frequency. *IEEE Trans. Instrum. Meas.*, 60(7):2292–2297, July 2011.

[114] Salahuddin Raju, Mansun Chan, and C. Patrick Yue. Modeling of an inductive link for wireless power applications. In *Intern. Conf. of Electron Devices and Solid-state Circ.*, pages 1–2, June 2013.

[115] Won Sokhui, Yang Dongsheng, Tian Jiangwei, Cheng Zixin, and Jon Songnam. A Mutual Inductance Measurement Method for the Wireless Power Transfer System. *IOP Conf. Ser.: Mater. Sci. Eng.*, 486:012146, July 2019.

[116] James Blanc. A Simple Technique for Characterization of WPT Coils. In *Wireless Power Transfer Conf.*, pages 1–4, June 2018.

[117] Luca Callegaro. *Electrical impedance principles, measurement, and applications*. CRC Press, Boca Raton, Fla., 2013.

[118] Congyin Shi, Sanghoon Lee, Sergio Soto Aguilar, and Edgar Sánchez-Sinencio. A Time-Domain Digital-Intensive Built-In Tester for Analog Circuits. *Journal of Electronic Testing*, 34(3):313–320, June 2018.

[119] *Impedance Measurement Handbook. A guide to measurement technology and techniques*. Keysight Technologies, 4th edition, 2014.

[120] S. Hackl, C. Lanschutzer, P. Raggam, and W.L. Randeu. A novel method for determining the mutual inductance for 13.56MHz RFID systems. In *Intern. Symp. on Comm. Sys., Networks and Digital Sig. Process.*, pages 297–300, July 2008.

[121] R. D. Cutkosky. Four-terminal-pair networks as precision admittance and impedance standards. *IEEE Trans. Comm. Electron.*, 83(70):19–22, January 1964.

[122] K. Suzuki. A new universal calibration method for four-terminal-pair admittance standards. *IEEE Trans. Instrum. Meas.*, 40(2):420–422, April 1991.

[123] S. Y. Hui. Planar Wireless Charging Technology for Portable Electronic Products and Qi. *Proceedings of the IEEE*, 101(6):1290–1301, June 2013.

[124] Lin Yang, Xiaoming Li, Sheng Liu, Ziwei Xu, and Changsong Cai. Analysis and Design of an LCCC/S-Compensated WPT System With Constant Output Characteristics for Battery Charging Applications. *IEEE J. Emerg. Sel. Topics Power Electron.*, 9(1):1169–1180, February 2021.

[125] Morten Birkerod Lillholm, Yi Dou, Xu Chen, and Zhe Zhang. Analysis and Design of 10-MHz Capacitive Power Transfer With Multiple Independent Outputs for Low-Power Portable Devices. *IEEE J. Emerg. Sel. Topics Power Electron.*, 10(1):149–159, February 2022.

[126] Fang Liu, Kainan Chen, Zhengming Zhao, Kai Li, and Liqiang Yuan. Transmitter-Side Control of Both the CC and CV Modes for the Wireless EV Charging System With the Weak Communication. *IEEE J. Emerg. Sel. Topics Power Electron.*, 6(2):955–965, June 2018.

[127] Lin Yang, Yanyan Shi, Meng Wang, and Li Ren. Constant Voltage Charging and Maximum Efficiency Tracking for WPT Systems Employing Dual-Side Control Scheme. *IEEE J. Emerg. Sel. Topics Power Electron.*, pages 1–1, 2021.

[128] Van-Binh Vu, Van-Tung Phan, Mohamed Dahidah, and Volker Pickert. Multiple Output Inductive Charger for Electric Vehicles. *IEEE Trans. Power Electron.*, 34(8):7350–7368, August 2019.

[129] John S. Ho, Sanghoek Kim, and Ada S. Y. Poon. Midfield Wireless Powering for Implantable Systems. *Proc. IEEE*, 101(6):1369–1378, June 2013.

[130] Kang Yue, Yu Liu, Peng Zhao, Minfan Fu, Haoyu Wang, and Junrui Liang. Coupling Coefficient and Load Estimation for Wireless Power Transfer Systems with Transmitter Side Input Current. In *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pages 709–713, Phoenix, AZ, USA, June 2021. IEEE.

[131] Yanjie Guo and Yuwang Zhang. Secondary Side Voltage and Current Estimation of Wireless Power Transfer Systems. *IEEE Trans. on Ind. Applicat.*, pages 1–1, 2021.

[132] Xin Dai, Xiaofei Li, Yanling Li, and Aiguo Patrick Hu. Maximum Efficiency Tracking for Wireless Power Transfer Systems With Dynamic Coupling Coefficient Estimation. *IEEE Trans. Power Electron.*, 33(6):5005–5015, June 2018.

[133] M. Ghovanloo and S. Atluri. An Integrated Full-Wave CMOS Rectifier With Built-In Back Telemetry for RFID and Implantable Biomedical Applications. *IEEE Trans. Circuits Syst. I, Reg. Papers*, 55(10):3328–3334, November 2008.

[134] Mehdi Kiani and Maysam Ghovanloo. An RFID-Based Closed-Loop Wireless Power Transmission System for Biomedical Applications. *IEEE Trans. Circuits Syst. II Express Briefs*, 57(4):260–264, April 2010.

[135] Byunghun Lee, Mehdi Kiani, and Maysam Ghovanloo. A Triple-Loop Inductive Power Transmission System for Biomedical Applications. *IEEE Trans. Biomed. Circuits Syst.*, 10(1):138–148, February 2016.

[136] Zhaotian Yan, Bin Yang, Huan Liu, Changxin Chen, Muhammad Waqas, Ruikun Mai, and Zhengyou He. Efficiency Improvement of Wireless Power Transfer Based on Multitransmitter System. *IEEE Trans. Power Electron.*, 35(9):9011–9023, September 2020.

[137] Hongchang Li, Jingyang Fang, Shuxin Chen, Kangping Wang, and Yi Tang. Pulse Density Modulation for Maximum Efficiency Point Tracking of Wireless Power Transfer Systems. *IEEE Trans. Power Electron.*, 33(6):5492–5501, June 2018.

[138] Yuanyuan Liu and Hongwei Feng. Maximum Efficiency Tracking Control Method for WPT System Based on Dynamic Coupling Coefficient Identification and Impedance Matching Network. *IEEE J. Emerg. Sel. Topics Power Electron.*, 8(4):3633–3643, December 2020.

[139] Xin Dai, Xiaofei Li, Yanling Li, and Aiguo Patrick Hu. Impedance-Matching Range Extension Method for Maximum Power Transfer Tracking in IPT System. *IEEE Trans. Power Electron.*, 33(5):4419–4428, May 2018.

[140] Minfan Fu, He Yin, Xinen Zhu, and Chengbin Ma. Analysis and Tracking of Optimal Load in Wireless Power Transfer Systems. *IEEE Trans. Power Electron.*, 30(7):3952–3963, July 2015.

[141] Zhicong Huang, Siu-Chung Wong, and Chi K. Tse. Control Design for Optimizing Efficiency in Inductive Power Transfer Systems. *IEEE Trans. Power Electron.*, 33(5):4523–4534, May 2018.

[142] W. X. Zhong and S. Y. R. Hui. Maximum Energy Efficiency Tracking for Wireless Power Transfer Systems. *IEEE Trans. Power Electron.*, 30(7):4025–4034, July 2015.

[143] Hao Jiang, Junmin Zhang, Di Lan, K. K. Chao, Shyshenq Liou, Hamid Shahnasser, Richard Fechter, Shinjiro Hirose, Michael Harrison, and Shuvo Roy. A Low-Frequency Versatile Wireless Power Transfer Technology for Biomedical Implants. *IEEE Trans. Biomed. Circuits Syst.*, 7(4):526–535, August 2013.

[144] Yechan Park, Seok-Tae Koh, Jeongeun Lee, Hongkyun Kim, Jaesuk Choi, Sohmyung Ha, Chul Kim, and Minkyu Je. A Wireless Power and Data Transfer IC for Neural Prostheses Using a Single Inductive Link With Frequency-Splitting Characteristic. *IEEE Transactions on Biomedical Circuits and Systems*, 15(6):1306–1319, December 2021.

[145] Gian Luca Barbruni, Paolo Motto Ros, Danilo Demarchi, Sandro Carrara, and Diego Ghezzi. Miniaturised Wireless Power Transfer Systems for Neurostimulation: A Review. *IEEE Trans. Biomed. Circuits Syst.*, 14(6):1160–1178, December 2020.

[146] Iman Abdali Mashhadi, Majid Pahlevani, Soheil Hor, Hamid Pahlevani, and Ehsan Adib. A New Wireless Power-Transfer Circuit for Retinal Prosthesis. *IEEE Trans. Power Electron.*, 34(7):6425–6439, July 2019.

[147] Tomoharu Nagashima, Xiuqin Wei, Elisenda Bou, Eduard Alarcon, and Hiroo Sekiya. Analytical design for resonant inductive coupling wireless power transfer system with class-E inverter and class-DE rectifier. In *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 686–689, Lisbon, Portugal, May 2015. IEEE.

[148] Jianan Chen, Dong Jiang, Wei Sun, Zewei Shen, and Yechi Zhang. A Family of Spread-Spectrum Modulation Schemes Based on Distribution Characteristics to Reduce Conducted EMI for Power Electronics Converters. *IEEE Transactions on Industry Applications*, 56(5):5142–5157, September 2020.

[149] Piotr Lezynski. Random Modulation in Inverters With Respect to Electromagnetic Compatibility and Power Quality. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 6(2):782–790, June 2018.

[150] S. Johnson and R. Zane. Custom Spectral Shaping for EMI Reduction in High-Frequency Inverters and Ballasts. *IEEE Transactions on Power Electronics*, 20(6):1499–1505, November 2005.

[151] J. Balcells, A. Santolaria, A. Orlandi, D. Gonzalez, and J. Gago. EMI Reduction in Switched Power Converters Using Frequency Modulation Techniques. *IEEE Transactions on Electromagnetic Compatibility*, 47(3):569–576, August 2005.

[152] David Gonzalez, Josep Balcells, Alfonso Santolaria, Jean-Charles Le Bunetel, Javier Gago, Didier Magnon, and StÉphane Brehaut. Conducted EMI Reduction in Power Converters by Means of Periodic Switching Frequency Modulation. *IEEE Transactions on Power Electronics*, 22(6):2271–2281, November 2007.

[153] A.M. Stankovic, G.C. Verghese, and D.J. Perreault. Analysis and synthesis of random modulation schemes for power converters. In *Proceedings of IEEE Power Electronics Specialist Conference - PESC '93*, pages 1068–1074, Seattle, WA, USA, 1993. IEEE.

[154] A. M. Stankovic and H. Lev-Ari. Randomized modulation in power electronic converters. *Proc. IEEE*, 90(5):782–799, May 2002.

[155] Hwa-Pyeong Park, Mina Kim, and Jee-Hoon Jung. Spread-Spectrum Technique Employing Phase-Shift Modulation to Reduce EM Noise for Parallel–Series LLC Resonant Converter. *IEEE Transactions on Power Electronics*, 34(2):1026–1031, February 2019.

[156] Ruchir Saraswat, Uwe Zillmann, Supriyanto Supriyanto, Guido Droege, and Ulrich Bretthauer. Programmable spread spectrum clock generation based on

successive phase selection technique. In *2008 IEEE International Symposium on Circuits and Systems*, pages 2845–2848, Seattle, WA, USA, May 2008. IEEE.

[157] Fabio Pareschi, Gianluca Setti, Riccardo Rovatti, and Giovanni Frattini. Practical Optimization of EMI Reduction in Spread Spectrum Clock Generators With Application to Switching DC/DC Converters. *IEEE Trans. Power Electron.*, 29(9):4646–4657, September 2014.

[158] Fabio Pareschi, Gianluca Setti, Riccardo Rovatti, and Giovanni Frattini. Short-term Optimized Spread Spectrum Clock Generator for EMI Reduction in Switching DC/DC Converters. *IEEE Trans. Circuits Syst. I, Reg. Papers*, 61(10):3044–3053, October 2014.

[159] Marco Liserre, Hamzeh Beiranvand, Yang Leng, Rongwu Zhu, and Peter A. Hoeher. Overview of Talkative Power Conversion Technologies. *IEEE Open Journal of Power Electronics*, 4:67–80, 2023.

[160] W. Stefanutti, S. Saggini, P. Mattavelli, and M. Ghioni. Power Line Communication in Digitally Controlled DC–DC Converters Using Switching Frequency Modulation. *IEEE Transactions on Industrial Electronics*, 55(4):1509–1518, April 2008.

[161] Xiangning He, Ruichi Wang, Jiande Wu, and Wuhua Li. Nature of power electronics and integration of power conversion with communication for talkative power. *Nature Communications*, 11(1):2479, May 2020.

[162] Ruichi Wang, Zhengyu Lin, Jin Du, Jiande Wu, and Xiangning He. Direct Sequence Spread Spectrum-Based PWM Strategy for Harmonic Reduction and Communication. *IEEE Transactions on Power Electronics*, 32(6):4455–4465, June 2017.

[163] Y. Liu, M. De Vos, and S. Van Huffel. Compressed sensing of multichannel EEG signals: the simultaneous cosparsity and low-rank optimization. *IEEE Trans. on Biom. Eng.*, 62(8):2055–2061, August 2015.

Appendix

A Dimensionless Converter analysis

In order to study the dimensionless converter of Figure 1.2 and get a closed expression for the four state variables describing the evolution of the circuit in the normalized time θ, i.e., $i_{\text{inv}}(\theta)$, $i_{\text{rec}}(\theta)$, $v_{\text{DS}}(\theta)$, and $v_{\text{KA}}(\theta)$, the following two simplifying assumptions are taken into account.

- The circuit can be found in many different *configurations*, according to the on/off state of the three non-linear devices considered (i.e., the MOS switch and the two diodes). Three binary variables m^{ON}, b^{ON} and d^{ON} are introduced to account for the device state (1 is on, 0 is off) of the MOS switch, its bulk diode, and the rectifying diode. Each circuit configuration is so identified by a different combination of $\left\{m^{\text{ON}}, b^{\text{ON}}, d^{\text{ON}}\right\}$. Furthermore, to allow a simpler analysis, when either $m^{\text{ON}} = 1$ or $b^{\text{ON}} = 1$ we assume that the capacitance $1/q_I$ (and its parasitic series resistance) has no effect on the circuit, and that

$$
\begin{cases}
\dfrac{1-k_I}{k_I} q_M \dfrac{i_{\text{inv}}(\theta)}{Q_I} + \dfrac{1-k_I}{k_I} q_M \dfrac{d\, i_{\text{inv}}(\theta)}{d\theta} + \left(\dfrac{1}{g_{\text{cm}}} + \dfrac{q_M}{Q_M}\right)\left(i_{\text{inv}}(\theta) + i_{\text{rec}}(\theta)\right) + q_M \dfrac{d\left(i_{\text{inv}}(\theta) + i_{\text{rec}}(\theta)\right)}{d\theta} + \\
\quad + m^{\text{ON}} \dfrac{i_{\text{inv}}(\theta)}{g_{\text{DS}}^{\text{ON}}} + b^{\text{ON}} \left(\dfrac{i_{\text{inv}}(\theta)}{g_b^{\text{ON}}} - v_b^{\text{ON}}\right) + (1 - m^{\text{ON}} - b^{\text{ON}}) \left(\dfrac{q_I}{Q_{C_{\text{inv}}}} i_{\text{inv}}(\theta) + v_{\text{DS}}(\theta)\right) + \dfrac{i_{\text{inv}}(\theta)}{g_{\text{inv}}} - 1 = 0 \\
\dfrac{1-k_R}{k_R} q_M \dfrac{i_{\text{rec}}(\theta)}{Q_R} + \dfrac{1-k_R}{k_R} q_M \dfrac{d\, i_{\text{rec}}(\theta)}{d\theta} + \left(\dfrac{1}{g_{\text{cm}}} + \dfrac{q_M}{Q_M}\right)\left(i_{\text{rec}}(\theta) + i_{\text{inv}}(\theta)\right) + q_M \dfrac{d\left(i_{\text{rec}}(\theta) + i_{\text{inv}}(\theta)\right)}{d\theta} + \\
\qquad + d^{\text{ON}} \left(\dfrac{i_{\text{rec}}(\theta)}{g_d^{\text{ON}}} - v_d^{\text{ON}}\right) + (1 - d^{\text{ON}}) \left(\dfrac{q_R}{Q_{C_{\text{rec}}}} i_{\text{rec}}(\theta) + v_{\text{KA}}(\theta)\right) + \dfrac{i_{\text{rec}}(\theta)}{g_{\text{rec}}} - 1 = 0 \\
i_{\text{inv}}(\theta) - \dfrac{1}{q_I} \dfrac{d\, v_{\text{DS}}(\theta)}{d\theta} = 0 \quad \left(m^{\text{ON}} + b^{\text{ON}} = 0 \text{ only}\right) \\
i_{\text{rec}}(\theta) - \dfrac{1}{q_R} \dfrac{d\, v_{\text{KA}}(\theta)}{d\theta} = 0 \quad \left(d^{\text{ON}} = 0 \text{ only}\right).
\end{cases}
\tag{A.1}
$$

the capacitance $1/q_R$ (and its parasitic resistance) has no effect when $d^{\mathrm{ON}} = 1$. We also assume the additional constraint that the MOS switch and its bulk diode cannot be on at the same time.

- When $m^{\mathrm{ON}} = 1$ we constrain $v_{\mathrm{DS}}(\theta) = 0$ and consider $1/g_{\mathrm{DS}}^{\mathrm{ON}}$ belonging to the inverter loop; when $b^{\mathrm{ON}} = 1$ we set $v_{\mathrm{DS}}(\theta) = -v_b^{\mathrm{ON}}$ and include $1/g_b^{\mathrm{ON}}$ in the inverter loop; when $m^{\mathrm{ON}} = b^{\mathrm{ON}} = 0$, $v_{\mathrm{DS}}(\theta)$ takes the value of the voltage across the capacitance $1/q_I$, and its parasitic resistance $q_I/Q_{C_{\mathrm{inv}}}$ is considered. When $d^{\mathrm{ON}} = 1$ we have $v_{\mathrm{KA}}(\theta) = -v_d^{\mathrm{ON}}$ and include $1/g_d^{\mathrm{ON}}$ in the rectifier loop, otherwise $v_{\mathrm{KA}}(\theta)$ takes the value of the voltage across the capacitance $1/q_R$, and its parasitic resistance $q_R/Q_{C_{\mathrm{rec}}}$ is considered. At the time instant when the MOS switch is turned on, the $v_{\mathrm{DS}}(\theta)$ is allowed to be discontinuous, with an abrupt change to 0; in any other condition, the continuity of all four state variables is ensured.

Under the assumptions detailed above, six different circuit configurations are possible, as summarized in Table A.1. For all of them, the converter evolution is regulated by the system of linear equations in (A.1).

$$
\begin{aligned}
&\frac{1}{Q_I} = \frac{L_{\mathrm{inv}}}{L_{\mathrm{inv}} + L_p - \frac{V_{\mathrm{inv}}}{V_{\mathrm{rec}}}M}\frac{1}{Q_{L_{\mathrm{inv}}}} + \frac{L_p}{L_{\mathrm{inv}} + L_p - \frac{V_{\mathrm{inv}}}{V_{\mathrm{rec}}}M}\frac{1}{Q_{L_p}} + \frac{-\frac{V_{\mathrm{inv}}}{V_{\mathrm{rec}}}M}{L_{\mathrm{inv}} + L_p - \frac{V_{\mathrm{inv}}}{V_{\mathrm{rec}}}M}\frac{1}{Q_M},\\
&\frac{1}{Q_R} = \frac{L_{\mathrm{rec}}}{L_{\mathrm{rec}} + L_s - \frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}}M}\frac{1}{Q_{L_{\mathrm{rec}}}} + \frac{L_s}{L_{\mathrm{rec}} + L_s - \frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}}M}\frac{1}{Q_{L_s}} + \frac{-\frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}}M}{L_{\mathrm{inv}} + L_s - \frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}}M}\frac{1}{Q_M}\\
&v_d^{\mathrm{ON}} = \frac{V_d^{\mathrm{ON}}}{V_{\mathrm{rec}}},\ v_b^{\mathrm{ON}} = \frac{V_b^{\mathrm{ON}}}{V_{\mathrm{inv}}},\ \frac{1}{g_{\mathrm{DS}}^{\mathrm{ON}}} = \frac{V_{\mathrm{rec}}\langle -I_{\mathrm{rec}}(t)\rangle}{V_{\mathrm{inv}}^2}R_{\mathrm{DS}}^{\mathrm{ON}},\ \frac{1}{g_d^{\mathrm{ON}}} = \frac{\langle -I_{\mathrm{rec}}(t)\rangle}{V_{\mathrm{rec}}}R_d^{\mathrm{ON}},\ \frac{1}{g_b^{\mathrm{ON}}} = \frac{V_{\mathrm{rec}}\langle -I_{\mathrm{rec}}(t)\rangle}{V_{\mathrm{inv}}^2}R_b^{\mathrm{ON}},\\
&\frac{1}{g_{\mathrm{inv}}} = \frac{V_{\mathrm{rec}}\langle -I_{\mathrm{rec}}(t)\rangle}{V_{\mathrm{inv}}^2}R_{\mathrm{in}},\ \frac{1}{g_{\mathrm{cm}}} = 0,\ \frac{1}{g_{\mathrm{rec}}} = \frac{\langle -I_{\mathrm{rec}}(t)\rangle}{V_{\mathrm{rec}}}R_{\mathrm{out}}
\end{aligned}
\tag{A.1}
$$

$$
\begin{aligned}
&\frac{1}{Q_I} = \frac{L_{\mathrm{inv}}}{L_{\mathrm{inv}} + L_p + \frac{V_{\mathrm{inv}}}{V_{\mathrm{rec}}}M}\frac{1}{Q_{L_{\mathrm{inv}}}} + \frac{L_p}{L_{\mathrm{inv}} + L_p + \frac{V_{\mathrm{inv}}}{V_{\mathrm{rec}}}M}\frac{1}{Q_{L_p}} + \frac{\frac{V_{\mathrm{inv}}}{V_{\mathrm{rec}}}M}{L_{\mathrm{inv}} + L_p + \frac{V_{\mathrm{inv}}}{V_{\mathrm{rec}}}M}\frac{1}{Q_M},\\
&\frac{1}{Q_R} = \frac{L_{\mathrm{rec}}}{L_{\mathrm{rec}} + L_s + \frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}}M}\frac{1}{Q_{L_{\mathrm{rec}}}} + \frac{L_s}{L_{\mathrm{rec}} + L_s + \frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}}M}\frac{1}{Q_{L_s}} + \frac{\frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}}M}{L_{\mathrm{inv}} + L_s + \frac{V_{\mathrm{rec}}}{V_{\mathrm{inv}}}M}\frac{1}{Q_M},\\
&v_d^{\mathrm{ON}} = \frac{V_d^{\mathrm{ON}}}{V_{\mathrm{rec}}},\ v_b^{\mathrm{ON}} = \frac{V_b^{\mathrm{ON}}}{V_{\mathrm{inv}}},\ \frac{1}{g_{\mathrm{DS}}^{\mathrm{ON}}} = \frac{V_{\mathrm{rec}}\langle -I_{\mathrm{rec}}(t)\rangle}{V_{\mathrm{inv}}^2}R_{\mathrm{DS}}^{\mathrm{ON}},\ \frac{1}{g_d^{\mathrm{ON}}} = \frac{\langle -I_{\mathrm{rec}}(t)\rangle}{V_{\mathrm{rec}}}R_d^{\mathrm{ON}},\ \frac{1}{g_b^{\mathrm{ON}}} = \frac{V_{\mathrm{rec}}\langle -I_{\mathrm{rec}}(t)\rangle}{V_{\mathrm{inv}}^2}R_b^{\mathrm{ON}},\\
&\frac{1}{g_{\mathrm{inv}}} = \frac{V_{\mathrm{inv}}\langle -I_{\mathrm{rec}}(t)\rangle}{V_{\mathrm{inv}}^2}R_{\mathrm{in}},\ \frac{1}{g_{\mathrm{cm}}} = 0,\ \frac{1}{g_{\mathrm{rec}}} = \frac{\langle -I_{\mathrm{rec}}(t)\rangle}{V_{\mathrm{rec}}}R_{\mathrm{out}}
\end{aligned}
\tag{A.2}
$$

The first and the second rows in (A.1) come from the Kirchhoff voltage law at the inverter loop and the rectifier loop, respectively. The last two rows come from the equations of the two capacitances $1/q_I$ and $1/q_R$, and hold only if the corresponding switching devices are off.

System (A.1) is piece-wise linear, and can be divided into a number of linear systems (depending on the value of m^{ON}, b^{ON} and d^{ON}) whose solutions, once continuity is ensured, can be combined to give the solution of (A.1) in an exact and semi-analytic way. Even if many approaches can be followed to solve each linear system (e.g., using the Laplace domain), we follow a procedure similar to that suggested in [31] based on the direct solution of the system of differential equations.

In more detail, let us conventionally set the initial time $\theta = 0$ as the time instant when the MOS switch is (instantaneously) turned on, and $\theta_D = 2\pi D$ as the time instant when it is (instantaneously) turned off, with $0 < D < 1$ being the clock duty-cycle. This pattern is then repeated with a 2π period, i.e., at every $\theta = 2k\pi$ the switch is turned on, with $k = 0, 1, 2, \ldots$. At all these time instants we have $v_{\mathrm{DS}}(2k\pi^{+}) = 0$ independently of the value of $v_{\mathrm{DS}}(2k\pi^{-})$.

Let $i_{\mathrm{inv}}^{(0)}$, $i_{\mathrm{rec}}^{(0)}$ and $v_{\mathrm{KA}}^{(0)}$ be the values of $i_{\mathrm{inv}}(\theta)$, $i_{\mathrm{rec}}(\theta)$ and $v_{\mathrm{KA}}(\theta)$ at the reference time $\theta = 0$. For angular time instants θ immediately after the zero, the bulk diode is off ($m^{\mathrm{ON}} = 1$, so that $b^{\mathrm{ON}} = 0$), while the rectifying diode can be either on (configuration Z_4 with $m^{\mathrm{ON}} = 1$, if $i_{\mathrm{rec}}^{(0)} < 0$ and $v_{\mathrm{KA}}^{(0)} = v_d^{\mathrm{ON}}$) or off (configuration Z_3 with $m^{\mathrm{ON}} = 0$, if $v_{\mathrm{KA}}^{(0)} > 0$). Once the circuit configuration has been properly identified, we can consider the Cauchy problem given by (A.1) with the proper values of m^{ON}, d^{ON} and d^{ON} and the initial conditions, and analytically compute the converter evolution. We refer to [31] for the mathematical details.

This solution is valid until the circuit configuration changes, i.e., either at the earliest instant between θ_D and the time θ_{Z4} when the rectifying diode turns off (when $i_{\mathrm{rec}}(\theta)$ turns positive) assuming configuration Z_4, or θ_{Z3} when it turns off ($v_{\mathrm{KA}}(\theta) + v_d^{\mathrm{ON}}$ decreases down to zero) assuming configuration Z_3. Even if the value of either θ_{Z4} or θ_{Z3} has to be numerically computed, the expression for $i_{\mathrm{inv}}(\theta)$, $i_{\mathrm{rec}}(\theta)$, $v_{\mathrm{DS}}(\theta)$ and $v_{\mathrm{KA}}(\theta)$ are actually non-linear but expressed in an analytic way. The values of the state variables at the time instant when the circuit configuration changes is used as initial conditions for the successive configuration.

B Dimensionless Converter Design

Being able to have a closed mathematical expression for $i_{\text{inv}}(\theta)$, $i_{\text{rec}}(\theta)$, $v_{\text{DS}}(\theta)$ and $v_{\text{KA}}(\theta)$ allows use to express as a mathematical expressions the constraint of a class-E converter operating at the optimal condition.

First, we have a stationary condition when the evolution is periodically repeated every 2π. This happens if

$$i_{\text{inv}}(2\pi) - i_{\text{inv}}^{(0)} = 0 \tag{B.1a}$$

$$i_{\text{rec}}(2\pi) - i_{\text{rec}}^{(0)} = 0 \tag{B.1b}$$

$$v_{\text{KA}}(2\pi) - v_{\text{KA}}^{(0)} = 0 \tag{B.1c}$$

while the $v_{\text{DS}}(\theta)$ does not give rise to an analog condition since it may be discontinuous at $\theta = 2k\pi$, $k = 0,1,2,\ldots$. Furthermore, it is necessary to satisfy the output power normalization by imposing an average value to the rectifying current

$$\langle i_{\text{rec}}(\theta)\rangle + 1 = \frac{1}{2\pi}\int_0^{2\pi} i_{\text{rec}}(\theta)\,d\theta + 1 = 0 \tag{B.1d}$$

Finally, ZVS and ZVDS need to be achieved, i.e., the $v_{\text{DS}}(\theta)$ has to reach gradually the zero level immediately before the MOS turn-on instant given by $\theta = 2\pi$. Let us define θ_b^{ON} as the angular time when the body diode would turn on if the converter was an autonomous circuit (i.e., the MOS was not externally turned on). The *effective* switch time is given by $\theta_{\text{sw}} = \min(2\pi, \theta_b^{\text{ON}})$. We have ZVS and ZVDS if

$$\theta_{\text{sw}} - 2\pi = 0 \tag{B.1e}$$

$$v_{\text{DS}}(\theta_{\text{sw}}) = 0 \tag{B.1f}$$

$$\frac{d}{d\theta}v_{\text{DS}}(\theta)\bigg|_{\theta=\theta_{\text{sw}}} = q_I i_{\text{inv}}(\theta_{\text{sw}}) = 0 \tag{B.1g}$$

where (B.1e) ensures that the body diode is not turned on, (B.1f) ensures ZVS and (B.1g) ZVDS. The first equality in (B.1g) holds since, given the definition of θ_{sw}, for $\theta < \theta_{\text{sw}}$ it is $m^{\text{ON}} = 0$ and $b^{\text{ON}} = 0$, so that i_{inv} is actually flowing into the capacitance $1/q_I$. Note also that (B.1g) is not strictly necessary if a designer is looking for class-E sub-optimal condition.

Note that the ZVDS constraint (B.1g), assuming that both constraints (B.1a) and (B.1e) are satisfied and $q_I \neq 0$, can be simplified in $i_{\text{inv}}^{(0)} = 0$. This initial value of i_{inv} will be always observed when optimal class-E condition is ensured.

C Lossy Parameters Conversion

Equation (A.1) includes lossy transformation rules for the in-phase coupled converter of Figure 1.1(a), whereas (A.2) for the 180° out-of-phase coupled converter of Figure 1.1(b).

Transformation rules of (A.1) generally hold also for all converters of Figure 1.4, with the following exceptions.

Inverting buck-boost configuration, type A:

$$\begin{aligned} \frac{1}{g_{\text{inv}}} &= \frac{V_{\text{rec}}\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}^2} R_{\text{in}} - \frac{(V_{\text{inv}} - V_{\text{rec}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}^2} R_{\text{out}} \\ \frac{1}{g_{\text{cm}}} &= \frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}} R_{\text{out}}, \quad \frac{1}{g_{\text{rec}}} = \frac{(V_{\text{inv}} - V_{\text{rec}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}} V_{\text{rec}}} R_{\text{out}} \end{aligned} \tag{C.3}$$

Buck configuration:

$$\begin{aligned} \frac{1}{g_{\text{inv}}} &= \frac{(V_{\text{rec}} - V_{\text{inv}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}^2} R_{\text{in}} + \frac{V_{\text{rec}}\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}^2} R_{\text{out}} \\ \frac{1}{g_{\text{cm}}} &= \frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}} R_{\text{in}}, \quad \frac{1}{g_{\text{rec}}} = -\frac{(V_{\text{rec}} - V_{\text{inv}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}} V_{\text{rec}}} R_{\text{in}} \end{aligned} \tag{C.4}$$

Inverting buck-boost configuration, type B:

$$\begin{aligned} \frac{1}{g_{\text{inv}}} &= \frac{(V_{\text{rec}} - V_{\text{inv}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}^2} R_{\text{in}}, \quad \frac{1}{g_{\text{cm}}} = \frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}} R_{\text{in}} \\ \frac{1}{g_{\text{rec}}} &= -\frac{(V_{\text{rec}} - V_{\text{inv}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}} V_{\text{rec}}} R_{\text{in}} + \frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{rec}}} R_{\text{out}} \end{aligned} \tag{C.5}$$

Boost configuration:

$$\begin{aligned} \frac{1}{g_{\text{inv}}} &= -\frac{(V_{\text{inv}}-V_{\text{rec}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}^2}R_{\text{out}}, \quad \frac{1}{g_{\text{cm}}} = \frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}}R_{\text{out}} \\ \frac{1}{g_{\text{rec}}} &= \frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{rec}}}R_{\text{in}} - \frac{(V_{\text{inv}}-V_{\text{rec}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}V_{\text{rec}}}R_{\text{out}} \end{aligned} \tag{C.6}$$

Transformation rules of (A.2) generally hold also for all converters of Figure 1.5, with the following exceptions.

Buck configuration:

$$\begin{aligned} \frac{1}{g_{\text{inv}}} &= \frac{V_{\text{rec}}\langle -I_{\text{rec}}(t)\rangle}{V_{\text{in}}^2}R_{\text{in}} + \frac{(V_{\text{inv}}+V_{\text{rec}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{in}}^2}R_{\text{out}} \\ \frac{1}{g_{\text{cm}}} &= -\frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}}R_{\text{out}}, \quad \frac{1}{g_{\text{rec}}} = \frac{(V_{\text{inv}}+V_{\text{rec}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}V_{\text{rec}}}R_{\text{out}} \end{aligned} \tag{C.7}$$

Boost configuration:

$$\begin{aligned} \frac{1}{g_{\text{inv}}} &= \frac{(V_{\text{inv}}+V_{\text{rec}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}^2}R_{\text{in}}, \quad \frac{1}{g_{\text{cm}}} = -\frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{inv}}}R_{\text{in}} \\ \frac{1}{g_{\text{rec}}} &= \frac{(V_{\text{inv}}+V_{\text{rec}})\langle -I_{\text{rec}}(t)\rangle}{V_{\text{in}}V_{\text{rec}}}R_{\text{in}} + \frac{\langle -I_{\text{rec}}(t)\rangle}{V_{\text{rec}}}R_{\text{out}} \end{aligned} \tag{C.8}$$