34 dBm GaN Doherty Power Amplifier for Ka-band satellite downlink

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***Abstract* — This paper presents the design and experimental characterization of a Doherty power amplifier cell targeting the satellite Ka-band downlink. The foreseen application is in a combined power amplifier, where two Doherty cells are combined in parallel to achieve power levels of the order of 6 W. The measured performance of the DPA cell well compares with the present state-of-the-art for the application, with output power in excess of 34 dBm in the 17.3–20.3 GHz band, gain around 12 dB, and efficiency higher than 25% and 20%, at saturation and 6 dB output power back-off, respectively.**

***Keywords* — Doherty, GaN, power amplifiers, satellite.**

I. Introduction

The increasing interest of the satellite communication market for lightweight, high efficiency transmitters is pushing the research toward solid state solutions, especially for the most demanding building block of the architecture in terms of performance and cost, the power amplifier (PA). In this scenario microwave monolithic integrated circuits (MMICs) are the reference choice for the PA realization [1], [2], [3]. The output power levels targeted are still significant (between 30–40 dBm, depending on the specific transmitter architecture), while the simplicity of the transmitter architecture is a must. The adopted signals are characterised by wide bandwidth and large amplitude dynamic, posing stringent linearity requirements to the transmitter. This leads to operate the PA far from its maximum efficiency region, with a detrimental impact on the entire transmitter power consumption. To complicate the picture, digital linearisers are not suitable for these applications since most of transmitters work as active repeaters; therefore there is no availability of the baseband signal and the PA must present a good intrinsic linearity.

A strong candidate for efficient amplification with non-constant envelope modulation schemes is the Doherty PA (DPA), a very popular solution at sub-6 GHz frequencies, especially as purely RF single-input [4], because it does not require additional digital signal processing to operate, with clear advantages in terms of instantaneous channel bandwidth, but also in dual-input [5], [6] implementation.

From a technology point of view, GaAs still dominates the market of the PAs in K-band, but when output power exceeds watt level for each MMIC, GaN based solutions are starting to appear [7], [8], [3], thanks to the power density of GaN leading to smaller devices, with more favorable impedance levels leading to simpler matching networks and eventually lower cost per watt thanks to MMIC area saving. This trend is demonstrated by the present efforts from companies and agencies, such as the European Space Agency and different Departments of Defense, for the exploitation of GaN technologies.

In this work, a DPA cell is designed targeting 34.5 dBm saturated output power, over the 17.3–20.3 GHz Ka-band downlink satellite frequency range. The adopted technology is the 100 nm GaN-Si process by OMMIC. The 2-stage DPA is matched on 100 Ω in order to be used as a cell in a combined structure without the need of additional output matching, but simply with the addition of a pre-driver to achieve the required gain. The measured performance is very promising and in line with the state of the art for the present scenario [3], also considering the limitations related to the space de-rating rules and the maximum junction temperature (160°C). In particular, the DPA presents a saturated power in excess of 34 dBm over the whole 3 GHz bandwidth, a gain around 12 dB, and efficiency higher than 25% and 20%, at saturation and 6 dB Output power Back-Off (OBO), respectively.

II. Technology assessment and design of the DPA

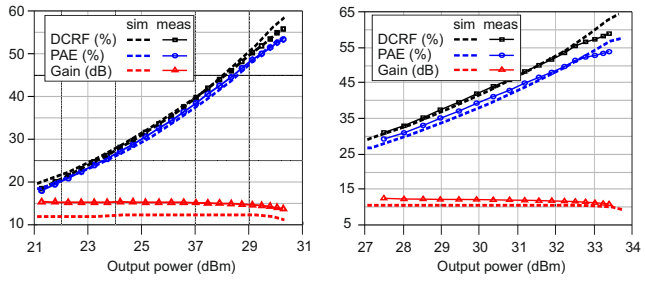
The D01GH technology provided by OMMIC is a GaN process on high resistivity Si substrate, suitable for high-power as well as low-noise electronic devices working in the microwave and millimetre-wave frequency range. The D01GH process provides an AlN/GaN/AlGaN active layer for Double Heterostructure Field Effect Transistors (DHFET) with gate length of 100 nm, leading to a cut-off frequency higher than 100 GHz. Two types of Metal- Insulator-Metal (MIM) capacitors are available: one to realize high capacitance values (400 pF/mm2) and the other for small values (49 pF/mm2). High resistivity Si with 100 nm thickness constitutes the substrate. An AlGaN buffer layer is interposed between Si and the GaN active layer to mitigate the lattice mismatch.

A. Experimental characterization of active devices

Before starting the actual DPA implementation, a source-/load-pull measurement campaign on devices with

different periphery was carried out at the centre frequency of the target bandwidth (18.8 GHz). For each periphery, output power, PAE and gain levels were measured under continuous wave (CW) stimulus by using an active load-pull system based on a vector signal analyser. The devices were biased in class AB at 60 mA/mm, with drain voltage reduced from 15 V to 11 V, in order to account for space de-rating. This preliminary activity was carried out in order to experimentally verify the power density of the process and the agreement with the nonlinear models provided by the foundry [9]. Considering the aforementioned space derating and maximum junction temperature, the process power density of 3 W/mm reduces to around 2 W/mm. Therefore, two $8 \times 100\,\mu$m devices are selected for the final stage to achieve the desired output power, taking into account the losses of the passive networks. Accounting for the gain penalty of the Doherty architecture and the gain achievable by the devices at the selected frequencies, a 2-stage DPA topology with the drivers embedded into each branch [10] is selected to achieve a reasonable gain not hampering the Power Added Efficiency (PAE).

Fig 1 shows the comparison between measured and simulated performance for the 6x50 μm and 8x100 μm devices (driver and final stage peripheries respectively) when terminated on the optimum load at 18.8 GHz. Notably, the agreement seems quite good even if the nonlinear model overestimates the output power of roughly 1 dB.



(a) (b)

Fig. 1. Comparison between measured and simulated performance of 6x50 μm (left) and 8x100 μm (right) devices as a function of output power at 18.8 GHz.

Source-/load-pull measurement were also performed in class C bias condition, considering that the Peaking devices work in that condition in a DPA. Fig.2 (left-center)shows the comparison between measured and simulated gain as a function of the output power at centre frequency for different class C bias conditions (i.e., V_{DD}=11 V & V_{GG} ranging from -1.7 V to -4.5 V) for the 8x100 μm device. Notably, there are some differences between actual and predicted results, especially for lower gate bias voltages. Similar trends have been observed on the other devices. Unfortunately, such a result is somehow expected when working with models from the foundry. Indeed, under class C operation, due to the presence of more severe gate and drain lag effects, the behaviour of the transistor can be substantially altered with respect to class AB operation. On the other hand, the Peaking device plays a key role in the implementation of a DPA. As a consequence, wrong estimation of its gate periphery and related performance can easily hinder the active load-pulling principle on which the DPA is based, thus preventing the achievement of the specified requirements. In the same Fig. 2 (right) are reported the measured optimum loads for output power at centre frequency for the same class C bias conditions. The dependency on the gate bias voltage highlights that the tailoring of the impedance matching for the Peaking can improve the DPA performance.

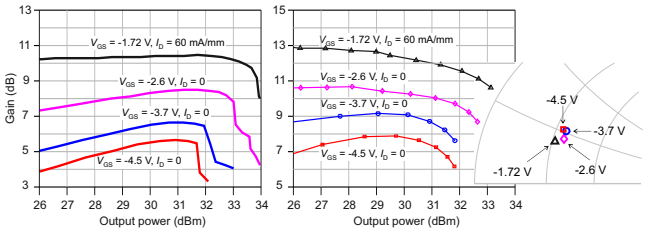
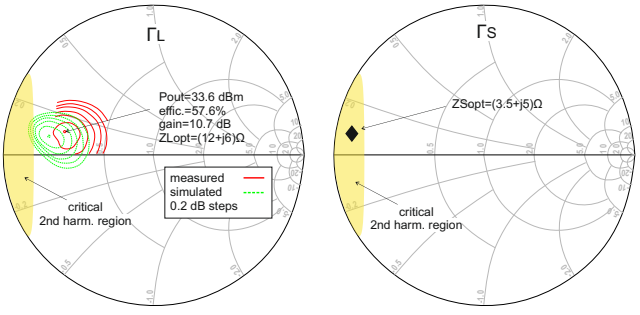


Fig. 2. Load-pull results at different gate bias points for the $8\times100\,\mu$m device. Simulated (left) and measured (center) gain vs. output power on the corresponding optimum load. Measured optimum load trajectories for output power (right).

Finally, it is worth mentioning that, for some bias conditions, also the impact of the second harmonic termination was investigated by fixing the magnitude to one at both input and output side, while sweeping the phase. Results have shown the presence of a region in both input and output plane, where the device performance changes significantly. On the other hand, in the remaining region, the device performance is almost constant and still reasonably high. Fig. 3 shows output power contours of the $8\times100\,\mu$m device in class AB with the critical region for the second harmonic highlighted, in both source and load plane. Balancing the complexity of the design with the achievable improvement by selecting the optimum harmonic terminations, in order to mitigate risks, it was decided to implement the DPA by keeping the second harmonic loads out from such a region.



(a) (b)

Fig. 3. Output power contours level for the $8\times100\,\mu$m device biased in class AB at 18.8 GHz with the critical region for the second harmonic highlighted (left). Optimum source impedance with the critical region for the second harmonic highlighted (right).

B. *Design*

The results of the experimental characterization reported above were compared against the requirements and used to confirm the power budget computation. The synthesised loads

across the devices within the DPA were monitored during all the design phases and compared against the measured contours.

The proposed DPA architecture is shown in Fig. 4.

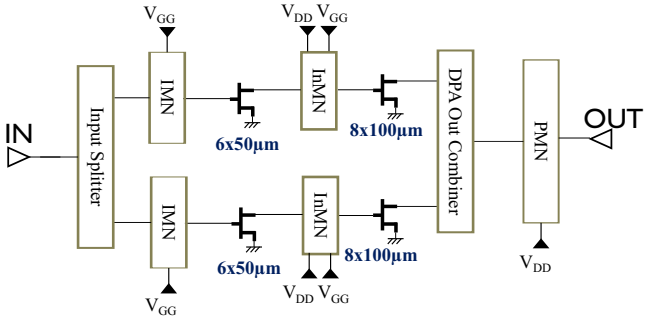


Fig. 4. Scheme of the proposed DPA.

As anticipated, $8\times100\,\mu$m devices are selected for both Carrier and Peaking final stages. Both branches include a driver realized with a $6\times50\mu$m device. Small-signal unconditional stability of the devices is enforced in- and out-of-band by means of an $R-C$ parallel network connected in series to the gate and an additional $R-L$ series network on the gate bias line. The Doherty combiner is implemented in semi-lumped form according to the strategy described in [11], which consists in embedding the drain parasitic elements into the $\lambda/4$ transmission line of each branch. On the Peaking path, an additional $\lambda/4$ element is required to cancel the impedance inversion and to ensure the desired matching. This implementation requires additional real-to-real post-matching at the output, since the characteristic impedance of the Carrier's $\lambda/4$ is determined by its C_{DS}. The post-matching network is based on [12] and matches to DPA cell to $100\,\Omega$ in order use it in a combined structure without the need of any additional output matching. The loads synthesized

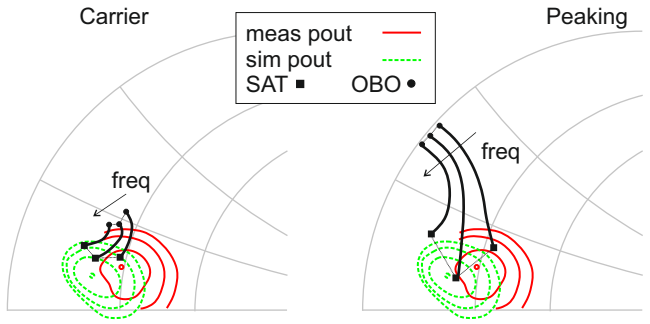


Fig. 5. Synthesised load modulation for Carrier (left) and Peaking (right) devices at 17.3, 18.8 and 20.3 GHz, compared to the simulated/measured load-pull power contours.

by the Doherty combiner at saturation are shown in Fig. 5. Given the discrepancy between simulated and measured optimum, the approach has been to target a trade-off between simulated and measured optimum load. The driver size and the inter-stage matching networks are equal in the two branches in order to maintain the signal phase alignment over the whole targeted frequency band. This represents a trade-off between performance and robustness to process variations.

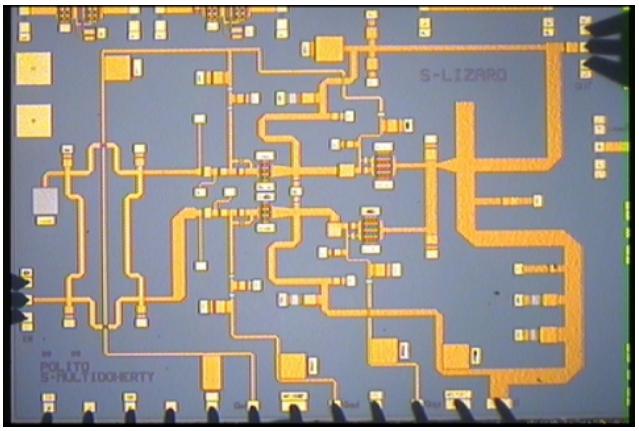


Fig. 6. Microscope photograph of the MMIC.

In fact, selecting different device peripheries and matching networks would allow to better optimize the performance over a narrow band, but ultimately results to be unfeasible over wide bands. For the same reason, the input matching networks designed according to the conjugate matching criterion are also symmetrical. The input splitter is therefore designed to provide uneven power splitting, with a Peaking/Carrier ratio of 1.25. This is again a trade-off between full turn-on of the Peaking power device, which is essential to ensure the desired OBO range, and the resulting gain penalty. The splitter is implemented as a branchline hybrid in semi-lumped form, which provides input isolation of the two branches while partially embedding the delay line needed in DPAs to ensure the proper phase alignment of the branch signals.

III. Fabrication and Experimental Characterization

The MMIC has been fabricated, mounted on a brass carrier and measured in small- and large-signal conditions. The microscope photograph of the DPA is shown in Fig. 6. The size is 3x4 mm^2. Fig. 7 reports the simulated and measured scattering parameters, measured in the 0.1–26 GHz frequency range for the nominal bias of the amplifier (V_{DD}=11 V, $V_{\mathrm{GCarrierDriver}}$=-1.3 V, $V_{\mathrm{GCarrierPower}}$=-1.3 V, $V_{\mathrm{GPeakDriver}}$=-1.8 V, $V_{\mathrm{GPeakPower}}$=-2 V, I_{D}=150 mA). They result in good agreement with the corresponding simulations except for some frequency shift toward high frequency. However, the DPA fully covers the targeted band 17.3–20.3 GHz. The measured CW performance in terms of output power, gain and efficiency versus input power is reported for 5 frequencies in the band (17.3 GHz, 18 GHz, 18.8 GHz, 19.6 GHz and 20.3 GHz) in Fig. 8 for the nominal bias condition and a load of $100\,\Omega$. The DPA achieves saturated output power and efficiency in excess of 34 dBm and 25%, respectively on the whole band. The measured efficiency at 6 dB OBO is maintained higher than 20 % in the 3 GHz bandwidth. Compared with the present state-of-the-art the adoption of the Doherty technique somehow sacrifice the peak efficiency, but thanks to its feature of high efficiency

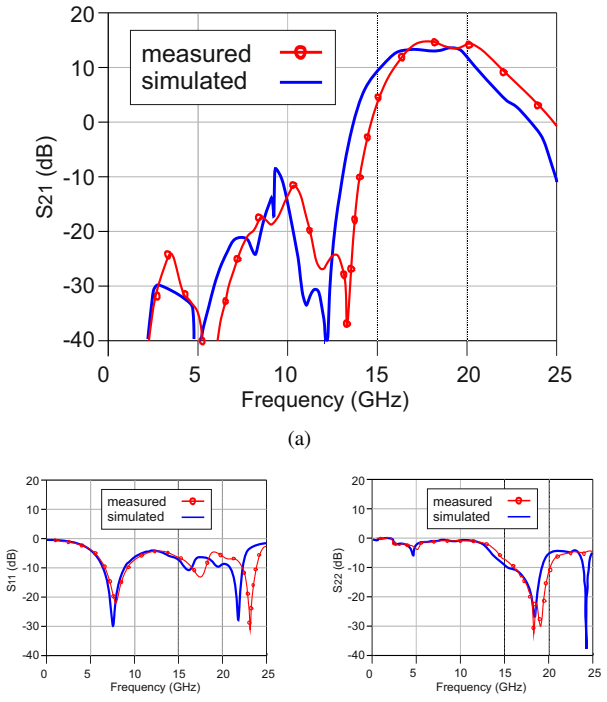


Fig. 7. Comparison of simulated (blue solid lines) and measured (red lines with circles) scattering parameters.

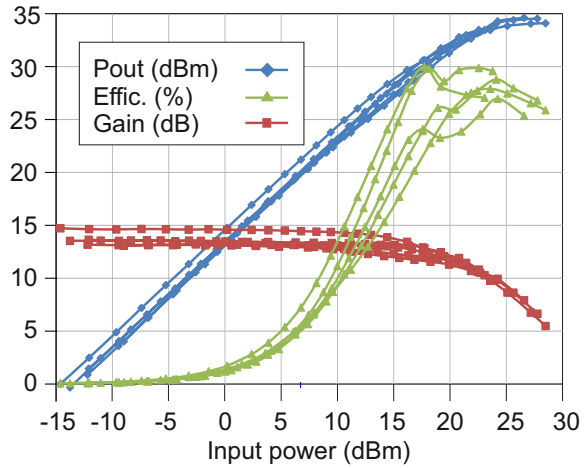


Fig. 8. Measured CW performance versus input power from 17.3 GHz to 20.3 GHz on a 100 Ω load. The curves refer to 5 frequencies in the band (17.3 GHz, 18 GHz, 18.8 GHz, 19.6 GHz and 20.3 GHz).

in back-off is foreseen as a winning solution with complex modulation schemes. The figure clearly highlights the proper Doherty behaviour of the proposed amplifier with an extended high efficiency region below saturation.

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IV. Conclusion

A Doherty power amplifier cell for satellite Ka-Band downlink applications has been designed, fabricated and measured. The results are in line with the present state-of-the-art for this application. The PA will be adopted as a building block of a parallel combined amplifier for this application.

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