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Original
Advances in Pixelated 2D Electromagnetic Optimization with Distributed and Lumped Devices for Microwave Circuit Design / Zhang, W., Ramella, C., Pirola, M., Zhang, Q.. - (2026), pp. 120-123. (2026 IEEE MTT-S Radio Frequency Technology and Techniques Symposium, IMS RFTT 2026 Boston (USA) 07-12 June 2026) [10.1109/imsrftt43070.2026.11602551].

Availability:
This version is available at: 11583/3016714 since: 2026-10-16T08:32:38Z

Publisher:
IEEE

Published
DOI:10.1109/imsrftt43070.2026.11602551

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(Article begins on next page)

22 October 2026

Advances in Pixelated 2D Electromagnetic Optimization with Distributed and Lumped Devices for Microwave Circuit Design

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***Abstract*— This paper presents a further research progress in optimization of pixelated electromagnetic structures for design of microwave planar structures. A hybrid Wilkinson power splitter is considered, which involves the presence of lumped resistors and/or capacitors within the pixelated layout. A 2-step genetic optimization approach is proposed to perform optimal design including pixelated layout, resistor/capacitor placement and value optimization. The proposed numerical example demonstrates how using the proposed technique, a 54% bandwidth solution can be achieved at X-band: a result well in line with, if not even outperforming, the best conventional wideband splitters.**

***Keywords*— microwave design optimization, wideband design, pixelated layout, electromagnetics, Wilkinson power splitter**

I. Introduction

Pixelated planar layout and electromagnetic topology optimization represent an exciting research direction in today's microwave design automation. The pixelated formulations, exploited in [1] as part of a 3D electromagnetic structural topological optimization and successfully applied to 2D electromagnetic design [2] open new directions beyond conventional optimization with continuous variables, yielding solutions that can outperform conventional structures. Research in such electromagnetic topology optimization [3]–[5] and AI-oriented pixelated design [6]–[9] is very active in the microwave community. This paper addresses a further step in this direction. Because of the unconventional pixelated structure, classical design formulas can be not-applicable in pixelated environment for the development of circuits where pixelated layouts must interface with other integrated or hybrid lumped elements to achieve specific network functionalities. Subsequently, a whole new set of design methods needs to be developed to extend pixel-based design to such circuits. In this paper, we address the case of hybrid design, where distributed elements coexist with surface mount device (SMD) ones, proposing a 2-step optimization approach. As a relatively simple, in terms of computation effort, but however representative example, we consider here the case of a wideband hybrid Wilkinson splitter [10]–[13], working in the X-band. The results obtained demonstrate the validity of the proposed technique, yielding an optimum solution covering a $> 54\%$ fractional bandwidth.

II. Formulation of pixelated layout and placement optimization

In this work, we are considering circuits that require both distributed and lumped elements. In the case of a Wilkinson splitter, these two parts also perform different functions. While even splitting and input (port 1) matching are simultaneously obtained, at least in narrowband formulation, with a pair of $\lambda/4$ transmission lines (distributed part), output matching and isolation (port 2 and 3) require the insertion of a lumped resistor, symmetrically deployed between the two branches not to affect splitting factor and input matching. Closed-form design equations can be easily derived at the center frequency, i.e. where the two microstrip arms are becoming $\lambda/4$, but, things are becoming more complicated when a larger frequency band is required. In conventional design, wideband optimization typically requires multi-section structure, increasing chip area, and optimization of resistance deployment along the splitter [10]. Moreover, electromagnetic (EM) simulations and optimization are required to properly account for layout-specific parasitics effects, which represent an extremely challenging and computationally intensive phase. The EM optimization of the distributed portion of the circuit can greatly benefit from the pixel-based formulation, allowing, thanks to the flexibility of the pixelated layout, for wideband matching in a more compact footprint with respect to classical approaches. On the other hand, it has been shown in [14], for a narrowband splitter, that the isolating element can be placed across any two points of a symmetric layout, provided that proper reactance is added. It is thus reasonable to assume that an optimum placement and admittance value exist able to provide wideband isolation.

The proposed method allows to identify both the optimum pixelated splitter and the optimum position and value of the lumped elements by following a two-step optimization as described in Fig. 1. An EM-based optimization of the pixelated splitter alone is run first, targeting wideband matching. Among the best solutions, i.e. those above a predefined quality threshold, those which layout allow for adding one or more lumped elements in standard SMD package, are then automatically selected, following a pseudo-convolution algorithm, and then used as basis for a second optimization, targeting optimum number, value and position of lumped elements, which can be only resistors (R) or a combination of resistors and capacitors (C). For both optimization loops, we exploit a genetic approach, thanks to its superior performance in discrete-value optimization, and the Keysight Momentum engine to achieve fast yet accurate EM simulation of the pixelated layouts.

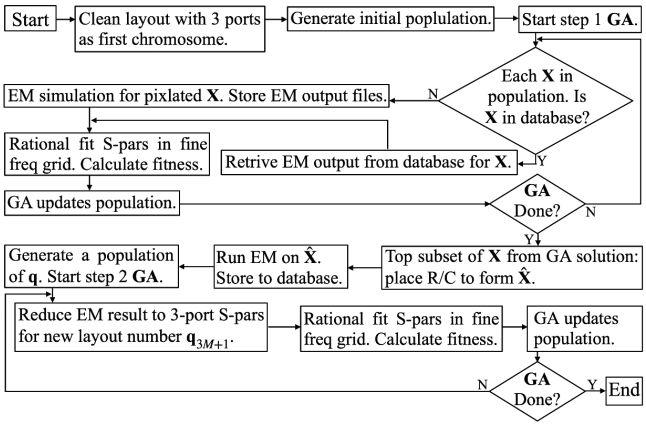

Fig. 1. Flowchart of the proposed 2-step genetic optimization for the design of microwave circuits with pixelated layout and lumped elements.

A. Step 1: pixelated layout optimization

Not to loose generality, we formulated the pixelated layout optimization as a generic 2D topology optimization problem in a rectangular area. Let the area be divided into rectangular pixels of several rows and several columns and let N_1 and N_2 be defined as the number of rows and columns of pixels in the overall layout area. Then $\mathbf{X}$ will be a binary matrix with size $N_1 \times N_2$ representing the pixelated optimization variables

$$\mathbf{X} = [x_{ij}] \tag{1}$$

where $x_{ij} = 1$ if the $(i,j)^{\text{th}}$ pixel is metal and $x_{ij} = 0$ if the $(i,j)^{\text{th}}$ pixel is non-metal. At the boundary of the layout area, we have one input port at the center left position, and 2 symmetric output ports at the right side. Indeed, since a 3-dB microstrip splitter is a symmetric structure, the matrix $\mathbf{X}$ to be optimized can represent just half of the effectively EM simulated circuit without loss of information.

As anticipated, we used Momentum for the EM simulation of the 3-port S-parameters from the pixelated layout encoded by $\mathbf{X}$ in (1). To speed up the process, we exploited the adaptive frequency algorithm of Momentum: a rational-fitting-based approach which limits at the minimum the number of frequency points to be effectively simulated to gather the correct S-parameter behavior. As the Momentum result file does not contain information on such fitting, the full-frequency-range behavior is then reconstructed within the optimization loop re-applying rational fitting.

The electromagnetic topology optimization problem consists of finding the $\mathbf{X}$ layout that minimizes the design objective function, in this case, the error between the EM simulated S_{21} and the target value of -3.1 dB which is enough due to the whole reactive structure. Transmission has been preferred to input return loss since, being a larger number, it provides better conditioned numeric results. The genetic algorithm (GA) is used for such optimization, where the negated version of the one-sided generalized least p^{th} function is used as the fitness function. We started with a clean layout, namely a basic splitter with $\lambda/4$, 70.7-Ω, branches at 10 GHz firstly created in ADS. This provides a rough estimation of the proper pixel size and number, as well as the desired maximum dimensions of the final solution. Moreover, in this step, we define the technological (EM stack-up) and simulation (frequency range, mesh, solver, etc.) parameters for Momentum. This setup will be shared by all subsequent EM simulations performed in the optimization loops, through command-line execution of Momentum. The reference layout is then "pixelated" and upon it, several new layouts are created following a perturbative approach, i.e. ,by randomly adding or eliminating pixels along the 2D axis around the original layout. The perturbation approach is preferred to a fully random one to limit the number of cases that are too far from a splitter to be useful. On the other hand, to ensure that no solutions are neglected, purely randomly generated layouts are also generated and included in the initial population (50% share). At the end of the GA optimization process, the best pixelated layout pattern is obtained, but all data from all layouts generated during the optimization are saved, so as to identify a number of good solutions to be used in the second optimization step.

B. Step 2: SMD placement and optimization

For Wilkinson power splitter, the addition of multiple resistors and/or capacitors along different locations of the branches allows for wideband optimization of output matching and isolation [11], [12], [14]. However, within a pixelated layout, an analytical approach for component sizing and placement is not applicable, hence requiring a different approach. In this work, we propose a twp-step procedure where, starting from the best pixelated solutions, we first identify the layouts that allow for the placement of one or more SMD components, of one or more given sizes (in this case two, namely 0201 and 0402), across the two symmetric halves of the circuit, and then we optimize their position and values. The possibility of performing the optimization in two steps is guaranteed by the fact that the use of some pixels as solder-pads for the SMD R/C can be considered a small perturbation to the original pixelated layouts.

1) Layout selection and solder-pad insertion

This task is performed by an automatic algorithm: given the geometrical dimensions of the SMD R/C solder-pads, defined in the component datasheets, we define h_k and v_k as the number of horizontal and vertical pixels of a solder-pad for SMD of size k. To automatically place a solder pad into a pixelated layout, we formulate a 2D kernel, similar to a kernel (or a filter) in convolutional neural network:

$$\mathbf{P}_k = [p_{ij}^k],\ i = 1, 2, \ldots, v_k + s_k,\ j = 1, 2, \ldots, h_k + 2 \tag{2}$$

where s_k is the number of gaps between the 2 solder pads of a resistor, and where we assume that the resistor is placed vertically in the layout area, consistent with Wilkinson splitter's structure. Let the top-left pixel of the kernel, i.e., p_{11}, represent the origin of the kernel. A pseudo-convolution is performed between kernel $\mathbf{P}_k$ and the 2D pixelated layout, such that the output of the convolution will be a new 2D

pixelated layout which will include solder pads placed in feasible locations. The word "convolution" here means that the kernel will move from one position to another position in the 2D design space of $\mathbf{X}$. In detail, when the kernel is at $(r,c)^{\text{th}}$ position (i.e. row r, column c), we perform the following operation between the kernel and the pixelated layout $\mathbf{X}$:

$$L_1 = \sum_{ij}(p_{ij}^k + x_{mn}),\ m = i + r, n = j + c \tag{3}$$

$$L_2 = \sum_{n}(g(x_{rc}, x_{mn})),\ m = r_{\text{center}} \tag{4}$$

$$L_3 = 1 - g(x_{rc}, x_{mn}),\ m = r_{\text{port2}}, n = c_{\text{port2}} \tag{5}$$

$$L_4 = 1 - g(x_{rc}, x_{mn}),\ m = r_{\text{port3}}, n = c_{\text{port3}} \tag{6}$$

$$\text{for } r = r_{center} - \left(v_k + \frac{s_k}{2}\right) + 1,\ c = 1, 2, \ldots, N_2$$

where $g(a,b)$ is an operator that indicates whether there is (1) or not (0) electrical continuity between a and b pixels, L_1 represents the necessary gaps between the two SMD terminals, L_2 the avoidance of indirect short circuits between them, and L_3 and L_4 the necessary electrical connection between the solder pads and the output ports in the pixelated layout. By performing convolution, a new layout $\hat{\mathbf{X}} = [\hat{x}_{mn}]$ is produced by moving the kernel over the 2D pixelated design $\mathbf{X}$:

- $\hat{x}_{mn} = 1$ if $L_1 + L_2 + L_3 + L_4 = 0$ and $r \leq m \leq (r + v_k - 1)$ and $(c+1) \leq n \leq (c + h_k - 2)$
- $\hat{x}_{mn} = x_{mn}$ otherwise

Notice that here (m,n) are pixel indices in $\mathbf{X}$ or $\hat{\mathbf{X}}$, while (r,c) moves the kernel over the 2D pixelated space. The new layout $\hat{\mathbf{X}}$ may have one or more SMDs, up to a maximum M, depending on the pixelated layout.

2) *R/C placement and value optimization*

To formulate resistor/capacitor optimal selection and their resistance/capacitance optimization, we will perform the convolution operation over a population of pixelated layouts $\mathbf{X}$, leading to a population of new pixelated layouts with $\hat{\mathbf{X}}$. Now we face a multiple optimization problem where the search space includes layout selection, SMD type (R/C) and value. These are all inter-dependent variables thus we consider all of them together into a new GA optimization. We cannot use continuous optimization methods, like quasi-Newton, because R/C selection and layout selection are discrete variables, as well as R/C values as we consider only standardized industry values (E24). The optimization variables of this second optimization can be represented by a vector of integers, representing the discrete nature of all the variables:

$$\mathbf{q} = [q_1, q_2, \ldots, q_M, q_{M+1}, \ldots, q_{3M+1}] \tag{7}$$

where

- for $j \leq M$
  - $q_j = 1$ if a resistor is placed at the jth solder pad port
  - $q_j = 0$ if a capacitor is placed at the jth solder pad port
- for $M < j \leq 2M$
  - q_j is the index of standardized resistor values for the $(j-M)^{\text{th}}$ solder pad port if that port connects to a resistor
- for $2M < j \leq 3M$
  - q_j is the index of standardized capacitor values for the $(j-2M)^{\text{th}}$ solder pad port if that port connects to a capacitor
- for $j = 3M + 1$
  - q_j is the layout number for $\hat{\mathbf{X}}$

The second step GA optimization, with $\mathbf{q}$ as chromosome, searches for optimum layout number, combination of R/C, and selection of standardized component values, that minimizes, in this case, isolation (S_{32}).

III. Example: X-band hybrid Wilkinson splitter

The example presented is a hybrid Wilkinson power splitter, implemented on a Rogers RO4350B substrate. The maximum layout area is fixed to $1.8 \times 4.7\,\text{mm}^2$. The layout is tiled into a grid of $16 \times 32 = 512$ pixels, but thanks to symmetry, we can reduce the design space down to 256 binary variables for optimization ($N_1 = 8$, $N_2 = 32$). The initial population for step-1 optimization counts 100 chromosomes (50% random variations of the reference layout, 50% completely random layouts). The overall pixelated layout optimization was programmed in Matlab, exploiting the GA toolbox. The number of stall generations was set to 80, while the fitness function is $S_{21} \geq -3.2\,\text{dB}$, enforced over the 5-15 GHz band (100%). Several GA processes were executed for an average of 200 generations after which we selected 100 top-ranked pixelated layouts to proceed with step-2 optimization. Considering SMD0201 and SMD0402 sizes, the solder pad turn out to occupy 3×2 and 5×4 pixels, respectively, i.e. $(v_1, h_1) = (3, 2)$ and $(v_2, h_2) = (5, 4)$. The gaps between the pairs of solder pads in terms of pixels are $s_1 = 2$ $s_2 = 4$. The discrete values for the SMDs are chosen in the E24 series. With the selected dimensions, the maximum number of SMD that can be added to a layout is $M = 3$. A maximum of 5 different solder pad placement combinations were attempted for each pixelated layout, achieving a total of 390 new layouts, each containing at least one SMD. Fig. 2 shows two examples of the new generated layout with SMD components. The population size is 80, while the number of stall generation is 20. The fitness function now includes also isolation, asking for $S_{32} \leq -15\,\text{dB}$. GA optimization was performed multiple times to confirm certainty of solution, because each time, random values are different. GA reaches optimal solution with average of 30 generations. The best solution is the layout shown in Fig. 2-bottom, with 91Ω resistor. As shown in Fig. 3, it satisfies the requirements in the 8-14 GHz range, representing over 54% of fractional bandwidth. These excellent results demonstrate the effectiveness of the proposed methodology in optimizing hybrid circuits and show that it can be extended to more complex structures.

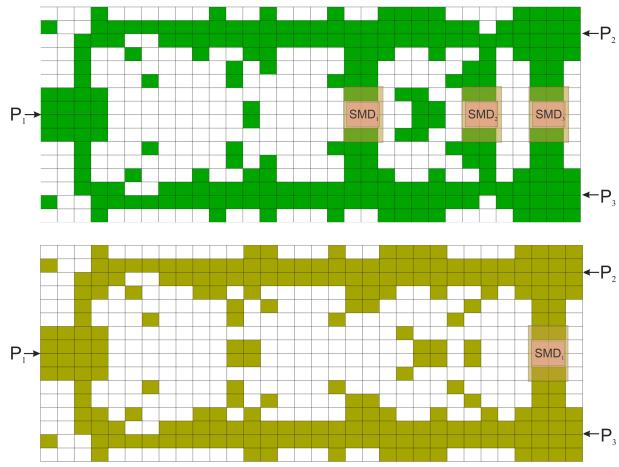

Fig. 2. Examples of pixelated layouts hosting three or one SMDs.

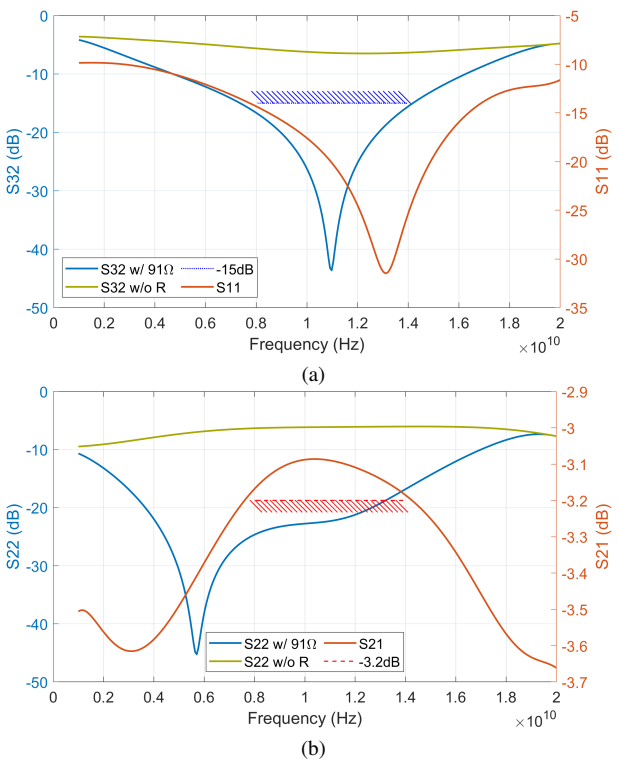

Fig. 3. Performance of the best pixelated layout with and without the SMD resistor: (a) input matching and isolation (-15 dB target); (b) output matching and transmission (–3.2 dB target).

IV. Conclusion

This paper presented a 2-step discrete optimization approach that addresses the design of pixelated layouts including lumped elements, which type, placement and value is optimized, too. This expands the pixelated-based strategy into a wider area of applications, where further optimization steps, expressively conceived for the pixelated environment, are required. The numerical results validate the proposed approach, reconfirming the potentialities of the pixelated design methodology in microwave circuit design.

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