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Monolithic 3-terminal perovskite/silicon HBT-based tandem compatible with both-side contact silicon cells: a theoretical study

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Abstract. The heterostructure bipolar transistor solar cell architecture offers an attractive route to realize monolithic 3-terminal perovskite/silicon tandem solar cells compatible with both-side contact Si photovoltaic technologies. Essentially, the HBT implements two counter series diodes with the common third terminal realized at the interface between the two diodes through an interdigitated contact. Concrete design solutions require optimizing the HBT multilayer stack for maximum power conversion efficiency of the intrinsic cell and designing appropriate layouts for the current collecting grid of the middle terminal. In this work, we develop a modeling framework that combines electro-optical simulations of the intrinsic tandem stack with circuit-level simulations to quantify the impact of shadow and resistive losses associated with the metal contacts on the scalability of the cell size. We present a design of a HBT with homojunction silicon bottom cell that can surpass 40% efficiency with a perovskite bandgap of 1.55 eV, i.e. much higher than the limit efficiency of a series connected tandem with the same material system. Then, we explore the implications of the middle contact in terms of interdependence between the subcells and parasitic losses, by considering a top interdigitated layout and cell architectures with both homojunction and heterojunction silicon cells. We show that in most configurations proper grid design can enable the scaling up of these devices to large areas, and that the scalability can be markedly improved, especially for the case of Si heterojunction bottom cells, by developing a layout with overlapped grids.

Keywords: Perovskite /silicon tandems / 3-terminal tandems / heterostructure bipolar transistor / current collecting grid / photovoltaics

1 Introduction

In the past decade, perovskites have emerged as one of the most promising classes of materials to combine with silicon in tandem photovoltaic cells. This is due to their widely tunable energy bandgap, excellent photo-physical properties, and their simple manufacturing, that could be adapted in a cost-effective way to the mainstream silicon industry [1–4]. Intensive research has triggered a sequence of power conversion efficiency (PCE) records culminating very recently in a 33.7% PCE for a lab-scale tandem of 1 cm² and a 28.6% PCE for a tandem with a large area of 258 cm² [5]. For comparison, large area single-junction silicon cells reach today 26.8% [5], and are close to their maximum achievable efficiency of $\approx 29.4\%$ [6].

In parallel to the efficiency maximization and demonstration of technology scalability to industry relevant cell size, research is also focusing on maximizing the long-term

stability and the energy yield in the field. These are fundamental figures of merit to lower the levelized cost of electricity and environmental impact enough to make perovskite/silicon tandem technology suitable for commercial electricity production [7].

Regarding stability, monolithic tandem devices have been reported to retain about 80% of their initial efficiency under field operation for periods up to 1 year [8,9]. Although this is still too low in comparison with silicon cells, which typically retain about 80% or more of their initial performance for more than 25 years, it suggests that perovskite cells might reach much longer lifespans in the future. Indeed, they had only a few hours of lifespan at their debut. Therefore, it is reasonable to assume that there is enough space for material optimization to replicate the impressive results achieved so far in terms of efficiency also in terms of stability, and reach enough long lifetime to hit the target cost needed to enter the photovoltaic market [10]. Notably, various intrinsic degradation mechanisms can be tackled by working on the composition of the perovskite layer [11].

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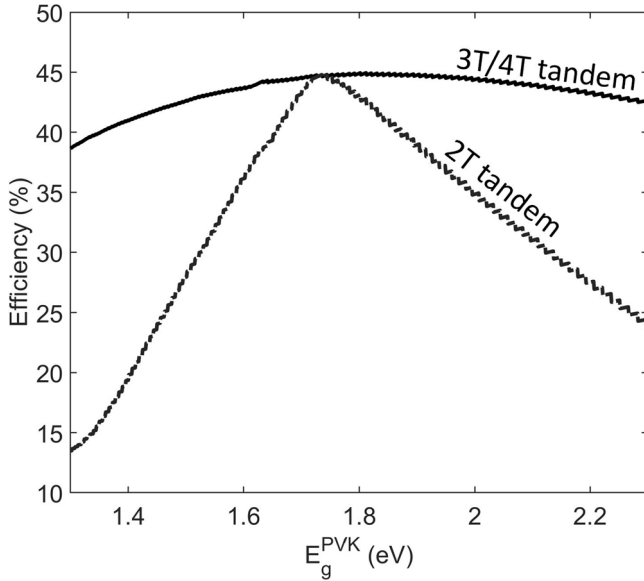


Fig. 1. Detailed balance efficiency limit of silicon (1.12 eV) based tandems with 2T, 3T and 4T architecture as a function of the perovskite top cell bandgap, calculated according to [12,13] under AM1.5G, 1000 W/m².

The energy yield in the field mainly depends on whether the two subcells forming the tandem are connected in series and power a unique load or work independently being connected to two different loads. The first option leads to a 2-terminal (2T) tandem, whereas the second one can be realized by either 3-terminal (3T) and 4-terminal (4T) configurations. 2T architectures are the most commonly considered, essentially because of their straightforward connection at module level – completely analogous to a single junction cell – and their suitability for realizing monolithic tandems. The above mentioned efficiency records refer indeed to 2T devices. However, they require current matching between the two subcells, implying stringent requirements on the gap of the top-cell to be integrated with the silicon one. Detailed balance calculations [12,13] in Figure 1 show that the different configurations reach almost the same maximum theoretical efficiency, but the 2T one remains competitive with the 3T and 4T ones only in a narrow range of the perovskite bandgap. This clearly imposes some tradeoff in the search of high efficiency and highly stable perovskites [11]. When turning to real world applications, the current matching constraint turns into a high sensitivity of the PCE to spectral fluctuations, impairing the energy yield of 2T tandems. Independent simulation studies have shown that 3T/4T provide maximum energy yield [14,15] because they remove the current matching constraint. Several perovskite/silicon 4T devices with mechanically stacked subcells have been reported, with record PCE higher than 28% [5]. This approach provides a high flexibility both in terms of material choice and manufacturing, since the two cells are fabricated separately, but at the cost of increased optical losses due to the additional metal grids and contact layers, and of greater fabrication complexity at cell and module level.

Recently, monolithic 3T devices have also started to emerge, which integrate a high gap cell on top of a silicon interdigitated back contact (IBC) bottom cell [16–18], or introduce an intermediate transparent conductive layer between the two subcells to realize the third electrode [19]. This last solution, used in [19] to enable the individual characterization of the subcells forming a monolithic tandem, has the advantage to be compatible with both-side contact silicon technologies, such as Al-BSF, PERX, and heterojunction (HTJ) [20,21], having a much larger market share than the IBC ones [22,23]. Yet, the additional transparent conductive layer could cause optical losses, as seen for the 4T architecture, and makes the cell more prone to carrier loss stemming from local shunts [16,24].

An interesting alternative approach to 3T monolithic tandems is offered by the heterostructure bipolar transistor (HBT) solar cell proposed in 2015 in the context of GaAs-based tandems [12]. It essentially consists of three alternating doped semiconductor layers (e.g., $N/P/n$ or $P/N/p$, where upper and lower case letters indicate high and low bandgap, respectively), each having its own electrical contact. Notably, about thirty years earlier Sakai and Umeno proposed a wavelength-division InP-based solar cell made of a $N/P/p/n$ stack [25] with three electrodes. Both structures in [12,25] are similar to that one of HBTs used in microelectronics, realize a double-junction cell with three terminals, and require the implementation of interdigitated contacts at the top or bottom surface. Maximizing the attainable PCE of the HBT tandem essentially requires independent operation of the two subcells, although intimately connected by the transport of carriers through the middle thin layers. Since the seminal work in [12], significant progress has been reported on GaAs-based HBT solar cells [26,27], that proves the feasibility of this idea with III-V technology.

To foster the development of this attractive concept for perovskite/silicon (PVS) tandem solar cells compatible with full both-side contact Si technologies, concrete design solutions are needed. With this objective, we have recently proposed possible practical configurations, either with planar [28,29] and textured [30] Si bottom cells. With the aid of quasi-1D numerical simulations, we have demonstrated the feasibility of this concept showing that HBT multi-layer stacks that use standard materials and layer thicknesses found in PVK and Si solar cells can indeed ensure the independent operation of the two junctions needed for maximum PCE. On the other hand, the introduction of a middle contact and the adoption of interdigitated grids for current collection causes optical and resistive loss that have to be quantified and minimized. In particular, the parasitic resistive mechanisms due to the lateral transport across the thin interface layers between the subcells could introduce an unwanted interdependence, or cross-talk [31], between the two junctions significantly degrading the attainable PCE.

In this study, we address these issues by taking advantage of a modeling framework that combines electro-optical simulations of the 3T-HBT tandem stack with circuit-level simulations of the full device. We discuss in detail the problem of the possible cross-talk between the junctions showing that it actually has a negligible effect at

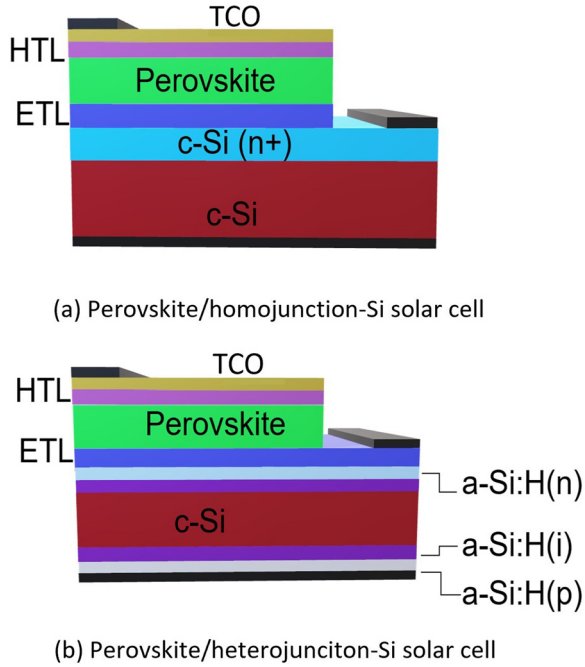


Fig. 2. Examples of structure of p - n - p 3T-HBT tandems based on n - i - p PVK cell combined with (a) homojunction and (b) heterojunction n - p Si bottom cell. The complementary n - p - n configurations can be formed by inverting the polarity of the two subcells.

maximum power point. Then, we analyze shading and resistive losses associated to the current collecting grids, and their implications in the perspective of scaling up to large areas. The limitations in terms of material properties inherent to different device realizations are taken into account by parametrizing the results to the resistivity of the thin interface layers, thus gaining useful insight for architectures based on homojunction as well as heterojunction Si technologies.

2 HBT-based tandem

Basic schemes for monolithic perovskite/silicon HBT tandems compatible with homojunction and heterojunction Si photovoltaic technologies are depicted in Figure 2. By stacking a n - i - p PVK subcell on top of a n - p Si-homojunction bottom cell, one realizes the p - n - p perovskite/silicon (PVS) HBT device shown in Figure 2a. Taking into account of the dominant conductivity of the layers (hole-reach or electron-reach), we can identify three main regions in analogy with a p - n - p bipolar transistor: from the top, the ITO/HTL/PVK stack forms the emitter, the ETL and (n^+) -c-Si form the base, and the p -type c-Si the collector.

The top *emitter-base* (E/B) and bottom *base-collector* (B/C) junctions constitute in fact the two tandem subcells and work as counter-series diodes connected through the common base. Since the layers forming the base are thin, carrier injection from the top junction towards the bottom one is possible (the counterway being absent because of the high/low gap structure) and could cause an interplay

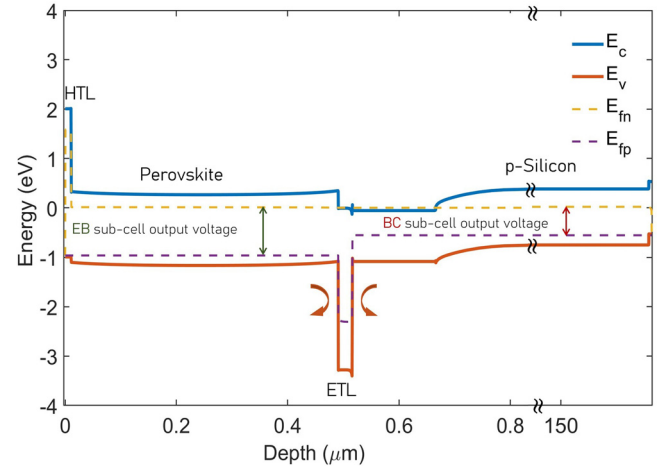


Fig. 3. Energy band diagram of the p - n - p 3T-HBT case study (Fig. 2a) with each junction biased at maximum power point. The dashed yellow and pink lines are the electron and hole quasi-Fermi levels, respectively.

between the two subcells. This phenomenon is known as *transistor effect*. On the other hand, for the maximization of the tandem PCE, the two subcells should work independently [12]. We have analyzed in previous works the implications of this mechanism in PVK/silicon HBT structures showing that it is not going to be of concern [28,30]. In this regard, one can consider the energy band diagram reported in Figure 3 for the PVK/homojunction-Si HBT device proposed in the present work, whose geometric and material details are given in Section 3.1. The energy bands alignment at the E/B (i.e. PVK/ETL) and B/C (i.e. (n^+) -Si/ p -Si) hetero-interfaces allows collection of electrons at the base contact, whereas *repels* holes photogenerated in each subcell towards their respective contacts, i.e. emitter and collector, avoiding any injection from one junction to the other. This turns into a bending of the hole quasi-Fermi-level across the base, enabling each subcell to sustain a different quasi-Fermi-level splitting, coherent with their own bandgap.

Similar considerations hold for 3T-HBT tandems with Si heterojunction bottom cell [28,30], whose basic architecture is shown in Figure 2b. In view of the following analysis on parasitic electrical losses, it has to be noted that the base region of the HBT with heterojunction-Si cell (Fig. 2b) includes thin layers of intrinsic and doped hydrogenated amorphous silicon (a-Si:H) instead of the highly doped c-Si present in the HBT with homojunction-Si cell (Fig. 2a). In particular, the base is formed by the ETL/a-Si:H(n)/a-Si:H(i) stack for the p - n - p architecture in Figure 2b, and by the HTL/a-Si:H(p)/a-Si:H(i) for the complementary n - p - n tandem.

Regardless of the Si technology exploited for the bottom subcell, it is necessary to engineer the HBT design to fabricate the base contact by accessing the interface layers between the two subcells. Interdigitated grids can be adopted for collecting the subcells currents. Antolín et al. [26] studied two possible solutions to access the base layer in III-V HBT tandems: from the cell front side by implementing a grid layout with top interdigitated

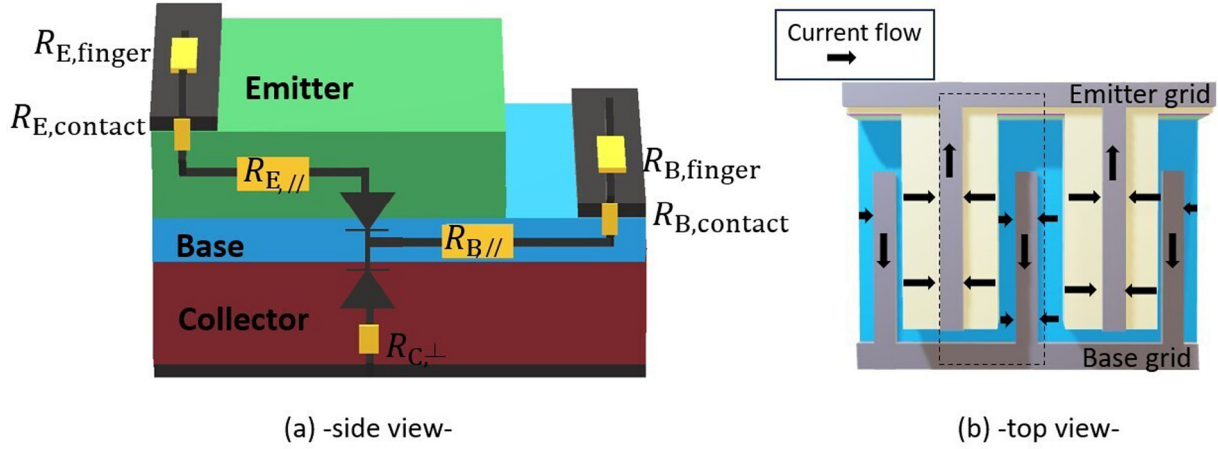


Fig. 4. 3T-HBT tandem with TIC configuration. The side view depicts the main parasitic resistive mechanisms causing PCE loss.

contacts (TIC) or from the back side by implementing a grid layout with bottom interdigitated contacts (BIC). For PVS HBT tandems, we adopt the TIC layout considering that the BIC one, although minimizing shading losses, would require to etch the Si substrate. Thus, the TIC scheme appears as more suitable and should mitigate the additional fabrication complexity and manufacturing costs implied by the fabrication of the third contact. **Figure 4** presents a scheme of the 3T-HBT with TIC layout, where the emitter stack is partially etched to fabricate the base metal contact, highlighting the main parasitic resistive mechanisms that affect the overall HBT performance: i) resistive loss due to the current flow in the fingers and busbars; ii) contact resistance at the semiconductor/metal interface; iii) resistive loss related to the lateral transport of carriers across the thin emitter and base layers ($R_{E//}$, $R_{B//}$), and longitudinal transport across the collector ($R_{C\perp}$). Furthermore, the TIC collecting grid introduces shadow losses due to the area covered by metallic contacts and, for the top-cell, to the emitter etched regions. Therefore, geometry and design optimization of the TIC layout, as well as of the thin-film layers, has to be carried out to minimize the aforementioned energy losses [32], above all for large-area devices.

3 Methods

3.1 Model

With the aim to analyze the effect of power losses associated to the 3-terminal configuration, we have used a modeling approach that combines quasi-1D electromagnetic and transport simulations of the HBT multilayer stack (see Supplementary Material), to characterize the performance of the intrinsic device, with circuit level simulations to account for the electrical and optical parasitic losses inherent to device geometry and TIC layout (**Fig. 4**).

Figure 5 shows the equivalent model of the 3T-HBT solar cell. It consists of the equivalent circuit of the intrinsic device under illumination (i.e. counter-series diodes and photocurrent generators) completed by lumped parasitic resistances R_E , R_B and R_C ($\Omega \text{ cm}^2$) at each terminal. From

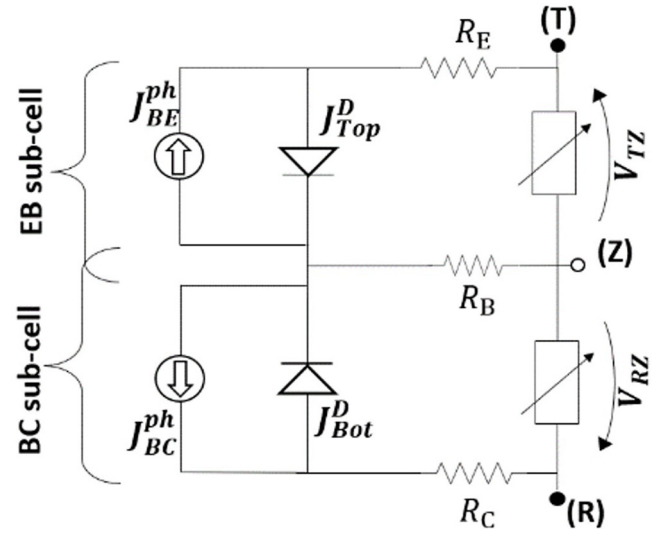


Fig. 5. Equivalent circuit of the 3T-HBT tandem. Emitter, base and collector contacts are named as T, Z and R respectively, following the notation in [33].

the circuit topology it is clearly seen that while the series resistances R_E and R_C act exclusively on their respective subcell, the base resistance R_B , being shared between the two subcells, could cause interdependence between their operating conditions [31].

According to the scheme in **Figure 4a**, R_E and R_B result as the superposition of contact resistance ($R_{E/B,c}$) at the semiconductor-metal interface, lateral transport equivalent resistance ($R_{E//}$ and $R_{B//}$) and finger resistance $R_{E/B,f}$.

These elements are estimated taking advantage of the symmetry of the cell layout and considering the power losses associated to an elementary *unit cell* of the metallic grid (black dashed box in **Fig. 4b**) [34]. The resistance $R_{C\perp}$ accounts for the longitudinal current flow, and its effect is marginal. Expressions for R_E , R_B and R_C and the different resistive components are summarized in **Table 1**.

Concerning the lateral transport path, the corresponding sheet resistance R_{sh} for emitter and base is affected by transport across all the materials forming the emitter and base regions. With reference to the device structure in

Table 1. Expressions of parasitic resistance components.

Resistive loss	Label	Expression
Lateral	$R_{//}$	$\frac{1}{12} R_{sh} d_f^2$
Contact	R_c	$\frac{1}{2} d_f \sqrt{\frac{R_{sh}}{\rho_c}} \coth\left(\frac{w_f}{2} \sqrt{\frac{R_{sh}}{\rho_c}}\right)$
Finger	R_f	$\frac{1}{3} \frac{\rho_m}{t_f w_f} l_f^2 d_f$
Emitter	R_E	$R_{E//} + R_{E,c} + R_{E,f}$
Base	R_B	$R_{B//} + R_{B,c} + R_{B,f}$
Collector	$R_{C\perp}$	$\rho_{p-Si} t_{collector}$

Figure 2a, the emitter and base R_{sh} is calculated as the parallel connection of the sheet resistances of those layers forming the emitter and base stacks, e.g. TCO/HTL/PVK and ETL/ n -Si, respectively:

$$R_{sh}^{Emitter} = \left(\frac{1}{R_{sh}^{TCO}} + \frac{1}{R_{sh}^{HTL}} + \frac{1}{R_{sh}^{PVK}} \right)^{-1}, \quad (1)$$

$$R_{sh}^{Base} = \left(\frac{1}{R_{sh}^{ETL}} + \frac{1}{R_{sh}^{Si}} \right)^{-1}. \quad (2)$$

As mentioned above, optical and transport simulations were carried out to characterize the intrinsic HBT device. Simulations were done by means of the Synopsys TCAD software [35]. In particular, we used the Transfer Matrix Method (TMM) to evaluate the optical generation rate of the planar HBT under study (see Supplementary Material and [36] for full details). The optical generation profile is then given as input to the Poisson-drift-diffusion transport model to evaluate photocurrent spectra and current-voltage characteristics of the E/B and B/C subcells. We previously used this simulation approach to study state-of-the-art 2T PVK/silicon tandems, demonstrating the ability of the model to satisfactorily reproduce the experimental spectral response and photovoltaic characteristics of the subcells [30]. By fitting these, we finally extract the parameters of the diodes and generators of the equivalent circuit in Figure 5.

Shadow losses caused by the TIC grid are included in the model by correcting the E/B and B/C photocurrents of the intrinsic device, estimated from the physics-based simulation, as follows:

$$J_{BE}^{ph} = J_{BE}^{ph'} (1 - 3f_{shadow}), \quad (3)$$

$$J_{BC}^{ph} = J_{BC}^{ph'} (1 - 2f_{shadow}), \quad (4)$$

where f_{shadow} is a shading loss factor given as [32]

$$f_{shadow} = \frac{w_f}{d_f}, \quad (5)$$

w_f being the grid width, and d_f the finger distance. $J_{BE/BC}^{ph'}$, $J_{BE/BC}^{ph}$ indicate the photocurrent values without and with shadow loss, respectively. The lost fraction of E/B photocurrent (Eq. (3)) is estimated as three times f_{shadow} , taking into account of the emitter surface covered by the metal grid and of the emitter region etched to realize the base contact. Rather conservatively, we have assumed an etched region width equal to twice the metal finger width. For reference, typical finger width resolution is $16 \pm 1 \mu m$ for ink-jet printing [32] and $23 \pm 4 \mu m$ for screen printing technique [37]. Finally, the fraction of lost BC current (Eq. (4)) is estimated as twice f_{shadow} , because of the B/C areas shadowed by the emitter and base finger metallizations.

3.2 Device details and simulation parameters

The device studied in this work is a PVS-HBT device (Fig. 2a) built on homojunction-Si cell; the PVK top subcell consists of 34 nm TCO layer made of Indium Tin Oxide (ITO), 11 nm PTAA hole transport layer, 480 nm of perovskite layer and 25 nm of SnO_2 electron transport layer. The Si homojunction bottom cell consists of 150 nm of n^+ c-Si and 150 μm thick p -type c-Si. The cell architecture is completed by a 92 nm thick MgF antireflection coating, and a 1 μm thick highly doped back surface field layer. The full rear contact is made of a 1 μm thick gold layer. Table 2 summarizes doping levels and main material parameters. Data for the wavelength-dependent optical properties can be found in [42].

Perovskite, ETL and HTL materials are modeled as classical crystalline semiconductors [38, 43–45]. The drift-diffusion model includes Shockley-Read-Hall recombination in c-Si only, with electron and hole time constants of 1 ms; Auger recombination in silicon is modeled following [46] with electron and hole coefficients equal to $3.2 \times 10^{-32} cm^6 s^{-1}$. Finally, the radiative recombination coefficient is set to: $4.73 \times 10^{-15} cm^3/s$ for c-Si [35] ($\tau_{rad}^{c-Si} = 105 ms$), and $8 \times 10^{-10} cm^3/s$ [47] for all the materials of the PVK subcell ($\tau_{rad}^{PVK} = 6.2 \mu s$, $\tau_{rad}^{HTL} = 0.25 ns$ and $\tau_{rad}^{ETL} = 0.12 ns$). Current-voltage characteristics are simulated under AM1.5G illumination spectrum (total power of $100 mW/cm^2$) at normal incidence.

Concerning the contact layout, we assume two identical grids for emitter and base with typical geometrical and material parameters summarized in Table 3 [32,34,48–50]. The emitter and base sheet resistances result as $R_{sh}^{Emitter} \approx R_{sh}^{ITO} = 274 \Omega/\square$ and $R_{sh}^{Base} \approx R_{sh}^{c-Si(n^+)} = 74 \Omega/\square$.

4 Results

Figure 6 shows the absorbance ($1-R$) and external quantum efficiency (EQE) spectra of the HBT tandem under study. The integrated photocurrent provided by the top and bottom subcells amounts to $22.3 mA/cm^2$ and $16.3 mA/cm^2$, respectively. The Si cell photocurrent is slightly penalized by the planar geometry which limits the absorbance at long wavelengths, while the PVK top-cell suffers from low carrier collection at short wavelengths. The $J-V$ characteristics under AM1.5G illumination are shown in Figure 7. The PVK and Si subcells reach V_{oc} of 1.06 V and

Table 2. Main parameters value. E_g : Bandgap χ : Electron Affinity ϵ_r : Permittivity $N_c(N_v)$: Density of states μ : Mobility τ : Lifetime. N : net doping. [e/h]: electron/hole; if not specified, the value is assumed the same for both carriers.

	PTAA	PVK	SnO ₂	c-Si [35]
E_g [eV]	2.95 [38]	1.55 [38]	3.28 [38]	1.1
$q\chi$ [eV]	2.18	4.35	3.9	4.05
ϵ_r	3	6.5 [39]	9.6	11.9
N_c [cm ⁻³]	2.2×10^{18}	2×10^{18}	4.1×10^{18}	2.8×10^{19}
N_v [cm ⁻³]	1.8×10^{19}	2×10^{18}	4.1×10^{18}	2.6×10^{19}
μ [cm ² /Vs]	0.0002 [40]	11.8 [40]	240 [41]	1177 ^[el] 424 ^[h]
N [cm ⁻³]	5×10^{18}	2×10^{14}	10^{19}	1×10^{16}

Table 3. Grid geometrical and material parameters.

Parameter	Label	Value
Finger width (μm)	w_f	40
Finger height (μm)	t_f	15
$\rho_{\text{Ag/ITO}}$ (m Ωcm^2)	ρ_c	1.27
$\rho_{\text{Ag/Si}}$ (Ag/Si) (m Ωcm^2)	ρ_c	1
Gridline resistivity (Ωcm)	ρ_m	2.65×10^{-6}
ITO res. (Ωcm)	ρ_{ITO}	9.31×10^{-4}
c-Si(n ⁺) res. (Ωcm)	ρ_{Si}	1.11×10^{-3}
SnO ₂ res. (Ωcm)	ρ_{SnO_2}	5.2×10^{-3}

0.64 V. The overall 3T tandem efficiency is $\approx 29.4\%$. This is quite a remarkable value, considering that the detailed balance efficiency limit in Figure 1 is $\approx 32\%$ and 43% for a tandem cell with 1.55 eV perovskite and 2T and 3T architecture, respectively. The present device approaches the 2T tandem limit, and could reach significantly higher efficiency by further optimization of the multilayer stack.

To analyze the efficiency penalty caused by the metallic grids, we can start by considering a small area HBT, with finger length $l_f = 1.5$ cm. In this case, the dominant resistive path is associated to the lateral transport across the base and emitter, while the finger R_{finger} and contact R_{contact} resistances are marginal. Figure 8 analyzes the amount of efficiency loss as a function of finger spacing, d_f , and sheet resistance of the base layer, $R_{\text{sh}}^{\text{Base}}$. In detail, in equation (2), we have made $R_{\text{sh}}^{\text{Si}}$ to change in the range $[1 \div 10^5] \Omega/\square$. The rationale is to gain a picture of the impact of the base metal grid for the different possible architectures of PVK on silicon tandems reported in Figure 2, which present a very large change in the electrical conductivity of the silicon bottom cell layers constituting the base. For example, for the tandem PVK/Si-homojunction of Figure 2a, we estimated a sheet base resistance of $\approx 74 \Omega/\square$, limited by the lateral transport across the (n⁺)c-Si layer. On the other hand, higher values of $R_{\text{sh}}^{\text{Si}}$ may be representative of tandem architectures on heterojunction Si cells, due to the high sheet resistance of the thin a-Si:H layers (up to $10^5 \Omega/\square$). In the p - n - p configuration in Figure 2b, the resulting base sheet resistance $R_{\text{sh}}^{\text{Base}}$ is mitigated by that one of the SnO₂ ETL ($\approx 10^3 \Omega/\square$), whereas a complementary n - p - n configuration could present

even higher $R_{\text{sh}}^{\text{Base}}$ values due to the typically very low electrical conductivity of HTL materials. The map shows that for $R_{\text{sh}}^{\text{Base}}$ up to $100 \Omega/\square$ (representative of PVS tandems on homojunction c-Si cells), the efficiency loss can be minimized to less than 3% with finger distance in the range $[1.5 \div 2.9]$ mm, in line with typical finger distance found in Si cells. For heterojunction bottom cells ($R_{\text{sh}}^{\text{Base}} \approx 1000 \Omega/\square$), the finger spacing shall be reduced to about 1 mm, with a minimum efficiency penalty of $\approx 5\%$. Lower finger distance implies a higher penalty due to the dominant effect of shadow losses.

To analyze more in detail the impact of the common base resistance (see Fig. 5), we can take as case study a cell with spacing $d_f = 1.5$ mm. For the tandem with homojunction bottom cell, the corresponding base and emitter resistances are $\approx 0.13 \Omega\text{cm}^2$ and $\approx 0.51 \Omega\text{cm}^2$, respectively, i.e. the base resistance R_B is about 1/3 of the emitter one. However, the fractional power loss ($\propto R^2$) caused by R_B and R_E are comparable. Indeed, the base layer collects carriers from both emitter and collector, resulting into a current flow across R_B about 70% higher than that one across the R_E . This shows the uttermost importance of parasitic resistive effects associated to the base terminal.

With regard to the possible cross-talk between the two subcells caused by R_B , Figure 9 shows the impact on the EB (BC) maximum power point (MPP) voltage $V_{\text{mpp}}^{\text{TZ}}$ ($V_{\text{mpp}}^{\text{RZ}}$) as a function of the V_{RZ} (V_{TZ}) and the corresponding efficiency reduction for several values of $R_{\text{sh}}^{\text{Base}}$. One can observe that the two subcells remain independent up to the MPP, regardless of the value of R_B . The R_B mediated cross-talk onsets only at voltages higher than the MPP one and causes an increase of the open circuit (OC) voltage as the bias of the other subcell grows towards open circuit. The same effect has been observed experimentally in III-V HBT tandems [31]. Therefore, the R_B mediated interdependence between the subcells has a marginal impact on the attainable PCE. On the other hand, because of the series resistance effect, the V_{mpp} of each subcell and the overall PCE become smaller as R_B increases. In this sense, it is important to assess the implications in terms of scalability of the technology.

The efficiency penalty for the TIC layout under study when scaling to larger areas is analyzed in Figure 10 as a function of finger length, l_f , and distance, d_f . We consider

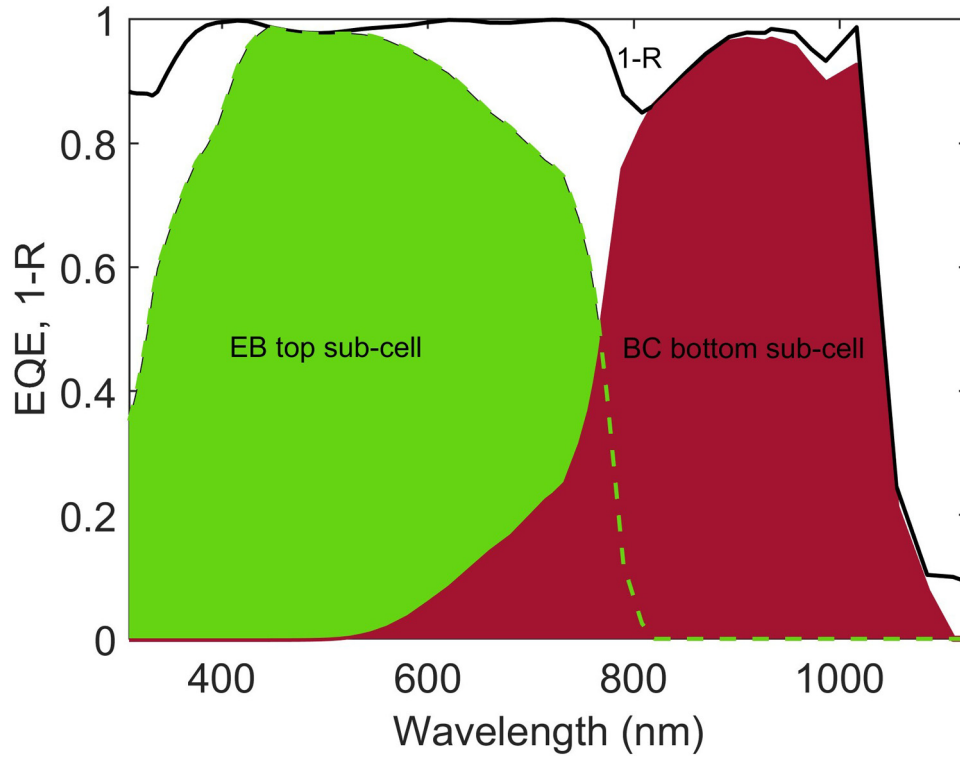


Fig. 6. EQE of the perovskite top-cell and silicon bottom cell and total absorbance ($1-R$, R being the reflectance) of the tandem multilayer stack.

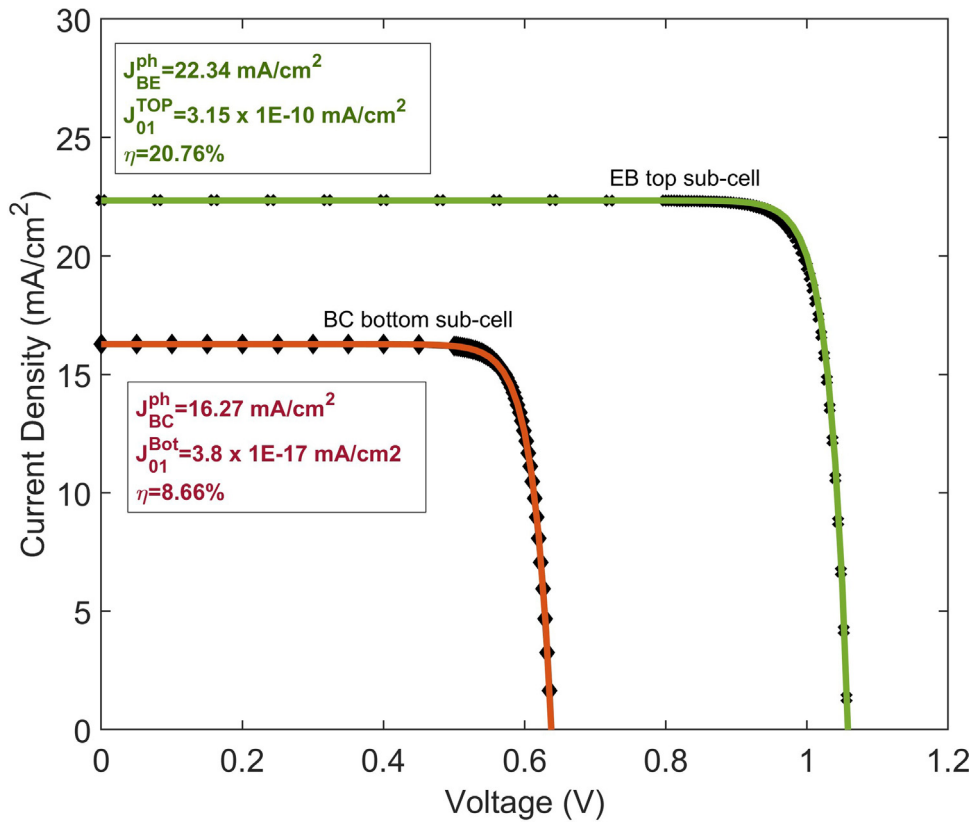


Fig. 7. $J-V$ characteristics obtained from TCAD simulations (solid lines) and best fit diode model for circuit level simulations (dashed lines). The numerical values of the one diode fit parameters are reported in the boxes.

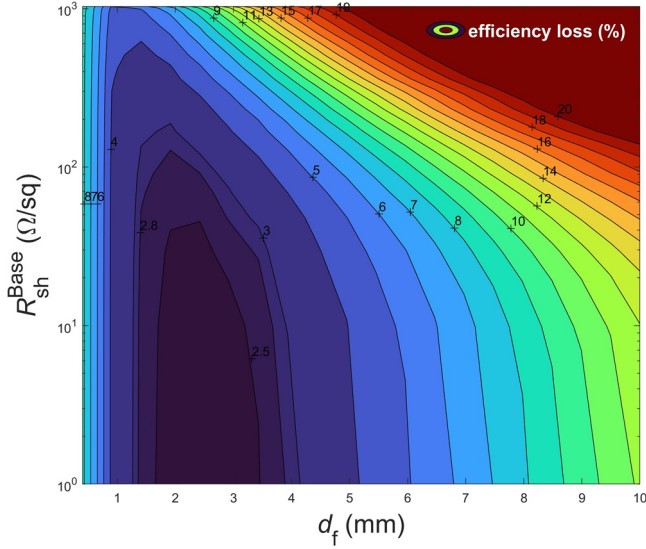


Fig. 8. Efficiency loss as a function of the finger distance (d_f) and base sheet resistance (R_{sh}^{Base}).

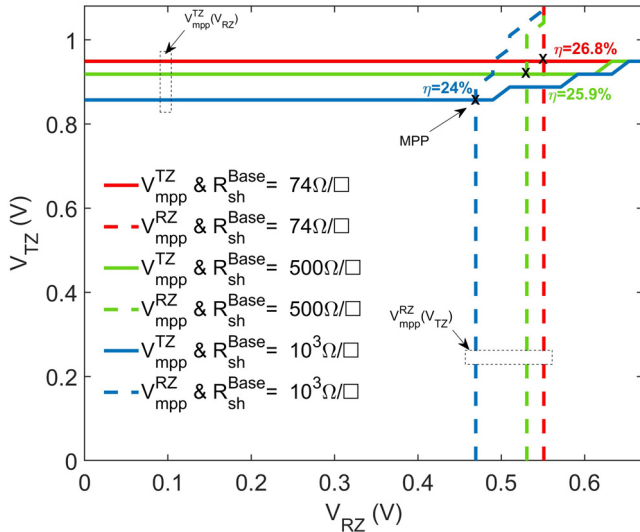
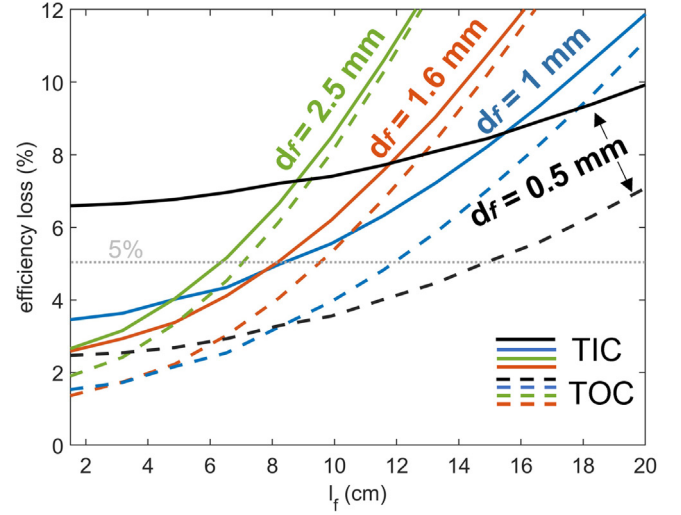
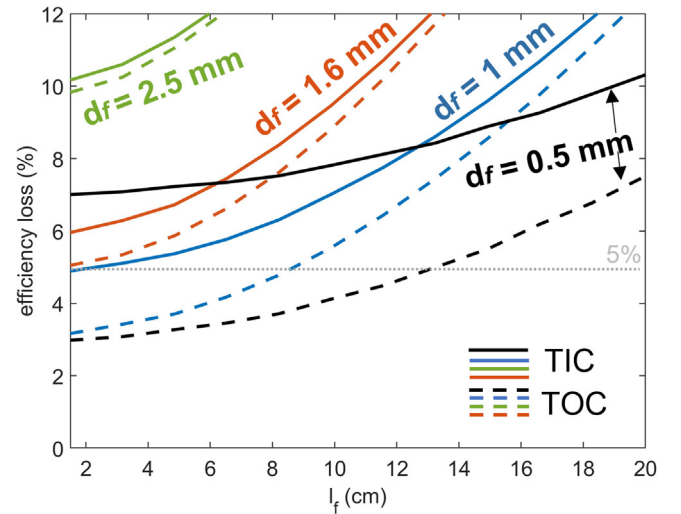


Fig. 9. EB and BC mpp voltages (V_{mpp}^{TZ} and V_{mpp}^{RZ}) as a function of V^{RZ} and V^{TZ} voltages.

two different case studies, with values of base sheet resistance representative of PVS HBT tandems based on homojunction ($R_{sh}^{Base} \approx 74 \Omega/\square$) and heterojunction c-Si cells ($R_{sh}^{Base} \approx 1000 \Omega/\square$). Clearly, the HBT device worsens its performances as the finger length or distance increases. The impact of l_f has a great effect on the efficiency, because the finger resistance, R_f in Table 1, scales quadratically with l_f , with a derivative as larger as larger d_f is. For the homojunction case, results in Figure 10a show that with an optimized layout, efficiency loss remains lower than 5% for finger lengths up to about 8 cm, while the heterojunction



(a) Perovskite/homojunction-Si solar cell



(b) Perovskite/heterojunction-Si solar cell

Fig. 10. Efficiency loss as a function of finger length (l_f) for the case studies of PVS 3T/HBT on (a) homojunction Si cell ($R_{sh}^{Base} \approx 74 \Omega/\square$) and (b) HTJ Si cell ($R_{sh}^{Base} \approx 1000 \Omega/\square$): TIC layout (solid line) and TOC layout (dashed line).

case is more critical and would demand closely spaced fingers to minimize the resistive loss. In this perspective, it is interesting to look at the possible performance improvement offered by an alternative layout with overlapped emitter/base grids (TOC), inspired to microelectronic metal interconnection technology. For the TOC layout, the EB and BC fraction of lost current of equations (3) and (4) can be rewritten as

$$J_{BE/BC}^{ph'} = J_{BE/BC}^{ph} (1 - w_f/d_f). \quad (6)$$

By overlapping emitter and base grids, optical losses become equivalent to a conventional 2-terminal device, with a significant improvement of the HBT performance for large area layouts with low finger distance. Indeed, in [Figure 10](#), the TOC layout provides minimized efficiency loss for $d_f = 0.5 \div 1$ mm, where the dominant loss is related to the shadowing one. Instead, as the finger distance increases, the efficiency loss of the TOC layout approaches that one of the TIC one, being dominated by resistive effects. With the TOC layout, both homojunction and heterojunction configurations maintain an efficiency penalty lower than 5% for finger lengths well above 10 cm, showing the good potential of the HBT approach also in the perspective of scaling up to large areas.

5 Conclusions

We have presented a simulation study on 3-terminal perovskite/silicon tandems based on the HBT architecture. The strong point of this approach with respect to other solutions proposed so far, such as 3-terminal tandems on IBC silicon cells, is its compatibility with more standard both-side contact crystalline silicon technologies such as Al-BSF, PERX, and heterojunction. However, getting rid of the IBC bottom cell requires the realization of a middle contact at the base layer that connects the two junctions and of interdigitated current collecting grids, causing additional optical and resistive loss. In this work, we have studied the implications of such parasitic mechanisms with the aid of electro-optical simulations of the intrinsic tandem stack and circuit-level simulations of the full device, included metal grids.

We have reported the design of a multilayer stack for the HBT tandem that, despite the non optimum perovskite bandgap of 1.55 eV, achieves efficiency higher than 29%, with room for further improvements. We have then examined the efficiency penalty associated to the implementation of a top interdigitated contact layout. In this regard, the parasitic base resistance is a critical factor for the device performance because it arises from charge lateral transport across thin layers and because the current of both subcells flows through it. Therefore, its effect is strongly dependent on the HBT configuration (n - p - n or p - n - p) and on the bottom cell technology and can cause high proportional power loss with respect to the emitter and collector resistances. Moreover, the base resistance might induce interdependence between the junctions, impairing the maximum achievable PCE. With respect to this last point, we find that such interdependence is actually significant only when the junctions are beyond the maximum power point, and therefore is of no concern in photovoltaic operating conditions. The main limitations associated to the additional base resistance involve the scalability of the HBT to large areas. For HBT tandems with Si-homojunction cell, thanks to the low c-Si base sheet resistance, the base resistance remains low enough to allow a scaling of PCE loss with finger length in line with other perovskite/silicon tandems. We find that an optimized finger spacing can keep the PCE penalty lower than 5% for

finger lengths up to 8 cm. Otherwise, for HBTs exploiting a HTJ-Si bottom cell technology, it is mandatory to mitigate the high sheet resistance of the a-Si:H layers. For the p - n - p configuration, this can be achieved thanks to the good electrical conductivity of currently used ETL materials, such as the SnO_2 considered in this work. For the n - p - n configuration, while organic HTL materials commonly used in PSCs have too low conductivity, a viable option could be provided by high mobility inorganic HTLs [51], such as nickel oxide [52,53].

Lastly, we have introduced a top contact layout with overlapped emitter and base grids. By minimizing shadow losses, the top overlapped layout allows to reduce the finger spacing in such a way that even HBT tandems with heterojunction Si bottom cell attain PCE loss lower than 5% with finger lengths well above 10 cm. These results show that the HBT architecture could be an attractive alternative to realize high efficiency, large area 3T perovskite/silicon tandems that can be integrated with standard silicon bottom cells. Besides the experimental demonstration of this concept, further theoretical studies could investigate more deeply the role of interfaces and ion migration at intrinsic device level and engineer the multilayer stack to achieve higher intrinsic PCE, as well as further develop the metal grid and circuit models, e.g. by including busbars, aiming at designing ad-hoc optimized layouts.

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Author contribution statement

Conceptualization, G.G., M.C., F.C. ; methodology, G.G. and F.C.; software, G.G.; validation, G.G., F.C.; resources, F.C.; data curation, G.G.; writing original draft preparation, G.G., F.C.; writing-review and editing, G.G., F.C. and M.C.; visualization, G.G.; supervision, F.C.; project administration, F.C.; funding acquisition, F.C. All authors have read and agreed to the published version of the manuscript.

Supplementary material

Figure S1. Perovskite/Silicon 3T-HBTsc with TIC configuration.

Figure S2. Geometry for the quasi-1D simulation of the intrinsic HBT device.

Figure S3. Energy band diagram at cutlines A and B in [Figure 2](#) (left) and at cutline C (right).

The Supplementary Material is available at <https://www.epj-pv.org/10.1051/epjpv/2023024/olm>.

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